IOPMP Task Group Meeting

April 25, 2024

Video link

Minutes

- Issues of draft 6:
  - Separate the record valid bit (**v**) from the interrupt pending (**ip**) in the ERR_REQINFO.
    - Not concluded yet.
  - SRCMD/MDLCK in the isolation/compact-*k* models with/without **sps**.
    - When the sps (in Appendix A3) is absent, SRCMD/MDLCK is absent, either since the two models don't need these registers.
  - What if improper MDCFG?
    - The unsuggested and transient case is left to be implementation-dependent as long as the two conditions are satisfied:
      1) an entry should belong to at most one MD, and
      2) the lower indexed MD has lower indexed entries.

Record valid bit and interrupt pending

- Separate the record valid bit (**v**) from the interrupt pending bit (**ip**) in the ERR_REQINFO.
  - Separating them makes the spec understood easier.
  - When interrupts are disabled but bus errors are still answered, using **ip** looks odd.
  - Clearing only **v** allows new record updating but not re-enter the ISR (since CPU has been already in ISR).
  - **ip**=1with **v**=0 implies that the error record is not implemented.
- In normal cases, ISR should clear both bits in the end.
  - No extra cycle is needed to clear them.

SRCMD/MDLCK in **isolation/compact-*k***

- With sps, the secondary permission setting extension:
  - SRCMD_EN(H) should be read-only and reflect the fact of the model
  - MDLCK is still programmable since it affects the bits in SRCMD_R/W(H).
- Without sps:
  - SRCMDs and MDLCK are not present.
  - Saves some gate-counts and MMIO space.

What if MDCFG.t's are NOT incremental

- Spec suggests they're incremental, but what if they aren't?
- Several proposals were mentioned last time, and each has its own pro-and-con. Not easy to converge.
- The spec leaves its behavior implementation-dependent, as long as:
  1) an entry should belong to at most one MD, and
  2) the lower indexed MD has lower indexed entries.