IOPMP TG Meeting

October 27th, 2022

Agenda

- Disclosure:
- Comparison between per-SID and per-MD schemes

Only RISC-V Members May Attend

- Non-members are asked to please leave except for Joint Working Groups (JWG).
- Members share IP protection by virtue of their common membership agreement. Non-members being present jeopardizes that protection. Joint working groups (JWG) agree that any IP discussed or worked on is fully open source and unencumbered as per the policy.
- It is easy to become a member. Check out riscv.org/membership
- If you need work done between non-members or or other orgs and RISC-V, please use a joint working group (JWG).
    - used to allow non-members in SIGs but the SIGs purpose has changed.
- Please put your name and company (in parens after your name) as your zoom name. If you are an individual member just use the word “individual” instead of company name.
- Non-member guests may present to the group but should only stay for the presentation. Guests should leave for any follow on discussions.

Antitrust Policy Notice

RISC-V International meetings involve participation by industry competitors, and it is the intention of RISC-V International to conduct all its activities in accordance with applicable antitrust and competition laws. It is therefore extremely important that attendees adhere to meeting agendas, and be aware of, and not participate in, any activities that are prohibited under applicable US state, federal or foreign antitrust and competition laws.

Examples of types of actions that are prohibited at RISC-V International meetings and in connection with RISC-V International activities are described in the RISC-V International Regulations Article 7 available here: https://riscv.org/regulations/

If you have questions about these matters, please contact your company counsel.

Collaborative & Welcoming Community

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/community/community-code-of-conduct/

Conventions

- **For one hour meetings, please start at 5 after the start time** in order to allow people going to other meetings have time for a short break between meetings. 30 minute meetings start on time.
- Unless it is a scheduled agenda topic, we don’t solve problems or detailed topics in most meetings unless specified in the agenda because we don’t often have enough time to do so and it is more efficient to do so offline and/or in email. We identify items and send folks off to do the work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unilaterally. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, …
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

Atomicity Issues on Updating

- On programming multiple rules in the run-time, there could be a moment that IOPMP works under incomplete settings. → It could transiently create a security hole.
- Atomicity requirement: A transaction should be checked either before no update takes effect or after all updates take effect .

Cherry-Pick Register (Per-MD scheme)

- For more complicated cases, we may want to select or unselect specific SIDs to stall, the Cherry-pick SID Register, *CPSID*, can do so.
- It is used to turn on or off one specific *SID-stalling* bit.

  - Bit *clean*: let *SID-stalling*[*SID*] = ! *clean* once the *CPSID* written.
  - Field *SID*: the SID to operate.

Comparison of MMIO Registers

	Per-SID	Per-MD
# of MMIO Register occupation	could vary	2: MD-stall-mask + Cherry-pick register
# of transactions to query/update	could vary	1

Comparison of Scenarios

Settings to Update	Per-SID	Per-MD
S1: Entries of MD(s)	User should look up the corresponding SID(s) from the MD(s) to update.	Just stall the MD(s)
S2: MDTOP(s) of MD(s)	User should look up the corresponding SID(s) from the MD(s) to update.	Just stall the MD(s)
S3: 1 *SRCMD*	No stall needed	No stall needed
S4: 2+ *SRCMDs*	Just stall SIDs to update	1. Specify the MD(s) to exempt 2. Cherry-pick SIDs to stall

Discussion on Per-MD Scheme

- Deadlock issue
- SID-BYPASS
- Stall-in-progress

Thank You