IOPMP Task Group Meeting
August 29, 2024

Video link

Minutes

- The feedback of the alternative SRCMD format: ➔ Let's stabilize the spec and get some feedback from Arch Review.

- Q1: Would there be a SRCMD_EN register ? I assume no, as the entry valid information would be only given by the Entries array?
- A1: SRCMD(i) could be considered as the PERM of entry i in wgC.

- Q2: SRCMD_R/W registers would be renamed ? since Read and Write permissions are not split into distinct registers in this alternate format.
- Q3: There would be no concern regarding Enable bit, lock or repurposing of registers in the SRCMD table. SPS on SRCMD would remain an option on full and rapid models.
- A2: According to the proposal, we won't have SRCMD_EN, SRCMD_R and SRCMD_W. That is, no SPS for SRCMD_FMT=2.

The Alternative SRCMD layout

RRID 31　　　　　　RRID *j*　　　　RRID 0

SRCMD(0) for MD/entry 0 | w | r | | w | r | | w | r |

SRCMD(*i*) for MD/entry *i* | w | r | | w | r | | w | r | == entry(*i*).PERM

SRCMD(62) for MD/entry 62 | w | r | | w | r | | w | r |

read and write perm of RRID *j* for the entry *i* are placed at SRCMD(*i*)[*j* x 2] and SRCMD(*i*)[*j* x 2 + 1]

No more SRCMD_EN, SRCMD_R and SRCMD_W.

- Q4: Also, as there would be no MDCFG table and the SRCMD table would be limited to the permission, this IOPMP model would be as follows:
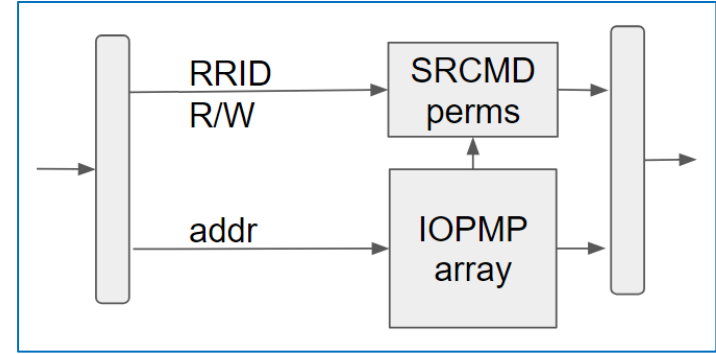
- A4: Yes, you can think and implement it in this way! But, technically, to avoid the MDCFG table, we will say that every MD has exactly one entry, a.k.a. the rapid-1 model.

- Q5: What about the lock ? Would the N first lock for the Entries array would also apply to the permissions hold in the SRCMD table ?
- A5: According to the spec literally, locking the SRCMD table and locking entries are <u>independent</u>.
  - Lock the first N entries (ENTRY_CFG, ENTRY_ADDR) by **ENTRYLCK**, and
  - lock perm bits for an entry/MD *j* (a.k.a. SRCMD(*j*)), by the bit **MDLCK[*j*]**.
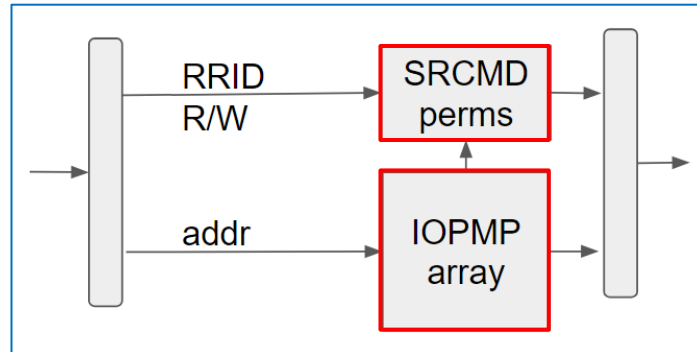
- Q6: However, I suggest having an alternate IOPMP Entries array format instead of an alternate SRCMD table format that would include the address range as well as the permissions per RRID. There would be no concern regarding Enable bit, lock or repurposing of registers in the SRCMD table. SPS on SRCMD would remain an option on full and rapid models. We could also support the alternate IOPMP Entries array in the full model or rapid-k. That may be interesting for a centralized IOPMP to have this capability instead of limiting it to the Rapid-1 model.
- A6: this would break the current flow and structure.