May 18, 2023 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: RobertC, Beeman, JohnS, BruceA, JeffS
- **Slides/video** here
- Fast-track extensions (S*csrind, S*cdeleg, Smcntrpmf) reviewed by AR Tuesday, awaiting minutes
    - S*csrind hasn't been shared publicly yet, but link is here
        - Does not include autoincrement, limited to a simple extension of what is in AIA
        - miselect values are defined by extensions that depend on S*csrind, this extension just lays the foundation
        - Has allocation for custom use
    - AR review is backed up right now, may not be cleared by June (our target AR review date)
- Server SoC Spec TG will look at PMU requirements for RISC-V servers, at CPU & SoC level
    - Not Server Spec TG as listed in slides, group is not taking on the whole server
- SBI bulk counter access extension spec revised and out for review
- No other topics, done early

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation