May 19, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong, LIU Zhiwei, tech.meetings@riscv.org

Agenda

- Gap analysis (60 min)

Notes

- Attendees: Beeman, Zhiwei, JojoR, Jessica, Atish, Anup Patel, Knute Linggard
- Slides posted here, audio to follow shortly (no video due to technical issues)
- SIG scope question: what constitutes a performance analysis tool?
    - Propose including all SW tools that are commonly used for SW perf analysis, even if pure SW (no PMU). Propose not including things like simulators that can be used for trace collection or HW perf validation, though may want to work with perf modeling SIG on this.
    - Knute: from perf modeling SIG. Agree on scope. Want to see how we can collaborate. Modeling SIG focused on HW perf analysis.
    - Beeman: though I'm interested in HW perf analysis, this SIG will focus on SW perf analysis
    - Knute: perf modeling tools enables perf simulation and frameworks that enable tools like Valgrind to pull in data, would love guidance on how to enable that
    - Beeman: agreed that this is a good area for collaboration. We will get to this class of tools later in the gap analysis
- CPU counter gaps
    - Jessica: can reduce context switch overhead with bulk SBI operations, but for sampling where one counter is in use then can't reduce LCOFI handler overhead with SBI approach
    - Beeman: agreed, needing a system call in the handler will add to sampling overhead. There is a counter delegation proposal we'll review that would avoid that.
    - Jessica: free-run counters are the only ones required, but would be nice to have common encodings for events
    - Anup: can be tricky to have too many standardized events if it puts a burden on HW to support them
        - Jessica: ARMv8 doesn't have many that are mandated
    - Beeman: standardized events will be covered later in the analysis, agree that it would be nice to have some. Separate questions on which are standardized and which (if any) are mandated
- CPU sampling gaps
    - Beeman: believe we'll want to prioritize a way to sample when interrupts are masked, and consider the need for some means for precise sampling
- Please send Beeman feedback on this method of analysis
- Finished the slides, will continue with more gap analysis categories next time

Action items

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