Oct 6, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: GuillemC, JohnS, Beeman, BruceA, Zhiwei, Anup, Philipp, Ved, Aaron, Greg, Atish
- **Slides/video** here
- Opens
    - Anup: are we considering adding filtering support for cycles & instret counters? Needed in order to be able to expose them to a VM, today they count hypervisor execution.
        - Beeman: let's take this up as a formal topic
    - Beeman: do others agree instret reads should be strongly ordered? Such that write 0 followed by read should always return 1?
        - Spec isn't explicit about this, but seems consistent with it
        - Downside is that reads require some serialization, which has perf impacts
        - Philipp: what if implementation supported OOO retire, what should counter reflect then?
        - Ved: counter should count consistent with program order
- Standardized and discoverable events
    - Reviewing tables in slides
    - Ved: would want data source breakdown for LR too
    - Bruce: would CYCLES.CPU count during WFI?
        - Beeman: depends on implementation. CYCLES.CPU would count all unhalted (non-sleep-state) cycles, so would only count for an implementation that doesn't enter a sleep state.
        - Spec: "The purpose of the WFI instruction is to provide a hint to the implementation, and so a legal implementation is to simply implement WFI as a NOP."
        - CYCLES.CPU would count unhalted cycles, but when the CPU halts is undefined/implementation-specific
        - Philipp: for CPI calculations, don't want to count WFI cycles
        - If WFI doesn't halt, might SW user still not want to count those cycles? Ignore wait state cycles?
            - Ved and Philipp prefer this
            - Count cycles when CPU is not halted/sleeping or waiting
    - Do we need CYCLES.REF/BUS in PMU?
        - These are standard Linux perf events, would behoove us to include
- Out of time. Next time add definitions to each event, to ensure we agree on them.
    - And add info on how events map to SBI events

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation