Jun 15, 2023 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: Beeman, Ludovic, RobertC, DmitryR, JohnS, BruceA, Anup
- **Slides/video** here
- Updates
  - Fast track extensions nearing end of ARC review. Smcntrpmf completed.
  - CTR TG progressing but behind ratification plan timeline
  - Qemu POCs done for S*csrind, CTR. WIP for Smcdeleg/Sscfg.
- Robert: why can't Qemu actually filter counters?
  - Cycle and instret have dummy value, just count wall-clock cycles
  - LCOFIs based on wall-clock as well
  - Spike has accurate instret modeling, better vehicle for validation. Qemu used for SW enabling, which doesn't require accurate counters.
- Looking at priorities, 2 items could be candidates for fast-track:
  - Counter freeze
  - Event modifiers
- Counter freeze
  - For kernel profiling, where LCOFIs are handled in a priv mode where counters are not inhibited, counter freeze synchronizes counters for snapshot, and reduces sample collection latency by saving need to write countinhibit
  - Requirements:
    - Freeze on LCOFI, not overflow. Otherwise lose counts without any way to know which inst caused freeze
    - Freeze only select counters. Otherwise violate counter independence.
- Event modifiers
  - Thresholds: allows creating histograms of event values, and identify regions with high/low rates
    - Bruce: could also only increment for event (e.g., stall) duration. Outstanding loads too.
  - Requirements
    - Configured per-counter, new field in event selector.
    - Challenge to determine size/scale of threshold to suit all events
- Reviewed ARM & Intel counter freeze
  - Both freeze on overflow
  - Intel freezes all counters, ARM freezes per counter partition
  - Neither has support in perf. Intel's removed due to lack of counter independence, and loss of counts which broke Mozilla RR
- Removed ARM & Intel event modifiers
  - Intel has threshold (CMASK), edge detect, and invert bit
  - ARM has threshold and configurable comparison

        - What size are these thresholds?
            - CMASK is 8 bits, not scalable. Not sure about ARM.
- Beeman: IMO, thresholds are useful but not sure we need to standardize anything. Can lean on event list to specify config not just for events but for appropriate thresholds for events.
    - Robert: concerned about every implementation doing something different, nightmare for tools
    - Beeman: if we want a standard way to apply a threshold for all events then we should standardize. Question is if we want that.
- **Out of time**. Will continue discussion on the email list.

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation