Jun 30, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong LIU Zhiwei tech.meetings@riscv.org

Notes

- **Attendees**: Ved, Bruce, Marc Casas, John Simpson, Mark H, Perrine Peresse, Jiangang, Allison, Daniel Gracia Perez, Zhiwei, Philipp, Atish, Guo Ren
- **Slides** here (sorry, forgot to record :()
- Intros for new attendees
    - Marc - work on HPC at BSC, interested in math libs for RISC-Vand perf tools, and comp arch
    - Perrine - SoC architect on IOMMU at SiFive
    - Jiangang - work at Intel, managing RV SW efforts
    - Allison - Rivos, open source and HW enablement, working on RV and security enablement
    - Daniel - work on critical embedded systems, security, working on IOMMU spec, from Thales
    - Ved - Rivos, working on RV ISA, including IOMMU and CFI, chair SoC Infra HC
- Remider: Call for chairs active! Send application to help@riscv.org by July 8.
- IOMMU PMU review
    - Slides
    - Overview of IOMMU operation
    - IOMMU PMU register interface
        - Very analogous to HPM regs in priv spec
            - But
        - Where do overflow interrupts go?
            - Can be MSIs or wire interrupts
    - IOMMU PMU is optional, but if implemented iohpmcycle and 7 programmable counters required, with min of 32 bits, along with required events
        - More typically approach (ala Priv spec) is to leave the number of counters up to platform spec or implementation, rather than in IOMMU spec
        - Discussed this in IOMMU TG, agreed that minimum requirement is warranted
        - No data behind the number 8 however, open to feedback
        - Number of events to count concurrently should inform number of counters
        - Leading edge CPUs have 8 programmable counters
        - *Agreed to take this offline*
    - Are events mapped to the 8 counters? No, the counters are programmable, numbers of events and counters are unintentionally aligned
    - Other typical MMU events might include filters for page size or request type (e.g., read vs write)
        - Didn't want to make those required, not all IOMMUs will support multiple page sizes

        - Grouping these events in the lowest event encodings does make it tricky to cluster, e.g., TLB miss, with future/custom permutations like read TLB miss, write TLB miss, etc.
            - Could use upper bits of event ID as sub-event ID
        - No other feedback. Number of counters remains to be discussed, but otherwise the proposal looks good to this group.
- Out of time, will discuss counter delegation next time

Action items

- [ ] Philipp Tomsich - Jun 2, 2022 - look for owner for perf RISC-V user interface