Jan 12, 2023 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: Beeman, JohnS, Atish, Bruce, Ved, Anup, StasN
- **Slides/recording** here
- Supervisor Counter Delegation interface
    - Recap of the proposal
        - Forgot to include shpmeventXh CSRs in slides, that adds 29 more CSRs total
    - Atish: we have around 500 RW CSRs, this would use 121 of those
    - Covered limitations of indirect counter interface, even with autoincrement. Doesn't help with common context switch scenarios, when counters to switch aren't consecutive.
    - Agreement that a direct interface is preferred
    - Beeman will revise the proposal and send to the group for review, then will send to AR committee
- minstret & mcycle priv mode filtering
    - Reviewing proposed ifc
    - Bruce: could use prog counters instead of cycle & instret
        - Beeman: true, but these counters aren't useful without filtering
    - No need for recommendation on how to count cycles on priv mode transitions. It will be up to implementations.
    - No concerns with proposal, Beeman will write up the extension and send to the group before pushing for fast-track
- User mode instret & cycle access usage (Linux)
    - Reviewed uABI and current usages of rdtime & rdcycle
    - Lots of noise in current usage, and concerns about leakage across priv modes and contexts
    - ARM & x86 require using counters through perf
    - Maintainers recommend breaking current uABI and requiring perf
    - For users that bypass perf, could trap on first access then enable context switch
        - Problem is we'll then be context switching for the rest of the process's life. No way to dealloc the counter when the app is done with it.
        - Ved: this wouldn't be a replacement for perf usage, just an alternative
        - Possible, but unlike other archs and probably not worth the effort
        - Existing users are broken anyway, using cycle for time
    - x86 clears the counters on context switch to a context that is not using them through perf, RV could do the same to avoid leakage
    - Better to clear scounteren for any apps that aren't using perf, so no risk of leakage. Will fault and SIGKILL apps that attempt to bypass perf and use rdtime/rdcycle.

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation