Aug 4, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**:
  - Beeman
  - Mark H
  - Bruce A
  - Wei Wu
  - John Simpson
  - Aaron D
  - Atish P
  - Robert C
  - Greg F
- **Slides and recording** here
- Quick recap of Supervisor Counter Delegation (from last week). Spec is here.
- **Starting review of Virtual Supervisor Counter Delegation**. Spec is here.
- Looked at interface (new bits and CSRs), and usages (full pass-through, full trap-and-emulate, and hybrid approaches)
- Greg: thinking about interrupt delegation w.r.t. context switch. Might just work but need to consider. Don't want to deliver LCOFI to the wrong guest.
  - Scenario: counter overflows just as trap to hypervisor (HV) occurs. Hypervisor switches to another guest, don't want LCOFI to be taken there.
  - Small window for this to happen
  - HV needs to save & clear guest interrupt pending. May need to clear interrupt enable bit first, to flush out any (skidding) LCOFI. Need to discuss this more offline.
  - Is skid ever bounded? Not really, so how to know you've waited long enough. Maybe clearing the interrupt enable does that?
- Typo: hideleg, not mideleg, delegates LCOFI to VS
- For TEE, if TVM is configured to use counters then TSM will delegate them. Don't want to have to context switch them if TVM is not using them. TSM could wait for first TVM access to counters before delegating them, and only then begin context switching them.
- Mark: Need to make sure spec includes best practices for SW
  - Beeman: tried to do that in current drafts
- For trap-and-emulate, can do lazy context switch but you still need to disable counters to ensure they don't keep counting in the next guest context. So do have to write event selectors before starting the next guest.
  - Perf core framework takes care of this, resets hpmevent regs
- How often will a guest want to access countinhibit?
  - Only scenario I (Beeman) had in mind is a guest OS profiling itself. Would write countinhibit at beginning of LCOFI handler, to avoid counting events there.

- Mark: HW designers, how onerous is this to implement?
    - Beeman & Greg: not too expensive
- Does this group agree with the direction?
- Greg: more argument for Supervisor delegation, for VS deleg how much perf difference? Esp if SBI has batch support
    - Beeman: agree that justifying VS delegation would need perf data
    - Atish: started PoC of batch support. Supervisor deleg is useful, save traps for config and counter start/stop. For VS deleg, deleg isn't useful for KVM because need traps. TSM not sure if VS deleg will be helpful, context switch overhead may be too much. Likely still will have some traps, to wait and see if TVM is using counters.
    - Will have Atish present new bulk SBI interface in next meeting
- Beeman will follow-up offline on where to go from here on delegation proposals

Action items

- ☐ Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- ☐ Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- ☐ Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation