May 5, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong LIU Zhiwei tech.meetings@riscv.org

Agenda

- Any new introductions (5 min)
- Charter review and approval (10 min)
- Gap analysis planning (45 min)

Notes

- Attendees: Beeman, Zhiwei, Bruce, Jessica, Anup, StephaneE, Atish, Aaron
- Slides and recording posted here
- No suggested changes to charter, or objections to ratifying it. **Charter is ratified!**
    - **AI**: Beeman Strong to update the github
- Gap analysis planning discussion
- Stephane: see CPU PMU but don't see platform PMU
    - Beeman: on next slide
- Stephane: virtualization of PMU
    - Beeman: that kind of falls under access, but yes we need to ensure PMU virtualization is straightforward
- Bruce: there is a standard set of events in SBI
    - Question about how much that implies that these encodings are standardized in the architecture, vs SBI translating event IDs to HW encodings
    - Jessica: Implementations vary quite a bit, SiFive CPUs don't have event IDs but have event bitmasks. Not needed with enough counters.
    - Atish: SBI just standardizes events from supervisor SW perspective. May be added to platform spec in the future.
    - Anup: also nice for VMs to know some events it can use w/o knowing underlying HW
- Bruce: would like to see auto-preset capability on at least one counter
- Stephane: Counter discovery, esp for VM
    - Don't want a number of counters where a VM assumes it has access to all, or a contiguous set
    - Discovery for width too
        - Stephane: not sure perf can handle counters of varying width
    - Atish: currently all are discovered by SBI call, one time at the beginning
- Stephane: is there a way to sample in critical sections where interrupts are masked
    - Could give LCOFI interrupt highest priority, so only LCOFI is taken?
        - Aaron: no HW managed context, so reentrancy is corrupting
    - Requirement to be able to sample when interrupts are masked, by whatever means
- Bruce: mtime, should there be standards for rate or access?
    - Gets complicated with multi-core/cluster, is it distributed and invariant?

    - Some of this may fall under SoC Infra HC, **AI** Beeman Strong to talk to Ved
- PAPI uses a library (libpfm4) to map event name to encoding, very simple
- Bruce: add kutrace tool
- Jessica: add FreeBSD to kernels. How to include emulator and perf modeling work (QEMU, SAIL, spike)? Should we be driving that?
    - Perf modeling SIG focused on perf models (like gem5)
- Stephane: look at IBM Power arch as well. Do have precise sampling, branch sampling, etc. Have top down. Some interesting things.
    - Need to have the events for initial bucketing, ala top-down
- Zhiwei (offline): look at both functional and cycle-accurate (perf) simulators, and tools to collect and analyze events
    - Beeman (offline): definitely need functional simulator to include PMU ISA. cycle-accurate is more implementation dependent, but could define some interfaces to help standardize event validation.

Action items

- [x] ~~Beeman Strong - Apr 25, 2022 - send out updated charter for review~~
- [x] ~~Beeman Strong - Apr 25, 2022 - add upcoming meetings to Tech calendar~~
- [ ] Beeman Strong - May 5, 2022 - to talk to Ved about mtime purview
- [ ] Beeman Strong - May 5, 2022 - to update the github with ratified charter updates