Nov 3, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: RobertC, Fei, Ved, BruceA, JohnS, Beeman, Atish, Anup
  - Fei Wu from RISC-V SW team at Intel, doing performance work
- **Slides/video** here
- Meeting cadence and timeslot sharing
  - *Group agrees with moving meeting time to weekly, sharing timeslot with CTH TG and any other TGs*
- Standardizing events vs encodings
  - Standardizing encodings adds some burden to HW, and would require an extension define more fields in event selector CSRs
  - Robert: for tools awkward when implementations do things similarly but not the same. Will always have some standard and some custom events.
  - Intel & SiFive use “type and mask” approach, where mask allows multiple events to be selected at once. But uses more bits.
  - ARM simply uses the next available value when standardizing a new event
  - Implementations may prefer to choose encodings based on implementation (e.g., type is based on functional block where the event is counted)
  - Ved: could firmware provide an event list through DT? Then don’t have to go find it, delivered with the implementation
  - Bruce: perf already supports JSON event lists
  - *Agreed to revisit once we settle on the events to be standardized*
- instret and Virtualization
  - Exposing inst counts across mode/trust boundaries is unusual
    - Can be confusing when counts don’t match expectations, due to a trap.
    - Robert: Or could be useful, to know when such traps occur.
    - Bruce: can use a programmable counter for filtered instret
  - Is there legacy SW that depends on this behavior?
  - Atish: Linux used to always expose instret and cycles, but removed it when SBI ifc added, out of side-channel concern.
    - Switched to enabling instret access on demand
    - That broke some user SW, but all broken SW should have been using time.
      - Dangerous assumption that time and cycle are interchangeable
    - Reverted kernel, now CSRs are available in user again
  - ARM64 allows access via sysfs, accessible only for your context
  - Intel also has priv mode filtering on all counters (but not RDTSC)
  - Atish: believe filtering not added for cycle & instret bc mcountinhibit used the CSR addr

    - Could have instret & cycle share filter config, would keep them in sync and avoid quirk with mhpmevent0 not available
    - *Beeman to consider drafting a fast-track extension*

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation