Sep 22, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: Beeman, John S, Marc, Atish, Bruce, Greg, Philipp, Anup, Aaron, Zhiwei, Jeff S
- **Slides/video** here
- Opens:
    - Please review Supervisor Counter Delegation Fast Track Architecture Extension
    - Control Transfer History TG interim chairs will be Beeman Strong (Rivos) and Bruce Ableidinger (SiFive). Will aim to start next month.
- Standardized and discoverable events
- Make tools portable
- X86 has short list of architectural events
- Lean on JSON file for providing events, encodings, etc to tools
- ARM has much longer list of common events, though only a few are required
- ARM has flat encoding approach, unlike x86. A bit disorganized.
- ARM often allows flexibility on retired vs speculative, which is nice for implementation flexibility but a bit unpredictable for tools
- Linux perf has list of standard events
- Linux cache events do have some nonsensical combinations (e.g., write to icache)
- An implementation could adopt the SBI encodings for their HW
- 20b field has 4b for event type (HW, CACHE, etc) then code below that
    - There are bits remaining to further filter the events
    - For raw events (type=0), can pass 48b encoding
- Bruce suggested looking at Rocket core and SiFive encodings
- What is standardized should be what is best/right, not biased toward existing implementations
- For discovery, trying to push unified discovery forward
    - But event discovery is different. Each implementation has a JSON file. ARM indicates which standard events are supported.
    - Want to originate discovery in the same place
    - JSON approach already works with existing SBI, infrastructure is in place
    - Let's discuss more how the two approaches relate as unified discovery progresses
- Only considering CPU events for this discussion, but on the list for future events is standardizing SoC/Uncore PMUs and events
- **Next meeting** let's start putting together a list, in the interim send any thoughts to the mailing list

Action items

- ☑ ~~Beeman Strong - Sep 8, 2022 - work on TG for branch history~~

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation