Apr 20, 2023 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: Beeman, Bruce, Guillem, JohnS, Ludovic, RobertC, Atish
- **Slides/video** here
- Introductions
    - Ludovic, working on perf analysis tools at Rivos
    - Guillem, working on PMU at Frontgrade Gaisler
- Updates
    - S*cdeleg/Smcntrpmf: awaiting AR review to complete. Believe we're close.
    - CTR TG: good progress, will have an initial spec soon. Aim to freeze Q2, ratify in Q3
    - Perf Events TG: awaiting volunteers to chair. On backburner until then.
        - Guillem: SBI events are interesting, including organization
        - Guillem: But would be nice to be able to create combinations of events
            - Would mean that HW wouldn't use SBI encodings, which is fine
    - Software:
        - KVM counting support pushed, sampling support WIP
        - SBI bulk access and ABI changes WIP
        - Sampling when interrupts masked direction defined
            - Robert: what will be the noise/latency of blindspot avoidance?
                - Should be faster because current LCOFI handler runs a lot of code
                - Still working on plan but will have numbers soon, will PoC on OpenSBI/QEMU
- Reviewed gaps and priorities agreed upon last year
    - See slides
    - No proposed changes
    - ISA gaps on hold until some resources emerge, likely once CTR freezes
    - Need to consider next steps to make progress on analysis tool(s). Investigate collaboration opportunities.

Action items

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