Dec 1, 2022 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: Beeman, Ved, RobertC, JojoR, JohnS, StanislavN, BruceA, GregF, Atish, AnupP
- **Slides/recording** here
- Background on instret/cycle counters
    - Main use is fast user reads, calculate deltas between
    - Linux/KVM devs concerned about exposure of kernel counts to user, removed access but put it back when code broke
- (started recording here)
- Robert: counter noise won't be a big problem, sampling interrupts aren't frequent
    - Beeman: more concerned about page faults, exceptions, & external interrupts, which are more common
- Robert: uarch events like cache misses are hard to get precise on mode change boundaries
- Proposal: new mhpmcfgic CSR with priv mode filter bits that apply both for instret & cycle
    - Same format as event selector CSRs. OF forced to 1, other bits WARL/rsvd
- Greg: should this be extended to S mode?
    - Beeman: would expect the delegation proposal to allow that
    - How would we delegate it, which bit(s) to set? Could influence CSR addr
    - S-mode shouldn't be able to write MINH
- Robert: should we implement things before we standardize them? Get them out in the field and get learnings first?
    - Beeman: SW enabling is harder if we build custom, and such an approach would delay RV maturation, takes 5+ years to get real feedback
    - Robert: this was the approach for trace extensions
- Anup: this method easy to POC, but think we should have separate priv mode filtering for cycle and instret
    - Easier for SBI, and more flexible
    - Greg: need to have justification, don't just add bits/CSRs without it. Motivation here is a security concern
    - Atish: having single filtering for both works for security concern. But if user asks for counter for kernel cycles, should we deny them? Or should that make instret count in kernel as well?
        - Could give them a programmable counter when they want different filtering for these events
        - Will these events be required? TBD, part of standardized event discussion
    - Ved: could say if a user asks for instret or cycles you get the other as well

    - Robert: believe we should make it separate
    - Greg: for performance monitoring these counters are special, don't have full functionality that other counters have. Is the motivation for this security, or performance monitoring? Will INH bits be set once at boot?
        - Beeman: these counters are for performance monitoring, but want to make sure they can't be used for attacks. This proposal should also benefit monitoring users, by eliminating noise.
    - These counters are assumed to be there by user code today, so part of uABI unintentionally.
        - At least most of them are using cycle when should be using time
        - Time can be slow and low-res, so some opt to use cycle
        - But if we're going to maintain this as part of uABI, that these counters are always available, then likely that priv mode bits are set once and static
        - Thus SW already treats these counters as special, this proposal does not make them so
    - Ved: if user can ask for counter to count kernel events and get it then it defeats this extension
- **Ran out of time**. Will continue discussion on email list.
- Did not get to freeze topic, and no meeting in 2 weeks (RISC-V summit)

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation