Sep 21, 2023 | RISC-V Perf Analysis SIG Meeting

Attendees: Beeman Strong tech.meetings@riscv.org Marc Casas

Notes

- **Attendees**: Beeman, BruceA, JohnS, Chun-Nan Ke, AtishP
- **Slides/video** here
- Extension updates:
  - Smcntrpmf frozen, S*csrind ARC approved, Smcdeleg/Ssccfg in ARC review
  - CTR TG has stable spec for internal review
- RISC-V Summit
  - Beeman & Atish will do an ISA & SW status talk
  - Have a room for in-person meeting Mon, Nov 6, 11:30am, Room 212
- RISE Debug & Profiling WG is working on SW enabling for RISC-V
  - Nice progress on perf, others moving more slowly
- SoC PMU discovery
  - ARM has standardized ACPI table (APMT) for this
  - Should consider something similar when standardizing SoC PMUs
- Priorities slide
  - What is DynamoRIO?
    - Dynamic binary instrumentation tool
  - Will autofdo be enabled once CTR is ratified?
    - Autofdo doesn't depend on CTR, but perf profiles with CTR will get better results. Autofdo may just work, need someone to try it.
  - Expect CTR TG members to roll off into the next TG when it disbands?
    - Hopefully yes!
- Done early

Action items

- [ ] Atish Kumar Patra - Aug 25, 2022 - check on how to read multiple counters in perf when taking an interrupt on one
- [ ] Beeman Strong - Jul 28, 2022 - Reach out about proprietary performance analysis tools
- [ ] Beeman Strong - Jul 28, 2022 - Reach out to VMware about PMU enabling
- [ ] Beeman Strong - Jul 28, 2022 - Talk to security HC about counter delegation