	Intel Resource Director Technology (RDT)	**ARM Memory Partitioning and Monitoring (MPAM)**	**AMD Platform Quality Of Service**
ID for allocation	32-bit wide (architecturally)	16-bit wide (architecturally)	Same as RDT
ID for monitoring	10-bit	8-bit	Same as RDT
Enforced on	CPU accesses	CPU and IO devices (request marking by SMMU)	Same as RDT
Cache Capacity Monitoring	L3	all cache heirarchies	Same as RDT
Cache capacity monitoring capabilities	L3 capacity usage for a monitoring ID	capacity usage filtered by a monitoring and allocation ID	Same as RDT
Cache Capacity Allocation	L2 and L3	all cache heirarchies	L3
Code vs. Data differentiation	L2 and L3	all cache heirarchies	L3
Cache Capacity allocation units	Capacity bitmap where each bit represents a portion of cache capacity	Capacity bitmap where each bit represents a portion of cache capacity + optional maximum fraction of cache capacity	Same as RDT
Memory bandwidth monitoring	Memory Bandwidth at egress of L3	Memory bandwidth (at memory channel)	Same as RDT
Memory bandwidth monitoring	BW to local memory, BW to remote memory - at egress of L3	read and write, read, write (at memory channel)	Read BW to local memory, Read BW to remote memory - at egress of L3
Memory bandwidth allocation	Memory Bandwidth at egress of L3	Memory bandwidth (at memory controller)	Memory Bandwidth at egress of L3
Memory bandwidth allocation units	delay values to throttle - linear or non-linear - in discrete increments (e.g, 6%)	fractions of bandwidth; min, max, and portion bitmap	Absolute BW in units of 1/8 GBps
Arbitration priority	Not supported	Supported	Not supported