



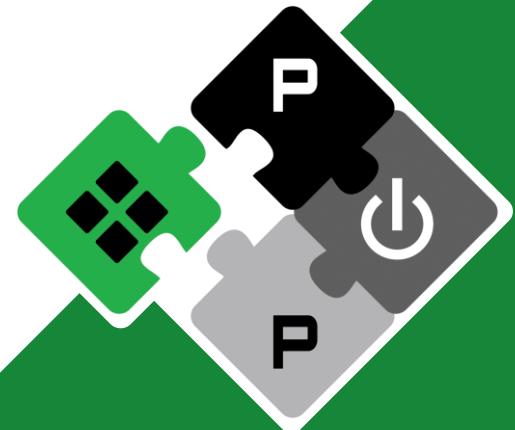
Industry Academia Collaborations on Open-Source Hardware

Integrated Systems Laboratory (ETH Zürich)

Frank K. Gürkaynak kgf@iis.ee.ethz.ch

PULP Platform

Open Source Hardware, the way it should be!



@pulp_platform

pulp-platform.org

youtube.com/pulp_platform

OCCAMY

432 RISC-V cores

Chiplets

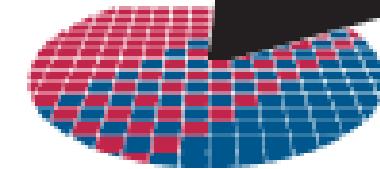
GF12nm

1GHz

Occamy: A 432-Core 28.1 DP-GFLOP/s/W 83% FPU Utilization Dual-Chiplet, Dual-HBM2E RISC-V-based Accelerator for Stencil and Sparse Linear Algebra Computations with 8-to-64-bit Floating-Point Support in 12nm FinFET

How do we manage to design projects of this size at a University?

2024 VLSI



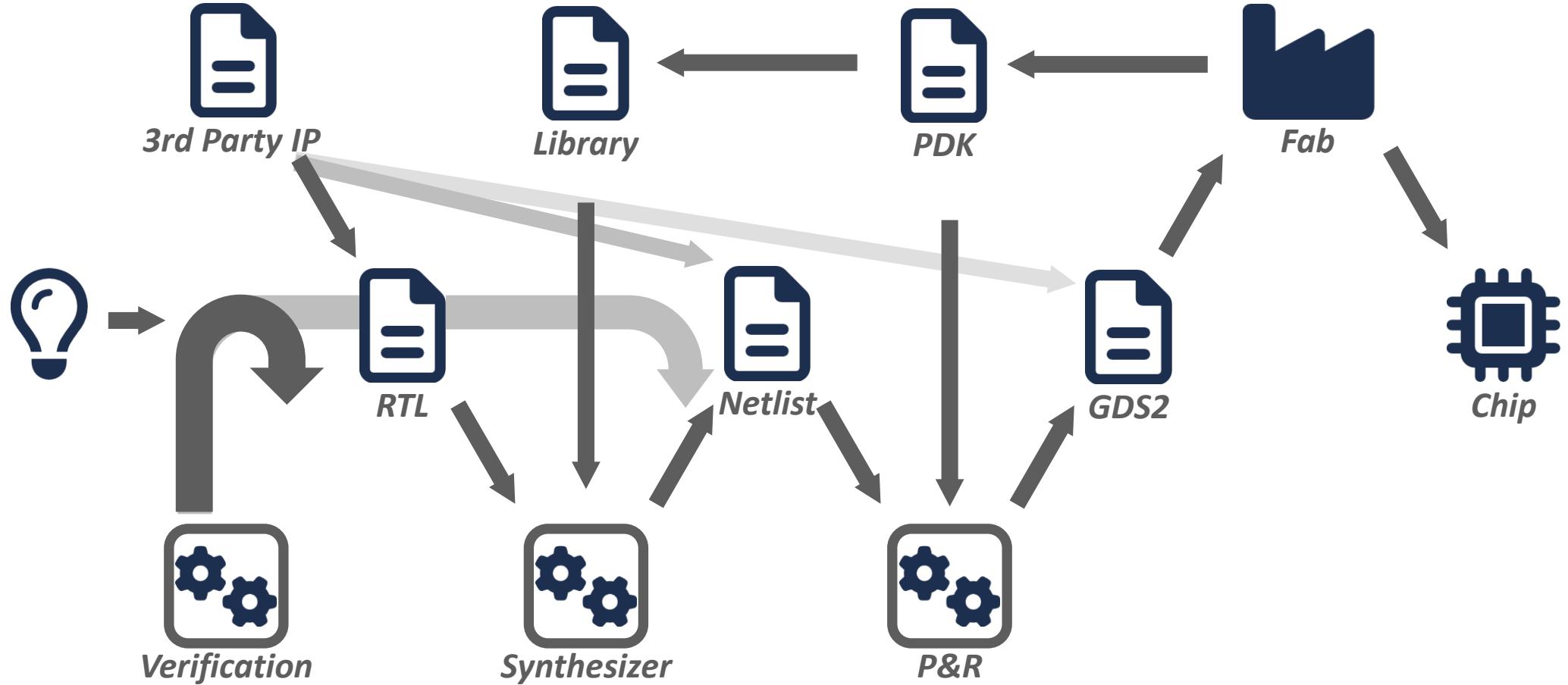
SYMPOSIUM

In 11 years PULP team has designed more than 60 chips



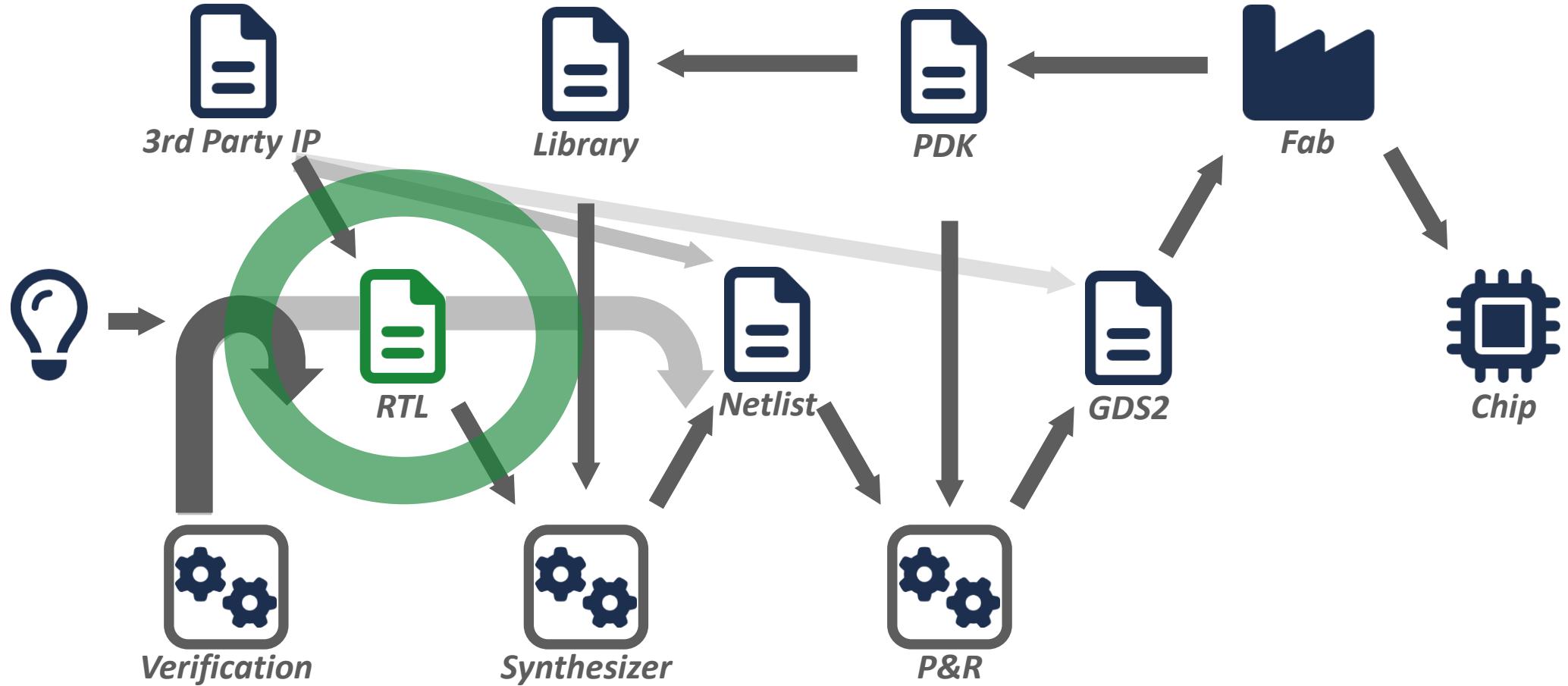
RISC-V and open-source hardware have been instrumental in our success

A simplified view of the IC design flow



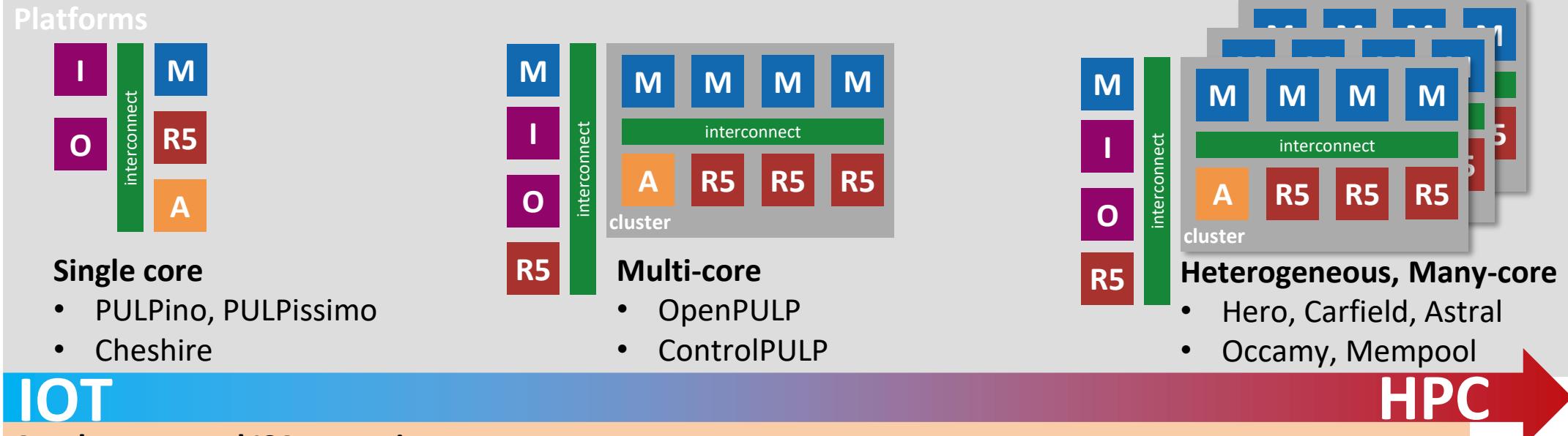
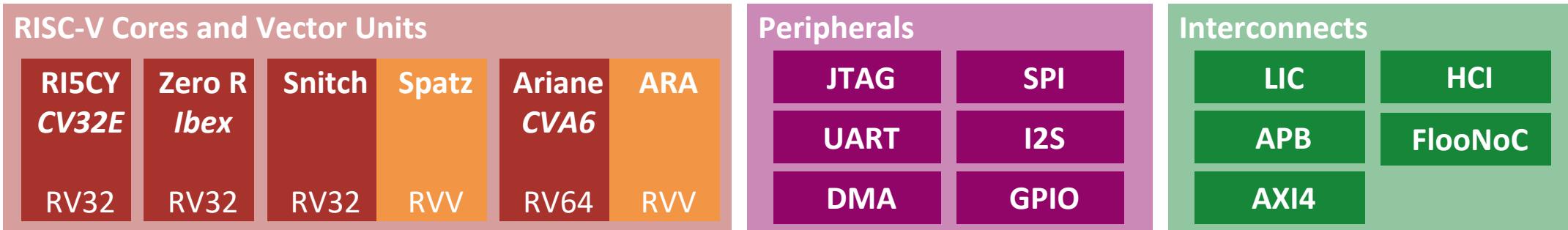
Icons taken from free icons from fontawesome.com

Most of open source hardware is at RTL level



Icons taken from free icons from fontawesome.com

We have created a sandbox to design System on Chips



We make everything (we can) available openly



- All our development is on GitHub using a **permissive** license
 - HDL source code, testbenches, software development kit, virtual platform

<https://github.com/pulp-platform>



- Allows anyone to use, change, and make products without restrictions.

pulp-platform

Overview Repositories 239 Projects 1 Packages 14 People 14

Pinned

pulp Public

This is the top-level project for the PULP Platform. It instantiates a PULP open-source system with a PULP SoC (microcontroller) domain accelerated by a PULP cluster with 8 cores.

SystemVerilog 312 93

pulpissimo Public

This is the top-level project for the PULPissimo Platform. It instantiates a PULPissimo open-source system with a PULP SoC domain, but no cluster.

SystemVerilog 288 137

snitch Public

Lean but mean RISC-V system!

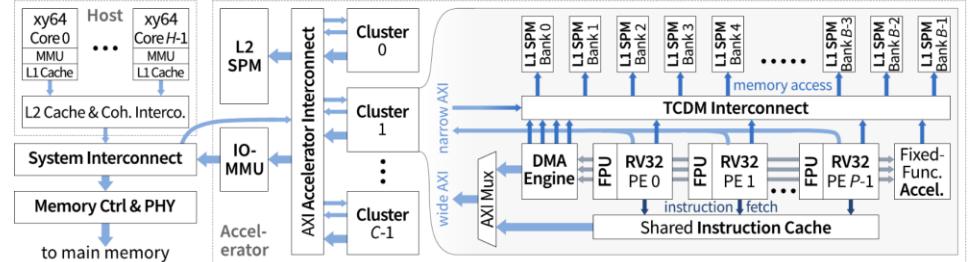
hero Public

Heterogeneous Research Platform (HERO) for exploration of

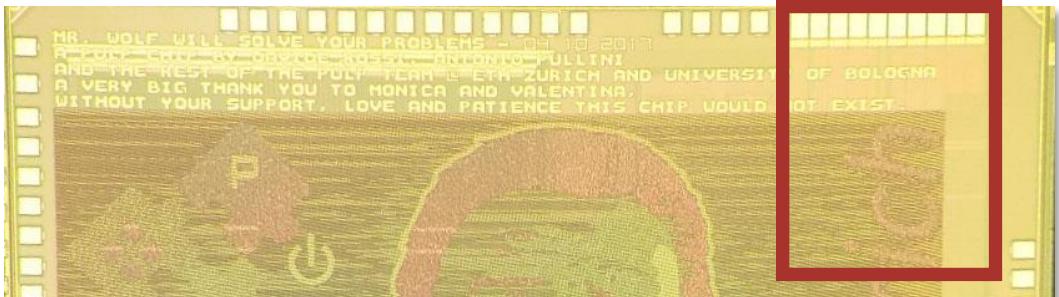
Heterogeneous Research Platform (HERO)

HERO is an **FPGA-based research platform** that enables accurate and fast exploration of **heterogeneous computers** consisting of **programmable many-core accelerators** and an **application-class host CPU**. Currently, 32-bit RISC-V cores are supported in the accelerator and 64-bit ARMv8 or RISC-V cores as host CPU. HERO allows to **seamlessly share data between host and accelerator** through a unified heterogeneous programming interface based on OpenMP 4.5 and a mixed-data-model, mixed-ISA heterogeneous compiler based on LLVM.

HERO's **hardware architecture**, shown below, combines a general-purpose host CPU (in the upper left corner) with a domain-specific programmable many-core accelerator (on the right side) so that data in the main memory (in the lower left corner) can be shared effectively.



Meet Mr. Wolf (2017) in TSMC40



- **Very successful IoT processor**
 - 8+1 RISC-V cores
- **Power converter IP from Dolphin**

Win (PULP): get to use professional IP in our chips



- the company to demonstrate their industry relevant design
 - RTL for the entire SoC openly available

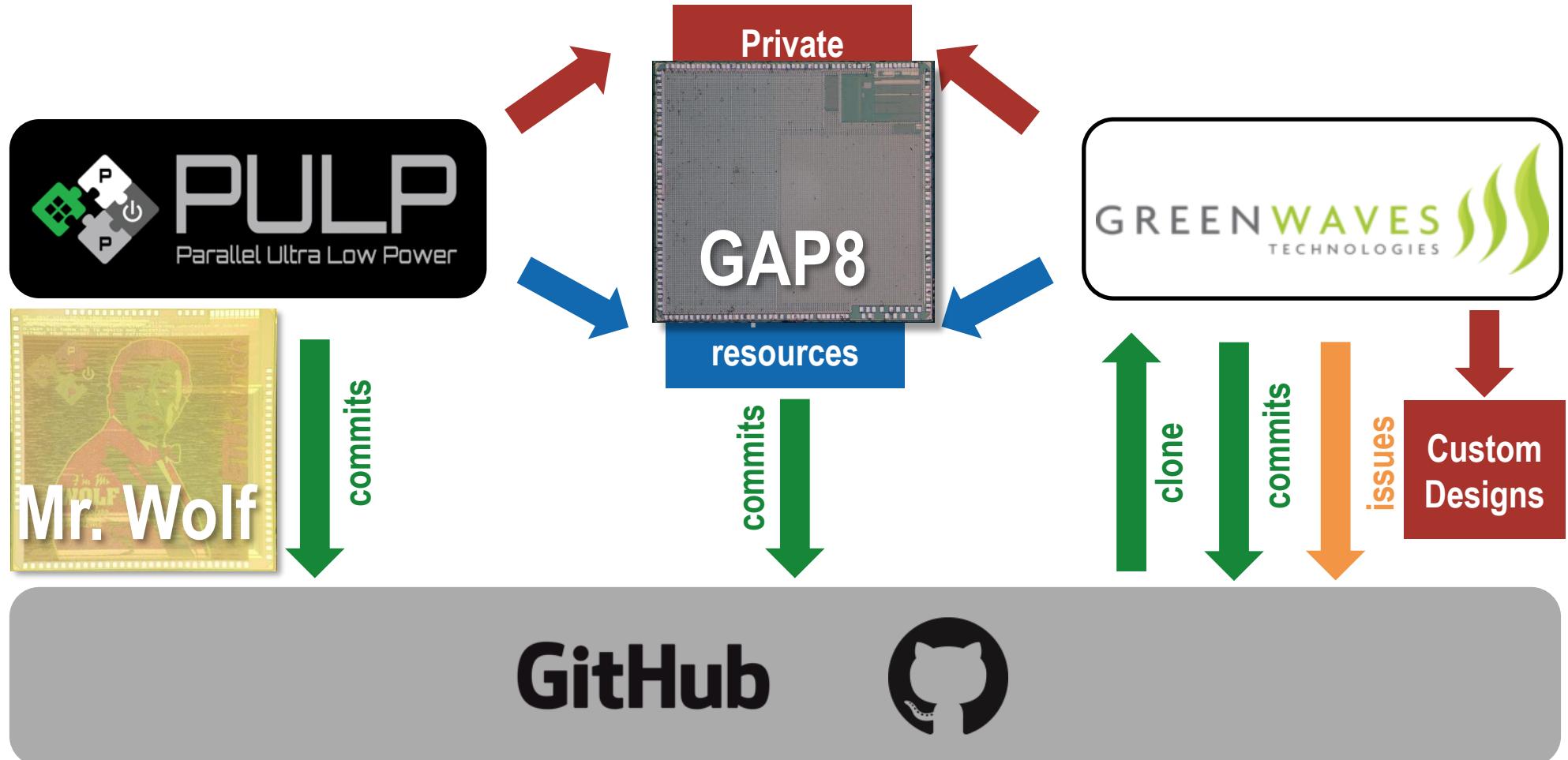
Win (Dolphin): demonstrate their IP on a SoA design



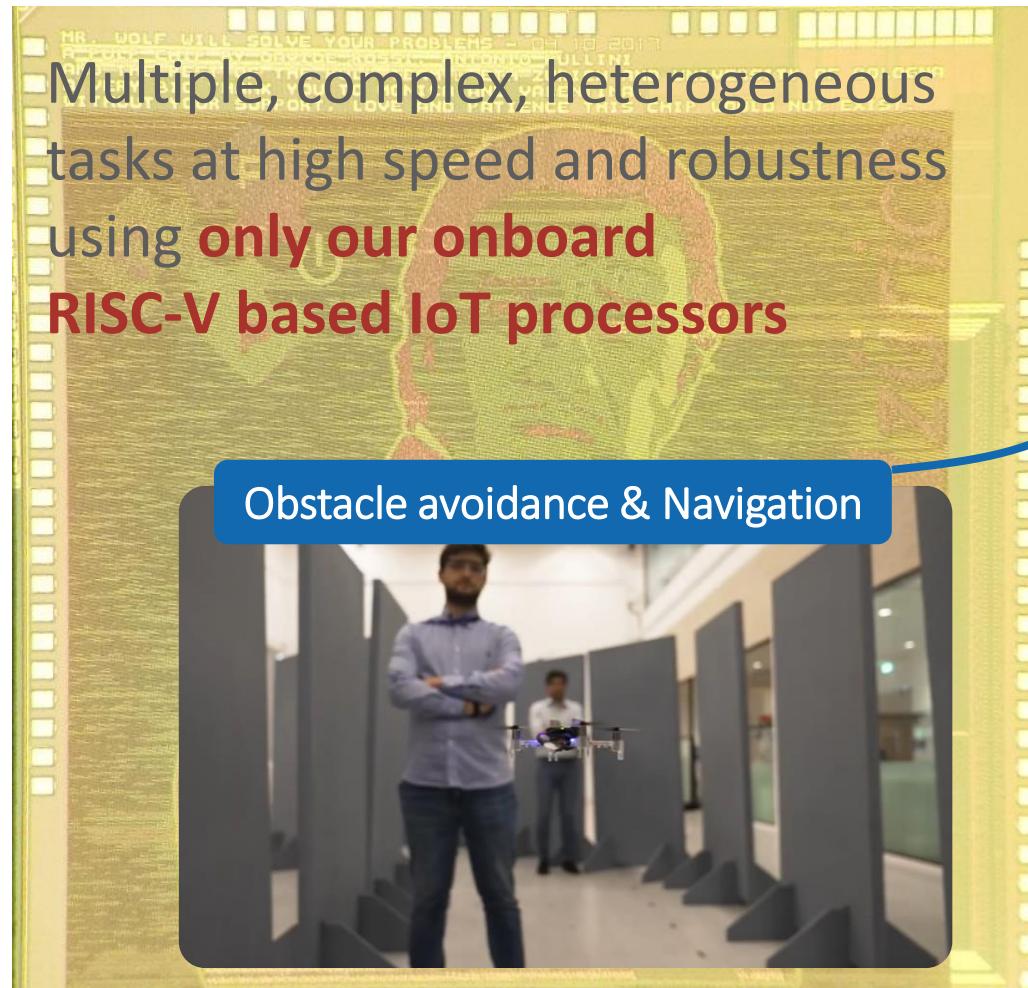
- **Design formed the basis of GAP8/9**
 - By Greenwaves Technologies

Win (Greenwaves): SoC template that can be easily productized

How does PULP collaborate with 3rd parties?

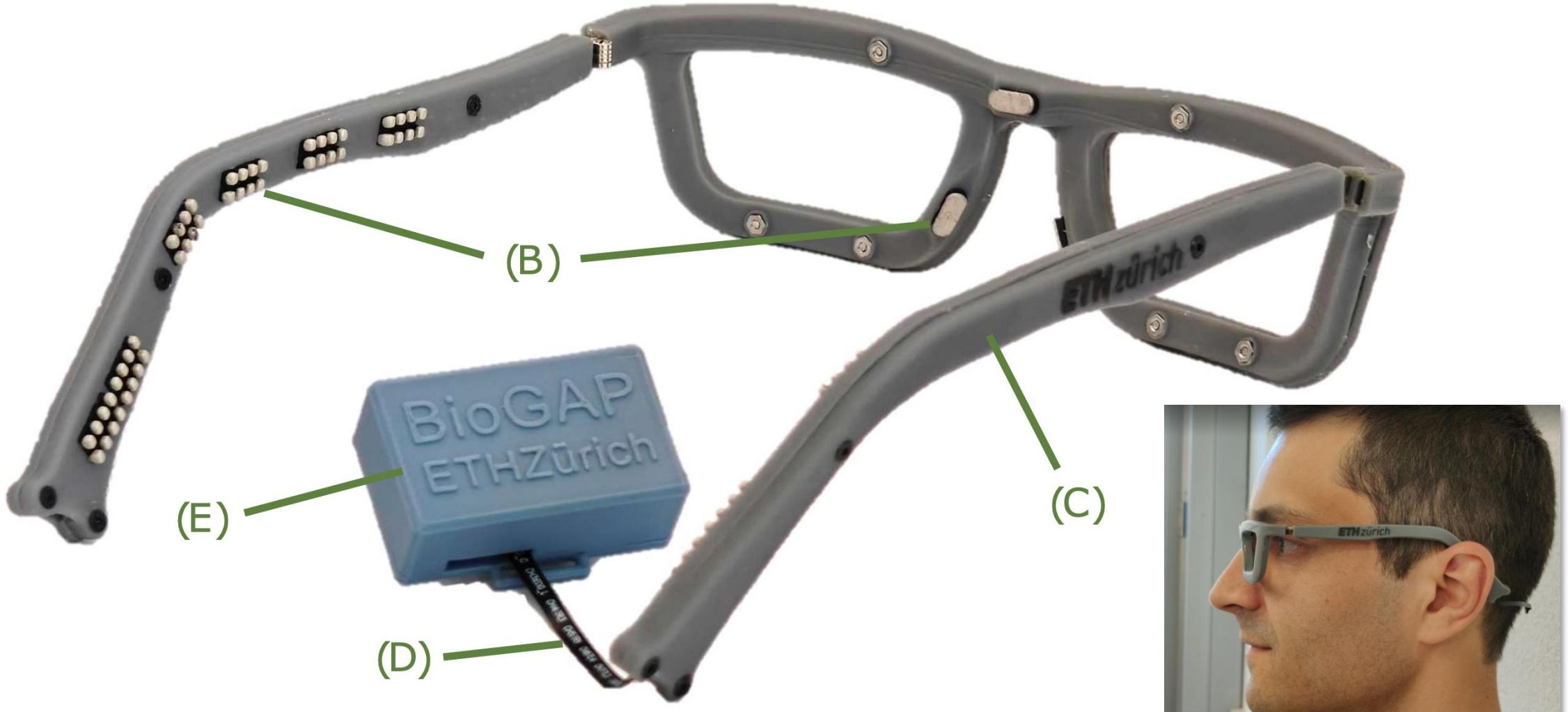


Designs derived from Mr. Wolf powered our nano-drones

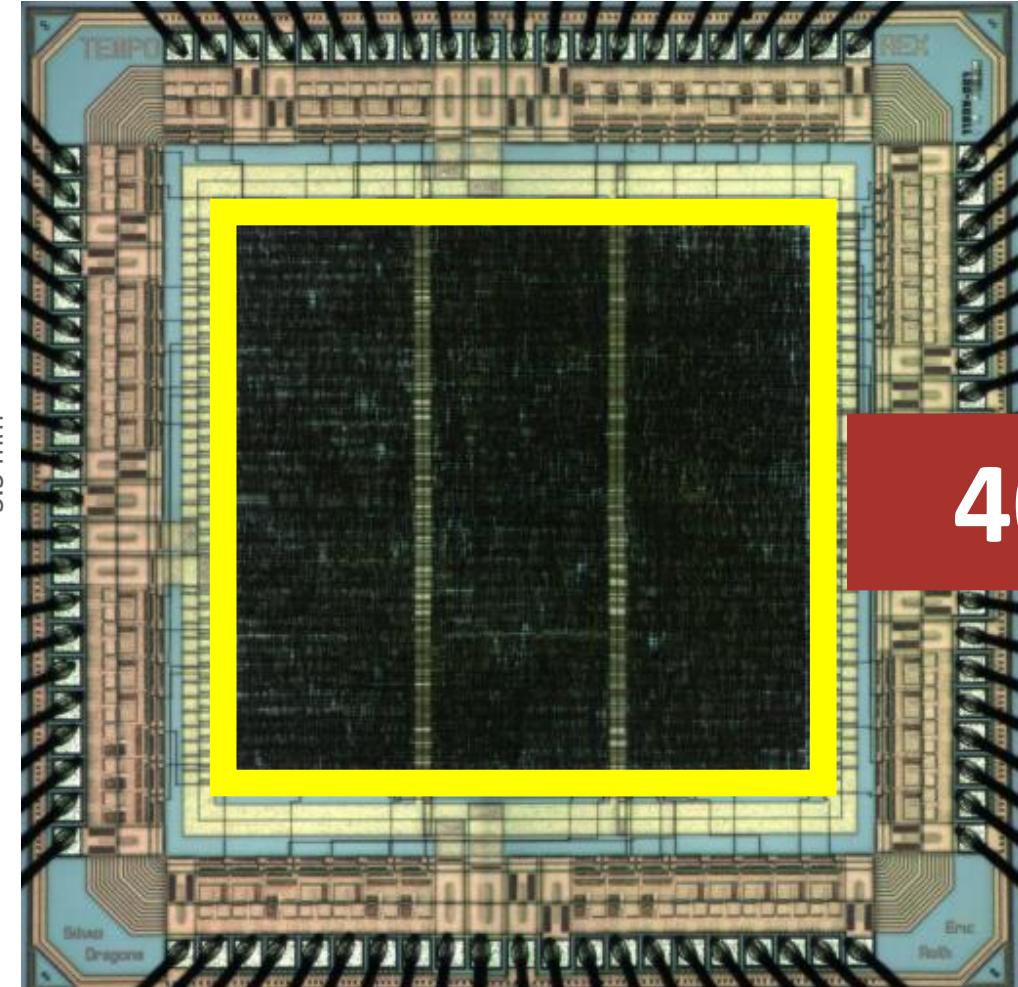


Multi-GOPS workload at extreme efficiency → P_{\max} 100mW

As well as our bio-signal acquisition systems



In the last 20 years IC Design has changed a lot



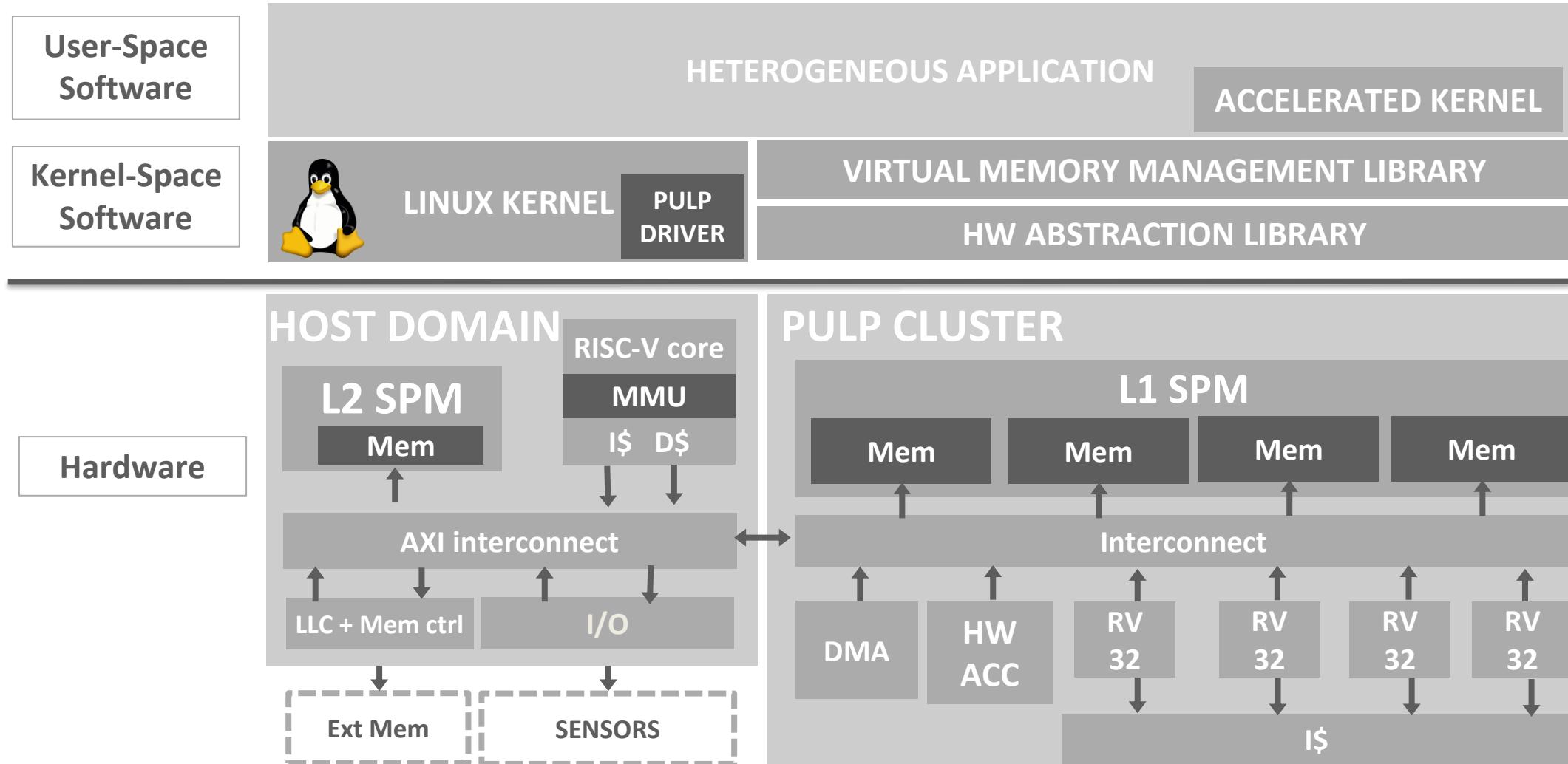
4000 x



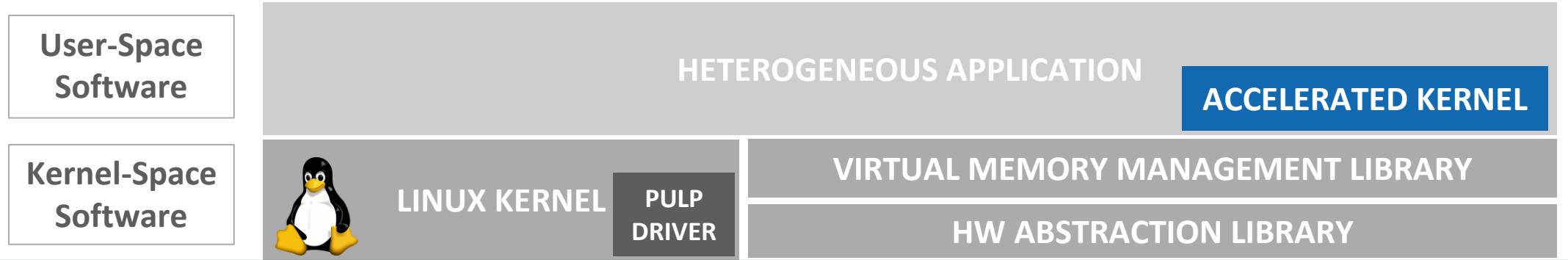
80 MGE

What used to be a complete chip is now a small part of a SoC !

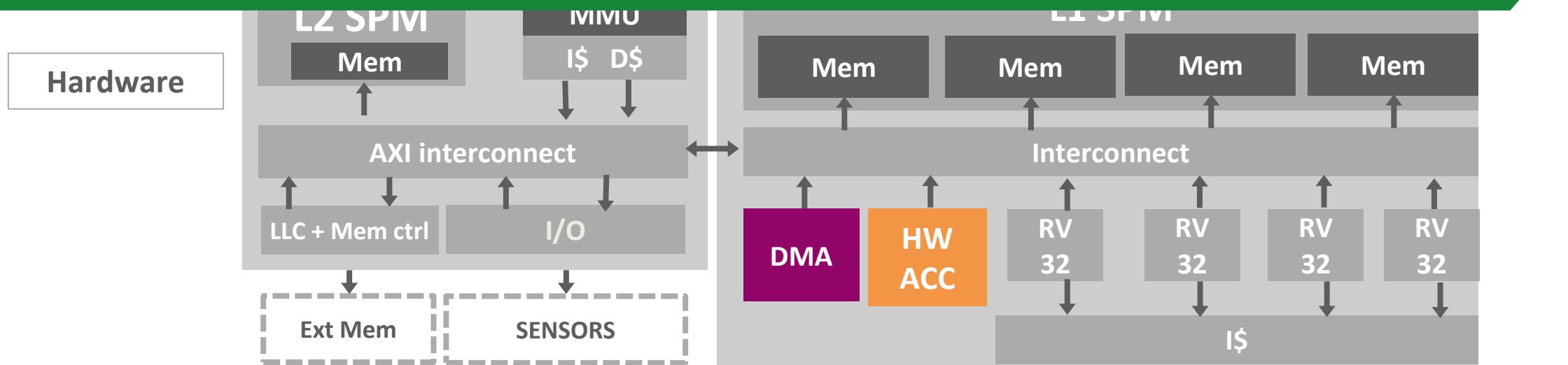
There is so much that makes up a modern SoC



In a typical design, innovation is only in a limited scope



Open-source silicon-proven SoC template helps concentrate work where it counts



Diverse set of open source based industry collaborations



GF22 (2018)

Arnold

eFPGA coupled with a RISC-V microcontroller.

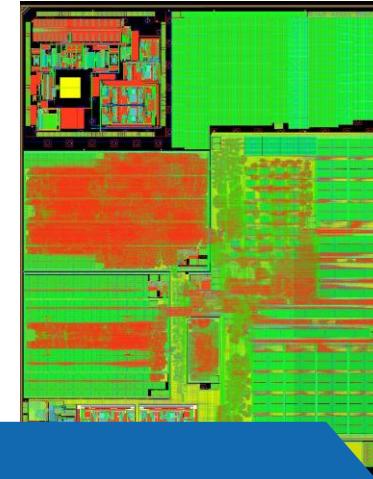
In one year from agreement to actual tapeout



GF22 (2022)

Marsellus

Heterogeneous IoT processor
With Aggressive voltage scaling

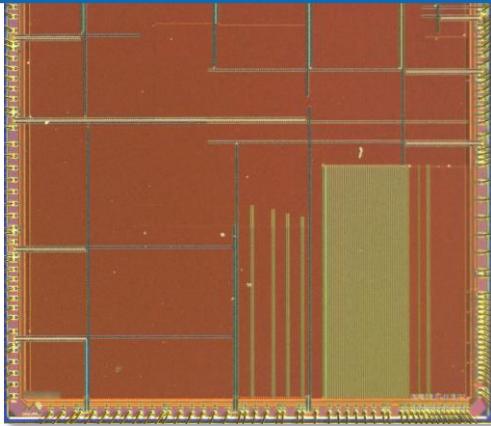


DU PHIN

Permissive open-source licensing key to our industrial relationships

Siracusa

SoC for Extended Reality visual processing

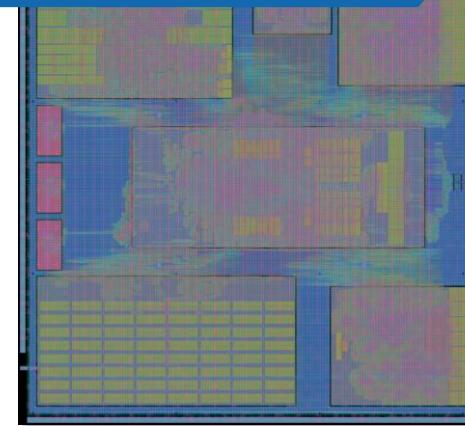


Meta

Carfield

Open-Research platform for safety, resilient and time-predictable systems

intel®



And many continue to use our work for their research



Smallest RISC-V Device for Next-Generation Edge Computing

RISC-V Workshop

Our 1st gen. processor and 2.5D integrated device

Processor SoC(D2) SoC size: 300µm x 250 µm, GF14LPP
SoC arch: Based on PULPino (RV32IMC) On chip memory: 2KB data SRAM + Authentication engine + Analog custom circuits(LDO, Clock/Reset, PD/LED IF)

Seiji Munetoh¹, Chitra K Subramanian², Arun Paidimari², Yasuteru Kohda¹, IBM Research – Tokyo¹ & T.J. Watson Research Center²

RISC-V week Barcelona 2018

An 8-core RISC-V Processor with Compute near Last Level Cache in Intel 4 CMOS

Gregory K. Chen, Phil C. Knag, Carlos Tokunaga, Ram K. Krishnamurthy
Circuit Research Lab, Intel Corporation, Hillsboro, OR, USA, gregory.k.chen@intel.com

Processor Dimensions: 1939 µm wide, 991 µm high.

ISA	RV64GC
Execution	Out-of-order
L1i	16kB/core, 4-way
L1D	8kB/core, 4-way
NoC	64 b 2D Mesh
L2 LLC	512kB, 4-way
LLC BW1GHz	1.0 Tb/s
CNC Area Overhead	1.4%
#CNC MACs	128
CNC RF	1kB/slice
Energy Eff. 0.6V	285 GOPS/W
LLC Energy Eff. 0.6V	1.6 TOPS/W

VLSI Symposium 2022

The Deep Learning Revolution and Its Implications for Computer Architecture and Chip Design

Presenting the work of **many** people at Google

AutoDMP: Automated DREAMPlace-based Macro Placement

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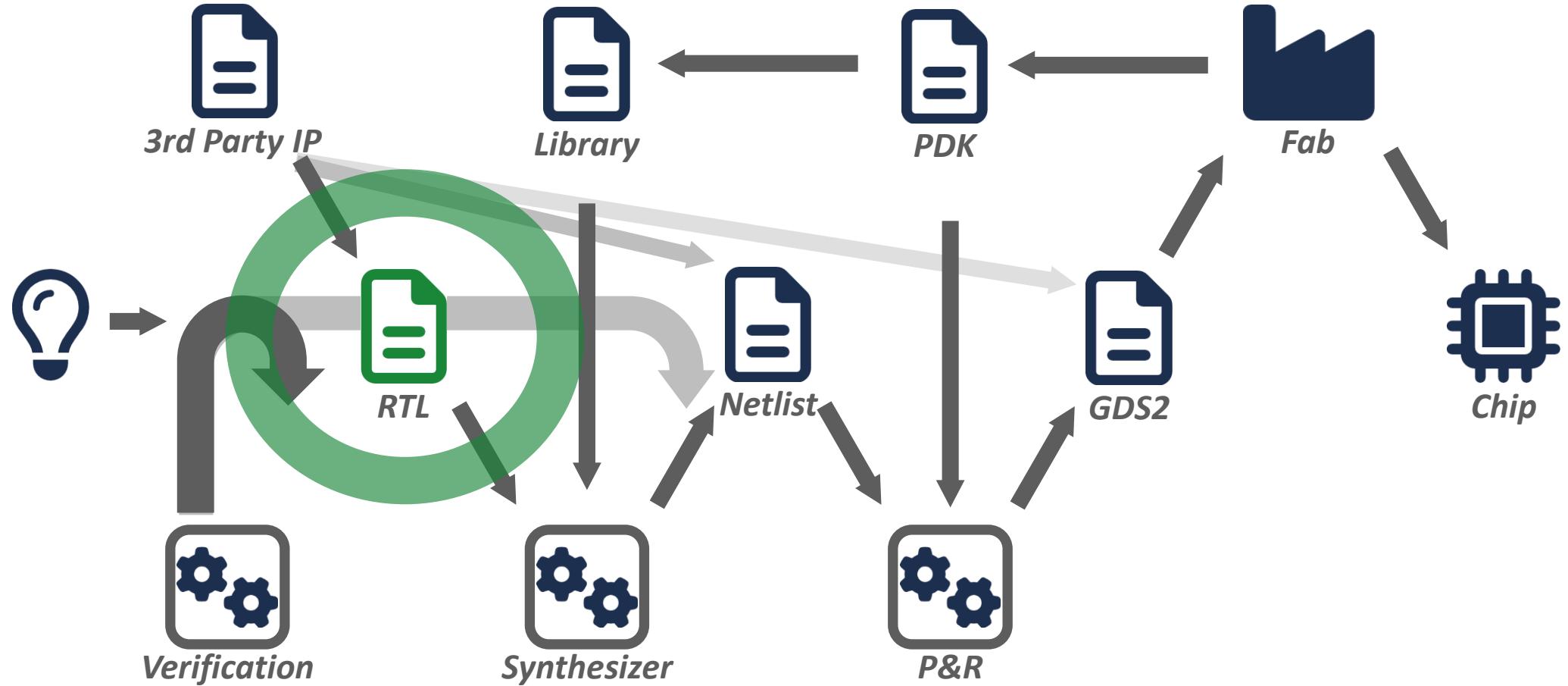
ISSCC Keynote 2020 – Nature 2020

Accepted: 13 April 2021
Published online: 9 June 2021
Quoc V. Le, James Laudon, Richard...

ISPD'23

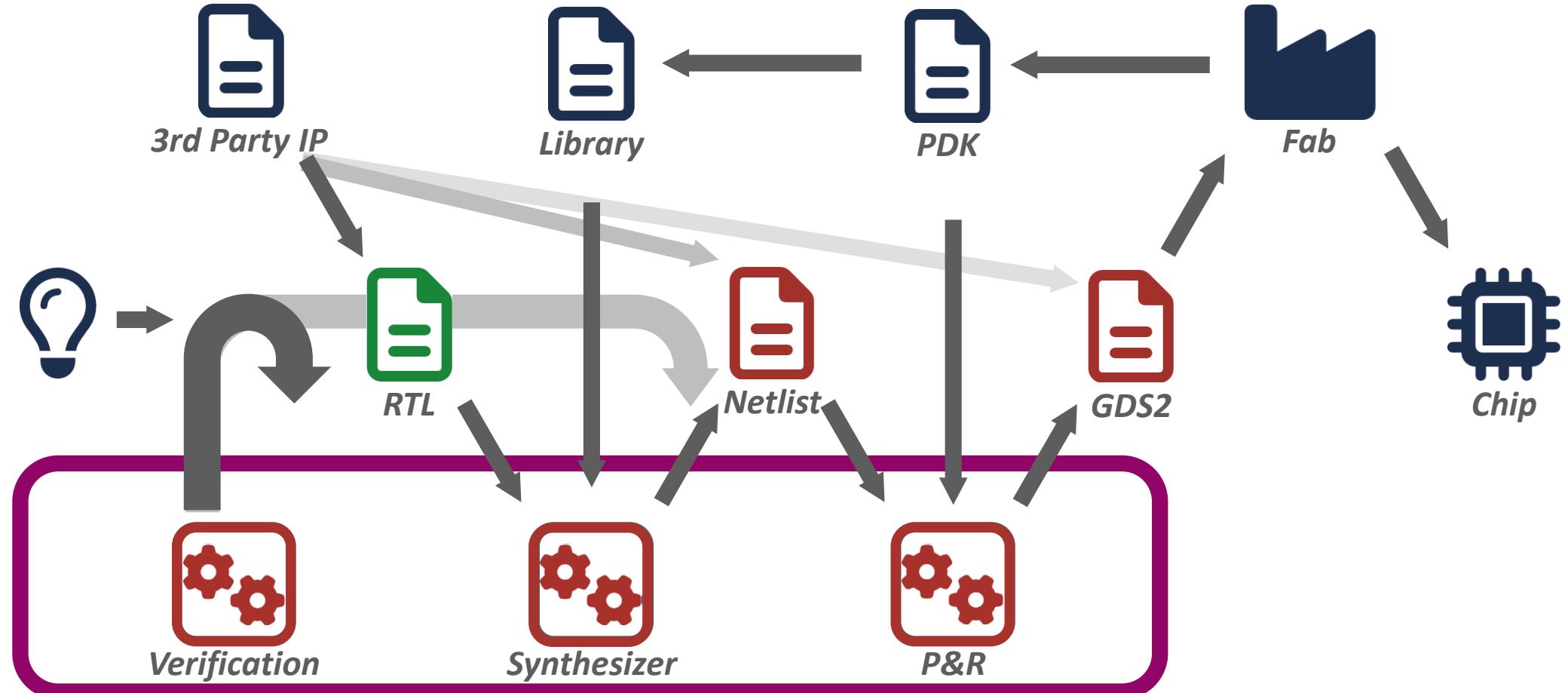
Figure 7: Pre-CTS placements of the logical groups and cell densities of the MemPool Group designs using NanGate 45nm process (freq. = 333 MHz, density = 68%). Congestion (H/V): Innovus (2.66%/1.54%), AutoDMP (3.48%/1.86%).

Unlocking the rest of the design flow: Open PDK and EDA



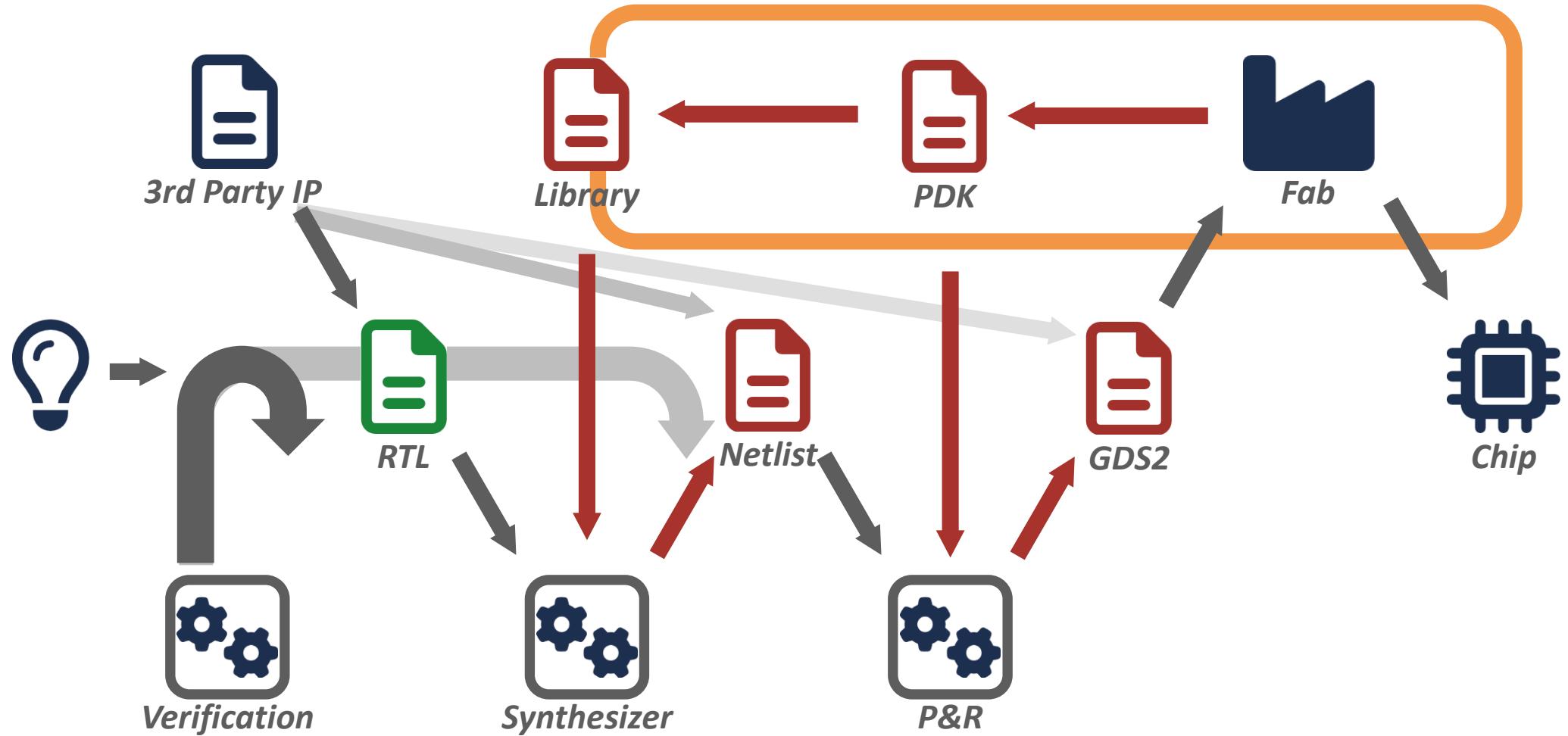
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The output (and even scripts) of EDA vendors are closed



EDA vendors limit the output of their tools

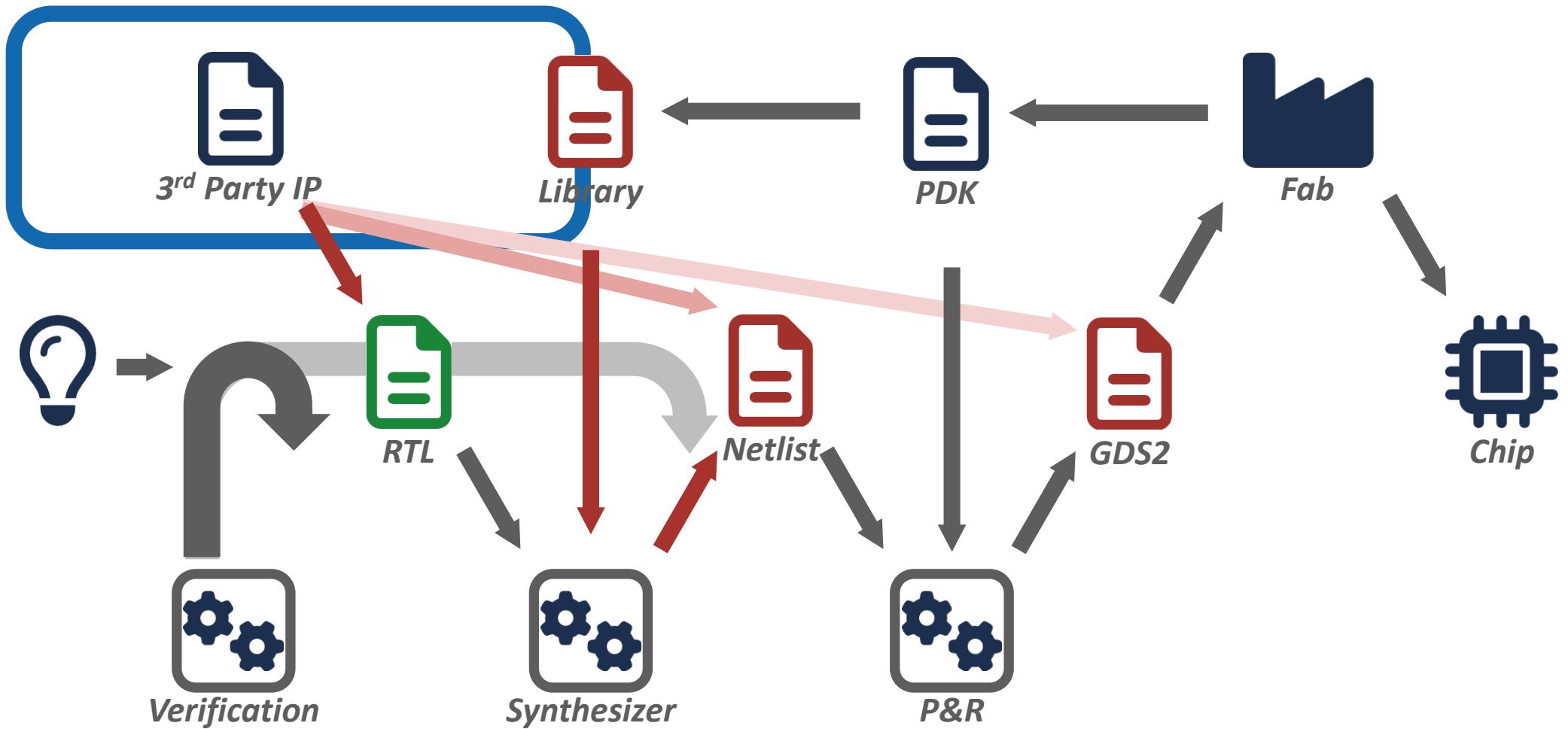
The chip will contain information from the PDK of the Fab



Icons taken from free icons from fontawesome.com

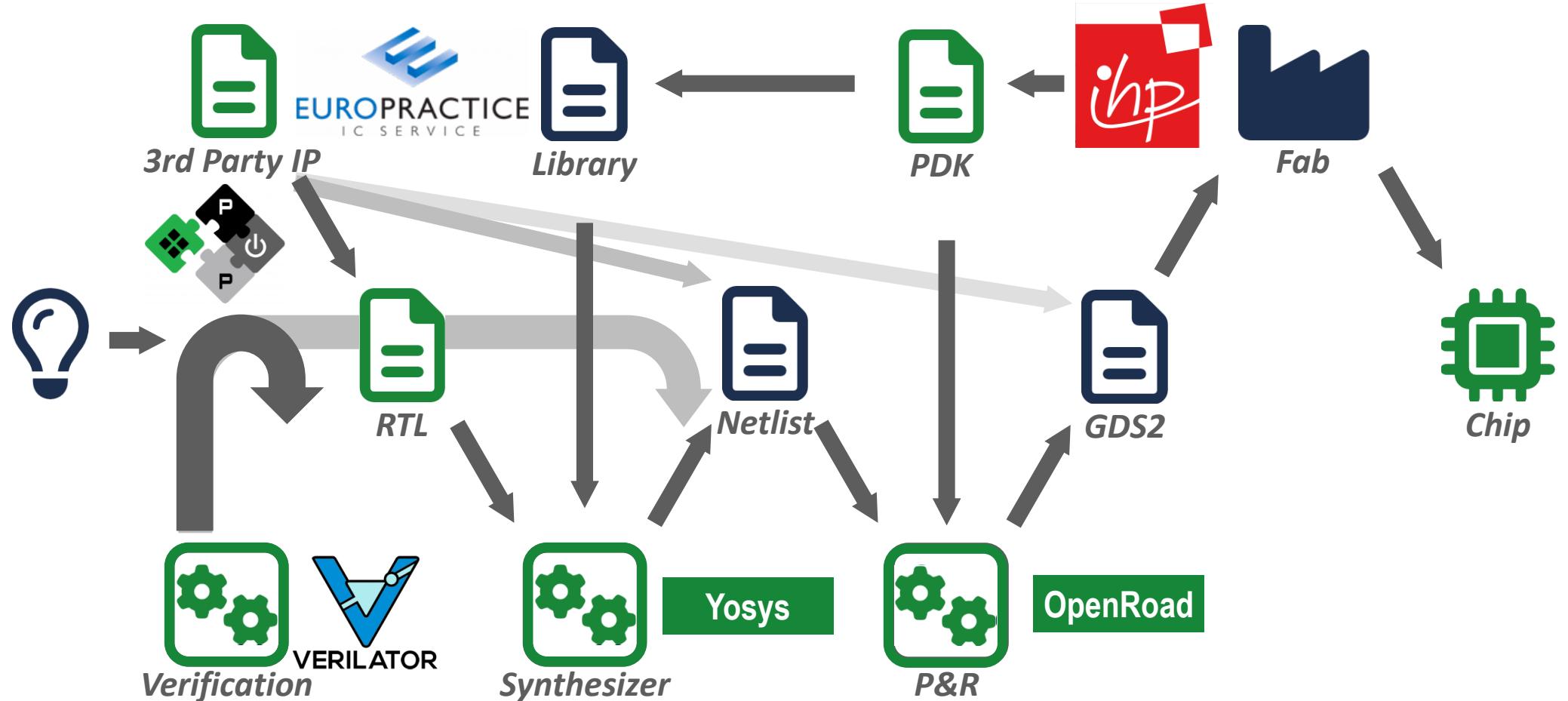
Fabs do not make PDK information accessible

Most designs will include some 3rd party IP



3rd party IP when included can limit what can be open sourced

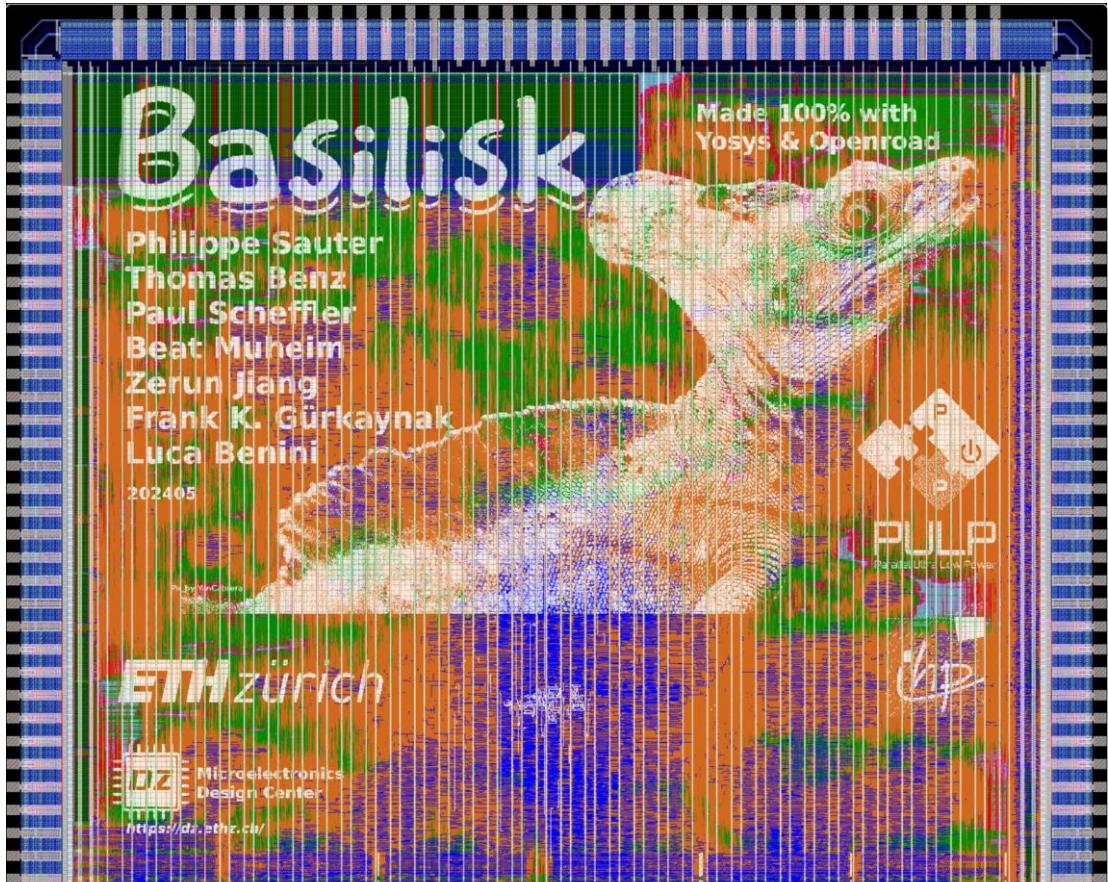
We need openness along the whole chain: RTL, EDA, PDK



Icons taken from free icons from fontawesome.com

We are getting there, first fully open chips are underway

Meet Basilisk: Open RTL, Open EDA, Open PDK



- **Designed in IHP 130nm OpenPDK**
 - 6.25mm x 5.50mm
 - 60MHz
 - 1.08 MGE logic, 60% density
 - 24 SRAM macros (114 KiB)
- **CVA6 based SoC**
 - Runs and boots Linux
- **Active collaboration with**

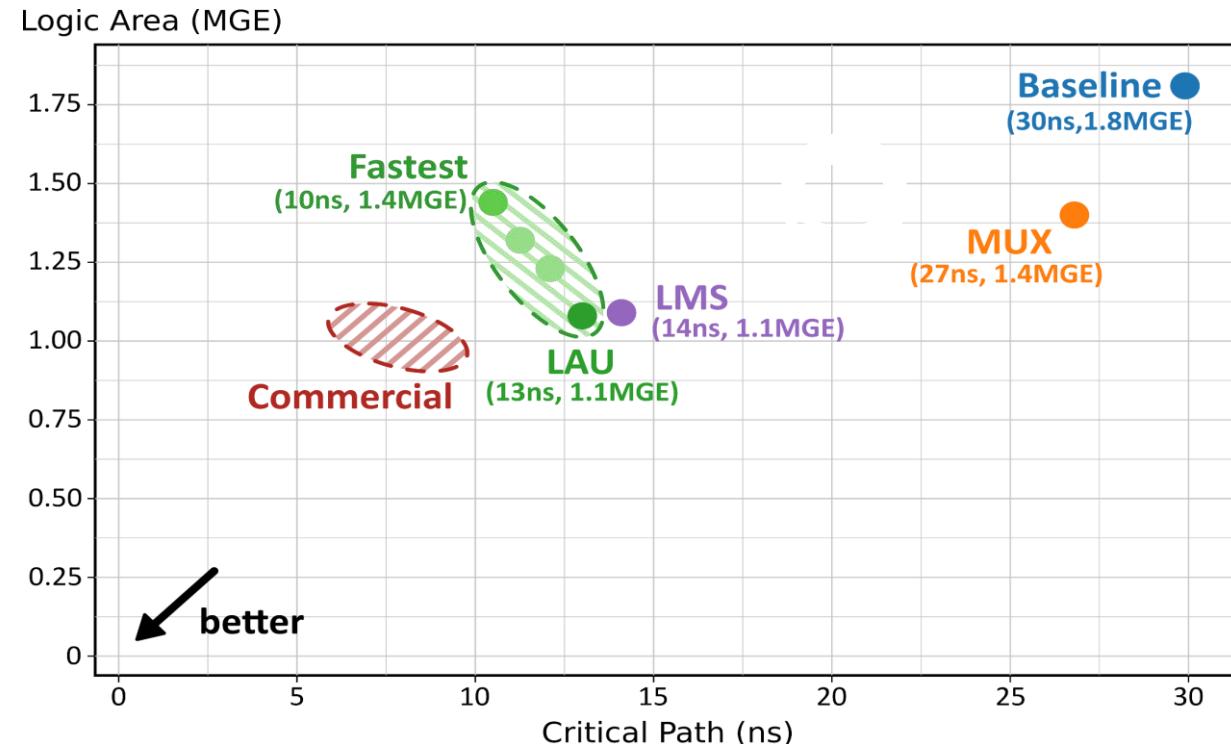


Open-source EDA tools already enable complex designs, it will only get better

Working with open-source EDA groups to close the gap!



- **Basilisk is the first end-to-end open-source Linux-capable RV64 SoC**
 - DRAM interface & rich IO (USB 1.1, VGA, SPI, ...)
 - Silicon-proven, configurable, MGE-scale design
- **Improved FOSS EDA flow**
 - SV-to-Verilog chain @ **<2min** runtime
 - Yosys synthesis:
 - **1.1 MGE (1.6x)** @ **77 MHz (2.3x)**
 - **2.5x** less runtime, **2.9x** less peak RAM
 - OpenROAD P&R: tuning
 - **-12%** die area, **+10%** core utilization



github.com/pulp-platform/cheshire-ihp130-o

Benefits of end to end openness



Research

- Easier collaboration (no NDAs)
- Reproducible results, benchmarking
- **Combined impact of design and design automation**

Education

- Increased accessibility
- No black boxes, full visibility
- **Experiment with flows and tools**

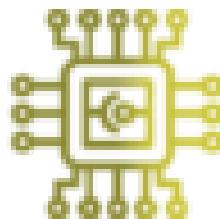
Industry

- Transparent chain of trust, sovereignty
- Lower initial cost
- **Faster research → product**

Our open source principles support funded projects



Successful partnerships with both industry and academia



CONVOLVE



Final words

- **We use open source because it works**

- Allows us to manage complex designs
- Facilitates Industry/Academia Relationships
- Creates Auditable Designs, Reproducible Results

There is still
more to come 😊

Helps us and others concentrate work where it matters

- **Open Source sees no borders**

- There is **no** 'European/Chinese/American Open Source',
- There **can be** 'European/Chinese/American support for Open Source'

Open Source is global, it just can have more or less support in a region/country

