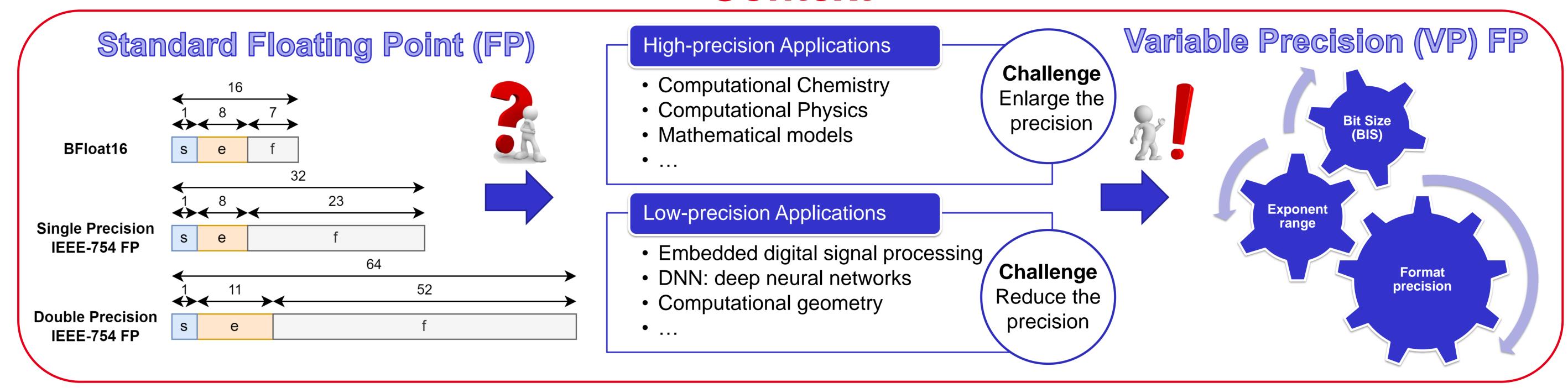


Hardware Support for Variable Precision Floating Point Formats Exploration

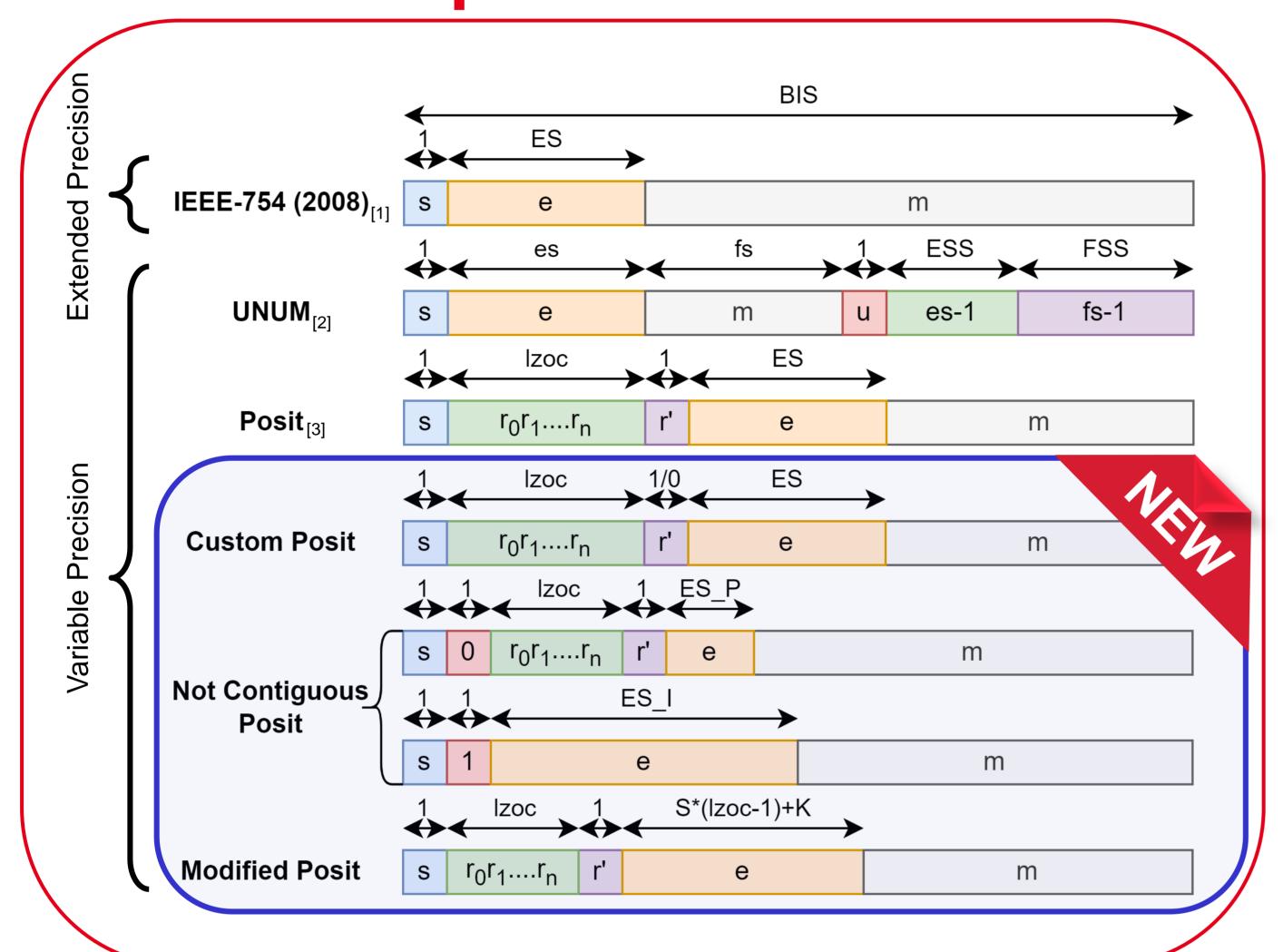
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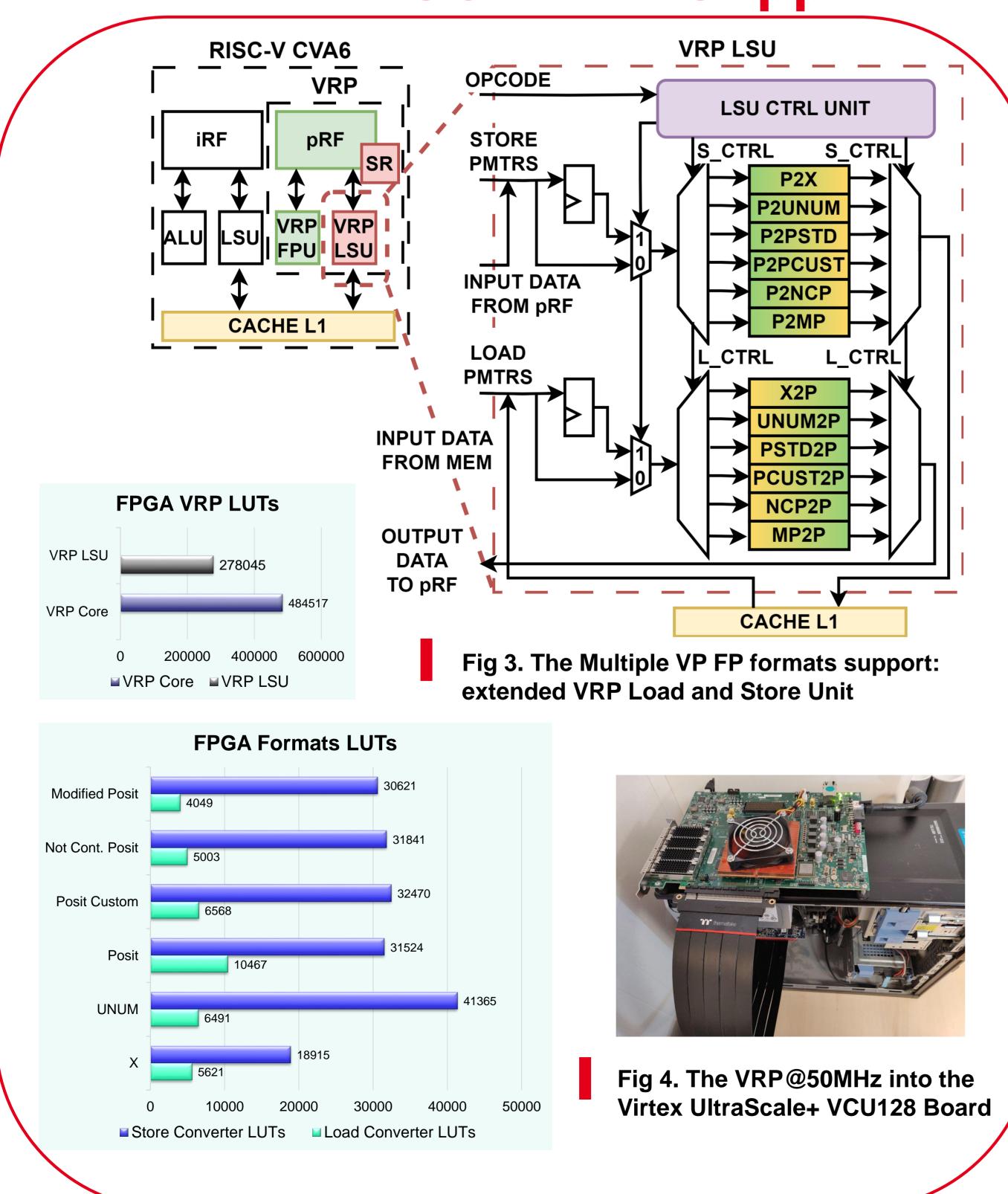
Context



SOA & Proposed VP FP Formats



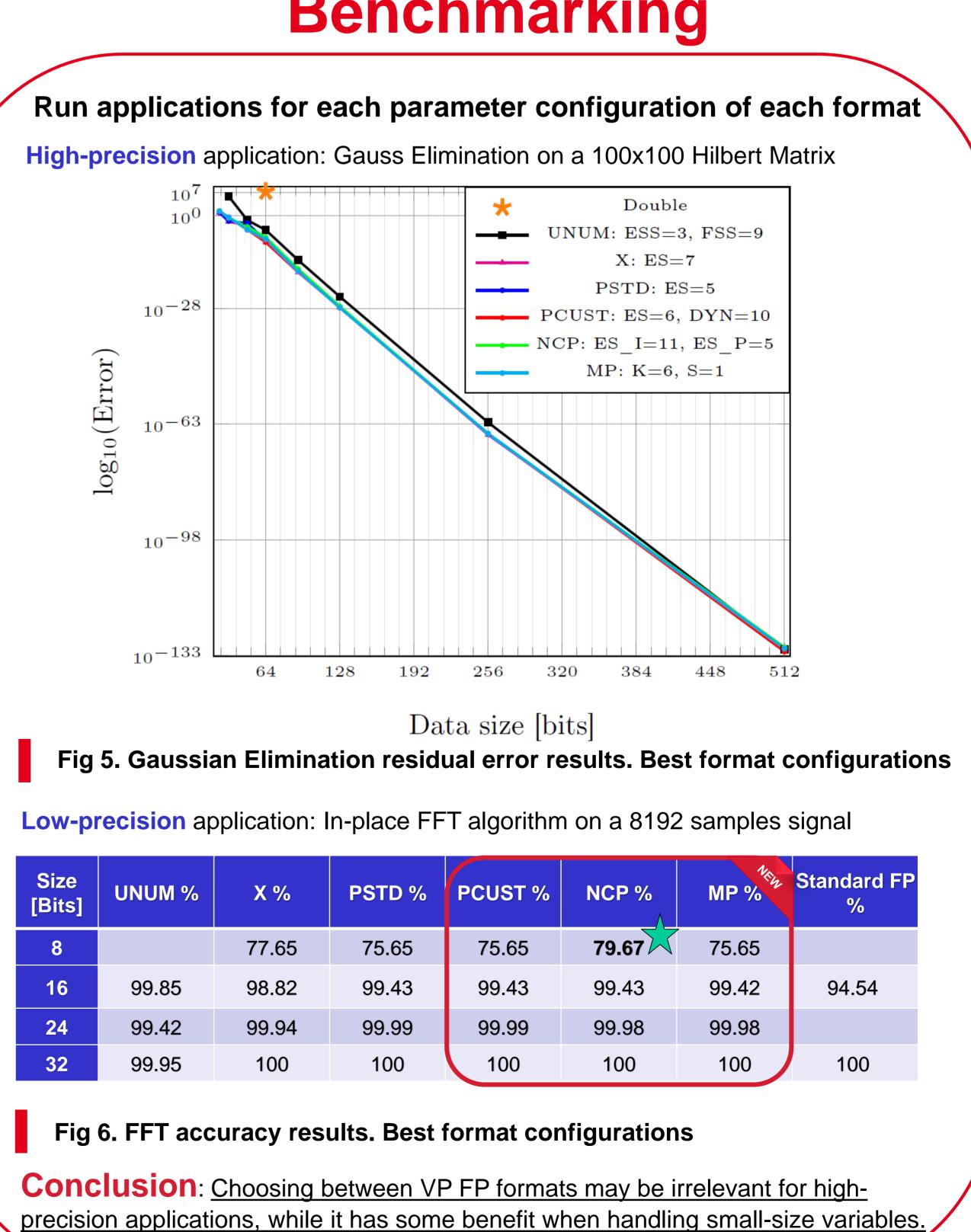
VP FP RISC-V HW Support



VaRiable Precision Core (VRP_[4])

s summ. bits L exp The VRP is a RISC-V CVA6 based accelerator for extendable FP computation [4]. It aims to facilitate the use of variable extended m_1 precision in order to improve the numerical stability of big linear algebra algorithms. $m_{2^{\Delta l}-1}$ Variable-Precision Core (VRP) Fig 2. The custom internal FP **Instruction Queue** format "P" I-Cache Decode (16KB) The VRP has two different FP formats Issue 1. P: Custom Internal FP format VRP Integer Fixed-size fields (64bit chunks) Scoreboard Regfile Regfile • Internal FP Operations (Add, Mul, ...) • Tunable Mantissa length (8 to 512bits, **Execute** 1 bit granularity) FPU 2. X: IEEE-754 Extendable **Memory** format LSU LSU ALU D-Cache Variable-size fields (32KB) Variable Integer Memory operation (Load/Store) Precision Tunable Bit Size (8 to 512bits, 1 bit granularity) Fig 1. The VRP Core_[4]

Benchmarking



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[4] Yves Durand et al. Accelerating Variants of the Conjugate Gradient with the Variable Precision Processor. doi: 10.1109/ARITH54963.2022.00017.