X-HEEP: an open-source eXtendible Heterogeneous Energy-Efficient RISC-V Platform for Embedded-class systems

Davide Schiavone, José Miranda, Simone Machetti, Miguel Peón-Quirós, Benoît Denkinger, Thomas Christoph Mueller, Rubén Rodríguez, and David Atienza

Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

Abstract

This abstract presents X-HEEP, an open-source, configurable, and extensible single-core RISC-V microcontroller targetting edge-computing, embedded-class applications.

Open-source hardware and RISC-V play key roles in a wide range of aspects, not only tackling the technology sides but also political and social consequences such as digital sovereignty, democratization, security, and many more [1]. From a technological viewpoint, open-source hardware acts like a library of Intellectual Properties (IPs) that lower the costs of developing system-on-chips: lack of fees and freedom on customization; fewer resources invested in design, and verification; and time saved for adding new features or fixing bugs, which do not depend anymore on external vendors. Within the open source revolution, RISC-V [2] emerges in many trends as the chosen Instruction Set Architecture (ISA) for microcontroller-based systems. The adoption of RISC-V brings many advantages such as high-quality specification and standardization, encouraging the leverage of the existing software frameworks such as compilers and operating systems, and customization, which today plays a crucial role to overcome energy and performance boundaries. Whereas from the social and political corners, open-source hardware bypasses restrictions over IPs, and gives everyone sovereignty. For these reasons, the Embedded Systems Laboratory (ESL) at EPFL in Switzerland, along with many other academic and industrial stakeholders, is rapidly moving towards the widespread adoption and contribution to open-source hardware. In this presentation, we will talk about *X-HEEP*, an open-source[1], configurable, and extensible single-core RISC-V microcontroller targeting edge-computing embedded-class applications.

The long-term goals of *X-HEEP* are summarized as follow:

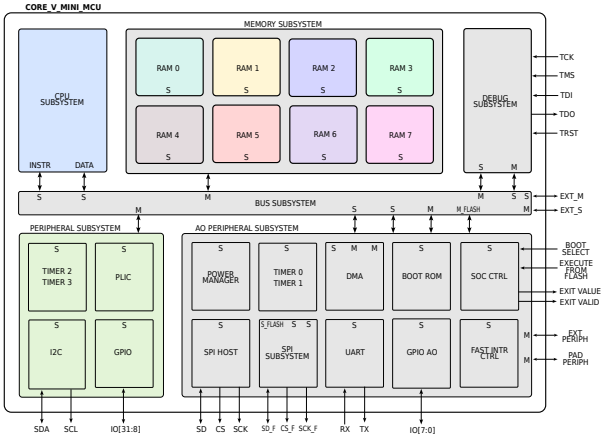

Figure 1: *X-HEEP architecture.*

- Providing a configurable and extendable IP for targeting from tiny microcontrollers to high-performance heterogeneous edge-computing devices for both ASIC and FPGA targets;
- providing an easy-to-use platform for educational purposes and lowering the barrier of open-source hardware and RISC-V adoption;
- providing an open-source platform compatible with commercial as well as open-source EDA tools to lower costs and increase adoption.

We will show how *X-HEEP* can be exploited by accelerator/peripheral developers to build RISC-V SoCs thanks to its simplicity, effectiveness and open source nature, and how we plan to use it for our goals.

The *X-HEEP* architecture is presented in Figure 1.

It is composed of a RISC-V CPU, memory, and peripherals. The CPUs can be configured at design time among the following RISC-V OpenHW Group IPs as: the cv32e40p [3], cv32e2 [4], and cv32e40x. *X-HEEP* employs such CPUs due to their open source, maturity, verification, and competitive features. The availability of open-source, verified and mature RISC-V CPUs is essential to develop a RISC-V-based platform, as it

[1] *X-HEEP* is freely downloadable at https://github.com/esl-epfl/x-heep under a permissive license. The development of the X-HEEP framework has been supported in part by Ecocloud, the EPFL research center on sustainable computing, PEDESITE Swiss NSF Sinergia project (GA No. SCRSII5 193813/1), and the ML-Edge Swiss National Science Foundation (NSF) Research project (GA No. 200020182009/1)

represents one of the most costly design and verification phases. *X-HEEP* employs a configurable number of SRAM banks. The amount of on-chip memory is one of the most important size and power consumption knobs. Low-cost tiny microcontrollers running bare-metal software would benefit from having only 32kB, while edge-computing platforms running FreeRTOS would benefit from having more memory up to 512 or 1024kB. *X-HEEP* offers standard peripherals such as interrupt controllers, a power manager and DMA, as well as JTAG, SPIs, UART, I2C, and GPIOs. Some of them are designed from scratch, but most are included from the open-source lowRISC OpenTitan, PULP, and Yosys projects. As for the CPUs, the availability of such a rich set of peripherals made the design and verification of *X-HEEP* cheaper and faster. The *ESL* research is mainly focused on ultra-low-power long-term biomedical applications, thus very slow and long signals are acquired before processing them, resulting in very long CPU idle periods while data are acquired, interleaved with the processing part, which is usually below 10% of the total application length. For this reason, *X-HEEP* employs a power manager responsible for implementing power-saving strategies such as operand isolation, clock gating, and power gating over the power domains shown in color in Figure 1. One of the key features *X-HEEP* has been designed for is extendability, which is implemented via memory-mapped accelerators/peripherals or via custom ISA extensions to the cv32e40x CPU. In fact, although *X-HEEP* itself can be used standalone in the configurations described above, it has also been designed to be instantiated inside a bigger design to act as a controller. This allows engineers focused on, for example, accelerators, to embrace RISC-V and open-source hardware by instantiating their IPs next to *X-HEEP*, and to use the CPU and its software routines to interact with it. The choice of making it extendable by design has the advantage that external users can focus on custom IP development without the costly operation of forking, modifying and maintaining *X-HEEP*. Not only are there new research and industrial projects, but due to their simplicity, *X-HEEP* has been used successfully by a growing number of educational projects such as adding a new peripheral, a new accelerator, a memory block or implementing new applications for embedded systems. *X-HEEP* targets both FPGA and ASIC projects, even if the hardware has been optimized to meet ASIC constraints. Although it is still in active development, its first version (*HEEPocrates*) has been tapped-out in TSMC65 with the cv32e2 CPU, and extended with custom blocks internally developed as a *CGRA*, and In-Memory Computing macros. The *X-HEEP* (without accelerators) occupies an area of 2.3mm2, has a maximum frequency of 250MHz, and consumes 28µW/MHz post place-and-route.

On the firmware side, *X-HEEP* provides a versatile, flexible, and heterogeneous environment that can support a wide range of applications or prototypes. The compilation flow is based on a standard RISC-V toolchain and CMake flows, and supports both bare metal and FreeRTOS-based applications, making it a viable choice for developers who require an operating system with real-time processing capabilities. To facilitate application development, we are adding the Segger Embedded Studio (SES) IDE support for *X-HEEP*, making application coding, debugging and testing quick and efficient. Furthermore, to support higher application memory requirements, we developed an open source board with flash memory and an FTDI chip to plug into either the FPGA or ASIC *X-HEEP* versions. The firmware is also extendable to allow external users to add the drivers and applications for their own custom hardware.

Finally, the *ESL* research plan includes the integration of *X-HEEP* into different next-generation wearable systems. For example, a wearable device will be developed to capture EEG signals and detect epilepsy seizures in real time with *X-HEEP* technology. This wearable device will be equipped with sensors to monitor the wearer's brain activity and will send alerts to their caregiver or medical team if a seizure is detected. The device's small size and low power consumption will make it perfect for continuous monitoring, allowing patients to carry out their daily activities without interruption. Overall, *X-HEEP* technology will allow the development of new configurable, heterogeneous, and extendable wearable devices that can enhance the quality of life of patients with epilepsy and other diseases by providing real-time monitoring and personalized healthcare.

References

[1] *Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies.* `https://digital-strategy.ec.europa.eu/en/library/recommendations-and-roadmap-european-sovereignty-open-source-hardware-software-and-risc-v`. Accessed: 2013-02-27.

[2] *RISC-V Specifications.* `https://riscv.org/technical/specifications/`. Accessed: 2013-02-27.

[3] Michael Gautschi et al. "Near-threshold RISC-V core with DSP extensions for scalable IoT endpoint devices". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.10 (2017), pp. 2700–2713.

[4] Pasquale Davide Schiavone et al. "Slow and steady wins the race? A comparison of ultra-low-power RISC-V cores for Internet-of-Things applications". In: *2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*. IEEE. 2017, pp. 1–8.