Accelerating RISC V Developments Through Network-on-Chip (NoC) Automation

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Abstract

The open-source RISC-V ISA has gained popularity due to its customizability and versatility. Its adoption presents challenges in Networks-on-Chips (NoCs) implementation, which impact performance, power consumption, and cost. This paper discusses different protocol options for RISC-V-based SoCs in the context of their unique advantages in terms of flexibility, performance, and coherency. We introduce a physically aware NoC development framework for non-cache-coherent applications. This framework enables better management of physical constraints, reducing interconnect area and power consumption. It addresses the impact of floor planning and layouts on NoC topology development and achieves up to 5X shorter turn-around time than manual iterations. Additionally, the paper introduces an IP development framework for multiprotocol AMBA CHI and ACE cache coherent interconnect.

Introduction

The open-source RISC-V instruction set architecture (ISA) has gained significant popularity recently due to its customizable nature and versatility for various applications, providing never-before-seen freedom to innovate through workload-optimized ISA extensions. However, its adoption in the semiconductor industry poses several challenges in the context of Networks-on-Chips (NoCs) [1], which, more often than not, have become the long pole toward timing closure. In today's and tomorrow's complex systems on chips (SoCs), a hierarchy of NoCs provides connectivity within and between subsystems for computing, graphics acceleration, machine learning, high-speed wired and wireless peripherals, safety & security, and I/O peripherals. Modern SoCs often use 100s of reused blocks that define significant portions of the floor plan and leave the area in-between for the NoCs – often up to 10% to 15% of the total area. Their implementation can significantly impact performance, power consumption, and cost.

Comparison of NoC Protocols

First, we will discuss in this paper the differences and advantages of different protocol options for RISC-V-based SoCs. Designers face a variety of options:

- NoC-based: NoC-based protocols can be customized for RISC-V SoCs to offer flexible topologies, such as mesh, torus, or tree, and advanced features like adaptive routing, Quality of Service (QoS), and fault tolerance. They divide the network into routers, channels, and interfaces, enabling scalable and modular designs.
- AMBA 3 AXI: AMBA 3 includes the AXI (Advanced eXtensible Interface) protocol, which applies to RISC-V SoCs due to its high performance and low-latency communication. It offers separate read and write channels, out-of-order transaction completion, and burst transfer support.
- AMBA 4 AXI and ACE: AMBA 4 extends AXI and introduces ACE (AXI Coherency Extensions), enabling system-level cache coherency in multi-core designs. ACE provides features such as barrier transactions and cache maintenance operations, making it suitable for RISC-V SoCs with multiple coherent processors.
- AMBA 5 CHI: AMBA 5 includes the CHI (Coherent Hub Interface) protocol, designed for high-performance, cache-coherent interconnects in multi-core systems. CHI offers advanced features like virtual networks, Quality of Service (QoS), and fault tolerance, making it a suitable option for RISC-V SoCs requiring high scalability and performance.
- TileLink: Explicitly developed for RISC-V-based SoCs, TileLink is a high-performance, cache-coherent NoC protocol. It provides a modular and scalable approach, supporting various coherency models and interconnect topologies. TileLink reduces overhead by supporting atomic operations and implementing configurable address mapping and cache policies.
- Custom: Designers can develop NoC protocols for RISC-V-based SoCs that cater to specific requirements, such as power consumption or application-specific communication patterns.

Physically Aware NoC Automation

To accelerate RISC-V developments, Arteris has introduced NoC automation for non-cache-coherent applications with a physically aware NoC development framework that enables system-on-chip (SoC) architecture teams, logic designers, and integrators to incorporate physical constraint management across power, performance, and area (PPA) to deliver a physically aware IP connecting the individual compute and peripheral blocks of SoCs. With its integrated physical awareness technology, the framework gives place and route teams a much better starting point while reducing interconnect area and power consumption.

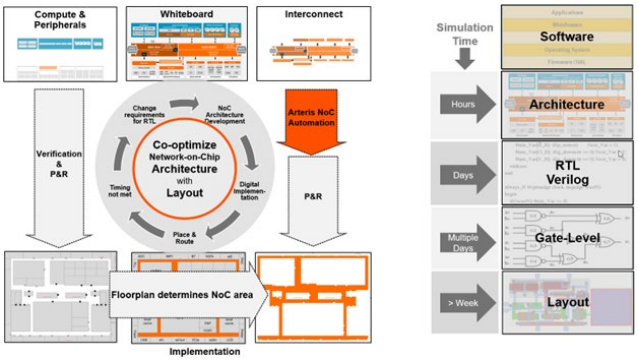

Figure 1: A physically aware NoC development flow

For modern technologies, place & route (P&R) technology and the effects of semiconductor technology significantly impact NoC development. There are three areas in which the floor planning and sometimes even the actual layouts after P&R can heavily impact NoC topology development.

Firstly, while the interconnect between the significant building blocks often becomes the long pole in the tent called timing closure, its silicon real estate, more often than not, depends on the primary building blocks in the system. In an NoC-centric view, these are often called "blockages." Designers ask the NoC to use what's left.

Secondly, these blockages determine with the ports of the layout building blocks of compute and peripheral components the layout position of the critical connections communicating through the NoC.

Thirdly, signal propagation becomes an issue once the port positions and the silicon real estate area made available for the NoC are known. Determining signal propagation has become very complicated, especially at smaller geometry nodes. At aggressive process geometries, the transport delay is a function of the chosen foundry, the routing stack, the type of driving cells, the process voltage and temperature, and many others.

The Arteris NoC IP development framework delivers up to 5X shorter turn-around time versus manual physical iterations by allowing design teams to consider the actual layout information importing .def descriptions from digital implementation flows. Using estimates derived from .lib technology information, the NoC IP development framework estimates the number of required pipeline stages and creates scripts that forward placement guidance to digital implementation and P&R tools.

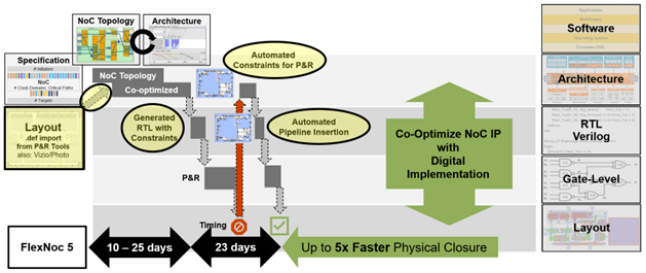

Figure 2: Example of time savings applying physically aware NoC design

In addition, for cache-coherent applications, we will introduce an IP development framework [2] for multiprotocol AMBA CHI and ACE cache coherent interconnect that offers multiple configurable snoop filters, multiple configurable proxy caches, and a modular, distributed architecture to provide system architects more degrees of freedom to innovate.

Outlook

Today, NoC development extends to chiplets, addressing the challenges of power, performance, and scalability in computing systems. NoC design streamlines communication between chip components, reducing latency and enhancing energy efficiency. Chiplets modularize and enable heterogeneous integration of different IPs, improving design flexibility and manufacturing yield. Together, these technologies will be critical for realizing advanced multi-chip architectures, supporting the growth of AI, 5G, edge computing, automotive electronics, and data centers.

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