



# SW Overlay

Jan 26<sup>th</sup> 2022

# Antitrust Policy Notice

RISC-V International meetings involve participation by industry competitors, and it is the intention of RISC-V International to conduct all its activities in accordance with applicable antitrust and competition laws. It is therefore extremely important that attendees adhere to meeting agendas, and be aware of, and not participate in, any activities that are prohibited under applicable US state, federal or foreign antitrust and competition laws.

Examples of types of actions that are prohibited at RISC-V International meetings and in connection with RISC-V International activities are described in the RISC-V International Regulations Article 7 available here: <https://riscv.org/regulations/>

If you have questions about these matters, please contact your company counsel.

# RISC-V International

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. [help@riscv.org](mailto:help@riscv.org)

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

<https://riscv.org/risc-v-international-community-code-of-conduct/>

# Agenda

1. Submission status update (llvm, binutils)
2. psABI status
3. Round table - q&a

# Submission status update

- LLVM/Clang
  - Overlay patches match latest changes to the HLD
    - <https://reviews.lvm.org/D109371>
    - <https://reviews.lvm.org/D109372>
  - Patch submitted to add new reserved register ELF attribute
    - <https://reviews.lvm.org/D113890>
- GNU Binutils - work in progress
  - Extends BFD to build overlay tables during link and resolve overlay relocations
  - Currently refactoring changes to be separate from main RISC-V BFD
  - Needs handling of reserved register attribute
- GNU GDB - work in progress
  - Adding overlay manager class to allow different overlay systems to be
  - supported

# psABI Status

- Request for Reserved registers Tag
  - psABI task group approved the change for adding a new elf attribute – [Tag\\_RISCV\\_reserved\\_register](#)
  - PR was created by @kito-cheng: [New attribute: Tag\\_RISCV\\_reserved\\_register](#)
- Overlay toolchain uses this Tag
  - To reserve register used by the RT-Engine

# Round table – Q&A

- Open issues



# Thank You

