RISC-V Processor OVP Model Simulator

riscvOVPsim User Guide

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Model Release Status

This software and model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Contents

Chapter 1

Overview of the riscvOVPsim simulator

This document provides documentation of the riscvOVPsim RISC-V processor model simulator.

1.1 The Imperas range of simulators

Imperas is the leading developer of RISC-V simulators for compliance testing, test development, hardware design verification, and operating system and application software development.

There are three simulators in the Imperas RISC-V range:

- the free riscvOVPsim from GitHub.com used for compliance testing and bare metal software runs
- the free riscvOVPsimPlus from OVPworld.org (requiring registration) targeting test development and initial hardware verification
- the commercial M*SIM from Imperas Software, Inc., for professional developers, hardware design verification teams, operating system and advanced software developers.

There are also Imperas partner specific variations of riscvOVPsimPlus product available from Imperas partners.

All simulators are based on the Imperas CpuManager simulator base technology utilizing the OVP open standard APIs, and are targeted at different uses and have different capabilities.

1.2 Description of riscvOVPsim

riscvOVPsim is an Instruction Accurate RISC-V processor simulator based on the Imperas Open Virtual Platform (OVP) technology with Just-in-Time Code Morphing simulation that executes RISC-V code on a Linux or Windows host computer.

The included RISC-V models are complete and cover the full RISC-V User and Privilege specifications.

The riscvOVPsim simulator is easy to understand and effective to use. It is flexible, accurate, and exceptionally fast, often over 2,000 MIPS. Suitable as a platform target to develop baremetal, OS Ports (Linux or RTOS), drivers and applications.

riscvOVPsim has been developed by Imperas Software. As a member of the RISC-V community of software and hardware innovators collaboratively driving RISC-V adoption, Imperas has developed the riscvOVPsim simulator to assist RISC-V adopters to become compliant to the RISC-V specifications. riscvOVPsim was included as part of RISC-V International's compliance test suite since 2018.

Imperas is revolutionizing the development of embedded software and systems and is the leading independent provider of commercial processor simulators for programmers view models for software development.

Imperas, along with Open Virtual Platforms (OVP), promotes open model availability for a spectrum of processors, IP vendors, CPU architectures, system IP and reference platform models of processors and systems ranging from simple single core bare metal platforms to full heterogeneous multi-core systems booting SMP Linux. Additional information can be found at www.imperas.com and www.OVPworld.org.

1.3 Usage and Purpose

There is no complex installation process or scripts for downloading and installing riscvOVPsim. It is just a matter of downloading and running the executable with appropriate configuration options and cross-compiled RISC-V programs.

riscvOVPsim is configurable to represent exactly the same implementation choices that RISC-V processor implementors choose thus making it an excellent tool for the usage of RISC-V application software and verification and compliance test suites.

riscvOVPsim has built in instruction functional coverage measurement and reporting to assess what is in tests. It is used to measure the completeness of the RISC-V compliance tests and test suites.

1.4 Licensing

The complete OVP RISC-V processor model is included with riscvOVPsim and is made available as open source under the Apache 2.0 license.

riscvOVPsim includes an industrial quality model and simulator of RISC-V processors for use for compliance and test development. It has been developed for personal, academic, or commercial use, and the model is provided as open source under the Apache 2.0 license. Visit the OVPworld.org website for the source. The simulator is provided under the under Open Virtual Platforms (OVP) Fixed Platform Kits license that enables download and usage. riscvOVPsim and Imperas RISC-V support is actively maintained and enhanced. To ensure you make use of the current version of riscvOVPsim this release will expire. Please download the latest version.

The full license terms are included within the download package and are listed in an appendix of this document.

Imperas provide different versions of the simulators with full commercial maintenance and support - please contact info@imperas.com for more information.

1.5 Limitations

Problems with installation or download may be reported to support@imperas.com.

Feedback and bug reports may be submitted to support@imperas.com.

riscvOVPsim is restricted to only run RISC-V processor model variants in a fixed platform configuration of one processor instance and one memory sub-system. Caches and other processor microarchitecture features are not included in programmer view models. If you need different platform configurations or to extend the platform or models then please contact contact Imperas or visit www.OVPworld.org.

1.6 Verification

Imperas have been developing simulators and processor models for over 10 years and are the leading independent provider of instruction accurate simulators, processor reference models and tools.

Each model is developed with a very controlled and precise methodology. As the model functionality is developed it is carefully stepped through and white box, directed tests are created.

A comprehensive test suite is developed until 100% model line coverage is achieved. Standard publicly available test suites are then used. Complete platforms are then constructed to run full operating systems. All of these tests are incorporated into a continuous integration and regression testing environment to ensure model quality.

The Imperas OVP RISC-V models have been run through the above process and virtual platforms incorporating them are available from Imperas running FreeRTOS, single core Linux, and SMP Linux on a five core RISC-V processor system.

The models have also been run through the full RISCV.org Compliance Suite and all tests pass. (The Imperas RISC-V simulator/model have been a reference for the RISC-V Compliance Suite tests since 2018.)

1.7 RISC-V Specifications currently supported in this riscvOVPsim product

- RISC-V - Instruction Set Manual, Volume I: User-Level ISA (user_version)
  - Version 2.2 : User Architecture Version 2.2
  - Version 2.3 : Deprecated and equivalent to 20191213
  - Version 20190305 : Deprecated and equivalent to 20191213
  - Version 20191213 : User Architecture Version 20191213
- RISC-V - Instruction Set Manual, Volume II: Privileged Architecture (priv_version)

  - Version 1.10 : Privileged Architecture Version 1.10
  - Version 1.11 : Privileged Architecture Version 1.11, equivalent to 20190608
  - Version 20190405 : Deprecated and equivalent to 20190608
  - Version 20190608 : Privileged Architecture Version Ratified-IMFDQC-and-Priv-v1.11
  - Version 20211203 : Privileged Architecture Version 20211203
  - Version 1.12 : Privileged Architecture Version 1.12, equivalent to 20211203
  - Version master : Privileged Architecture Master Branch as of commit 6bdeb58 (this is subject to change)

- RISC-V I Base ISA
- RISC-V E Embedded ISA
- RISC-V M Multiply/Divide
- RISC-V A Atomic Instructions
- RISC-V F Single precision floating point
- RISC-V D Double precision floating point
- RISC-V C Compressed instructions
- RISC-V S Supervisor mode
- RISC-V U User mode
- RISC-V N User-level interrupts
- RISC-V V Vector Extension (vector_version)

  - Version 0.7.1-draft-20190605 : Vector Architecture Version 0.7.1-draft-20190605
  - Version 0.7.1-draft-20190605+ : Vector Architecture Version 0.7.1-draft-20190605 with custom features (not for general use)
  - Version 0.8-draft-20190906 : Vector Architecture Version 0.8-draft-20190906
  - Version 0.8-draft-20191004 : Vector Architecture Version 0.8-draft-20191004
  - Version 0.8-draft-20191117 : Vector Architecture Version 0.8-draft-20191117
  - Version 0.8-draft-20191118 : Vector Architecture Version 0.8-draft-20191118
  - Version 0.8 : Vector Architecture Version 0.8
  - Version 0.9 : Vector Architecture Version 0.9
  - Version 1.0-draft-20210130 : Vector Architecture Version 1.0-draft-20210130
  - Version 1.0-rc1-20210608 : Vector Architecture Version 1.0-rc1-20210608
  - Version 1.0 : Vector Architecture Version 1.0 (frozen for public review)
  - Version master : Vector Architecture Master Branch as of commit 8cdce6c (this is subject to change)

- RISC-V B Bit Manipulation Extension (bitmanip_version)

  - Version 0.90 : Bit Manipulation Architecture Version v0.90-20190610
  - Version 0.91 : Bit Manipulation Architecture Version v0.91-20190829
  - Version 0.92 : Bit Manipulation Architecture Version v0.92-20191108
  - Version 0.93-draft : Bit Manipulation Architecture Version 0.93-draft-20200129
  - Version 0.93 : Bit Manipulation Architecture Version v0.93-20210110
  - Version 0.94 : Bit Manipulation Architecture Version v0.94-20210120
  - Version 1.0.0 : Bit Manipulation Architecture Version 1.0.0
  - Version master : Bit Manipulation Master Branch as of commit 1f56afe (this is subject to change)

- RISC-V K Cryptographic Extension (crypto_version)
  - Version 0.7.2 : Cryptographic Architecture Version 0.7.2
  - Version 0.8.1 : Cryptographic Architecture Version 0.8.1
  - Version 0.9.0 : Cryptographic Architecture Version 0.9.0
  - Version 0.9.2 : Cryptographic Architecture Version 0.9.2
  - Version 1.0.0-rc1 : Cryptographic Architecture Version 1.0.0-rc1
  - Version 1.0.0-rc5 : Cryptographic Architecture Version 1.0.0-rc5

1.8 Additional specifications available in Imperas simulators currently not supported in this product

- RISC-V H Hypervisor Extension (hypervisor_version)
  - Version 0.6.1 : Hypervisor Architecture Version 0.6.1
  - Version 1.0 : Hypervisor Architecture Version 1.0
- RISC-V P DSP/SIMD Extension (dsp_version)
  - Version 0.5.2 : DSP Architecture Version 0.5.2
  - Version 0.9.6 : DSP Architecture Version 0.9.6
- RISC-V Debug Module (debug_version)
  - Version 0.13.2
  - Version 0.14.0

1.9 About OVP & Imperas Software

Open Virtual Platforms (www.OVPworld.org) was set up in 2008 to provide an open standard approach to creating virtual platforms. OVP provides full definitions of standard APIs to enable the modeling and simulation of digital hardware. There are over 500 OVP models with tools to easily create virtual platforms. With OVP, users create their own models and platforms and can develop software on simulations of hardware. OVPworld.org also provides a full simulation and debug capability that is licensed and usable for non-commercial use.

Most OVP models are available under an Apache 2.0 open source license. For a full list of publicly available OVP processor models, visit here: www.ovpworld.org/variants. To browse the OVP library of peripheral models, visit here: www.ovpworld.org/peripherals.

For commercial use, Imperas provide a full suite of simulators, verification / analysis / profiling, debug, and platform / model development tools. Imperas is the leader in heterogeneous multi-core simulation and debug.

Imperas can be contracted to develop new models of processor, peripheral components, or full platforms.

Imperas also provide a RISC-V processor compliance testing service if you need to ensure that your RISC-V RTL is compliant with RISC-V specifications.

Imperas can also provide additional tools and services to assist with RISC-V processor compliance if you need to ensure that your RISC-V RTL is compliant with either the latest or earlier versions of the RISC-V specifications. Please contact Imperas for the latest information.

Chapter 2

The riscvOVPsim Fixed Platform Simulator

riscvOVPsim has a built-in fixed platform which comprises one CPU instance of a RISC-V processor model variant and one memory sub-system.

The RISC-V processor model variant is selected by a command line switch and the details of its options can be configured using override commands. See the the section below on using the OVP RISC-V processor model.

The default memory fully populates the appropriate address space for the configured processor. It is implemented in the simulator using a sparse memory algorithm and so there are no capacity issues. Alternatively, the memory regions may be configured and any access outside of these regions will cause a memory fault.

riscvOVPsim has built in instruction functional coverage measurement and reporting to assess what is in tests. It is used to measure the completeness of the RISC-V compliance tests and test suites.

Chapter 3

Host Platforms

3.1 Availability

riscvOVPsim is available on Windows 64 bit, and Linux 64 bit hosts.

3.2 Selecting Host

There are two different binary directory trees provided with riscvOVPsim. In the directories will be the appropriate binary files needed for the different hosts.

Chapter 4

Running High Speed Simulations

The riscvOVPsim.exe program is a standalone executable that performs the following tasks:

- Sets up the platform with a cpu model and memory
- Configures the behavior of the platform and model by changing run-time command line switches
- Loads application code in .elf format into memory to run on the processor model
- Loads an appropriate semihost library to allow application code to interact with the host computer (for example to display application code 'printf's to the simulation console without the need for a simulated UART)
- Runs the simulator which executes the RISC-V cross compiled binary instructions
- Reports performance statistics when simulation is complete

4.1 An Introduction and First Simulation

riscvOVPsim is used to simulate application code in bare metal environments by just loading up a cross compiled .elf file and selecting a CPU variant. There are configuration options to select other parameters.

4.1.1 Running using provided scripts and applications

In the main directory, there is an examples directory with several different sub directories, one for each example. If you open one of these directories, you will see several scripts that are either .bat for Windows or .sh for Linux. These can just be executed. In this document we will assume Linux usage:

```
> cat RUN_RV32_Dhrystone.sh
...
${bindir}/riscvOVPsim.exe --variant RVB32I \
--override riscvOVPsim/cpu/add_Extensions_mask=MACSU \
--program dhrystone.RISCV32.elf
```

The '–variant' selects a specific processor model variant to be simulated. The '–program' specifies which application .elf program to run. To run the simulation:

```
> RUN_RV32_Dhrystone.sh
```

The simulator will run, showing the results of the dhrystone simulation (similar to that shown below for a base RVB32I+MACSU extensions):

```
riscvOVPsim (64-Bit) v20180221.0 Open Virtual Platform simulator from www.IMPERAS.com.
Copyright (c) 2005-2023 Imperas Software Ltd.  Contains Imperas Proprietary Information.
Licensed Software, All Rights Reserved.
Visit www.IMPERAS.com for multicore debug, verification and analysis solutions.

riscvOVPsim started: Fri Apr 13 02:40:19 2018

Info (OR_OF) Target riscvOVPsim/cpu has object file read from dhrystone.RISCV32-O0-g.elf
Info (OR_PH) Program Headers:
Info (OR_PH) Type           Offset     VirtAddr   PhysAddr   FileSiz    MemSiz     Flags Align
Info (OR_PD) LOAD           0x00000000 0x00010000 0x00010000 0x00017dc0 0x00017dc0 R-E   1000
Info (OR_PD) LOAD           0x00017dc0 0x00028dc0 0x00028dc0 0x000009c0 0x00003228 RW-   1000

Dhrystone Benchmark, Version 2.1 (Language: C)

Program compiled without 'register' attribute

Execution starts, 5000000 runs through Dhrystone

...

Measured time too small to obtain meaningful results
Please increase number of runs

Info
Info ------------------------------------------------------
Info CPU 'riscvOVPsim/cpu' STATISTICS
Info   Type                  : riscv (RV32I+MAC)
Info   Nominal MIPS          : 100
Info   Final program counter : 0x100ac
Info   Simulated instructions: 6,955,075,157
Info   Simulated MIPS        : 1388.9
Info ------------------------------------------------------
Info
Info ------------------------------------------------------
Info SIMULATION TIME STATISTICS
Info   Simulated time        : 69.55 seconds
Info   User time             : 5.01 seconds
Info   System time           : 0.00 seconds
Info   Elapsed time          : 5.01 seconds
Info   Real time ratio       : 13.89x faster
Info ------------------------------------------------------

riscvOVPsim finished: Fri Apr 13 02:40:24 2018

riscvOVPsim (64-Bit) v20180221.0 Open Virtual Platform simulator from www.IMPERAS.com.
Visit www.IMPERAS.com for multicore debug, verification and analysis solutions.
```

4.1.2 Using command line options to show available RISC-V CPU variants

To see the list of processor model variants available in riscvOVPsim:

```
> ./bin/Linux64/riscvOVPsim.exe --showvariants
```

4.1.3 Selecting a RISC-V CPU variant

The '–variant' selects a specific processor model variant to be simulated.

```
> ./bin/Linux64/riscvOVPsim.exe --variant RVB64I \
    --override riscvOVPsim/cpu/add_Extensions=MACSU \
    --program dhrystone.RISCV64.elf
```

4.1.4 Specifying a RISC-V program .elf file to run

The

'--program <app.elf>'

specifies which application .elf program to run.

4.1.5 Specifying Custom Memory Map

By default, the memory space is fully populated i.e. 0 to maximum high address contain memory. If a specific memory layout is required it can be specified using the command line argument '–memory memory definition string'. The memory argument takes a string defining the low and high addresses, and, if required, a name and the memory access permissions. The memory access permission defaults to RWX i.e. read, write and execute. The permission is defined by bits 1:Read 2:Write 3:eXecute. The memory argument may be supplied multiple times or once with a comma separated list.

'--memory [<name>:]<low address>:<high address>[:<permissions>][,repeat]'

The following example shows setting up a memory space which has two memory regions, named loram and hiram. The lower has RWX permissions and the upper has only RW permissions. All other memory spaces will cause an access failure.

```
> ./bin/Linux64/riscvOVPsimPlus.exe --memory loram:0x00000000:0x0001ffff:rwx \
                                    --memory hiram:0xffff0000:0xffffffff:rw
```

which could also be entered as

```
> ./bin/Linux64/riscvOVPsimPlus.exe \
      --memory loram:0x00000000:0x0001ffff:rwx,hiram:0xffff0000:0xffffffff:rw
```

4.1.6 –help and –helpall command line option

There are command line arguments '–help' and '–helpall' that list the options available. For example:

```
> ./bin/Linux64/riscvOVPsim.exe --help
```

See the appendix for details of the help commands.

4.2 Measuring Instruction Functional Coverage during simulation

For any simulation run, you can enable instruction functional coverage to be collected.

The simplest form is:

```
> ./bin/Linux64/riscvOVPsimPlus.exe --variant RVB32I --program prog.elf \
      --cover basic --extensions RVI --reportfile cover_report.log
```

Which will display one line to the simulation console:

```
TOTAL INSTRUCTION COVERAGE :: threshold : 1 : instructions: seen 2/2 : 100.00%, coverage points hit: 242/542 :  44.65%
```

And will write out a full report in the specified file.

See the chapter on Instruction Functional Coverage for full details.

4.3 Reporting performance statistics when simulation is complete

At the end of a simulation run, the simulator will display results and statistics:

```
...

Info
Info ------------------------------------------------------
Info CPU 'riscvOVPsim/cpu' STATISTICS
Info   Type                  : riscv (RV32I+MAC)
Info   Nominal MIPS          : 100
Info   Final program counter : 0x100ac
Info   Simulated instructions: 6,955,075,157
Info   Simulated MIPS        : 1388.9
Info ------------------------------------------------------
Info
Info ------------------------------------------------------
Info SIMULATION TIME STATISTICS
Info   Simulated time        : 69.55 seconds
Info   User time             : 5.01 seconds
Info   System time           : 0.00 seconds
Info   Elapsed time          : 5.01 seconds
Info   Real time ratio       : 13.89x faster
Info ------------------------------------------------------

riscvOVPsim finished: Fri Apr 13 02:40:24 2018

riscvOVPsim (64-Bit) v20180221.0 Open Virtual Platform simulator from www.IMPERAS.com.
Visit www.IMPERAS.com for multicore debug, verification and analysis solutions.
```

This shows the fixed platform name (riscvOVPsim), the processor instance (cpu), the variant type (RV32I with extensions MAC). The Nominal MIPS is effectively the clock speed that the CPU is clocked at in the platform (this can be overridden). The Simulated MIPS is the number of instructions simulated per second. The Simulated time is the time simulated in the simulation. User, System, and Elapsed time is how long the simulation took if you looked at your watch. The Real time ratio shows how much faster/slower the simulation was compared to real time.

4.4 Running the provided examples

The examples directory provides some easy to run examples to show how riscvOVPsim is used. These come with a script to run and configure the simulator and the source and elf files that are needed.

4.4.1 Basic benchmark examples

The directory fibonacci is the simplest to show a program running. The other examples provide standard benchmarks.

4.4.2 Instruction Functional Coverage examples

In the coverage directory there is also a script to run the different provided examples.

Chapter 5

The OVP RISC-V processor model

The OVP RISC-V processor model is written in C and makes calls to the standard OVP VMI API interface.

The source of the OVP RISC-V processor model is available as open source under the Apache 2.0 license where you got this document (see below).

For information on how OVP CPU models are written look at the OVP Processor Modeling Guide and for information on the VMI API look at OVP VMI Morph-Time Reference and OVP VMI Run-Time Reference.

The model has been written to contain all the functionality of the standard RISC-V specifications and the functionality of the specification is subset within the model into 'model variants' that are selected at runtime and configure the model. When a model variant is selected, only the defined capabilities of that model variant are available. For example if a floating point instruction is attempted to be executed by a variant that does not implement floating point instructions, then an un-implemented instructed exception is triggered. If an instruction accessed a register that was not present in the selected variant, then again the model would indicate an error, for example trying to use register 31 in an E variant.

5.1 The OVP RISC-V processor model source

The full source of the OVP RISC-V processor is provided with this document as a reference. It is the source that is compiled into the model that is being simulated by riscvOVPsim.

If you want to modify the model source and recompile it and use it for simulation, then you need to use either the simulator from OVP or from Imperas as they are simulators that allow this loading of user compiled models. Visit `www.ovpworld.org` or `www.imperas.com`.

5.2 The different 'standard' RISC-V ISA features and instruction extensions

The model supports the following architectural features:

- RV32I/64I/128I base ISA
- RV32E base ISA
- extension M (integer multiply/divide instructions)
- extension A (atomic instructions)
- extension B (bit manipulation instructions)
- extension F (single-precision floating point)
- extension D (double-precision floating point)
- extension C (compressed instructions)
- extension N (user-level interrupts)
- extension S (Supervisor mode)
- extension U (User mode)
- extension K (Crypto)
- extension V (Vector instructions)
- extension P (DSP instructions)
- 32-bit, 64-bit XLEN

All features and registers in the RISC-V Privilege Specification are implemented and configured as required.

Note that the model may implement instruction extensions that the specific simulator in use may not support. For example, riscvOVPsim only supports the ratified instruction extensions, and riscvOVPsimPlus does not support those extensions that are still experimental etc.

5.3 Selecting a specific RISC-V Processor Variant

To see the list of processor model variants available in riscvOVPsim:

```
> ./bin/Linux64/riscvOVPsimPlus.exe --showvariants
```

The '–variant' command selects a specific processor model variant to be simulated.

NOTE: the variant name is case sensitive.

```
> ./bin/Linux64/riscvOVPsimPlus.exe --variant RVB64I \
    --override riscvOVPsim/cpu/add_Extensions=MACSU \
    --program application/dhrystone.RISCV64.elf
```

5.4 Available riscvOVPsim RISC-V variants

For each RISC-V variant there is a detailed document that describes the features and limitations of the implementation. It also lists all the registers, ports, modes, exceptions, etc., and importantly, it lists all the configuration parameters that can be set for that variant.

Each variant is unique and has a different document.

5.4.1 RV32I

A detailed document of the model variant is available: RV32I

5.4.2 RV32IM

A detailed document of the model variant is available: RV32IM

5.4.3 RV32IMC

A detailed document of the model variant is available: RV32IMC

5.4.4 RV32IMCZce

A detailed document of the model variant is available: RV32IMCZce

5.4.5 RV32IMAC

A detailed document of the model variant is available: RV32IMAC

5.4.6 RV32G

A detailed document of the model variant is available: RV32G

5.4.7 RV32GC

A detailed document of the model variant is available: RV32GC

5.4.8 RV32GCZfinx

A detailed document of the model variant is available: RV32GCZfinx

5.4.9 RV32GCK

A detailed document of the model variant is available: RV32GCK

5.4.10 RV32GCP

A detailed document of the model variant is available: RV32GCP

5.4.11 RV32E

A detailed document of the model variant is available: RV32E

5.4.12 RV32EC

A detailed document of the model variant is available: RV32EC

5.4.13 RV32EM

A detailed document of the model variant is available: RV32EM

5.4.14 RV64I

A detailed document of the model variant is available: RV64I

5.4.15 RV64IM

A detailed document of the model variant is available: RV64IM

5.4.16 RV64IMC

A detailed document of the model variant is available: RV64IMC

5.4.17 RV64IMCZce

A detailed document of the model variant is available: RV64IMCZce

5.4.18 RV64IMAC

A detailed document of the model variant is available: RV64IMAC

5.4.19 RV64G

A detailed document of the model variant is available: RV64G

5.4.20 RV64GC

A detailed document of the model variant is available: RV64GC

5.4.21 RV64GCZfinx

A detailed document of the model variant is available: RV64GCZfinx

5.4.22 RV64GCK

A detailed document of the model variant is available: RV64GCK

5.4.23 RV64GCP

A detailed document of the model variant is available: RV64GCP

5.4.24 RVB32I

A detailed document of the model variant is available: RVB32I

5.4.25 RVB32E

A detailed document of the model variant is available: RVB32E

5.4.26 RVB64I

A detailed document of the model variant is available: RVB64I

5.5 Configuring riscvOVPsim to exactly match your processor

The OVP model of the RISC-V specification has many detailed configuration options. These can be set option by option, or, as explained above, the model can be configured by selecting a 'variant'. This is basically a predefined list of settings of many of the different configuration options. To see the details of how a variant configures the model, see the detailed variant documentation as referenced in the previous section.

In many cases, the RISC-V specifications give freedom to the processor implementer to make detailed choices of which parts of the RISC-V specification are implemented and in which way. In a coarse way this might be choosing to not implement hardware floating point, or in a detailed way it might be making a register read only - as allowed in the specifications.

The Imperas OVP RISC-V model can be configured to reflect the specific detailed hardware design decisions that have been chosen.

This detailed configuration of a model is essential when trying to write specification compliance and design tests as the tester needs to know that they are stimulating parts of the specification that should not be in their design and so they need the model to tell them there are errors.

5.5.1 Detailed Model Configuration options

To see the list of processor model configuration options available in riscvOVPsim for a variant:

```
> ./bin/Linux64/riscvOVPsim.exe --variant RVB32E --showmodeloverrides
```

The complete set of configuration options are listed as an appendix to this document.

NOTE: it is important to set the variant as that selects features and thus what can be configured. Each variant may have different configuration parameters.

5.5.2 Configuring the model

An example configuring the model:

```
> ./bin/Linux64/riscvOVPsim.exe --variant RVB64I \
    --override riscvOVPsim/cpu/add_Extensions=MAFDCNSU \
    --override riscvOVPsim/cpu/mtvec_is_ro=T \
    --override riscvOVPsim/cpu/updatePTEA=F \
    --program app.elf
```

Where mtvec_is_ro is a parameter that if set T (true) means mtvec is read only, and where updatePTEA is a parameter that configures the model saying in this case (false) that hardware update of PTEA is not supported.

5.5.3 Changing which extensions are enabled in a variant

In the RISC-V architecture the misa CSR specifies which extensions are implemented. The reset value for the misa register's extensions field may be specified as a configuration option by using the misa_Extensions parameter, thus allowing the user to control which extensions are implemented by the simulation model.

In the document for each variant (linked to in the sections above) is a description of which extensions are enabled (in the section titled Extensions) and which extensions are available but not enabled (in the sections titled Available (But Not Enabled) Extensions). The bit locations for each extension may be found there.

For example, to model an RV64IMCD configuration we start with an RVB64I variant and enable the M, C and D extensions using the add_Extensions override.

```
> ./bin/Linux64/riscvOVPsim.exe --variant RVB64I \
      --override riscvOVPsim/cpu/add_Extensions=MCDSU \
      --showmodeloverrides | grep "_Extensions="

   --override riscvOVPsim/cpu/misa_Extensions=0x14110c (Uns32)
              (default=0x14110c) (default)
              Override default value of misa.Extensions

   --override riscvOVPsim/cpu/add_Extensions=MCFD (String) (default=)
              (override) Add extensions specified by letters to misa Extensions
              (for example, specify "FD" to add F and D features)
```

5.6 Adding user extensions to the OVP RISC-V model

If you want to add new registers or new instructions to the OVP RISC-V model, then there are better ways than modifying the source. Imperas has developed the concept of intercept libraries that can intercept model operation and dynamically modify it - without any of the risks of modifying (maybe incorrectly) the original model source. Imperas has used this very successfully to add user defined custom instructions and registers for different RISC-V customers. For more information contact info@imperas.com.

Chapter 6

RISC-V Verification and Compliance Usage

6.1 How to Verify Tests and the Coverage they are Producing

A test will exercise a specific feature of the processor. This may be a specific set of instructions, virtual memory, exceptions or one of many other things. Tests are typically small and specific with a measurable outcome.

When a test is executed on the virtual platform it can be observed either by using tools or in a debug environment.

6.1.1 Trace Tools

This simulator does not have built in trace features, other Imperas RISC-V simulators have many configurable trace capabilities that are invaluable for verification and test - please refer to them for more information.

6.1.2 Measuring test coverage to assess the model

When a suite of tests has been created we want to be sure that they are stimulating all expected aspects of the processor. This can be done by examining the coverage of the processor model.

All Imperas simulators provide instruction functional coverage. Please refer to the appropriate document sections.

Also, advanced tools are provided by Imperas in the M*SDK tool suite that allow code coverage of the model and instruction usage profiles to be generated.

The processor model code coverage can be used to determine if all instructions and variations of those instructions have been executed. Similarly, it can be used to determine if all exceptions have been stimulated, modes entered etc.

The instruction profile can be used to determine how many times each instruction has been executed

within each test of the test suite providing further details of how well an instruction is tested.

6.1.3 Measuring functional coverage of tests

The simulator includes a tool to measure instruction functional coverage. This is used to see what instructions, operands, and values are used in tests. See the chapter below.

6.1.4 Configuring RISC-V model for compliance checking

The OVP Fast Processor Model is configured from the base execution model using parameters and overrides. The parameter named variant is used to select between the permitted extension and permitted mode combinations of A, B, C, D, E, F, I, M, N, S, U and V.

The RISC-V processor model is configured using overrides to default model parameter values are applied to the processor model instance in the virtual platform, using the -override argument. For example:

```
-override riscvOVPsim/cpu/parameter=value
```

A list of all the available configuration parameters for the model can be obtained using the argument -showmodeloverrides

These are also described in the RISC-V processor model specific documentation available from the OVP website or in an OVP or Imperas product installation.

6.1.5 Fundamental RISC-V Configuration Options

1. What version of Privileged Architecture is implemented? (e.g. 1.10 or 1.11 or 20190405).

   parameter user_version

2. What version of User Architecture is implemented? (e.g. 2.2 or 2.3 or 20190305) .

   parameter priv_version

3. What extensions and modes are supported?

   Use -showvariants to get a list of the available variants that can be used and then set using -variant

6.1.6 Machine Mode Control and Status Register (CSR) Constraints

1. Is misa CSR writable? If so, which bits are writable, and which fixed?

   parameter misa_extension_mask

2. What is the value of the mvendorid CSR?

   parameter mvendorid

3. What is the value of the marchid CSR?

   parameter marchid

4. What is the value of the mimpid CSR?

   parameter mimpid

5. What is the value of the mhartid CSR?

   parameter mhartid

6. Is the mtvec CSR writable or fixed?

   parameter mtvec_is_ro is set to True to make the mtvec read only

7. Does the mtvec CSR have a defined initial value?

   parameter mtvec is used to set an initial value

8. Is the time CSR defined, or are accesses to it trapped and emulated?

   parameter time_undefined is set to cause a trap exception if a time instruction is executed

9. Is the cycle CSR defined, or are accesses to it trapped and emulated?

   parameter cycle_undefined is set to cause a trap exception if a cycle instruction is executed

10. Is the instret CSR defined, or are accesses to it trapped and emulated?

    parameter instret_undefined is set to cause a trap exception if a instret instruction is executed

11. On an Illegal Instruction exception, are mtval (and stval, if present) set to 0 or the instruction bit pattern?

    parameter tval_ii_code is set to True so that the mtval (stval) registers are set to the instruction bit pattern on an illegal instruction

6.1.7 Interrupts and Exceptions

1. What is the reset vector address

   parameter reset_address is used to set the reset vector address

2. How many local interrupts are implemented?

   parameter local_int_num is used to set the number of supplemental local interrupts

3. Is an NMI interrupt implemented?

   If the NMI interrupt is implemented a net connection should be made to the nmi signal port on the model. If no connection is made the nmi is disabled.

4. If NMI is implemented, what is the NMI vector address?

   parameter nmi_address is used to set the nmi vector address

6.1.8 Physical memory

1. What is the physical address bus size?

   The physical address bits for the bus port is set to match the size of the bus connected to the processor so no additional configuration need be applied to the processor model.

2. Are Physical Memory protection (PMP) registers implemented? If so, how many regions are there? (up to 16).

   parameter PMP_registers is used to set the number of implemented PMP address registers

6.1.9 Virtual memory

1. If virtual memory is implemented, what address translation modes are implemented? (model supports Sv32, Sv39, Sv48).

   parameter Sv_modes is used to set specify a bit mask indicating the number of Sv modes implemented, for example 1<<8 indicates Sv39

2. Is ASID-managed address translation implemented? If so, how many bits of ASID are implemented?

   parameter ASID_bits is used to specify the number of ASID bits

3. Is update of page table entry A bit performed by hardware or software?

   parameter updatePTEA is set to True to indicate support for hardware update of PTE A bit

4. Is update of page table entry D bit performed by hardware or software?

   parameter updatePTED is set to True to indicate support for hardware update of PTE D bit

6.1.10 Miscellaneous

1. If atomic (A) extension is supported, what is the size in bytes of the lock granule (e.g. 32-byte cache line).

   parameter lr_sc_grain

2. Is the WFI instruction a true wait or a NOP?

   parameter wfi_is_nop is set to True so that wfi is implemented as a nop instruction, otherwise halt while waiting for interrupt

3. Does the processor support unaligned memory accesses?

   parameter unaligned is set to True to specify the processor supports unaligned operations.

6.2 Signature File

6.2.1 Introduction

A signature file is the contents of a memory region that is output to a file after the execution of an application on a RISC-V processor.

It is used in some of the tests written to validate the RISC-V processor.

By default, the signature file is generated at the end of simulation or when the function 'write_to_host' is called. It contains the memory contents bounded by the symbols 'signature_begin' and 'signature_end'.

The signature file generation is implemented as an Imperas intercept/extension library and provides the detection of the end of a test and the dump of memory signature to a file.

6.2.2 Configuration

The signature file operation can be configured from the default using the following arguments

- SignatureFile : The name of the file created containing the signature
- SignatureAtEnd : Write the signature file at the end of simulation. By default the signature file is written on the 'write_tohost' function call.
- SignatureGranularity : The number of bytes per line in the signature file output. This is 16 by default but current test definitions use 4.

Defining the Start of the memory region containing the signature

- StartAddress : The address of the memory
- StartSymbol : The symbol, default 'signature_start'

Defining the End of the memory region containing signature

- EndAddress : The address of the memory
- EndSymbol : The symbol, default 'signature_end'
- ByteCount : The size in bytes

6.2.3 Data Format

The signature format, defined by RISCV.org, consists of 4 bytes per line (was previously 16 bytes per line) and can be set using the SignatureGranularity parameter. This requires that the size of the signature memory always starts and ends on a the granularity (4-byte) boundary. The end is reduced to the previous boundary if too big; in so doing we ensure that only data intended for the signature is included and not additional 'random' data.

6.2.4 Usage Example

The intercept/extension library is enabled on the virtual platform simulation using the -signaturedump argument and configured using the override argument on the command line.

6.2.4.1 Basic operation

```
> riscvOVPsim.exe -signaturedump \
    -override riscvOVPsim/cpu/sigdump/SignatureFile=<my filename>
```

Changing the memory region to use an alternative symbol

```
> riscvOVPsim.exe -signaturedump \
    -override riscvOVPsim/cpu/sigdump/SignatureFile=<my filename>
    -override riscvOVPsim/cpu/sigdump/StartSymbol=<symbol of start of memory>
    -override riscvOVPsim/cpu/sigdump/ByteCount=<number of bytes from start>
    -override riscvOVPsim/cpu/sigdump/SignatureAtEnd=T
```

If the program does not call 'write_to_host' we must also enable the signature to be written when simulation completes, typically this is when 'exit' is called.

6.3 Custom Instruction

6.3.1 Introduction

When running basic tests on the processor without C libraries or hardware to provide character output e.g. a UART; a custom instruction can be used to provide character output in the simulation environment. The custom instruction is added to a test using a MACRO so that the test can be compiled without the custom instruction for execution on hardware or with the custom instruction for execution on the simulator. Note: On hardware there is, therefore, no logging of the test execution and so only a pass/fail result can be obtained. On the simulator the logging can be used to indicate the flow of the test and where it diverges from the expected behavior.

6.3.2 Usage Example

The intercept/extension library is enabled on the virtual platform simulation using the -customcontrol argument.

```
> riscvOVPsim.exe -customcontrol
```

If the program executes the custom instruction a character will be displayed at stdout.

Chapter 7

Instruction Functional Coverage Usage

7.1 Overview of Instruction Functional Coverage

Instruction Functional Coverage as it relates to processor verification is a technology solution to measure what is being stimulated in the ISA in terms of which instructions, operands and values are driven into a processor.

If a signature comparison based verification methodology is adopted (as in the RISC-V Compliance suites) for comparison between device under test and reference, then functional coverage is only part of the story, as it is essential to measure the successful propagation of the results of the input instructions/values into the signature. Read more about this in the section below on Mutation Testing.

The Imperas coverage technology is built using the Imperas VAP intercept technology and is available as an extension library as source as a standard part of the Imperas commercial product offerings. This allows users to extend and modify functionality and coverage capability. Contact Imperas for more information.

riscvOVPsim includes a built in functional coverage engine which can be enabled to measure the executing instruction stream during simulation. There is no need for trace files post processing, or any other interaction.

Functional coverage commands are listed below, to see all commands use:

```
> riscvOVPsimPlus.exe --help
> riscvOVPsimPlus.exe --helpall
```

Example coverage command:

```
> riscvOVPsimPlus.exe --variant RVB32I --program eg.elf \
    --cover basic --extensions I --reportfile impCov.log
```

7.2 Basic Usage

The Imperas instruction functional coverage works by monitoring every instruction as it retires and recording information about it.

At the end of simulation this data is summarized in the console and simulation log file.

```
COVERAGE :: I :: threshold : 1 : instructions: seen 13/40 :  32.50%
    coverage points hit: 262/2952 :   8.88%
```

To see full data and write out a coverage report use –**reportfile**:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf \
    --cover basic --extensions I --reportfile impCov.log
```

To see those coverpoints not hit, use –**showuncovered**:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf \
    --cover basic --extensions I --reportfile impCov.log --showuncovered
```

7.2.1 Selecting what is covered

To measure coverage across different extensions use –**extensions** with a comma separated list:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf \
    --cover basic --extensions I,M,C
```

If you want to just see coverage on one instruction, use the –**instructions** command:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf
    --cover basic --instructions add
```

Or for several, use a comma separated list:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf
    --cover basic --instructions mul,div
```

Note: only one of –extensions or –instructions can be given.

By default a coverpoint is reported as covered if it is hit once, you can change this with –**countthreshold**:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf
    --cover basic --extensions I --countthreshold 4
```

Which will report 1 hit as 25%, 4 hits as 100% etc.

7.3 Coverage types

With the –**cover basic** command selected, it will report:

- instructions seen
- operands hit
- sign of operands
- cross of sign of values

With the –**cover extended** command selected, it will report:

- all of basic, plus
- comparison of if same registers used as different operands
- values of min, max, -1, 1, 0, marching 0s, marching 1s

7.4 Coverage data files

At the end of simulation coverage data can be written to a data file (yaml format):

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf
    --cover basic --extensions I --outputfile run1.yaml
```

This is a text file and can examined to see what coverpoints have been measured (and their current count values).

7.4.1 Accumulating coverage across multiple runs

If you have saved the data file from one run, you can use that as the start of coverage in a subsequent run:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg.elf \
    --cover basic --extensions I --inputfiles run1.yaml \
    --outputfile run2.yaml
```

And so to measure coverage for a complete test suite, run each test with its own output data file, and then at the end read them all in and write a coverage report:

Process each test, creating the data files:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg1.elf \
    --cover basic --extensions I --outputfile run1.yaml
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg2.elf \
    --cover basic --extensions I --outputfile run2.yaml
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg3.elf \
    --cover basic --extensions I --outputfile run3.yaml
```

Then collate the data and write a coverage report:

```
> $ riscvOVPsimPlus.exe --nosimulation \
    --cover basic --extensions RVI \
    --inputfiles run1.yaml,run2.yaml,run3.yaml \
    --reportfile impCov.log
```

Note the –**nosimulation** command does not simulate any instructions but does process the coverage commands.

7.5 Not measuring start up and shutdown instructions

Often when running a test suite there will be target specific code at the start and end of a test. It makes no sense to measure this as it is highly likely that each target will use different instructions. It makes more sense to control when the coverage starts and stops - this can be done using labels or addresses that control when coverage is counting.

There are two commands –**startcover**, –**finishcover**. For example:

```
> $ riscvOVPsimPlus.exe --variant RVB32I --program eg1.elf \
    --cover basic --extensions I \
    --startcover begin_testcode \
    --finishcover end_testcode
```

7.6 Covering Pseudo instructions

If you specify main extensions, like I, M etc., then pseudo instructions will be mapped to these main instructions and the main instructions covered.

Often hand written assembler code will use pseudo instructions and it might be necessary to measure the coverage on those. If you select the pseudo extensions, then any pseudo instruction encountered will not be mapped to main instructions, but will be measured and reported themselves. To see the list of available extensions, put in an illegal extension name, for example:

```
> $ riscvOVPsimPlus.exe --cover basic --extensions RVSS


    Error (ICV_INVI) ISA specification 'RVSS' contains 'RVSS' which is
    not a recognized ISA. Valid ISAs:
    I,M,A,F,D,C,Zicsr,Zifencei,
    Ipseudo,Fpseudo,Dpseudo,ZicsrPseudo,
    V,Vb,Vf,Vi,Vm,Vp,Vr,Vx,Zvamo,
    K,Zkn,Zkr,Zks,
    B,Zba,Zbb,Zbc,Zbe,Zbf,Zbm,Zbp,Zbr,Zbs,Zbt
```

7.7 Measuring Test Quality (Mutation Testing)

The RISC-V Compliance Suites use a methodology of testing where a reference runs the test and during that run records data into memory and subsequently saves the memory into a signature file. The test is then run on a device-under-test which also saves a signature file. The signature file is then compared to see if the device-under-test reports the same signature as the reference run.

Functional coverage measures the input instructions and a signature comparison checks if the device-under-test and the reference device created matching signatures.

So if you have 100% instruction functional coverage and matching signatures - then the device-under-test and the reference device behave the same - right. Well actually it is not yes - but maybe...

What happens if due to bad coding of the test, some of the input values do not actually affect anything in the signature. What happens if the signature writing actually writes the wrong bit of memory. (Don't laugh - that is what one of the RISC-V Compliance tests did for a year until the Imperas Mutating Simulator found that sections of the signature were all 1's as the test had happily been writing initialized memory out and not where it had recorded test results... - so the test passed and none of the test code might have actually ran!)

To measure test quality Imperas have developed an extremely fast mutating fault simulator that automatically detects if test instructions do not affect the signature and thus are not really of any use.

Without use of tool such as the Imperas Mutating Simulator it is not possible to say with certainty that a test is high quality and in fact does what it claims to do.

Functional coverage measures how much is stimulated, and a mutating simulator measures what is detected.

Functional coverage is not a measure of quality - it is only an indication of a hope - and a mutating simulator confirms that hope.

For more information on the Imperas mutating simulator - contact Imperas.

7.8 Command summary

For list of all commands and their short descriptions, see the Appendix.

Chapter 8

Building your own platform and components

Note that an Imperas OVP Fixed Platform is restricted and may only run as provided is and can not be further extended.

However, a platform in OVP is made up from models of processors, memories, and other components such as behavioral peripherals connected using hierarchical bus connections. All components have APIs defined in C and platforms can be created in C/C++ or SystemC that instantiate these components.

You can create models and platforms directly in C/C++ using the standard OVP APIs. To execute and run these models, you need a simulator that implements the OVP APIs. This fixed platform does not support this and you can get access to OVP simulators from Imperas Software and OVPworld.org.

Imperas/OVP provide iGen which is a productivity tool that from a simple iGen input script creates a set of C files in the correct structure, all the main structural parts of the components and provides the placeholders for the behavioral code. For more information on iGen visit this link: www.imperas.com/iGen. To read the iGen user guide, visit this link: www.ovpworld.org/igen-model-generator-introduction.

8.1 Creating Peripheral Models with iGen

A peripheral model template created by iGen as a C file will

1. Construct a model instance
2. Construct bus and net ports for connection to the platform
3. Construct memory mapped registers and memory regions
4. Construct formal parameters which can be set when the peripheral is instanced in a platform or module and overridden by the simulator to control features of the peripheral model.

The peripheral template will provide empty functions, stubs, that can be filled in by the user to add behavior to the model.

The peripheral template can be compiled and used in simulations to provide the peripheral device programmers view i.e. the register structure and a default behavior.

iGen can also generate a SystemC TLM2 interface for the model. Examples of SystemC TLM2 interfaces for OVP peripherals have been tested with all major SystemC TLM2 simulators.

For more information on iGen and peripherals visit: www.ovpworld.org/igen-peripheral-generator-user-guide.

Most peripherals are available as open source and there over 200 listed on the OVPworld website here: www.ovpworld.org/library. You can download and look at the source and modify it to make it your own peripherals, or you can use them directly in your platforms.

8.2 Creating Platforms with iGen

OVP platforms are a collection of components connected together into levels of hierarchy in a system to be simulated. This is a program in C/C++ making calls into OVP APIs and normally compiled into an executable or as a shared object/dynamically linked library and loaded by the simulator at run time.

Platforms are created by writing scripts and then using iGen to generate C or SystemC code that calls functions from the OP API.

For more information on iGen and platforms/modules visit:

www.ovpworld.org/igen-platform-and-module-creation-user-guide.

8.3 Creating Processor Models

With the OVP open standard APIs you can write your own processor models in C. Imperas has developed over 200 processor models using this standard modeling approach. Visit www.ovpworld.org/variants for more information on the available processor models.

For MIPS there are over 45 different MIPS processor models. See: www.ovpworld.org/library.

For ARM there are over 100 different ARM processor models. See: www.ovpworld.org/library.

For RISC-V there are over 25 different RISC-V models. See: www.ovpworld.org/library.

For most processors model source is available from www.OVPworld.org as source under the Apache 2.0 open source license and so you can download the source and modify it if you want to. However modifying the main model source might not be the best approach in terms of maintainable models with extensions, and so Imperas has developed a standard way to extend existing processor models to add instructions and registers without making changes to the source of the main model. See www.ovpworld.org/creating-instruction-accurate-processor-models-using-the-vmi-api chapter 26 for more information.

Chapter 9

Debugging Multi-Core platforms

When you have a single processor instance in a platform the normal software debug approach is to connect up a GDB to the processor and be able to accomplish source code debug. This works well for a single processor and single GDB but problems occur when you have different processor cores in the platform or have complex peripherals as well. A single GDB is not much help and neither is having a different GDB connected to each processor. You the user become the debug scheduler and having to click continue and step in a variety of different windows etc.

It is very difficult to debug a multicore platform with just GDB.

If the platform has more than one core, Imperas has developed an advanced multi-core debugger called Multi-Processor Debug (MPD). An introduction to this is found: www.imperas.com/MPD.

There is a good video introduction of MPD on a platform incorporating a quad core ARM Cortex-A15MPx4 and an Andes RISC-V N25 core here:

www.imperas.com/mpd-andes-risc-v-n25-running-freertos-and-arm-cortex.

Another good video shows the SiFive RISC-V U540-MC virtual platform running SMP Linux being debugged with the Imperas Multi-Processor debugger:

www.imperas.com/sifive-risc-v-u54-mc-booting-smp-linux-being-debugged-with-MPD.

Appendices

Appendix A

riscvOVPsim Help Commands

To see commonly used command line options:

```
riscvOVPsim.exe --help
```

To see all command line options:

```
riscvOVPsim.exe --helpall
```

To see the list of processor variants:

```
riscvOVPsim.exe --showvariants
```

To run a program:

```
riscvOVPsim.exe --variant <processor variant>
      --program <path to program>
```

A.1 help

A.1.1 control

Flag	Short	Argument	Description
–finishafter	I	[processor=]integer	Finish simulation after this many instructions
–finishtime	F	[module=]seconds	Finish simulation at this time
–showexpiry		[module]	Show how many days before this executable expires and can no longer run

Table A.1: control

A.1.2 coverage

Flag	Short	Argument	Description
–countthreshold		uns32	Number of counts of each cover point required to report 100% coverage
–cover		string	Turn on functional coverage and choose the set of cover points
–extensions		string	List of ISA extensions to cover (comma separated list)
–finishcover		string	Address of end of code to be covered (label or address)
–inputfiles		string	Comma separated list of files or directories (a directory is scanned for *.yaml). Used to accumulate data from other runs
–instructions		string	List of instructions to cover (comma separated list)
–outputfile		string	Write a coverage output data file.
–reportfile		string	Write a coverage report.
–showuncovered			Show in coverage report the coverpoints not hit
–startcover		string	Address of start of code to be covered (label or address)

Table A.2: coverage

A.1.3 diagnostics

Flag	Short	Argument	Description
–help	h		Print list of flags
–helpall			Print complete list of flags
–showmodeloverrides		[module]	Show all model parameters that can be overridden

Table A.3: diagnostics

A.1.4 library

Flag	Short	Argument	Description
–showvariants		[processor=]	Show processor variants

Table A.4: library

A.1.5 log

Flag	Short	Argument	Description
–logfile		filename	Output log file
–logflush			Flush data to the log file after each write
–output	o	filename	Output log file
–version			Print version information

Table A.5: log

A.1.6 parameters

Flag	Short	Argument	Description
–override	O	name=value	Override a parameter value. Use -showoverrides or -showmodeloverrides for a list
–variant		[processor=]variant	Set a processor variant. Use -showvariants for a list

Table A.6: parameters

A.1.7 platform

Flag	Short	Argument	Description
–addressbits		uns32	Number of bits on address bus (default=32)
–customcontrol			Load the custom control utility - provides character output using custom instruction
–ecallresultreg		uns32	When set the specified register is read on an ecall instruction to specify test pass/fail (3=GP, 10=A0 or 28=T3)
–exitonaddress		uns64	Specify an address that if executed will cause simulation exit
–exitonsymbol		string	Specify a symbol that if executed will cause simulation exit
–finishonaddress		uns64	Specify an address that if executed will cause simulation exit
–finishonopcode		uns64	Specify an opcode that if executed will cause simulation exit
–finishonsymbol		string	Specify a symbol that if executed will cause simulation exit
–finishonterminate			If the function terminate() is called the simulation will exit
–finishonwritetohost			If the function write_to_host() is called the simulation will exit
–signaturedump			Load the signature dump utility
–signaturedumphelp			Information about the signature dump utility
–usehwregnames			Use hardware register names x0-x31 and f0-f31 instead of ABI register names

Table A.7: platform

A.1.8 program

Flag	Short	Argument	Description
–argv		arguments	Pass all remaining values to the application main (applies to all processors)
–program		[processor=]filename	Execute this program (on this processor)

Table A.8: program

A.2 helpall

A.2.1 control

Flag	Short	Argument	Description
–callcommand		command	Call a command in a plugin. Use -showcommands for a list.
–controlfile	C	filename	Read a control file
–finishafter	I	[processor=]integer	Finish simulation after this many instructions
–finishtime	F	[module=]seconds	Finish simulation at this time
–nosimulation		[module]	Do not simulate. Simulator will exit after loading the platform
–showexpiry		[module]	Show how many days before this executable expires and can no longer run
–stoponcontrolc		[module]	Installs SIGINT and SIGTERM handlers used by the simulator to stop when safe to do so

Table A.9: control

A.2.2 coverage

Flag	Short	Argument	Description
–countthreshold		uns32	Number of counts of each cover point required to report 100% coverage
–cover		string	Turn on functional coverage and choose the set of cover points
–extensions		string	List of ISA extensions to cover (comma separated list)
–finishcover		string	Address of end of code to be covered (label or address)
–inputfiles		string	Comma separated list of files or directories (a directory is scanned for *.yaml). Used to accumulate data from other runs
–instructions		string	List of instructions to cover (comma separated list)
–outputfile		string	Write a coverage output data file.
–reportfile		string	Write a coverage report.
–showuncovered			Show in coverage report the coverpoints not hit
–startcover		string	Address of start of code to be covered (label or address)

Table A.10: coverage

A.2.3 diagnostics

Flag	Short	Argument	Description
–help	h		Print list of flags
–helpall			Print complete list of flags
–showcommands		[module]	Show commands that can be called with –callcommand
–showmodeloverrides		[module]	Show all model parameters that can be overridden
–showoverrides		[module]	Show all parameters that can be overridden
–showsystemoverrides		[module]	Show all the simulator parameters
–verbosecpu		[processor]	Puts the processor model in verbose mode

Table A.11: diagnostics

A.2.4 library

Flag	Short	Argument	Description
–showvariants		[processor=]	Show processor variants

Table A.12: library

A.2.5 log

Flag	Short	Argument	Description
–logfile		filename	Output log file
–logflush			Flush data to the log file after each write
–nowarnings	w		Suppress warnings
–output	o	filename	Output log file
–version			Print version information
–werror	W		Treat warnings as errors

Table A.13: log

A.2.6 parameters

Flag	Short	Argument	Description
–override	O	name=value	Override a parameter value. Use -showoverrides or -showmodeloverrides for a list
–variant		[processor=]variant	Set a processor variant. Use -showvariants for a list

Table A.14: parameters

A.2.7 platform

Flag	Short	Argument	Description
–addressbits		uns32	Number of bits on address bus (default=32)

–customcontrol			Load the custom control utility - provides character output using custom instruction
–ecallresultreg		uns32	When set the specified register is read on an ecall instruction to specify test pass/fail (3=GP, 10=A0 or 28=T3)
–exitonaddress		uns64	Specify an address that if executed will cause simulation exit
–exitonsymbol		string	Specify a symbol that if executed will cause simulation exit
–finishonaddress		uns64	Specify an address that if executed will cause simulation exit
–finishonopcode		uns64	Specify an opcode that if executed will cause simulation exit
–finishonsymbol		string	Specify a symbol that if executed will cause simulation exit
–finishonterminate			If the function terminate() is called the simulation will exit
–finishonwritetohost			If the function write_to_host() is called the simulation will exit
–signaturedump			Load the signature dump utility
–signaturedumphelp			Information about the signature dump utility
–usehwregnames			Use hardware register names x0-x31 and f0-f31 instead of ABI register names

Table A.15: platform

A.2.8 program

Flag	Short	Argument	Description
–argv		arguments	Pass all remaining values to the application main (applies to all processors)
–elfusevma		[processor]	Use ELF VMA addresses rather than LMA
–envp		name=value	Pass values (until the next '-') to the application environment list
–loadlimit32		[processor]	Limit each memory load to 32 bits
–loadlimit64		[processor]	Limit each memory load to 64 bits
–loadphysical		[processor]	Use ELF physical addresses
–loadsignextend		[processor]	Sign-extend ELF addresses from 32 to 64 bits
–objfile		[processor=]filename	Load object onto CPU. Set PC to start address
–objfilenoentry		[processor=]filename	Load object onto CPU. Do not set PC to start address
–objfileuseentry	f	[processor=]filename	Load object onto CPU. Set PC to start address
–program		[processor=]filename	Execute this program (on this processor)

Table A.16: program

Appendix B

riscvOVPsim model configuration options

RV32GC Model Overrides

Fundamental

```
--override riscvOVPsim/cpu/Smepmp_version=none (Enumeration) (default=none) (default) Specify required Smepmp Architecture
      version
--override riscvOVPsim/cpu/add_Extensions=MAFDC (String) (default=) (override) Add extensions specified by letters to
      misa.Extensions (for example, specify "VD" to add V and D features)
--override riscvOVPsim/cpu/add_Extensions_mask= (String) (default=) (default) Add extensions specified by letters to
      mask of writable bits in misa.Extensions (for example, specify "VD" to add V and D features)
--override riscvOVPsim/cpu/add_implicit_Extensions= (String) (default=) (default) Add extensions specified by letters
      to implicitly-present extensions not visible in misa.Extensions
--override riscvOVPsim/cpu/enable_expanded=F (Boolean) (default=F) (default) Specify that 48-bit and 64-bit expanded
      instructions are supported
--override riscvOVPsim/cpu/endian=none (Endian) (default=none) (default) Model endian
--override riscvOVPsim/cpu/endianFixed=F (Boolean) (default=F) (default) Specify that data endianness is fixed (mstatus.{MBE,SBE,UBE}
      fields are read-only)
--override riscvOVPsim/cpu/misa_Extensions=0x14112d (Uns32) (default=0x14112d) (default) Override default value of misa.Extensions
--override riscvOVPsim/cpu/misa_Extensions_mask=0x112d (Uns32) (default=0x112d) (default) Override mask of writable bits
      in misa.Extensions
--override riscvOVPsim/cpu/misa_MXL=1 (Uns32) (default=1) (default) Override default value of misa.MXL
--override riscvOVPsim/cpu/numHarts=0 (Uns32) (default=0) (default) Specify the number of hart contexts in a multiprocessor
--override riscvOVPsim/cpu/priv_version=1.12 (Enumeration) (default=1.12) (default) Specify required Privileged Architecture
      version
--override riscvOVPsim/cpu/sub_Extensions= (String) (default=) (default) Remove extensions specified by letters from
      misa.Extensions (for example, specify "VD" to remove V and D features)
--override riscvOVPsim/cpu/sub_Extensions_mask= (String) (default=) (default) Remove extensions specified by letters
      from mask of writable bits in misa.Extensions (for example, specify "VD" to remove V and D features)
--override riscvOVPsim/cpu/sub_implicit_Extensions= (String) (default=) (default) Remove extensions specified by letters
      from implicitly-present extensions not visible in misa.Extensions
--override riscvOVPsim/cpu/user_version=20191213 (Enumeration) (default=20191213) (default) Specify required User Architecture
      version
--override riscvOVPsim/cpu/variant=RV32GC (Enumeration) (default=RV32I) (override) Selects variant (either a generic
      UISA or a specific model)
```

Compressed Extension

```
--override riscvOVPsim/cpu/Zca=T (Boolean) (default=T) (default) Specify that Zca is implemented
--override riscvOVPsim/cpu/Zcb=F (Boolean) (default=F) (default) Specify that Zcb is implemented
--override riscvOVPsim/cpu/Zcf=T (Boolean) (default=T) (default) Specify that Zcf is implemented
--override riscvOVPsim/cpu/Zcmb=F (Boolean) (default=F) (default) Specify that Zcmb is implemented
--override riscvOVPsim/cpu/Zcmp=F (Boolean) (default=F) (default) Specify that Zcmp is implemented
--override riscvOVPsim/cpu/Zcmpe=F (Boolean) (default=F) (default) Specify that Zcmpe is implemented
--override riscvOVPsim/cpu/Zcmt=F (Boolean) (default=F) (default) Specify that Zcmt is implemented
--override riscvOVPsim/cpu/compress_version=0.70.1 (Enumeration) (default=0.70.1) (default) Specify required Compressed
      Architecture version
```

Debug Extension

```
--override riscvOVPsim/cpu/debug_mode=none (Enumeration) (default=none) (default) Specify how Debug mode is implemented
--override riscvOVPsim/cpu/debug_version=1.0.0-STABLE (Enumeration) (default=1.0.0-STABLE) (default) Specify required
      Debug Architecture version
```

Interrupts Exceptions

```
--override riscvOVPsim/cpu/CLINT_address=0 (Uns64) (default=0) (default) Specify base address of internal CLINT model
      (or 0 for no CLINT)
--override riscvOVPsim/cpu/ecode_mask=0x7fffffff (Uns64) (default=0x7fffffff) (default) Specify hardware-enforced mask
      of writable bits in xcause.ExceptionCode
--override riscvOVPsim/cpu/ecode_nmi=0 (Uns64) (default=0) (default) Specify xcause.ExceptionCode for NMI
--override riscvOVPsim/cpu/external_int_id=F (Boolean) (default=F) (default) Whether to add nets allowing External Interrupt
      ID codes to be forced
--override riscvOVPsim/cpu/force_mideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts always delegated
      to lower-priority execution level from Machine execution level
--override riscvOVPsim/cpu/force_sideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts always delegated
      to User execution level from Supervisor execution level
--override riscvOVPsim/cpu/local_int_num=0 (Uns32) (default=0) (default) Specify number of supplemental local interrupts
--override riscvOVPsim/cpu/mtvec_is_ro=F (Boolean) (default=F) (default) Specify whether mtvec CSR is read-only
--override riscvOVPsim/cpu/nmi_address=0 (Uns64) (default=0) (default) Override NMI vector address
--override riscvOVPsim/cpu/no_edeleg=0 (Uns64) (default=0) (default) Specify mask of exceptions that cannot be delegated
      to lower-priority execution levels
--override riscvOVPsim/cpu/no_ideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts that cannot be delegated
      to lower-priority execution levels
--override riscvOVPsim/cpu/reset_address=0 (Uns64) (default=0) (default) Override reset vector address
--override riscvOVPsim/cpu/rnmi_version=none (Enumeration) (default=none) (default) Specify required RNMI Architecture
      version
--override riscvOVPsim/cpu/trap_preserves_lr=F (Boolean) (default=F) (default) Whether a trap preserves active LR/SC
      state
--override riscvOVPsim/cpu/tval_ii_code=T (Boolean) (default=T) (default) Specify whether mtval/stval contain faulting
      instruction bits on illegal instruction exception
--override riscvOVPsim/cpu/tval_zero=F (Boolean) (default=F) (default) Specify whether mtval/stval/utval are hard wired
      to zero
--override riscvOVPsim/cpu/tval_zero_ebreak=F (Boolean) (default=F) (default) Specify whether mtval/stval/utval are set
      to zero by an ebreak
--override riscvOVPsim/cpu/tvec_align=0 (Uns32) (default=0) (default) Specify hardware-enforced alignment of mtvec/stvec/utvec
      when Vectored interrupt mode enabled
--override riscvOVPsim/cpu/unimp_int_mask=0 (Uns64) (default=0) (default) Specify mask of unimplemented interrupts (e.g.
      1<<9 indicates Supervisor external interrupt unimplemented)
--override riscvOVPsim/cpu/xret_preserves_lr=F (Boolean) (default=F) (default) Whether an xret instruction preserves
      active LR/SC state
```

Floating Point

```
--override riscvOVPsim/cpu/Zfh=F (Boolean) (default=F) (default) Specify that Zfh is implemented (IEEE half-precision
      floating point is supported)
--override riscvOVPsim/cpu/Zfhmin=F (Boolean) (default=F) (default) Specify that Zfhmin is implemented (restricted IEEE
      half-precision floating point is supported)
--override riscvOVPsim/cpu/Zfinx_version=none (Enumeration) (default=none) (default) Specify version of Zfinx implemented
      (use integer register file for floating point instructions)
--override riscvOVPsim/cpu/d_requires_f=F (Boolean) (default=F) (default) If D and F extensions are separately enabled
      in the misa CSR, whether D is enabled only if F is enabled
--override riscvOVPsim/cpu/enable_fflags_i=F (Boolean) (default=F) (default) Whether fflags_i artifact register present
      (shows per-instruction floating point flags)
--override riscvOVPsim/cpu/mstatus_FS=0 (Uns32) (default=0) (default) Override default value of mstatus.FS (initial state
      of floating point unit)
--override riscvOVPsim/cpu/mstatus_fs_mode=write_1 (Enumeration) (default=write_1) (default) Specify conditions causing
      update of mstatus.FS to dirty
```

Simulation Artifact

```
--override riscvOVPsim/cpu/ABI_d=T (Boolean) (default=T) (default) Specify whether D registers are used for parameters
      (ABI SemiHosting)
--override riscvOVPsim/cpu/ASID_cache_size=8 (Uns32) (default=8) (default) Specifies the number of different ASIDs for
      which TLB entries are cached; a value of 0 implies no limit
--override riscvOVPsim/cpu/CSR_remap= (String) (default=) (default) Comma-separated list of CSR number mappings, each
      of the form <csrName>=<number>
--override riscvOVPsim/cpu/enable_CSR_bus=F (Boolean) (default=F) (default) Add artifact CSR bus port, allowing CSR registers
      to be externally implemented
--override riscvOVPsim/cpu/no_pseudo_inst=F (Boolean) (default=F) (default) Specify whether pseudo-instructions should
      not be reported in trace and disassembly
--override riscvOVPsim/cpu/traceVolatile=F (Boolean) (default=F) (default) Specify whether volatile registers (e.g. minstret)
      should be shown in change trace
--override riscvOVPsim/cpu/use_hw_reg_names=F (Boolean) (default=F) (default) Specify whether to use hardware register
      names x0-x31 and f0-f31 instead of ABI register names
--override riscvOVPsim/cpu/verbose=T (Boolean) (default=F) (platform) Specify verbose output messages
```

Memory

```
--override riscvOVPsim/cpu/ASID_bits=9 (Uns32) (default=9) (default) Specify the number of implemented ASID bits
--override riscvOVPsim/cpu/Sv_modes=3 (Uns32) (default=3) (default) Specify bit mask of implemented address translation
       modes (e.g. (1<<0)+(1<<8) indicates "bare" and "Sv39" modes may be selected in satp.MODE)
--override riscvOVPsim/cpu/amo_aborts_lr_sc=F (Boolean) (default=F) (default) Specify whether AMO operations abort any
       active LR/SC pair
--override riscvOVPsim/cpu/lr_sc_grain=1 (Uns32) (default=1) (default) Specify byte granularity of ll/sc lock region
       (constrained to a power of two)
--override riscvOVPsim/cpu/unaligned=F (Boolean) (default=F) (default) Specify whether the processor supports unaligned
       memory accesses
--override riscvOVPsim/cpu/unalignedAMO=F (Boolean) (default=F) (default) Specify whether the processor supports unaligned
       memory accesses for AMO instructions
--override riscvOVPsim/cpu/unaligned_low_pri=F (Boolean) (default=F) (default) Specify whether address misaligned exceptions
       are lower priority than page or access fault exceptions
--override riscvOVPsim/cpu/updatePTEA=F (Boolean) (default=F) (default) Specify whether hardware update of PTE A bit
       is supported
--override riscvOVPsim/cpu/updatePTED=F (Boolean) (default=F) (default) Specify whether hardware update of PTE D bit
       is supported
```

Instruction CSR Behavior

```
--override riscvOVPsim/cpu/counteren_mask=0xffffffff (Uns32) (default=0xffffffff) (default) Specify hardware-enforced
       mask of writable bits in mcounteren/scounteren registers
--override riscvOVPsim/cpu/cycle_undefined=F (Boolean) (default=F) (default) Specify that the cycle CSR is undefined
--override riscvOVPsim/cpu/hpmcounter_undefined=F (Boolean) (default=F) (default) Specify that the hpmcounter CSRs are
       undefined
--override riscvOVPsim/cpu/instret_undefined=F (Boolean) (default=F) (default) Specify that the instret CSR is undefined
--override riscvOVPsim/cpu/noinhibit_mask=0 (Uns32) (default=0) (default) Specify hardware-enforced mask of always-zero
       bits in mcountinhibit register
--override riscvOVPsim/cpu/time_undefined=F (Boolean) (default=F) (default) Specify that the time CSR is undefined
--override riscvOVPsim/cpu/wfi_is_nop=F (Boolean) (default=F) (default) Specify whether WFI should be treated as a NOP
       (if not, halt while waiting for interrupts)
```

CSR Masks

```
--override riscvOVPsim/cpu/envcfg_mask=0x8000000000000001 (Uns64) (default=0x8000000000000001) (default) Specify hardware-enforced
       mask of writable bits in envcfg registers
--override riscvOVPsim/cpu/mip_mask=0x337 (Uns64) (default=0x337) (default) Specify hardware-enforced mask of writable
       bits in mip register
--override riscvOVPsim/cpu/mtvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
       in mtvec register
--override riscvOVPsim/cpu/mtvec_sext=F (Boolean) (default=F) (default) Specify whether mtvec is sign-extended from most-significant
       bit
--override riscvOVPsim/cpu/sip_mask=0x103 (Uns64) (default=0x103) (default) Specify hardware-enforced mask of writable
       bits in sip register
--override riscvOVPsim/cpu/stvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
       in stvec register
--override riscvOVPsim/cpu/stvec_sext=F (Boolean) (default=F) (default) Specify whether stvec is sign-extended from most-significant
       bit
--override riscvOVPsim/cpu/tdata1_mask=0xffffffffffffffff (Uns64) (default=0xffffffffffffffff) (default) Specify hardware-enforced
       mask of writable bits in Trigger Module tdata1 register
```

Trigger

```
--override riscvOVPsim/cpu/amo_trigger=F (Boolean) (default=F) (default) Specify whether AMO load/store operations activate
       triggers
--override riscvOVPsim/cpu/mcontext_bits=6 (Uns32) (default=6) (default) Specify the number of implemented bits in mcontext
--override riscvOVPsim/cpu/mcontext_undefined=F (Boolean) (default=F) (default) Specify that the mcontext CSR is undefined
--override riscvOVPsim/cpu/mcontrol_maskmax=63 (Uns32) (default=63) (default) Specify mcontrol.maskmax value
--override riscvOVPsim/cpu/mscontext_undefined=F (Boolean) (default=F) (default) Specify that the mscontext CSR is undefined
       (Debug Version 0.14.0 and later)
--override riscvOVPsim/cpu/mvalue_bits=6 (Uns32) (default=6) (default) Specify the number of implemented bits in textra.mvalue
       (if zero, textra.mselect is tied to zero)
--override riscvOVPsim/cpu/no_hit=F (Boolean) (default=F) (default) Specify that tdata1.hit is unimplemented
--override riscvOVPsim/cpu/no_sselect_2=F (Boolean) (default=F) (default) Specify that textra.sselect=2 is not supported
       (no trigger match by ASID)
--override riscvOVPsim/cpu/scontext_bits=16 (Uns32) (default=16) (default) Specify the number of implemented bits in
       scontext
--override riscvOVPsim/cpu/scontext_undefined=F (Boolean) (default=F) (default) Specify that the scontext CSR is undefined
--override riscvOVPsim/cpu/svalue_bits=16 (Uns32) (default=16) (default) Specify the number of implemented bits in textra.svalue
       (if zero, textra.sselect is tied to zero)
--override riscvOVPsim/cpu/tcontrol_undefined=F (Boolean) (default=F) (default) Specify that the tcontrol CSR is undefined
--override riscvOVPsim/cpu/tinfo=125 (Uns32) (default=125) (default) Override tinfo register (for all triggers)
--override riscvOVPsim/cpu/tinfo_undefined=F (Boolean) (default=F) (default) Specify that the tinfo CSR is undefined
--override riscvOVPsim/cpu/trigger_num=4 (Uns32) (default=4) (default) Specify the number of implemented hardware triggers
```

PMP Configuration

```
--override riscvOVPsim/cpu/PMP_decompose=F (Boolean) (default=F) (default) Whether unaligned PMP accesses are decomposed
       into separate aligned accesses
--override riscvOVPsim/cpu/PMP_grain=0 (Uns32) (default=0) (default) Specify PMP region granularity, G (0 => 4 bytes,
       1 => 8 bytes, etc)
--override riscvOVPsim/cpu/PMP_initialparams=F (Boolean) (default=F) (default) Enable parameters to change the reset
       values for PMP CSRs
--override riscvOVPsim/cpu/PMP_maskparams=F (Boolean) (default=F) (default) Enable parameters to change the read-only
       masks for PMP CSRs
--override riscvOVPsim/cpu/PMP_max_page=0 (Uns32) (default=0) (default) Specify the maximum size of PMP region to map
       if non-zero (may improve performance; constrained to a power of two)
--override riscvOVPsim/cpu/PMP_registers=16 (Uns32) (default=16) (default) Specify the number of implemented PMP address
       registers
--override riscvOVPsim/cpu/PMP_undefined=F (Boolean) (default=F) (default) Whether accesses to unimplemented PMP registers
       are undefined (if True) or write ignored and zero (if False)
```

Other Extensions

```
--override riscvOVPsim/cpu/Smstateen=F (Boolean) (default=F) (default) Specify that Smstateen is implemented
--override riscvOVPsim/cpu/Svinval=F (Boolean) (default=F) (default) Specify that Svinval is implemented
--override riscvOVPsim/cpu/Svnapot_page_mask=0 (Uns64) (default=0) (default) Specify mask of implemented Svnapot intermediate
       page sizes (e.g. 1<<16 means 64KiB contiguous regions are supported)
--override riscvOVPsim/cpu/Svpbmt=F (Boolean) (default=F) (default) Specify that Svpbmt is implemented
--override riscvOVPsim/cpu/Zicbom=F (Boolean) (default=F) (default) Specify that Zicbom is implemented
--override riscvOVPsim/cpu/Zicbop=F (Boolean) (default=F) (default) Specify that Zicbop is implemented
--override riscvOVPsim/cpu/Zicboz=F (Boolean) (default=F) (default) Specify that Zicboz is implemented
--override riscvOVPsim/cpu/Zicsr=T (Boolean) (default=T) (default) Specify that Zicsr is implemented
--override riscvOVPsim/cpu/Zifencei=T (Boolean) (default=T) (default) Specify that Zifencei is implemented
--override riscvOVPsim/cpu/Zmmul=F (Boolean) (default=F) (default) Specify that Zmmul is implemented
```

CSR Defaults

```
--override riscvOVPsim/cpu/marchid=0 (Uns64) (default=0) (default) Override marchid register
--override riscvOVPsim/cpu/mconfigptr=0 (Uns64) (default=0) (default) Override mconfigptr register
--override riscvOVPsim/cpu/mhartid=0 (Uns64) (default=0) (default) Override mhartid register (or first mhartid of an
       incrementing sequence if this is an SMP variant)
--override riscvOVPsim/cpu/mimpid=0 (Uns64) (default=0) (default) Override mimpid register
--override riscvOVPsim/cpu/mseccfg=0 (Uns64) (default=0) (default) Override mseccfg register
--override riscvOVPsim/cpu/mtvec=0 (Uns64) (default=0) (default) Override mtvec register
--override riscvOVPsim/cpu/mvendorid=0 (Uns64) (default=0) (default) Override mvendorid register
```

Fast Interrupt

```
--override riscvOVPsim/cpu/CLICLEVELS=0 (Uns32) (default=0) (default) Specify number of interrupt levels implemented
       by CLIC, or 0 if CLIC absent
```

pk

```
--override riscvOVPsim/cpu/pk/userargv=0x0 (Pointer) (default=0x0) (default) Pointer to argv structure
--override riscvOVPsim/cpu/pk/userenvp=0x0 (Pointer) (default=0x0) (default) Pointer to envp structure
--override riscvOVPsim/cpu/pk/reportExitErrors=F (Boolean) (default=F) (default) Report non-zero exit() return codes as simulator
       errors
--override riscvOVPsim/cpu/pk/initsp=0 (Uns64) (default=0) (default) Stack Pointer initialization
--override riscvOVPsim/cpu/pk/strace=F (Boolean) (default=F) (default) trace  proxy system calls (default)
```

sigdump

```
--override riscvOVPsim/cpu/sigdump/ResultReg=28 (Uns32) (default=28) (default) Result Register for RISCV.org Conformance
          Test. 3=GP, 10=A0 or 28=T3 (default)
--override riscvOVPsim/cpu/sigdump/SignatureFile=(null) (String) (default=(null)) (default) Name of the signature file
--override riscvOVPsim/cpu/sigdump/SignatureAtEnd=F (Boolean) (default=F) (default) Generate a Signature file at the end
          of simulation (default to generate on detection of call to write_tohost())
--override riscvOVPsim/cpu/sigdump/SignatureGranularity=16 (Uns32) (default=16) (default) Granularity of signature file (supports
          default 16 or 4 bytes)
--override riscvOVPsim/cpu/sigdump/SignatureMinWrites=1 (Uns32) (default=1) (default) Specify the minimum number of writes
          to signature. Error generated it not reached. Set to 0 to disable.
--override riscvOVPsim/cpu/sigdump/StartAddress=0 (Uns32) (default=0) (default) Address of the Start Symbol
--override riscvOVPsim/cpu/sigdump/StartSymbol=begin_signature (String) (default=begin_signature) (default) Name of the Start
          Symbol
```

```
--override riscvOVPsim/cpu/sigdump/EndAddress=0 (Uns32) (default=0) (default) Address of the End Symbol
--override riscvOVPsim/cpu/sigdump/EndSymbol=end_signature (String) (default=end_signature) (default) Name of the End Symbol
--override riscvOVPsim/cpu/sigdump/ByteCount=16 (Uns32) (default=16) (default) Size of region in bytes (must be granularity
          sizebyte blocks)
--override riscvOVPsim/cpu/sigdump/SignatureDumpToStdout=T (Boolean) (default=T) (default) Control of dumping Signature values
          to Stdout (default enabled)
```

RV64GCN Model Overrides

Fundamental

```
--override riscvOVPsim/cpu/Smepmp_version=none (Enumeration) (default=none) (default) Specify required Smepmp Architecture
       version
--override riscvOVPsim/cpu/add_Extensions=MAFDCN (String) (default=) (override) Add extensions specified by letters to
       misa.Extensions (for example, specify "VD" to add V and D features)
--override riscvOVPsim/cpu/add_Extensions_mask= (String) (default=) (default) Add extensions specified by letters to
       mask of writable bits in misa.Extensions (for example, specify "VD" to add V and D features)
--override riscvOVPsim/cpu/add_implicit_Extensions= (String) (default=) (default) Add extensions specified by letters
       to implicitly-present extensions not visible in misa.Extensions
--override riscvOVPsim/cpu/enable_expanded=F (Boolean) (default=F) (default) Specify that 48-bit and 64-bit expanded
       instructions are supported
--override riscvOVPsim/cpu/endian=none (Endian) (default=none) (default) Model endian
--override riscvOVPsim/cpu/endianFixed=F (Boolean) (default=F) (default) Specify that data endianness is fixed (mstatus.{MBE,SBE,UBE}
       fields are read-only)
--override riscvOVPsim/cpu/misa_Extensions=0x14312d (Uns32) (default=0x14312d) (default) Override default value of misa.Extensions
--override riscvOVPsim/cpu/misa_Extensions_mask=0x312d (Uns32) (default=0x312d) (default) Override mask of writable bits
       in misa.Extensions
--override riscvOVPsim/cpu/misa_MXL=2 (Uns32) (default=2) (default) Override default value of misa.MXL
--override riscvOVPsim/cpu/numHarts=0 (Uns32) (default=0) (default) Specify the number of hart contexts in a multiprocessor
--override riscvOVPsim/cpu/priv_version=1.12 (Enumeration) (default=1.12) (default) Specify required Privileged Architecture
       version
--override riscvOVPsim/cpu/sub_Extensions= (String) (default=) (default) Remove extensions specified by letters from
       misa.Extensions (for example, specify "VD" to remove V and D features)
--override riscvOVPsim/cpu/sub_Extensions_mask= (String) (default=) (default) Remove extensions specified by letters
       from mask of writable bits in misa.Extensions (for example, specify "VD" to remove V and D features)
--override riscvOVPsim/cpu/sub_implicit_Extensions= (String) (default=) (default) Remove extensions specified by letters
       from implicitly-present extensions not visible in misa.Extensions
--override riscvOVPsim/cpu/user_version=20191213 (Enumeration) (default=20191213) (default) Specify required User Architecture
       version
--override riscvOVPsim/cpu/variant=RV64GCN (Enumeration) (default=RV32I) (override) Selects variant (either a generic
       UISA or a specific model)
```

Compressed Extension

```
--override riscvOVPsim/cpu/Zca=T (Boolean) (default=T) (default) Specify that Zca is implemented
--override riscvOVPsim/cpu/Zcb=F (Boolean) (default=F) (default) Specify that Zcb is implemented
--override riscvOVPsim/cpu/Zcf=T (Boolean) (default=T) (default) Specify that Zcf is implemented
--override riscvOVPsim/cpu/Zcmb=F (Boolean) (default=F) (default) Specify that Zcmb is implemented
--override riscvOVPsim/cpu/Zcmp=F (Boolean) (default=F) (default) Specify that Zcmp is implemented
--override riscvOVPsim/cpu/Zcmpe=F (Boolean) (default=F) (default) Specify that Zcmpe is implemented
--override riscvOVPsim/cpu/Zcmt=F (Boolean) (default=F) (default) Specify that Zcmt is implemented
--override riscvOVPsim/cpu/compress_version=0.70.1 (Enumeration) (default=0.70.1) (default) Specify required Compressed
       Architecture version
```

Debug Extension

```
--override riscvOVPsim/cpu/debug_mode=none (Enumeration) (default=none) (default) Specify how Debug mode is implemented
--override riscvOVPsim/cpu/debug_version=1.0.0-STABLE (Enumeration) (default=1.0.0-STABLE) (default) Specify required
       Debug Architecture version
```

Interrupts Exceptions

```
--override riscvOVPsim/cpu/CLINT_address=0 (Uns64) (default=0) (default) Specify base address of internal CLINT model
       (or 0 for no CLINT)
--override riscvOVPsim/cpu/ecode_mask=0x7fffffffffffffff (Uns64) (default=0x7fffffffffffffff) (default) Specify hardware-enforced
       mask of writable bits in xcause.ExceptionCode
--override riscvOVPsim/cpu/ecode_nmi=0 (Uns64) (default=0) (default) Specify xcause.ExceptionCode for NMI
--override riscvOVPsim/cpu/external_int_id=F (Boolean) (default=F) (default) Whether to add nets allowing External Interrupt
       ID codes to be forced
--override riscvOVPsim/cpu/force_mideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts always delegated
       to lower-priority execution level from Machine execution level
--override riscvOVPsim/cpu/force_sideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts always delegated
       to User execution level from Supervisor execution level
```

```
--override riscvOVPsim/cpu/local_int_num=0 (Uns32) (default=0) (default) Specify number of supplemental local interrupts
--override riscvOVPsim/cpu/mtvec_is_ro=F (Boolean) (default=F) (default) Specify whether mtvec CSR is read-only
--override riscvOVPsim/cpu/nmi_address=0 (Uns64) (default=0) (default) Override NMI vector address
--override riscvOVPsim/cpu/no_edeleg=0 (Uns64) (default=0) (default) Specify mask of exceptions that cannot be delegated
      to lower-priority execution levels
--override riscvOVPsim/cpu/no_ideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts that cannot be delegated
      to lower-priority execution levels
--override riscvOVPsim/cpu/reset_address=0 (Uns64) (default=0) (default) Override reset vector address
--override riscvOVPsim/cpu/rnmi_version=none (Enumeration) (default=none) (default) Specify required RNMI Architecture
      version
--override riscvOVPsim/cpu/trap_preserves_lr=F (Boolean) (default=F) (default) Whether a trap preserves active LR/SC
      state
--override riscvOVPsim/cpu/tval_ii_code=T (Boolean) (default=T) (default) Specify whether mtval/stval contain faulting
      instruction bits on illegal instruction exception
--override riscvOVPsim/cpu/tval_zero=F (Boolean) (default=F) (default) Specify whether mtval/stval/utval are hard wired
      to zero
--override riscvOVPsim/cpu/tval_zero_ebreak=F (Boolean) (default=F) (default) Specify whether mtval/stval/utval are set
      to zero by an ebreak
--override riscvOVPsim/cpu/tvec_align=0 (Uns32) (default=0) (default) Specify hardware-enforced alignment of mtvec/stvec/utvec
      when Vectored interrupt mode enabled
--override riscvOVPsim/cpu/unimp_int_mask=0 (Uns64) (default=0) (default) Specify mask of unimplemented interrupts (e.g.
      1<<9 indicates Supervisor external interrupt unimplemented)
--override riscvOVPsim/cpu/xret_preserves_lr=F (Boolean) (default=F) (default) Whether an xret instruction preserves
      active LR/SC state
```

Floating Point

```
--override riscvOVPsim/cpu/Zfh=F (Boolean) (default=F) (default) Specify that Zfh is implemented (IEEE half-precision
      floating point is supported)
--override riscvOVPsim/cpu/Zfhmin=F (Boolean) (default=F) (default) Specify that Zfhmin is implemented (restricted IEEE
      half-precision floating point is supported)
--override riscvOVPsim/cpu/Zfinx_version=none (Enumeration) (default=none) (default) Specify version of Zfinx implemented
      (use integer register file for floating point instructions)
--override riscvOVPsim/cpu/d_requires_f=F (Boolean) (default=F) (default) If D and F extensions are separately enabled
      in the misa CSR, whether D is enabled only if F is enabled
--override riscvOVPsim/cpu/enable_fflags_i=F (Boolean) (default=F) (default) Whether fflags_i artifact register present
      (shows per-instruction floating point flags)
--override riscvOVPsim/cpu/mstatus_FS=0 (Uns32) (default=0) (default) Override default value of mstatus.FS (initial state
      of floating point unit)
--override riscvOVPsim/cpu/mstatus_fs_mode=write_1 (Enumeration) (default=write_1) (default) Specify conditions causing
      update of mstatus.FS to dirty
```

Simulation Artifact

```
--override riscvOVPsim/cpu/ABI_d=T (Boolean) (default=T) (default) Specify whether D registers are used for parameters
      (ABI SemiHosting)
--override riscvOVPsim/cpu/ASID_cache_size=8 (Uns32) (default=8) (default) Specifies the number of different ASIDs for
      which TLB entries are cached; a value of 0 implies no limit
--override riscvOVPsim/cpu/CSR_remap= (String) (default=) (default) Comma-separated list of CSR number mappings, each
      of the form <csrName>=<number>
--override riscvOVPsim/cpu/enable_CSR_bus=F (Boolean) (default=F) (default) Add artifact CSR bus port, allowing CSR registers
      to be externally implemented
--override riscvOVPsim/cpu/no_pseudo_inst=F (Boolean) (default=F) (default) Specify whether pseudo-instructions should
      not be reported in trace and disassembly
--override riscvOVPsim/cpu/traceVolatile=F (Boolean) (default=F) (default) Specify whether volatile registers (e.g. minstret)
      should be shown in change trace
--override riscvOVPsim/cpu/use_hw_reg_names=F (Boolean) (default=F) (default) Specify whether to use hardware register
      names x0-x31 and f0-f31 instead of ABI register names
--override riscvOVPsim/cpu/verbose=T (Boolean) (default=F) (platform) Specify verbose output messages
```

Memory

```
--override riscvOVPsim/cpu/ASID_bits=16 (Uns32) (default=16) (default) Specify the number of implemented ASID bits
--override riscvOVPsim/cpu/Sv_modes=0x701 (Uns32) (default=0x701) (default) Specify bit mask of implemented address translation
      modes (e.g. (1<<0)+(1<<8) indicates "bare" and "Sv39" modes may be selected in satp.MODE)
--override riscvOVPsim/cpu/amo_aborts_lr_sc=F (Boolean) (default=F) (default) Specify whether AMO operations abort any
      active LR/SC pair
--override riscvOVPsim/cpu/lr_sc_grain=1 (Uns32) (default=1) (default) Specify byte granularity of ll/sc lock region
      (constrained to a power of two)
--override riscvOVPsim/cpu/unaligned=F (Boolean) (default=F) (default) Specify whether the processor supports unaligned
      memory accesses
--override riscvOVPsim/cpu/unalignedAMO=F (Boolean) (default=F) (default) Specify whether the processor supports unaligned
      memory accesses for AMO instructions
--override riscvOVPsim/cpu/unaligned_low_pri=F (Boolean) (default=F) (default) Specify whether address misaligned exceptions
      are lower priority than page or access fault exceptions
--override riscvOVPsim/cpu/updatePTEA=F (Boolean) (default=F) (default) Specify whether hardware update of PTE A bit
      is supported
--override riscvOVPsim/cpu/updatePTED=F (Boolean) (default=F) (default) Specify whether hardware update of PTE D bit
      is supported
```

Instruction CSR Behavior

```
--override riscvOVPsim/cpu/counteren_mask=0xffffffff (Uns32) (default=0xffffffff) (default) Specify hardware-enforced
      mask of writable bits in mcounteren/scounteren registers
--override riscvOVPsim/cpu/cycle_undefined=F (Boolean) (default=F) (default) Specify that the cycle CSR is undefined
--override riscvOVPsim/cpu/hpmcounter_undefined=F (Boolean) (default=F) (default) Specify that the hpmcounter CSRs are
      undefined
--override riscvOVPsim/cpu/instret_undefined=F (Boolean) (default=F) (default) Specify that the instret CSR is undefined
--override riscvOVPsim/cpu/noinhibit_mask=0 (Uns32) (default=0) (default) Specify hardware-enforced mask of always-zero
      bits in mcountinhibit register
--override riscvOVPsim/cpu/time_undefined=F (Boolean) (default=F) (default) Specify that the time CSR is undefined
--override riscvOVPsim/cpu/wfi_is_nop=F (Boolean) (default=F) (default) Specify whether WFI should be treated as a NOP
      (if not, halt while waiting for interrupts)
```

CSR Masks

```
--override riscvOVPsim/cpu/MXL_writable=F (Boolean) (default=F) (default) Specify that misa.MXL is writable (feature
      under development)
--override riscvOVPsim/cpu/SXL_writable=F (Boolean) (default=F) (default) Specify that mstatus.SXL is writable (feature
      under development)
--override riscvOVPsim/cpu/UXL_writable=F (Boolean) (default=F) (default) Specify that mstatus.UXL is writable (feature
      under development)
--override riscvOVPsim/cpu/envcfg_mask=0x8000000000000001 (Uns64) (default=0x8000000000000001) (default) Specify hardware-enforced
      mask of writable bits in envcfg registers
--override riscvOVPsim/cpu/mip_mask=0x337 (Uns64) (default=0x337) (default) Specify hardware-enforced mask of writable
      bits in mip register
--override riscvOVPsim/cpu/mtvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
      in mtvec register
--override riscvOVPsim/cpu/mtvec_sext=F (Boolean) (default=F) (default) Specify whether mtvec is sign-extended from most-significant
      bit
--override riscvOVPsim/cpu/sip_mask=0x103 (Uns64) (default=0x103) (default) Specify hardware-enforced mask of writable
      bits in sip register
--override riscvOVPsim/cpu/stvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
      in stvec register
--override riscvOVPsim/cpu/stvec_sext=F (Boolean) (default=F) (default) Specify whether stvec is sign-extended from most-significant
      bit
--override riscvOVPsim/cpu/tdata1_mask=0xffffffffffffffff (Uns64) (default=0xffffffffffffffff) (default) Specify hardware-enforced
      mask of writable bits in Trigger Module tdata1 register
--override riscvOVPsim/cpu/uip_mask=1 (Uns64) (default=1) (default) Specify hardware-enforced mask of writable bits in
      uip register
--override riscvOVPsim/cpu/utvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
      in utvec register
--override riscvOVPsim/cpu/utvec_sext=F (Boolean) (default=F) (default) Specify whether utvec is sign-extended from most-significant
      bit
```

Trigger

```
--override riscvOVPsim/cpu/amo_trigger=F (Boolean) (default=F) (default) Specify whether AMO load/store operations activate
      triggers
--override riscvOVPsim/cpu/mcontext_bits=13 (Uns32) (default=13) (default) Specify the number of implemented bits in
      mcontext
--override riscvOVPsim/cpu/mcontext_undefined=F (Boolean) (default=F) (default) Specify that the mcontext CSR is undefined
--override riscvOVPsim/cpu/mcontrol_maskmax=63 (Uns32) (default=63) (default) Specify mcontrol.maskmax value
--override riscvOVPsim/cpu/mscontext_undefined=F (Boolean) (default=F) (default) Specify that the mscontext CSR is undefined
      (Debug Version 0.14.0 and later)
--override riscvOVPsim/cpu/mvalue_bits=13 (Uns32) (default=13) (default) Specify the number of implemented bits in textra.mvalue
      (if zero, textra.mselect is tied to zero)
--override riscvOVPsim/cpu/no_hit=F (Boolean) (default=F) (default) Specify that tdata1.hit is unimplemented
--override riscvOVPsim/cpu/no_sselect_2=F (Boolean) (default=F) (default) Specify that textra.sselect=2 is not supported
      (no trigger match by ASID)
--override riscvOVPsim/cpu/scontext_bits=34 (Uns32) (default=34) (default) Specify the number of implemented bits in
      scontext
--override riscvOVPsim/cpu/scontext_undefined=F (Boolean) (default=F) (default) Specify that the scontext CSR is undefined
--override riscvOVPsim/cpu/svalue_bits=34 (Uns32) (default=34) (default) Specify the number of implemented bits in textra.svalue
      (if zero, textra.sselect is tied to zero)
--override riscvOVPsim/cpu/tcontrol_undefined=F (Boolean) (default=F) (default) Specify that the tcontrol CSR is undefined
--override riscvOVPsim/cpu/tinfo=125 (Uns32) (default=125) (default) Override tinfo register (for all triggers)
--override riscvOVPsim/cpu/tinfo_undefined=F (Boolean) (default=F) (default) Specify that the tinfo CSR is undefined
--override riscvOVPsim/cpu/trigger_num=4 (Uns32) (default=4) (default) Specify the number of implemented hardware triggers
```

PMP Configuration

```
--override riscvOVPsim/cpu/PMP_decompose=F (Boolean) (default=F) (default) Whether unaligned PMP accesses are decomposed
      into separate aligned accesses
--override riscvOVPsim/cpu/PMP_grain=0 (Uns32) (default=0) (default) Specify PMP region granularity, G (0 => 4 bytes,
      1 => 8 bytes, etc)
--override riscvOVPsim/cpu/PMP_initialparams=F (Boolean) (default=F) (default) Enable parameters to change the reset
      values for PMP CSRs
```

```
--override riscvOVPsim/cpu/PMP_maskparams=F (Boolean) (default=F) (default) Enable parameters to change the read-only
      masks for PMP CSRs
--override riscvOVPsim/cpu/PMP_max_page=0 (Uns32) (default=0) (default) Specify the maximum size of PMP region to map
      if non-zero (may improve performance; constrained to a power of two)
--override riscvOVPsim/cpu/PMP_registers=16 (Uns32) (default=16) (default) Specify the number of implemented PMP address
      registers
--override riscvOVPsim/cpu/PMP_undefined=F (Boolean) (default=F) (default) Whether accesses to unimplemented PMP registers
      are undefined (if True) or write ignored and zero (if False)
```

Other Extensions

```
--override riscvOVPsim/cpu/Smstateen=F (Boolean) (default=F) (default) Specify that Smstateen is implemented
--override riscvOVPsim/cpu/Svinval=F (Boolean) (default=F) (default) Specify that Svinval is implemented
--override riscvOVPsim/cpu/Svnapot_page_mask=0 (Uns64) (default=0) (default) Specify mask of implemented Svnapot intermediate
      page sizes (e.g. 1<<16 means 64KiB contiguous regions are supported)
--override riscvOVPsim/cpu/Svpbmt=F (Boolean) (default=F) (default) Specify that Svpbmt is implemented
--override riscvOVPsim/cpu/Zicbom=F (Boolean) (default=F) (default) Specify that Zicbom is implemented
--override riscvOVPsim/cpu/Zicbop=F (Boolean) (default=F) (default) Specify that Zicbop is implemented
--override riscvOVPsim/cpu/Zicboz=F (Boolean) (default=F) (default) Specify that Zicboz is implemented
--override riscvOVPsim/cpu/Zicsr=T (Boolean) (default=T) (default) Specify that Zicsr is implemented
--override riscvOVPsim/cpu/Zifencei=T (Boolean) (default=T) (default) Specify that Zifencei is implemented
--override riscvOVPsim/cpu/Zmmul=F (Boolean) (default=F) (default) Specify that Zmmul is implemented
```

CSR Defaults

```
--override riscvOVPsim/cpu/marchid=0 (Uns64) (default=0) (default) Override marchid register
--override riscvOVPsim/cpu/mconfigptr=0 (Uns64) (default=0) (default) Override mconfigptr register
--override riscvOVPsim/cpu/mhartid=0 (Uns64) (default=0) (default) Override mhartid register (or first mhartid of an
      incrementing sequence if this is an SMP variant)
--override riscvOVPsim/cpu/mimpid=0 (Uns64) (default=0) (default) Override mimpid register
--override riscvOVPsim/cpu/mseccfg=0 (Uns64) (default=0) (default) Override mseccfg register
--override riscvOVPsim/cpu/mtvec=0 (Uns64) (default=0) (default) Override mtvec register
--override riscvOVPsim/cpu/mvendorid=0 (Uns64) (default=0) (default) Override mvendorid register
```

Fast Interrupt

```
--override riscvOVPsim/cpu/CLICLEVELS=0 (Uns32) (default=0) (default) Specify number of interrupt levels implemented
      by CLIC, or 0 if CLIC absent
```

pk

```
--override riscvOVPsim/cpu/pk/userargv=0x0 (Pointer) (default=0x0) (default) Pointer to argv structure
--override riscvOVPsim/cpu/pk/userenvp=0x0 (Pointer) (default=0x0) (default) Pointer to envp structure
--override riscvOVPsim/cpu/pk/reportExitErrors=F (Boolean) (default=F) (default) Report non-zero exit() return codes as simulator
      errors
--override riscvOVPsim/cpu/pk/initsp=0 (Uns64) (default=0) (default) Stack Pointer initialization
--override riscvOVPsim/cpu/pk/strace=F (Boolean) (default=F) (default) trace  proxy system calls (default)
```

sigdump

```
--override riscvOVPsim/cpu/sigdump/ResultReg=28 (Uns32) (default=28) (default) Result Register for RISCV.org Conformance
      Test. 3=GP, 10=A0 or 28=T3 (default)
--override riscvOVPsim/cpu/sigdump/SignatureFile=(null) (String) (default=(null)) (default) Name of the signature file
--override riscvOVPsim/cpu/sigdump/SignatureAtEnd=F (Boolean) (default=F) (default) Generate a Signature file at the end
      of simulation (default to generate on detection of call to write_tohost())
--override riscvOVPsim/cpu/sigdump/SignatureGranularity=16 (Uns32) (default=16) (default) Granularity of signature file (supports
      default 16 or 4 bytes)
--override riscvOVPsim/cpu/sigdump/SignatureMinWrites=1 (Uns32) (default=1) (default) Specify the minimum number of writes
      to signature. Error generated it not reached. Set to 0 to disable.
--override riscvOVPsim/cpu/sigdump/StartAddress=0 (Uns32) (default=0) (default) Address of the Start Symbol
--override riscvOVPsim/cpu/sigdump/StartSymbol=begin_signature (String) (default=begin_signature) (default) Name of the Start
      Symbol
--override riscvOVPsim/cpu/sigdump/EndAddress=0 (Uns32) (default=0) (default) Address of the End Symbol
--override riscvOVPsim/cpu/sigdump/EndSymbol=end_signature (String) (default=end_signature) (default) Name of the End Symbol
--override riscvOVPsim/cpu/sigdump/ByteCount=16 (Uns32) (default=16) (default) Size of region in bytes (must be granularity
      sizebyte blocks)
--override riscvOVPsim/cpu/sigdump/SignatureDumpToStdout=T (Boolean) (default=T) (default) Control of dumping Signature values
      to Stdout (default enabled)
```

Fundamental

```
--override riscvOVPsim/cpu/Smepmp_version=none (Enumeration) (default=none) (default) Specify required Smepmp Architecture
      version
--override riscvOVPsim/cpu/add_Extensions=MAFDCK (String) (default=) (override) Add extensions specified by letters to
      misa.Extensions (for example, specify "VD" to add V and D features)
--override riscvOVPsim/cpu/add_Extensions_mask= (String) (default=) (default) Add extensions specified by letters to
      mask of writable bits in misa.Extensions (for example, specify "VD" to add V and D features)
--override riscvOVPsim/cpu/add_implicit_Extensions= (String) (default=) (default) Add extensions specified by letters
      to implicitly-present extensions not visible in misa.Extensions
--override riscvOVPsim/cpu/enable_expanded=F (Boolean) (default=F) (default) Specify that 48-bit and 64-bit expanded
      instructions are supported
--override riscvOVPsim/cpu/endian=none (Endian) (default=none) (default) Model endian
--override riscvOVPsim/cpu/endianFixed=F (Boolean) (default=F) (default) Specify that data endianness is fixed (mstatus.{MBE,SBE,UBE}
      fields are read-only)
--override riscvOVPsim/cpu/misa_Extensions=0x14152d (Uns32) (default=0x14152d) (default) Override default value of misa.Extensions
--override riscvOVPsim/cpu/misa_Extensions_mask=0x152d (Uns32) (default=0x152d) (default) Override mask of writable bits
      in misa.Extensions
--override riscvOVPsim/cpu/misa_MXL=2 (Uns32) (default=2) (default) Override default value of misa.MXL
--override riscvOVPsim/cpu/numHarts=0 (Uns32) (default=0) (default) Specify the number of hart contexts in a multiprocessor
--override riscvOVPsim/cpu/priv_version=1.12 (Enumeration) (default=1.12) (default) Specify required Privileged Architecture
      version
--override riscvOVPsim/cpu/sub_Extensions= (String) (default=) (default) Remove extensions specified by letters from
      misa.Extensions (for example, specify "VD" to remove V and D features)
--override riscvOVPsim/cpu/sub_Extensions_mask= (String) (default=) (default) Remove extensions specified by letters
      from mask of writable bits in misa.Extensions (for example, specify "VD" to remove V and D features)
--override riscvOVPsim/cpu/sub_implicit_Extensions= (String) (default=) (default) Remove extensions specified by letters
      from implicitly-present extensions not visible in misa.Extensions
--override riscvOVPsim/cpu/user_version=20191213 (Enumeration) (default=20191213) (default) Specify required User Architecture
      version
--override riscvOVPsim/cpu/variant=RV64GCK (Enumeration) (default=RV32I) (override) Selects variant (either a generic
      UISA or a specific model)
```

Bit Manipulation Extension

```
--override riscvOVPsim/cpu/Zba=T (Boolean) (default=T) (default) Specify that Zba is implemented
--override riscvOVPsim/cpu/Zbb=T (Boolean) (default=T) (default) Specify that Zbb is implemented
--override riscvOVPsim/cpu/Zbc=T (Boolean) (default=T) (default) Specify that Zbc is implemented
--override riscvOVPsim/cpu/Zbe=T (Boolean) (default=T) (default) Specify that Zbe is implemented (ignored if version
      1.0.0)
--override riscvOVPsim/cpu/Zbf=T (Boolean) (default=T) (default) Specify that Zbf is implemented (ignored if version
      1.0.0)
--override riscvOVPsim/cpu/Zbm=T (Boolean) (default=T) (default) Specify that Zbm is implemented (ignored if version
      1.0.0)
--override riscvOVPsim/cpu/Zbp=T (Boolean) (default=T) (default) Specify that Zbp is implemented (ignored if version
      1.0.0)
--override riscvOVPsim/cpu/Zbr=T (Boolean) (default=T) (default) Specify that Zbr is implemented (ignored if version
      1.0.0)
--override riscvOVPsim/cpu/Zbs=T (Boolean) (default=T) (default) Specify that Zbs is implemented
--override riscvOVPsim/cpu/Zbt=T (Boolean) (default=T) (default) Specify that Zbt is implemented (ignored if version
      1.0.0)
--override riscvOVPsim/cpu/bitmanip_version=1.0.0 (Enumeration) (default=1.0.0) (default) Specify required Bit Manipulation
      Architecture version
```

Compressed Extension

```
--override riscvOVPsim/cpu/Zca=T (Boolean) (default=T) (default) Specify that Zca is implemented
--override riscvOVPsim/cpu/Zcb=F (Boolean) (default=F) (default) Specify that Zcb is implemented
--override riscvOVPsim/cpu/Zcf=T (Boolean) (default=T) (default) Specify that Zcf is implemented
--override riscvOVPsim/cpu/Zcmb=F (Boolean) (default=F) (default) Specify that Zcmb is implemented
--override riscvOVPsim/cpu/Zcmp=F (Boolean) (default=F) (default) Specify that Zcmp is implemented
--override riscvOVPsim/cpu/Zcmpe=F (Boolean) (default=F) (default) Specify that Zcmpe is implemented
--override riscvOVPsim/cpu/Zcmt=F (Boolean) (default=F) (default) Specify that Zcmt is implemented
--override riscvOVPsim/cpu/compress_version=0.70.1 (Enumeration) (default=0.70.1) (default) Specify required Compressed
      Architecture version
```

Cryptographic Extension

```
--override riscvOVPsim/cpu/Zbkb=T (Boolean) (default=T) (default) Specify that Zbkb is implemented
--override riscvOVPsim/cpu/Zbkc=T (Boolean) (default=T) (default) Specify that Zbkc is implemented
--override riscvOVPsim/cpu/Zbkx=T (Boolean) (default=T) (default) Specify that Zbkx is implemented
--override riscvOVPsim/cpu/Zkb=T (Boolean) (default=T) (default) Specify that Zkb is implemented (deprecated alias of
      Zbkb)
--override riscvOVPsim/cpu/Zkg=T (Boolean) (default=T) (default) Specify that Zkg is implemented (deprecated alias of
      Zbkc)
--override riscvOVPsim/cpu/Zknd=T (Boolean) (default=T) (default) Specify that Zknd is implemented
--override riscvOVPsim/cpu/Zkne=T (Boolean) (default=T) (default) Specify that Zkne is implemented
--override riscvOVPsim/cpu/Zknh=T (Boolean) (default=T) (default) Specify that Zknh is implemented
```

```
--override riscvOVPsim/cpu/Zkr=T (Boolean) (default=T) (default) Specify that Zkr is implemented
--override riscvOVPsim/cpu/Zksed=T (Boolean) (default=T) (default) Specify that Zksed is implemented
--override riscvOVPsim/cpu/Zksh=T (Boolean) (default=T) (default) Specify that Zksh is implemented
--override riscvOVPsim/cpu/crypto_version=1.0.0-rc5 (Enumeration) (default=1.0.0-rc5) (default) Specify required Cryptographic
      Architecture version
--override riscvOVPsim/cpu/mnoise_undefined=F (Boolean) (default=F) (default) Specify that the mnoise CSR is undefined
```

Debug Extension

```
--override riscvOVPsim/cpu/debug_mode=none (Enumeration) (default=none) (default) Specify how Debug mode is implemented
--override riscvOVPsim/cpu/debug_version=1.0.0-STABLE (Enumeration) (default=1.0.0-STABLE) (default) Specify required
      Debug Architecture version
```

Interrupts Exceptions

```
--override riscvOVPsim/cpu/CLINT_address=0 (Uns64) (default=0) (default) Specify base address of internal CLINT model
      (or 0 for no CLINT)
--override riscvOVPsim/cpu/ecode_mask=0x7fffffffffffffff (Uns64) (default=0x7fffffffffffffff) (default) Specify hardware-enforced
      mask of writable bits in xcause.ExceptionCode
--override riscvOVPsim/cpu/ecode_nmi=0 (Uns64) (default=0) (default) Specify xcause.ExceptionCode for NMI
--override riscvOVPsim/cpu/external_int_id=F (Boolean) (default=F) (default) Whether to add nets allowing External Interrupt
      ID codes to be forced
--override riscvOVPsim/cpu/force_mideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts always delegated
      to lower-priority execution level from Machine execution level
--override riscvOVPsim/cpu/force_sideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts always delegated
      to User execution level from Supervisor execution level
--override riscvOVPsim/cpu/local_int_num=0 (Uns32) (default=0) (default) Specify number of supplemental local interrupts
--override riscvOVPsim/cpu/mtvec_is_ro=F (Boolean) (default=F) (default) Specify whether mtvec CSR is read-only
--override riscvOVPsim/cpu/nmi_address=0 (Uns64) (default=0) (default) Override NMI vector address
--override riscvOVPsim/cpu/no_edeleg=0 (Uns64) (default=0) (default) Specify mask of exceptions that cannot be delegated
      to lower-priority execution levels
--override riscvOVPsim/cpu/no_ideleg=0 (Uns64) (default=0) (default) Specify mask of interrupts that cannot be delegated
      to lower-priority execution levels
--override riscvOVPsim/cpu/reset_address=0 (Uns64) (default=0) (default) Override reset vector address
--override riscvOVPsim/cpu/rnmi_version=none (Enumeration) (default=none) (default) Specify required RNMI Architecture
      version
--override riscvOVPsim/cpu/trap_preserves_lr=F (Boolean) (default=F) (default) Whether a trap preserves active LR/SC
      state
--override riscvOVPsim/cpu/tval_ii_code=T (Boolean) (default=T) (default) Specify whether mtval/stval contain faulting
      instruction bits on illegal instruction exception
--override riscvOVPsim/cpu/tval_zero=F (Boolean) (default=F) (default) Specify whether mtval/stval/utval are hard wired
      to zero
--override riscvOVPsim/cpu/tval_zero_ebreak=F (Boolean) (default=F) (default) Specify whether mtval/stval/utval are set
      to zero by an ebreak
--override riscvOVPsim/cpu/tvec_align=0 (Uns32) (default=0) (default) Specify hardware-enforced alignment of mtvec/stvec/utvec
      when Vectored interrupt mode enabled
--override riscvOVPsim/cpu/unimp_int_mask=0 (Uns64) (default=0) (default) Specify mask of unimplemented interrupts (e.g.
      1<<9 indicates Supervisor external interrupt unimplemented)
--override riscvOVPsim/cpu/xret_preserves_lr=F (Boolean) (default=F) (default) Whether an xret instruction preserves
      active LR/SC state
```

Floating Point

```
--override riscvOVPsim/cpu/Zfh=F (Boolean) (default=F) (default) Specify that Zfh is implemented (IEEE half-precision
      floating point is supported)
--override riscvOVPsim/cpu/Zfhmin=F (Boolean) (default=F) (default) Specify that Zfhmin is implemented (restricted IEEE
      half-precision floating point is supported)
--override riscvOVPsim/cpu/Zfinx_version=none (Enumeration) (default=none) (default) Specify version of Zfinx implemented
      (use integer register file for floating point instructions)
--override riscvOVPsim/cpu/d_requires_f=F (Boolean) (default=F) (default) If D and F extensions are separately enabled
      in the misa CSR, whether D is enabled only if F is enabled
--override riscvOVPsim/cpu/enable_fflags_i=F (Boolean) (default=F) (default) Whether fflags_i artifact register present
      (shows per-instruction floating point flags)
--override riscvOVPsim/cpu/mstatus_FS=0 (Uns32) (default=0) (default) Override default value of mstatus.FS (initial state
      of floating point unit)
--override riscvOVPsim/cpu/mstatus_fs_mode=write_1 (Enumeration) (default=write_1) (default) Specify conditions causing
      update of mstatus.FS to dirty
```

Simulation Artifact

```
--override riscvOVPsim/cpu/ABI_d=T (Boolean) (default=T) (default) Specify whether D registers are used for parameters
      (ABI SemiHosting)
--override riscvOVPsim/cpu/ASID_cache_size=8 (Uns32) (default=8) (default) Specifies the number of different ASIDs for
      which TLB entries are cached; a value of 0 implies no limit
--override riscvOVPsim/cpu/CSR_remap= (String) (default=) (default) Comma-separated list of CSR number mappings, each
```

```
      of the form <csrName>=<number>
--override riscvOVPsim/cpu/enable_CSR_bus=F (Boolean) (default=F) (default) Add artifact CSR bus port, allowing CSR registers
      to be externally implemented
--override riscvOVPsim/cpu/no_pseudo_inst=F (Boolean) (default=F) (default) Specify whether pseudo-instructions should
      not be reported in trace and disassembly
--override riscvOVPsim/cpu/traceVolatile=F (Boolean) (default=F) (default) Specify whether volatile registers (e.g. minstret)
      should be shown in change trace
--override riscvOVPsim/cpu/use_hw_reg_names=F (Boolean) (default=F) (default) Specify whether to use hardware register
      names x0-x31 and f0-f31 instead of ABI register names
--override riscvOVPsim/cpu/verbose=T (Boolean) (default=F) (platform) Specify verbose output messages
```

Memory

```
--override riscvOVPsim/cpu/ASID_bits=16 (Uns32) (default=16) (default) Specify the number of implemented ASID bits
--override riscvOVPsim/cpu/Sv_modes=0x701 (Uns32) (default=0x701) (default) Specify bit mask of implemented address translation
      modes (e.g. (1<<0)+(1<<8) indicates "bare" and "Sv39" modes may be selected in satp.MODE)
--override riscvOVPsim/cpu/amo_aborts_lr_sc=F (Boolean) (default=F) (default) Specify whether AMO operations abort any
      active LR/SC pair
--override riscvOVPsim/cpu/lr_sc_grain=1 (Uns32) (default=1) (default) Specify byte granularity of ll/sc lock region
      (constrained to a power of two)
--override riscvOVPsim/cpu/unaligned=F (Boolean) (default=F) (default) Specify whether the processor supports unaligned
      memory accesses
--override riscvOVPsim/cpu/unalignedAMO=F (Boolean) (default=F) (default) Specify whether the processor supports unaligned
      memory accesses for AMO instructions
--override riscvOVPsim/cpu/unaligned_low_pri=F (Boolean) (default=F) (default) Specify whether address misaligned exceptions
      are lower priority than page or access fault exceptions
--override riscvOVPsim/cpu/updatePTEA=F (Boolean) (default=F) (default) Specify whether hardware update of PTE A bit
      is supported
--override riscvOVPsim/cpu/updatePTED=F (Boolean) (default=F) (default) Specify whether hardware update of PTE D bit
      is supported
```

Instruction CSR Behavior

```
--override riscvOVPsim/cpu/counteren_mask=0xffffffff (Uns32) (default=0xffffffff) (default) Specify hardware-enforced
      mask of writable bits in mcounteren/scounteren registers
--override riscvOVPsim/cpu/cycle_undefined=F (Boolean) (default=F) (default) Specify that the cycle CSR is undefined
--override riscvOVPsim/cpu/hpmcounter_undefined=F (Boolean) (default=F) (default) Specify that the hpmcounter CSRs are
      undefined
--override riscvOVPsim/cpu/instret_undefined=F (Boolean) (default=F) (default) Specify that the instret CSR is undefined
--override riscvOVPsim/cpu/noinhibit_mask=0 (Uns32) (default=0) (default) Specify hardware-enforced mask of always-zero
      bits in mcountinhibit register
--override riscvOVPsim/cpu/time_undefined=F (Boolean) (default=F) (default) Specify that the time CSR is undefined
--override riscvOVPsim/cpu/wfi_is_nop=F (Boolean) (default=F) (default) Specify whether WFI should be treated as a NOP
      (if not, halt while waiting for interrupts)
```

CSR Masks

```
--override riscvOVPsim/cpu/MXL_writable=F (Boolean) (default=F) (default) Specify that misa.MXL is writable (feature
      under development)
--override riscvOVPsim/cpu/SXL_writable=F (Boolean) (default=F) (default) Specify that mstatus.SXL is writable (feature
      under development)
--override riscvOVPsim/cpu/UXL_writable=F (Boolean) (default=F) (default) Specify that mstatus.UXL is writable (feature
      under development)
--override riscvOVPsim/cpu/envcfg_mask=0x8000000000000001 (Uns64) (default=0x8000000000000001) (default) Specify hardware-enforced
      mask of writable bits in envcfg registers
--override riscvOVPsim/cpu/mip_mask=0x337 (Uns64) (default=0x337) (default) Specify hardware-enforced mask of writable
      bits in mip register
--override riscvOVPsim/cpu/mtvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
      in mtvec register
--override riscvOVPsim/cpu/mtvec_sext=F (Boolean) (default=F) (default) Specify whether mtvec is sign-extended from most-significant
      bit
--override riscvOVPsim/cpu/sip_mask=0x103 (Uns64) (default=0x103) (default) Specify hardware-enforced mask of writable
      bits in sip register
--override riscvOVPsim/cpu/stvec_mask=0 (Uns64) (default=0) (default) Specify hardware-enforced mask of writable bits
      in stvec register
--override riscvOVPsim/cpu/stvec_sext=F (Boolean) (default=F) (default) Specify whether stvec is sign-extended from most-significant
      bit
--override riscvOVPsim/cpu/tdata1_mask=0xffffffffffffffff (Uns64) (default=0xffffffffffffffff) (default) Specify hardware-enforced
      mask of writable bits in Trigger Module tdata1 register
```

Trigger

```
--override riscvOVPsim/cpu/amo_trigger=F (Boolean) (default=F) (default) Specify whether AMO load/store operations activate
      triggers
--override riscvOVPsim/cpu/mcontext_bits=13 (Uns32) (default=13) (default) Specify the number of implemented bits in
```

```
      mcontext
--override riscvOVPsim/cpu/mcontext_undefined=F (Boolean) (default=F) (default) Specify that the mcontext CSR is undefined
--override riscvOVPsim/cpu/mcontrol_maskmax=63 (Uns32) (default=63) (default) Specify mcontrol.maskmax value
--override riscvOVPsim/cpu/mscontext_undefined=F (Boolean) (default=F) (default) Specify that the mscontext CSR is undefined
      (Debug Version 0.14.0 and later)
--override riscvOVPsim/cpu/mvalue_bits=13 (Uns32) (default=13) (default) Specify the number of implemented bits in textra.mvalue
      (if zero, textra.mselect is tied to zero)
--override riscvOVPsim/cpu/no_hit=F (Boolean) (default=F) (default) Specify that tdata1.hit is unimplemented
--override riscvOVPsim/cpu/no_sselect_2=F (Boolean) (default=F) (default) Specify that textra.sselect=2 is not supported
      (no trigger match by ASID)
--override riscvOVPsim/cpu/scontext_bits=34 (Uns32) (default=34) (default) Specify the number of implemented bits in
      scontext
--override riscvOVPsim/cpu/scontext_undefined=F (Boolean) (default=F) (default) Specify that the scontext CSR is undefined
--override riscvOVPsim/cpu/svalue_bits=34 (Uns32) (default=34) (default) Specify the number of implemented bits in textra.svalue
      (if zero, textra.sselect is tied to zero)
--override riscvOVPsim/cpu/tcontrol_undefined=F (Boolean) (default=F) (default) Specify that the tcontrol CSR is undefined
--override riscvOVPsim/cpu/tinfo=125 (Uns32) (default=125) (default) Override tinfo register (for all triggers)
--override riscvOVPsim/cpu/tinfo_undefined=F (Boolean) (default=F) (default) Specify that the tinfo CSR is undefined
--override riscvOVPsim/cpu/trigger_num=4 (Uns32) (default=4) (default) Specify the number of implemented hardware triggers
```

PMP Configuration

```
--override riscvOVPsim/cpu/PMP_decompose=F (Boolean) (default=F) (default) Whether unaligned PMP accesses are decomposed
      into separate aligned accesses
--override riscvOVPsim/cpu/PMP_grain=0 (Uns32) (default=0) (default) Specify PMP region granularity, G (0 => 4 bytes,
      1 => 8 bytes, etc)
--override riscvOVPsim/cpu/PMP_initialparams=F (Boolean) (default=F) (default) Enable parameters to change the reset
      values for PMP CSRs
--override riscvOVPsim/cpu/PMP_maskparams=F (Boolean) (default=F) (default) Enable parameters to change the read-only
      masks for PMP CSRs
--override riscvOVPsim/cpu/PMP_max_page=0 (Uns32) (default=0) (default) Specify the maximum size of PMP region to map
      if non-zero (may improve performance; constrained to a power of two)
--override riscvOVPsim/cpu/PMP_registers=16 (Uns32) (default=16) (default) Specify the number of implemented PMP address
      registers
--override riscvOVPsim/cpu/PMP_undefined=F (Boolean) (default=F) (default) Whether accesses to unimplemented PMP registers
      are undefined (if True) or write ignored and zero (if False)
```

Other Extensions

```
--override riscvOVPsim/cpu/Smstateen=F (Boolean) (default=F) (default) Specify that Smstateen is implemented
--override riscvOVPsim/cpu/Svinval=F (Boolean) (default=F) (default) Specify that Svinval is implemented
--override riscvOVPsim/cpu/Svnapot_page_mask=0 (Uns64) (default=0) (default) Specify mask of implemented Svnapot intermediate
      page sizes (e.g. 1<<16 means 64KiB contiguous regions are supported)
--override riscvOVPsim/cpu/Svpbmt=F (Boolean) (default=F) (default) Specify that Svpbmt is implemented
--override riscvOVPsim/cpu/Zicbom=F (Boolean) (default=F) (default) Specify that Zicbom is implemented
--override riscvOVPsim/cpu/Zicbop=F (Boolean) (default=F) (default) Specify that Zicbop is implemented
--override riscvOVPsim/cpu/Zicboz=F (Boolean) (default=F) (default) Specify that Zicboz is implemented
--override riscvOVPsim/cpu/Zicsr=T (Boolean) (default=T) (default) Specify that Zicsr is implemented
--override riscvOVPsim/cpu/Zifencei=T (Boolean) (default=T) (default) Specify that Zifencei is implemented
--override riscvOVPsim/cpu/Zmmul=F (Boolean) (default=F) (default) Specify that Zmmul is implemented
```

CSR Defaults

```
--override riscvOVPsim/cpu/marchid=0 (Uns64) (default=0) (default) Override marchid register
--override riscvOVPsim/cpu/mconfigptr=0 (Uns64) (default=0) (default) Override mconfigptr register
--override riscvOVPsim/cpu/mhartid=0 (Uns64) (default=0) (default) Override mhartid register (or first mhartid of an
      incrementing sequence if this is an SMP variant)
--override riscvOVPsim/cpu/mimpid=0 (Uns64) (default=0) (default) Override mimpid register
--override riscvOVPsim/cpu/mseccfg=0 (Uns64) (default=0) (default) Override mseccfg register
--override riscvOVPsim/cpu/mtvec=0 (Uns64) (default=0) (default) Override mtvec register
--override riscvOVPsim/cpu/mvendorid=0 (Uns64) (default=0) (default) Override mvendorid register
```

Fast Interrupt

```
--override riscvOVPsim/cpu/CLICLEVELS=0 (Uns32) (default=0) (default) Specify number of interrupt levels implemented
      by CLIC, or 0 if CLIC absent
```

pk

```
--override riscvOVPsim/cpu/pk/userargv=0x0 (Pointer) (default=0x0) (default) Pointer to argv structure
--override riscvOVPsim/cpu/pk/userenvp=0x0 (Pointer) (default=0x0) (default) Pointer to envp structure
```

```
--override riscvOVPsim/cpu/pk/reportExitErrors=F (Boolean) (default=F) (default) Report non-zero exit() return codes as simulator
          errors
--override riscvOVPsim/cpu/pk/initsp=0 (Uns64) (default=0) (default) Stack Pointer initialization
--override riscvOVPsim/cpu/pk/strace=F (Boolean) (default=F) (default) trace  proxy system calls (default)
```

sigdump

```
--override riscvOVPsim/cpu/sigdump/ResultReg=28 (Uns32) (default=28) (default) Result Register for RISCV.org Conformance
          Test. 3=GP, 10=A0 or 28=T3 (default)
--override riscvOVPsim/cpu/sigdump/SignatureFile=(null) (String) (default=(null)) (default) Name of the signature file
--override riscvOVPsim/cpu/sigdump/SignatureAtEnd=F (Boolean) (default=F) (default) Generate a Signature file at the end
          of simulation (default to generate on detection of call to write_tohost())
--override riscvOVPsim/cpu/sigdump/SignatureGranularity=16 (Uns32) (default=16) (default) Granularity of signature file (supports
          default 16 or 4 bytes)
--override riscvOVPsim/cpu/sigdump/SignatureMinWrites=1 (Uns32) (default=1) (default) Specify the minimum number of writes
          to signature. Error generated it not reached. Set to 0 to disable.
--override riscvOVPsim/cpu/sigdump/StartAddress=0 (Uns32) (default=0) (default) Address of the Start Symbol
--override riscvOVPsim/cpu/sigdump/StartSymbol=begin_signature (String) (default=begin_signature) (default) Name of the Start
          Symbol
--override riscvOVPsim/cpu/sigdump/EndAddress=0 (Uns32) (default=0) (default) Address of the End Symbol
--override riscvOVPsim/cpu/sigdump/EndSymbol=end_signature (String) (default=end_signature) (default) Name of the End Symbol
--override riscvOVPsim/cpu/sigdump/ByteCount=16 (Uns32) (default=16) (default) Size of region in bytes (must be granularity
          sizebyte blocks)
--override riscvOVPsim/cpu/sigdump/SignatureDumpToStdout=T (Boolean) (default=T) (default) Control of dumping Signature values
          to Stdout (default enabled)
```

Appendix C

Compiling RISC-V programs

The Imperas and OVP simulators load programs compiled into .elf format. So to execute RISC-V programs you need to cross compile the C programs or assemble the asm files into .elf files.

To accomplish this you need to download and install compiler tool chains - either GNU GCC or LLVM.

You can use any tool chain that produces an elf file and load this with one of the built-in loaders.

Note: Although not supported by the fixed platform an Imperas or OVP platform can use the OVP APIs to directly load any binary into memory from which it can be simulated.

Installing GNU GCC tool chains from OVP

As a convenience OVP makes available a pre-built GCC tool chain that is compatible with its simulators and models. This can be obtained here: www.ovpworld.org/riscv.toolchains.

For instructions on using the cross compilers, please consult: www.ovpworld.org/installation chapter 7.

Appendix D

Information on Open Virtual Platforms

Imperas and others announced OVP in March 2008 and have since put the OVPsim simulator, full documentation, and examples / demos and processor models on www.ovpworld.org site. There are many models of processors from many ISA families: - ARM, MIPS, Synopsys ARC, Renesas v850 / RH850 / RL78 / M16C, openCores OR1K, PowerPC, Altera Nios II, Xilinx MicroBlaze, SiFive, Andes, Microsemi, RISC-V, single core, multicore, manycore, C, C++, SystemC, TLM2 etc.

Imperas and others have put many of the processor and peripheral models into open source and made them available on the OVP site on the www.ovpworld.org/downloads and www.ovpworld.org/library pages.

What is OVP?

It is simulation to develop software on: Fast Simulation, Free open source models, Easy to use!

Imperas Software Ltd developed some fantastic virtual platform and modeling technology to enable simulating embedded systems running real application code. These simulations run at speeds of 100s and 100s of MIPS on typical desktop PCs and are completely Instruction Accurate and model the whole system.

	RISC-V RV32G			ARM32			Imagination MIPS32		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	5,942,442,478	3.24s	1834	1,214,194,084	0.81s	1506	1,665,624,452	0.99s	1682
Dhrystone	5,564,075,544	3.75s	1488	4,920,070,302	3.38s	1458	1,560,089,486	0.84s	1857
Whetstone	12,726,977,092	8.46s	1504	1,269,185,283	1.09s	1164	1,894,381,527	0.76s	2493
peakSpeed2	27,000,012,085	3.61s	7500	27,500,007,040	3.95s	6962	5,600,004,984	0.79s	7124
	RISC-V RV64GC			ARM AARCH64			Imagination MIPS64		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	2,423,371,379	1.1s	2203	4,999,878,343	2.76s	1812	1,843,945,304	0.95s	1962
Dhrystone	5,600,060,511	3.43s	1637	2,390,060,024	1.67s	1431	1,794,088,951	1.59s	1130
Whetstone	1,782,196,148	1.11s	1606	1,576,656,496	1.68s	939	1,453,142,044	0.64s	2274
peakSpeed2	28,000,002,559	4.98s	5623	27,500,004,076	4s	6875	28,000,004,416	5.34s	5243
	PowerPC			Renesas v850			Synopsys ARC		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	3,143,920,699	2.02s	1557	5,372,682,210	3.62s	1488	996,212,491	0.86s	1159
Dhrystone	802,066,836	0.55s	1458	12,790,132,941	8.01s	1597	2,470,110,910	2.11s	1171
Whetstone	6,424,865,755	3.94s	1631	10,296,940,591	6.04s	1708	1,214,268,961	0.68s	1774
peakSpeed2	27,500,003,291	6.48s	4246	27,500,009,239	3.89s	7069	28,500,007,430	3.97s	7179
	Altera Nios II			Xilinx MicroBlaze			OpenCores OR1K		
Benchmark	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS	Simulated Instructions	Run time	Simulated MIPS
linpack	3,494,897,435	1.93s	1811	10,871,290,698	4.39s	2477	5,027,664,578	3.53s	1426
Dhrystone	3,610,082,777	3.08s	1176	7,620,119,106	4.98s	1530	2,062,114,425	1.02s	2042
Whetstone	5,850,887,389	2.67s	2193	27,108,532,655	10.39s	2609	11,151,873,005	5.2s	2145
peakSpeed2	27,000,014,679	3.71s	7278	16,500,024,223	3.33s	4955	39,000,012,784	7.35s	5308

All measurements on 3.50GHz Intel i7-4770K, Linux FC20, OVPsim 20180221.0

Imperas decided to open up this technology and OVP is the vehicle to make it public.

OVP has three main components - the OVP APIs that enable a C model to be written, a library of free open source processor and peripheral models, and OVPsim a fast, easy to download and use reference simulator that executes these models.

There is also the iGen Model Building Wizard that is part of the OVP download and makes it easy to create platforms and models.

With OVP you can put together a simulation model of a platform, compile it to an executable, and connect it to your debugger to provide a very efficient fast embedded software development environment.

To read more about OVP visit: Why?, Virtual Platforms?, Rationale?, Continuous Integration, Partners, Licensing, Downloading.

Appendix E

Information on Imperas Software tools

For the last 10 years Imperas Software Limited has been developing simulation technology, models, and tools to assist embedded software developers getting their software written, tested, and debugged.

For information on the Imperas Advanced Multicore Software Development Kit (M*SDK), the CPU Model Generator (cpuGen), Virtual Platform Simulation Acceleration (QuantumLeap), the Instruction Set Simulator (ISS), Virtual Platform Development and Simulation (C*DEV, S*DEV, M*DEV), or RISC-V solutions (RISC-V) - please visit: www.imperas.com/products.

To read about how Imperas solutions accelerate Embedded Software Development, how developers use simulation of virtual platforms in their continuous integration environments, and how automotive users adopt simulation for failsafe reliability verification - please visit: www.imperas.com/solutions. There are several case studies: www.imperas.com/imperas-case-studies.

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Appendix F

Imperas License governing use of riscvOVPsim

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