Documentation

Version 1.0

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1 Overview

1.1 About Steel Core

Steel is a 3-stage single-issue in-order RISC-V microprocessor core designed to be simple and easy to use. It can be used as processing unit in microcontrollers and embedded systems.

1.2 Licensing

Steel is distributed under the MIT License. The license text is reproduced below. Read it carefully and make sure you understand its terms before using Steel in your own projects.

1.3 Specifications version

Steel aims to be compliant with the following RISC-V specifications:

- Version 20191213 of RISC-V Unprivileged ISA
- Version 20190608-Priv-MSU-Ratified of RISC-V Privileged Architecture

1.4 Online repository

Steel files and documentation are available at GitHub (`github.com/rafaelcalcada/steel-core`).

1.5 Hardware description language

The hardware of Steel is described in Verilog (IEEE Std. 1364-2005).

1.6 Supported privilege levels

Steel supports only M-mode.

1.7 Implemented extensions

Steel implements the base instruction set RV32I and the Zicsr extension.

1.8 Implemented control and status registers

The control and status registers implemented in Steel are shown in table 1 (below). The required M-mode registers not shown in the table return the hardwired value predicted by the specifications when read.

Table 1 – Steel Core implemented CSRs

CSR	Name	Address
cycle	*Cycle Counter*	`0xC00`
time	*System Timer*	`0xC01`
instret	*Instructions Retired*	`0xC02`
mstatus	*Machine Status*	`0x300`
misa	*Machine ISA*	`0x301`
mie	*Machine Interrupt Enable*	`0x304`
mtvec	*Machine Trap Vector*	`0x305`
mscratch	*Machine Scratch*	`0x340`
mepc	*Machine Exception Program Counter*	`0x341`
mcause	*Machine Cause*	`0x342`
mtval	*Machine Trap Value*	`0x343`
mip	*Machine Interrupt Pending*	`0x344`
mcycle	*Machine Cycle Counter*	`0xB00`
minstret	*Machine Instructions Retired*	`0xB01`
mcountinhibit	*Machine Counter Inhibit*	`0x320`

1.9 Integration with other devices

Steel must be connected to a word addressed memory with read/write latency of 1 clock cycle. These characteristics facilitate integration with Block RAMs in FPGAs.

Steel can optionally be connected to an interrupt controller and a real-time counter.

1.10 Memory alignment rules

An address-misaligned exception occurs when the running software attempts to access an address in disagreement with the following alignment rules:

- the address in jump, branch and load/store word instructions must be aligned on a 4-byte boundary (the last two bits of the address must be zero);
- the address in load/store halfword instructions (`lh`, `lhu` and `sh`) must be aligned on a 2-byte boundary (the last bit of the address must be zero);
- the address in load/store byte instructions (`lb`, `lbu` and `sb`) does not need to be aligned.

Address-misaligned exceptions must be resolved by the trap handler.

1.11 Microarchitecture

Steel has 3 pipeline stages, a single execution thread and issues only one instruction per clock cycle. Therefore, all instructions are executed in program order.

Fig. 1 (below) shows Steel microarchitecture in register-transfer level (RTL). Circles and trapezoids represent combinational logic units. Rectangles represent sequential logic units. Implementation details can be found in section 7.

Fig. 2 (next page) shows the tasks performed by each pipeline stage. In the first stage, the core generates the program counter and fetches the instruction from memory. In the second, the instruction is decoded and the control signals for all units are generated. Branches, jumps and stores are executed in advance in this stage, which also generates the immediates and fetches the data from memory for load instructions. The last stage executes all other instructions and writes back the results in the register file.

Figure 1 – Steel Core microarchitecture in detail

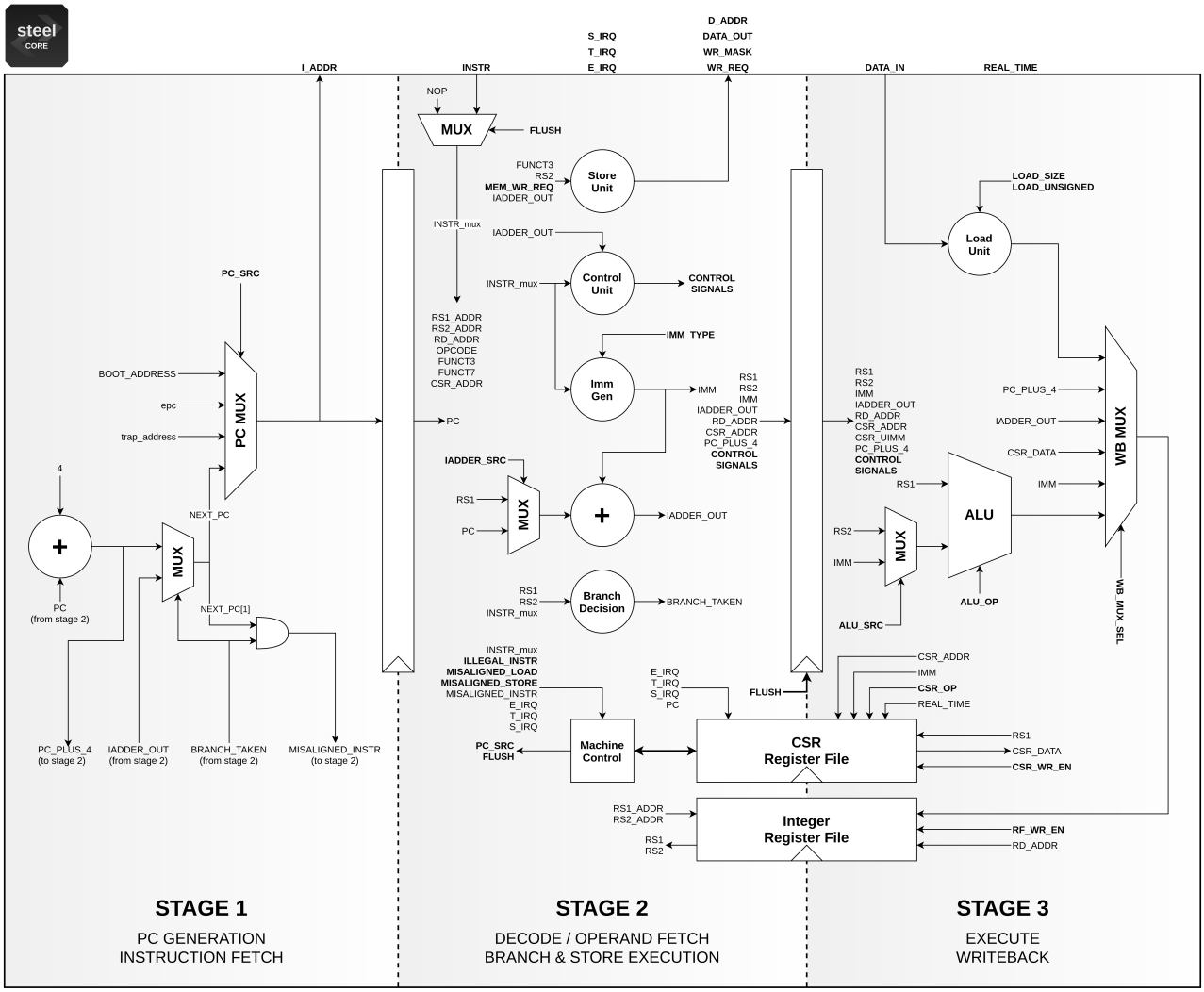
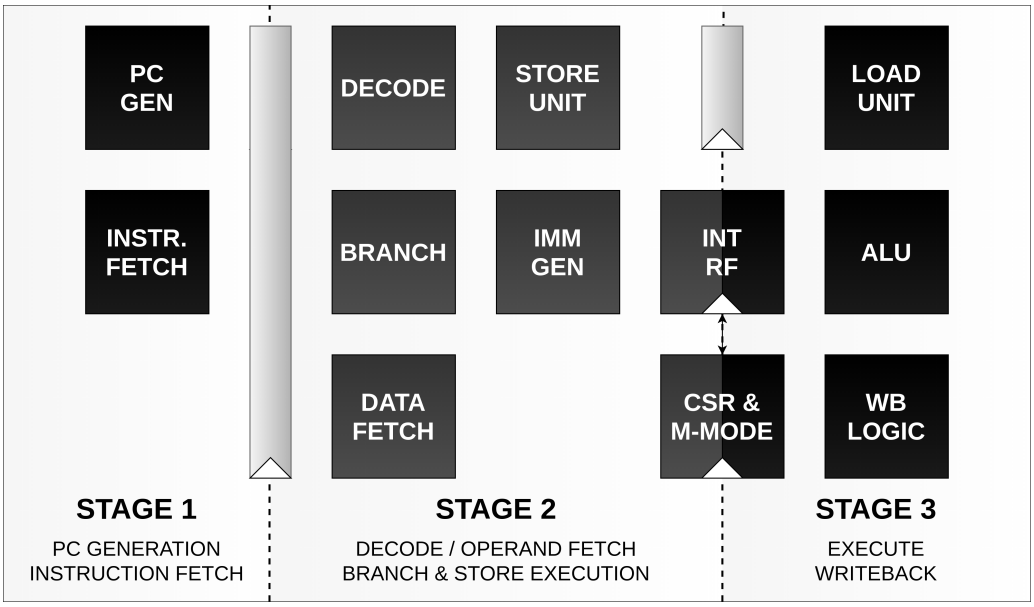


Figure 2 – Steel Core pipeline overview



2 Configuration

Steel configuration parameters can be modified by editing the `globals.vh` file (located inside the `rtl` directory). The following sections describe the parameters that can be changed.

2.1 Boot address

The BOOT_ADDRESS parameter sets the memory position of the first instruction the core will fetch after reset. It can be changed to any 32-bit value.

2.2 CSRs reset values

The reset values of several control and status registers (CSRs) can be modified. Table 2 shows these CSRs and the accepted values.

Table 2 – Steel Core configuration parameters

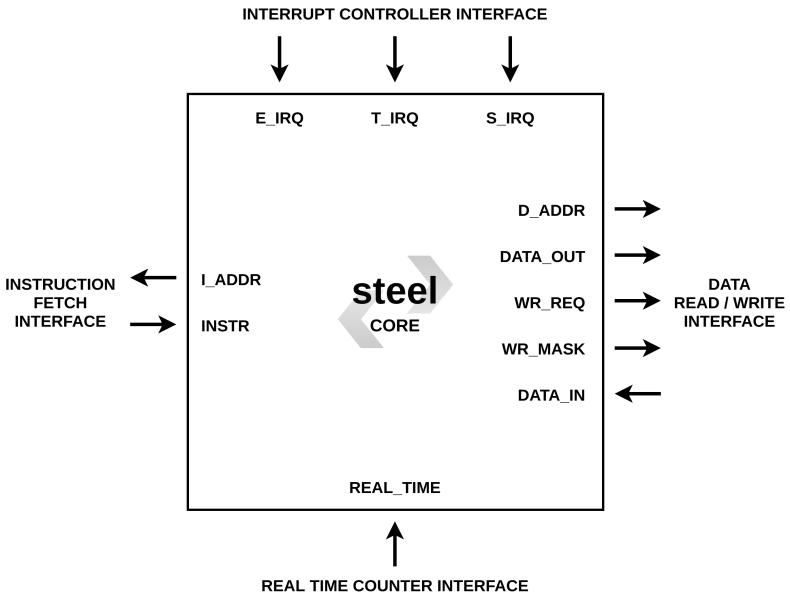
Parameter	Description
MCYCLE_RESET	Value of register `mcycle` after reset. It can be changed to any 32-bit value.
MCYCLEH_RESET	Value of register `mcycleh` after reset. It can be changed to any 32-bit value.
TIME_RESET	Value of register `time` after reset. It can be changed to any 32-bit value.
TIMEH_RESET	Value of register `timeh` after reset. It can be changed to any 32-bit value.
MINSTRET_RESET	Value of register `minstret` after reset. It can be changed to any 32-bit value.
MINSTRETH_RESET	Value of register `minstreth` after reset. It can be changed to any 32-bit value.
MTVEC_BASE_RESET	Value of `base` field of `mtvec` register after reset. The value is used in the trap handler address calculation (see section 5). It can be changed to any 30-bit value.
MTVEC_MODE_RESET	Value of `mode` field of `mtvec` register after reset. It defines the interrupt mode (see section 5) and can be changed to the value 00 (direct mode) or 01 (vectored mode).
MSCRATCH_RESET	Value of register `mscratch` after reset. It can be changed to any 32-bit value.
MEPC_RESET	Value of register `mepc` after reset. It can be changed to any 32-bit address aligned on a four byte boundary (the last two bits must be set to zero).
MCOUNTINHIBIT_CY_RESET	Enables or inhibits cycle counting (1 inhibits, 0 enables).
MCOUNTINHIBIT_IR_RESET	Enables or inhibits instructions retired counting (1 inhibits, 0 enables).

3 Input and output signals

Fig. 3 (below) shows Steel input and output signals (except CLK and RESET). The following sections explain their functions in detail.

The interfaces to fetch instructions and to read/write data can be connected to any type of memory, but were designed to facilitate integration with Block RAMs in FPGAs.

Figure 3 – Steel Core input and output signals



3.1 Interrupt controller interface

The interrupt controller interface has three signals used to request external, timer and software interrupts, shown in table 3. The interrupt request process is explained in sections 4.4 and 5.

Table 3 – Interrupt controller interface signals

Signal	Width	Direction	Description
E_IRQ	1 bit	Input	When high indicates an external interrupt request.
T_IRQ	1 bit	Input	When high indicates a timer interrupt request.
S_IRQ	1 bit	Input	When high indicates a software interrupt request.

3.2 Instruction fetch interface

The instruction fetch interface has two signals used in the instruction fetch process, shown in table 4 (below). The process of fetching instructions is explained in section 4.1.

Table 4 – Instruction fetch interface signals

Signal	Width	Direction	Description
INSTR	32 bits	Input	Contains the instruction fetched from memory.
I_ADDR	32 bits	Output	Contains the address of the instruction the core wants to fetch from memory.

3.3 Data read/write interface

The data read/write interface has five signals used in the process of reading/writing data from/to memory. The signals are shown in table 5 (below). The process of fetching data from memory is explained in section 4.2. The process of writing data is explained in section 4.3.

Table 5 – Data read/write interface signals

Signal	Width	Direction	Description
DATA_IN	32 bits	Input	Contains the data fetched from memory.
D_ADDR	32 bits	Output	In a write operation, contains the address of the memory position where the data will be stored. In a read operation, contains the address of the memory position where the data to be fetched is. The address is always aligned on a four byte boundary (the last two bits are always zero).
DATA_OUT	32 bits	Output	Contains the data to be stored in memory. Used only with write operations.
WR_REQ	1 bit	Output	When high, indicates a request to write data. Used only with write operations.
WR_MASK	4 bits	Output	Contains a mask of four *byte-write enable* bits. A bit high indicates that the corresponding byte must be written. See section 4.3 for details. Used only with write operations.

3.4 Real time counter interface

The real time counter interface has just one signal used to update the `time` CSR, shown in table 6. The process of updating the `time` register is explained in section 4.5.

Table 6 – Real time counter interface

Signal	Width	Direction	Description
REAL_TIME	64 bits	Input	Contains the current value read from a real time counter.

3.5 CLK and RESET signals

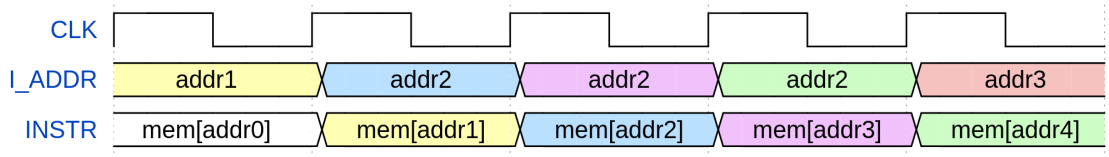
The core also has the CLK and RESET input signals, which are not shown in figure 3 (above). The CLK signal must be connected to a clock source. The RESET signal is active high and resets the core asynchronously.

4 Timing diagrams

4.1 Instruction fetch

To fetch an instruction, the core places the instruction address on the I_ADDR bus. The memory must place the instruction on the INSTR bus at the next clock rising edge. Fig. 4 (below) shows the timing diagram of this process. In the figure, `mem[addrX]` denotes the instruction stored at the memory position `addrX`.

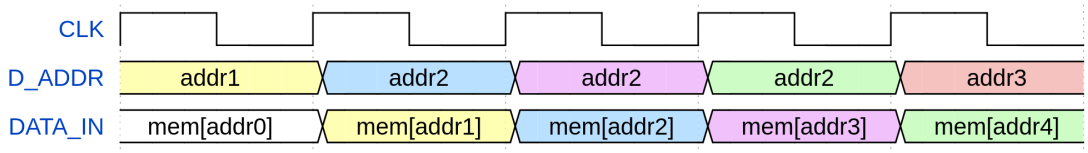
Figure 4 – Instruction fetch timing diagram



4.2 Data fetch

To fetch data from memory, the core puts the data address on the D_ADDR bus. The memory must place the data on the DATA_IN bus at the next clock rising edge. Fig. 5 (below) shows the timing diagram of this process. In the figure, `mem[addrX]` denotes the data stored at the memory position `addrX`.

Figure 5 – Data fetch timing diagram



4.3 Data writing

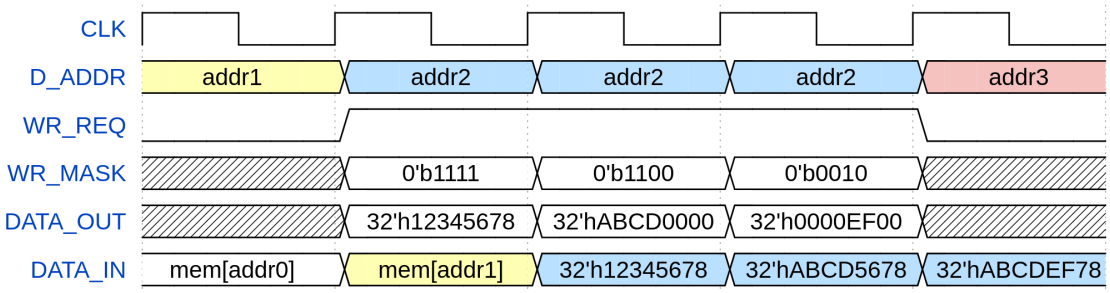
To write data to memory, the core drives D_ADDR, DATA_OUT, WR_REQ and WR_MASK signals as follows:

- D_ADDR receives the address of the memory position where the data must be written;
- DATA_OUT receives the data to be written;
- WR_REQ is set high;
- WR_MASK receives a byte-write enable mask that indicates which bytes of DATA_OUT must be written.

The memory must perform the write operation at the next clock rising edge. The core can request to write bytes, halfwords and words.

Fig. 6 (next page) shows the process of writing data to memory. DATA_IN is not used in the process and appears only to show the memory contents after writing. The figure shows five clock cycles, in which the core requests to write in the second, third and fourth cycles. In the second clock cycle, the core requests to write the word `0x12345678` at the address `addr2`. In the third, requests to write the halfword `0xABCD` at the upper half of `addr2`, and in the fourth requests to write the byte `0xEF` at the second least significant byte of `addr2`. The content of `addr2` after each of these operations appears on the DATA_IN bus and are highlighted in blue.

Figure 6 – Data writing timing diagram

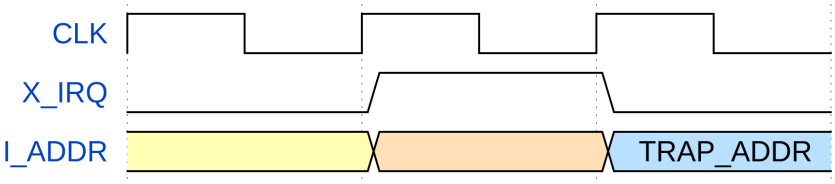


4.4 Interrupt request

An external device (or an interrupt controller managing several devices) can request interrupts by setting high the appropriate IRQ signal, which is E_IRQ for external interrupts, T_IRQ for timer interrupts and S_IRQ for software interrupts. The IRQ signal of the requested interrupt must be set high for one clock cycle and set low for the next.

Fig. 7 (below) shows the timing diagram of the interrupt request process. Since the process is the same for all types of interrupt, X_IRQ is used to denote E_IRQ, T_IRQ or S_IRQ. TRAP_ADDR denotes the address of the trap handler first instruction.

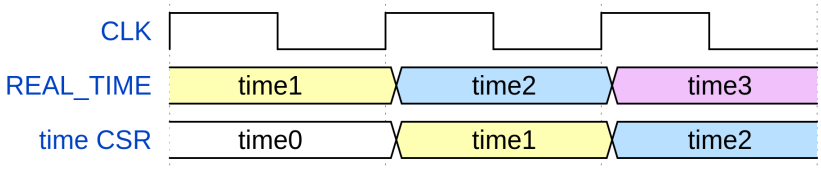
Figure 7 – Interrupt request timing diagram



4.5 `time` CSR update

When connected to a real-time counter, the core updates the `time` CSR with the value placed on REAL_TIME at each clock rising edge, as shown in Fig. 8 (below). In the figure, `timeX` denotes arbitrary time values.

Figure 8 – `time` CSR update timing diagram



5 Exceptions and Interrupts

5.1 Supported exceptions and interrupts

Steel supports the exceptions and interrupts shown in table 7 (below). They are listed in descending priority order (the highest priority is at the top of the table). If two or more exceptions/interrupts occur at the same time, the one with the highest priority is taken.

Exceptions always cause a trap to be taken. An interrupt will cause a trap only if enabled. Each type of interrupt has an interrupt-enable bit in the `mie` register. Interrupts are globally enable/disabled by setting the MIE bit of `mstatus` register.

Table 7 – Steel supported exceptions and interrupts

	`mcause` **value**	
Exception / Interrupt	**Interrupt**	**Exception code**
Machine external interrupt	1	11
Machine software interrupt	1	3
Machine timer interrupt	1	7
Illegal instruction exception	0	2
Instruction address-misaligned exception	0	0
Environment call from M-mode exception	0	11
Environment break exception	0	3
Store address-misaligned exception	0	6
Load address-misaligned exception	0	4

5.2 Trap handling in Steel

Exceptions and interrupts are handled by a trap handler routine stored in memory. The address of the trap handler first instruction is configured using the `mtvec` register. Steel supports both direct and vectorized interrupt modes. More information on interrupt modes and configuration of the `mtvec` register can be found in RISC-V specifications.

When a trap is taken, the core proceeds as follows:

- the address of the interrupted instruction (or the instruction that encountered the exception) is saved in the `mepc` register;
- the value of the `mtval` register is set to zero;
- the value of the `mstatus` MIE bit is saved in the MPIE field and then set to zero;
- the program counter is set to the trap handler first instruction.

The `mret` instruction is used to return from traps. When executed, the core proceeds as follows:

- the value of the `mstatus` MPIE bit is saved in the MIE field and then set to one;
- the program counter is set to the value of `mepc` register.

5.3 Nested interrupts capability

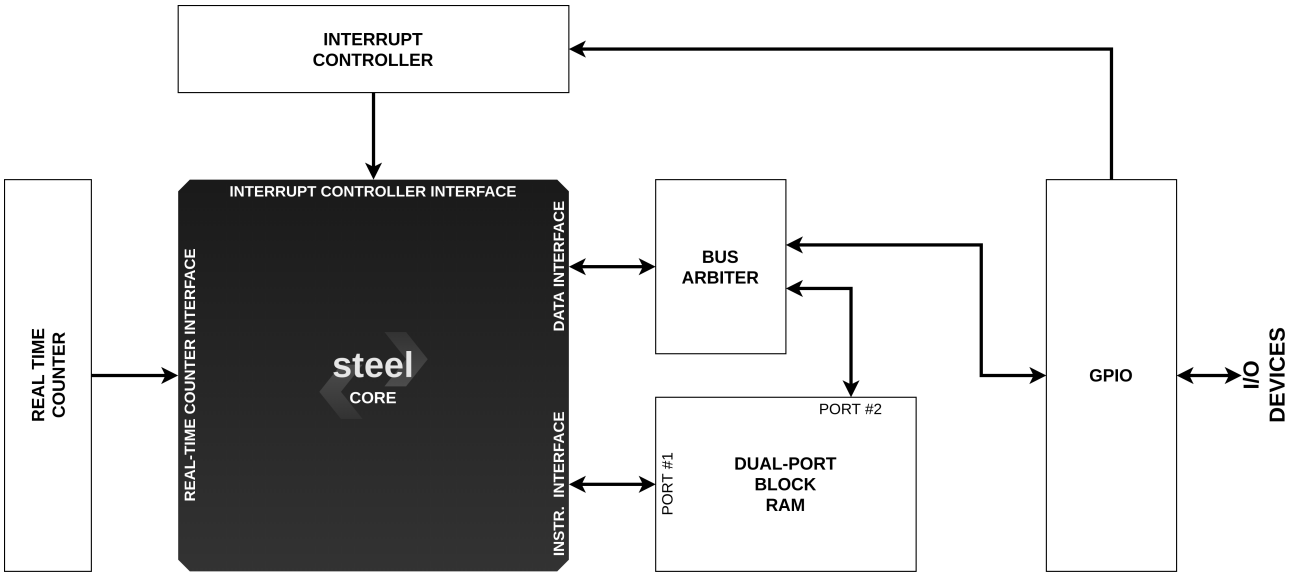
The core globally disables interrupts when takes into a trap. The trap handler can re-enable interrupts by setting the `mstatus` MIE bit to one, enabling nested interrupts. To return from nested traps, the trap handler must stack and manage the values of the `mepc` register in memory.

6 Steel-based system example

Fig. 9 (below) shows an example of how Steel can be used as processing unit in embedded systems projects. The same architecture can be used to build other systems. The example is composed of a dual-port Block RAM, a memory mapped GPIO unit, a bus arbiter, an interrupt controller and a real-time counter. In this system, the address space is divided into two ranges, one assigned to memory and the other to the GPIO unit. The bus arbiter is used to multiplex the data interface signals according to the address the core wants to access.

Software for this system can be compiled and assembled with RISC-V GNU Toolchain. The generated ELF files can be converted to HEX, MIF or COE formats and then used to initialize the Block RAM.

Figure 9 – Steel-based system example



7 Implementation details

This section contains information on implementation details. It is intended for those who want to know more about how Steel works.

7.1 Control Unit

The Control Unit (`control_unit.v`) decodes the instruction and generates the signals that control the memory, the Load Unit, the Store Unit, the ALU, the two register files (Integer and CSR), the Immediate Generator and the Writeback Multiplexer. The description of its input and output signals are shown in table 8 (below).

Table 8 – Control Unit signals

Signal name	Width	Direction	Description
OPCODE_6_TO_2	5 bits	Input	Connected to the instruction *opcode* field.
FUNCT7_5	1 bit	Input	Connected to the instruction *funct7* field.
FUNCT3	3 bits	Input	Connected to the instruction *funct3* field.
IADDER_OUT_1_TO_0	2 bits	Input	Used to verify the alignment of loads and stores.
ALU_OPCODE	4 bits	Output	Selects the operation to be performed by the ALU. See table 10 for possible values.
MEM_WR_REQ	1 bit	Output	When high indicates a request to write to memory.
LOAD_SIZE	2 bits	Output	Indicates the word size of load instruction. See table 15.
LOAD_UNSIGNED	1 bit	Output	Indicates the type of load instruction (signed or unsigned). See table 15.
ALU_SRC	1 bit	Output	Selects the ALU 2nd operand.
IADDER_SRC	1 bit	Output	Selects the Immediate Adder 2nd operand.
CSR_WR_EN	1 bit	Output	Controls the WR_EN input of CSR Register File.
RF_WR_EN	1	Output	Controls the WR_EN input of Integer Register File. See table 12.
WB_MUX_SEL	3	Output	Selects the data to be written in the Integer Register File.
IMM_TYPE	3	Output	Selects the immediate based on the type of the instruction.
CSR_OP	3	Output	Selects the operation to be performed by the CSR Register File (read/write, set or clear).
ILLEGAL_INSTR	1 bit	Output	When high indicates that an invalid or not implemented instruction was fetched from memory.
MISALIGNED_LOAD	1 bit	Output	When high indicates an attempt to read data in disagreement with the memory alignment rules. See section 1.10.
MISALIGNED_STORE	1 bit	Output	When high indicates an attempt to write data to memory in disagreement with the memory alignment rules. See section 1.10.

7.2 ALU

The ALU (`alu.v`) applies ten distinct logical and arithmetic operations in parallel to two 32-bit operands, outputting the result selected by `OPCODE`. ALU input and output signals are shown in table 9, and opcodes are shown in table 10.

The opcode values were assigned to facilitate instruction translation. The most significant bit of `OPCODE` matches with the second most significant bit in the instruction *funct7* field. The remaining three bits match with the instruction *funct3* field.

Table 9 – ALU signals

Signal name	Width	Direction	Description
OP_1	32 bits	Input	Operation first operand.
OP_2	32 bits	Input	Operation second operand.
OPCODE	4 bits	Input	Operation code. This signal is driven by *funct7* and *funct3* instruction fields.
RESULT	32 bits	Output	Result of the requested operation.

Table 10 – ALU opcodes

Opcode	Operation	Binary value
ALU_ADD	Addition	4'b0000
ALU_SUB	Subtraction	4'b1000
ALU_SLT	Set on less than	4'b0010
ALU_SLTU	Set on less than unsigned	4'b0011
ALU_AND	Bitwise logical AND	4'b0111
ALU_OR	Bitwise logical OR	4'b0110
ALU_XOR	Bitwise logical XOR	4'b0100
ALU_SLL	Logical left shift	4'b0001
ALU_SRL	Logical right shift	4'b0101
ALU_SRA	Arithmetic right shift	4'b1101

7.3 Integer Register File

The Integer Register File (`integer_file.v`) has 32 general-purpose registers and supports read and write operations. Reads are requested in the pipeline stage 2 and provide data from one or two registers. Writes are requested in the pipeline stage 3 and put the data coming from the Writeback Multiplexer into the selected register. If stage 3 requests to write to a register being read by stage 2, the data to be written is immediately forwarded to stage 2. Each operation is driven by a distinct set of signals, shown in tables 11 and 12.

Table 11 – Integer Register File signals for read operation

Signal name	Width	Direction	Description
RS_1_ADDR	5 bits	Input	*Register source 1 address*. The data is placed at RS_1 immediately after an address change.
RS_2_ADDR	5 bits	Input	*Register source 2 address*. The data is placed at RS_2 immediately after an address change.
RS_1	32 bits	Output	Data read (source 1).
RS_2	32 bits	Output	Data read (source 2).

Table 12 – Integer Register File signals for write operation

Signal name	Width	Direction	Description
RD_ADDR	5 bits	Input	*Destination register address*.
RD	32 bits	Input	Data to be written in the destination register.
WR_EN	1 bit	Input	*Write enable*. When high, the data placed on RD is written in the destination register at the next clock rising edge.

7.4 Branch Unit

The Branch Unit (`branch_unit.v`) decides if a branch instruction must be taken or not. It receives two operands from the Integer Register File and, based on the value of *opcode* and *funct3* instruction fields, decides the branch. Jump instructions are interpreted as branches that must always be taken. Internally, the unit realizes just two comparisions, deriving other four from them. Table 13 shows the module input and output signals.

Table 13 – Branch Unit signals

Signal name	Width	Direction	Description
OPCODE_6_TO_2	5 bits	Input	Connected to the *opcode* instruction field.
FUNCT3	3 bits	Input	Connected to the *funct3* instruction field.
RS1	32 bits	Input	Connected to the register file 1st operand source.
RS2	32 bits	Input	Connected to the register file 2nd operand source.
BRANCH_TAKEN	1 bit	Output	High if the branch must be taken, low otherwise.

7.5 Load Unit

The Load Unit (`load_unit.v`) reads DATA_IN input signal and forms a 32-bit value based on the load instruction type (encoded in the *funct3* field). The formed value (placed on OUTPUT) can then be written in the Integer Register File. The module input and output signals are shown in table 14. The value of OUTPUT is formed as shown in table 15.

Table 14 – Load Unit signals

Signal name	Width	Direction	Description
LOAD_SIZE	2 bits	Input	Connected to the two least significant bits of the *funct3* instruction field.
LOAD_UNSIGNED	1 bit	Input	Connected to the most significant bit of the *funct3* instruction field.
DATA_IN	32 bits	Input	32-bit word read from memory.
IADDER_OUT_1_TO_0	2 bits	Input	Indicates the byte/halfword position in DATA_IN. Used only with load byte/halfword instructions.
OUTPUT	32 bits	Output	32-bit value to be written in the Integer Register File.

Table 15 – Load Unit output generation

LOAD_SIZE	**Effect on OUTPUT**
2'b00	The byte in the position indicated by IADDER_OUT_1_TO_0 is placed on the least significant byte of OUTPUT. The upper 24 bits are filled according to the LOAD_UNSIGNED signal.
2'b01	The halfword in the position indicated by IADDER_OUT_1_TO_0 is placed on the least significant halfword of OUTPUT. The upper 16 bits are filled according to the LOAD_UNSIGNED signal.
2'b10	All bits of DATA_IN are placed on OUTPUT.
2'b11	All bits of DATA_IN are placed on OUTPUT.
LOAD_UNSIGNED	**Effect on OUTPUT**
1'b0	The remaining bits of OUTPUT are filled with the sign bit.
1'b1	The remaining bits of OUTPUT are filled with zeros.

7.6 Store Unit

The Store Unit (`store_unit.v`) drives the signals that interface with memory. It places the data to be written (which can be a byte, halfword or word) in the right position in DATA_OUT and sets the value of WR_MASK in an appropriate way. Table 16 (below) shows the unit input and output signals.

Table 16 – Store Unit signals

Signal name	Width	Direction	Description
FUNCT3	3 bits	Input	Connected to the *funct3* instruction field. Indicates the data size (byte, halfword or word).
IADDER_OUT	32 bits	Input	Contains the address (possibly unaligned) where the data must be written.
RS2	32 bits	Input	Connected to Integer Register File source 2. Contains the data to be written (possibly in the wrong position).
MEM_WR_REQ	1 bit	Input	Control signal generated by the Control Unit. When high indicates a request to write to memory.
DATA_OUT	32 bits	Output	Contains the data to be written in the right position.
D_ADDR	32 bits	Output	Contains the address (aligned) where the data must be written.
WR_MASK	4 bits	Output	A bitmask that indicates which bytes of DATA_OUT must be written. For more information, see section 4.3.
WR_REQ	1 bit	Output	When high indicates a request to write to memory.

7.7 Immediate Generator

The Immediate Generator (`imm_generator.v`) rearranges the immediate bits contained in the instruction and, if necessary, sign-extends it to form a 32-bit value. The unit is controlled by the IMM_TYPE signal, generated by the Control Unit. Table 17 shows the unit input and output signals.

Table 17 – Immediate Generator signals

Signal name	Width	Direction	Description
INSTR	25 bits	Input	Connected to the instruction bits (32 to 7).
IMM_TYPE	2 bits	Input	Control signal generated by the Control Unit that indicated the type of immediate that must be generated.
IMM	32 bits	Output	32-bit generated immediate.

7.8 CSR Register File

The CSR Register File (`csr_file.v`) has the control and status registers required for the implementation of M-mode. Read/write, set and clear operations can be applied to the registers. Table 18 shows the unit input and output signals, except those used for communication with the Machine Control, which are shown in table 19.

Table 18 – CSR Register File signals

Signal name	Width	Direction	Description
WR_EN	1 bit	Input	*Write enable*. When high, updates the CSR addressed by CSR_ADDR at the next clock rising edge according to the operation selected by CSR_OP.
CSR_ADDR	12 bits	Input	Address of the CSR to read/write/modify.
CSR_OP	3 bits	Input	Control signal generated by the Control Unit. Selects the operation to be performed (read/write, set, clear or no operation).
CSR_UIMM	5 bits	Input	*Unsigned immediate*. Connected to the five least significant bits from the Immediate Generator output.
CSR_DATA_IN	32 bits	Input	In write operations, contains the data to be written. In set or clear operations, contains a bit mask.
PC	32 bits	Input	*Program counter* value. Used to update the `mepc` CSR.
E_IRQ	1 bit	Input	*External interrupt request*. Used to update the `MEIP` bit of `mip` CSR.
T_IRQ	1 bit	Input	*Timer interrupt request*. Used to update the `MTIP` bit of `mip` CSR.
S_IRQ	1 bit	Input	*Software interrupt request*. Used to update the `MSIP` bit of `mip` CSR.
REAL_TIME	64 bits	Input	Current value of the real time counter. Used to update the `time` and `timeh` CSRs.
CSR_DATA_OUT	32 bits	Output	Contains the data read from the CSR addressed by CSR_ADDR.
EPC_OUT	32 bits	Output	Current value of the `mepc` CSR.
TRAP_ADDRESS	32 bits	Output	Address of the trap handler first instruction.

Table 19 – CSR Register File and Machine Control interface signals

Signal name	Width	Direction[1]	Description
I_OR_E	1 bit	Input	*Interrupt or exception*. When high indicates an interrupt, otherwise indicates an exception. Used to update the most significant bit of `mcause` register.
CAUSE_IN	4 bits	Input	Contains the exception code. Used to update the `mcause` register. See table 7.
SET_CAUSE	1 bit	Input	When high updates the `mcause` register with the values of I_OR_E and CAUSE_IN.
SET_EPC	1 bit	Input	When high, updates the `mepc` register with the value of PC.
INSTRET_INC	1 bit	Input	When high enables the instructions retired counting.
MIE_CLEAR	1 bit	Input	When high sets the MIE bit of `mstatus` to zero (which globally disables interrupts). The old value of MIE is saved in the `mstatus` MPIE field.
MIE_SET	1 bit	Input	When high sets the MPIE bit of `mstatus` to one. The old value of MPIE is saved in the `mstatus` MIE field.
MIE	1 bit	Output	Current value of MIE bit of `mstatus` CSR.
MEIE_OUT	1 bit	Output	Current value of MEIE bit of `mie` CSR.
MTIE_OUT	1 bit	Output	Current value of MTIE bit of `mie` CSR.
MSIE_OUT	1 bit	Output	Current value of MSIE bit of `mie` CSR.
MEIP_OUT	1 bit	Output	Current value of MEIP bit of `mip` CSR.
MTIP_OUT	1 bit	Output	Current value of MTIP bit of `mip` CSR.
MSIP_OUT	1 bit	Output	Current value of MSIP bit of `mip` CSR.

[1] Direction regarding to the CSR Register File. An input of CSR Register File is an output of Machine Control and vice-versa.

7.9 Machine Control

The Machine Control module (`machine_control.v`) implements the M-mode, controlling the the program counter generation and updating several CSRs. It has a special communication interface with the CSR Register File, already shown in table 19 (above). Its input and output signals are shown in table 20 (below).

Internally, the module implements the finite state machine shown in figure 10 (next page).

Table 20 – Machine Control module signals

Signal name	Width	Direction	Description
ILLEGAL_INSTR	1 bit	Input	*Illegal instruction*. When high indicates that an invalid or not implemented instruction was fetched from memory.
MISALIGNED_INSTR	1 bit	Input	*Misaligned instruction*. When high indicates an attempt to fetch an instruction which address is in disagreement with the memory alignment rules. See section 1.10.
MISALIGNED_LOAD	1 bit	Input	*Misaligned load*. When high indicates an attempt to read data in disagreement with the memory alignment rules. See section 1.10.
MISALIGNED_STORE	1 bit	Input	*Misaligned store*. When high indicates an attempt to write data to memory in disagreement with the memory alignment rules. See section 1.10.
OPCODE_6_TO_2	5 bits	Input	Value of the *opcode* instruction field.
FUNCT3	3 bits	Input	Value of the *funct3* instruction field.
FUNCT7	7 bits	Input	Value of the *funct7* instruction field.
RS1_ADDR	5 bits	Input	Value of the *rs1* instruction field.
RS2_ADDR	5 bits	Input	Value of the *rs2* instruction field.
RD_ADDR	5 bits	Input	Value of the *rd* instruction field.
E_IRQ	1 bit	Input	*External interrupt request*.
T_IRQ	1 bit	Input	*Timer interrupt request*.
S_IRQ	1 bit	Input	*Software interrupt request*.
PC_SRC	2 bit	Output	Selects the program counter source.
FLUSH	1 bit	Output	Flushes the pipeline when set.

Figure 10 – M-mode finite state machine