BHARGAV D V

International Institute of Information Technology, Bangalore
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Education

International Institute of Information Technology, Bangalore **2023 – Present**
Master of Science by Research (VLSI) *3.85/4 CGPA*

BNM Institute of Technology, Bangalore **2018 – 2022**
Bachelor of Engineering in Electronics and Communication *8.89/10 CGPA*

Sri Kumaran Composite Junior College, Bangalore **2017 – 2018**
Class 12 – Science *91.33% Grade*

Work Experience

Synamedia **June 2022 – January 2023**
Associate Technical Consultant *Bangalore*

- Gained insights into linux scripting, python scripting, and video streaming technologies.

Projects

Physical Design Flow of Custom RISC-V processor

- Developed C code for RISC-V processor designed to work as Display Controller.
- Implemented custom RISC-V processor based on required instructions.
- Executed RTL to GDS flow on custom RISC-V processor using OpenLane Sky130 PDK kit.

Image processing using FPGA

- Interfaced embedded processor(PS) with programmable logic (PL) unit to read images from SD card and perform edge detection on the Zedboard.
- Created AXI-Lite memory interface in PL for data sharing between PS and PL.
- Implementation of VGA control unit in PL to display input and processed images.

Publications

- Bhargav DV, Pradyumna G and Dr.Madhav Rao, ***Meta-Heuristic Optimization of Custom Heterogeneous Blocks defined eFPGA Design***, accepted at VLSID 2025.
- Bhargav DV, Dantu Nandini Devi, Rachana Kaparthi and Dr.Madhav Rao, ***LibApprox: A Comprehensive Library for Performance Efficient Approximate Circuits***, accepted at ISQED 2025.

Skills

Scripting: Python, C/CUDA
Academic OpenSource Tools: Icarus Verilog(Verilog simulator), GTK Wave (Waveform viewer), OpenRoad(RTL to GDS tool), Verilog-to-routing (FPGA CAD exploration tool), Ngspice(Spice simulator)

Additional Activities

- Teaching Assistant in NPTEL course **Design and Analysis of VLSI Subsystems** from January 2025 - Present.
- Assisted Technical Program Chairs (TPC) to manage all stages of the Conference **VLSID 2025** from submission of technical papers to ensuring smooth presentations.