KANISH R

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Education

International Institute of Information Technology, Bangalore **2023 – Present**
Master of Science by Research (VLSI) *4/4 CGPA*

Rajalakshmi Engineering College **2019 – 2023**
Bachelor of Engineering in Electronics and Communication *9.7/10 CGPA*

Internship Experience

Aheesa Digital Innovations Private Limited **January 2023 – April 2023**
Application Specific Integrated Circuit Design Intern *Chennai*

- Developed and implemented AES Encryption and Frame Check Sequence (FCS) encoder networking sub-modules using Verilog.
- Conducted preliminary board testing and debugged the RS485 interface.

Mentorship

Teaching Assistant **August 2024 – December 2024**
Digital CMOS VLSI Design *IIIT Bangalore*

- Interactive teaching sessions with students on various topics in the operating systems.

Projects

Compact Bit Parallel Implementation of Systolic Array over $GF(2^m)$

- This project re-implements the paper: A. Ibrahim, F. Gebali, Y. Bouteraa, U. Tariq, T. Ahanger and K. Alnowaiser, "Compact Bit-Parallel Systolic Multiplier Over $GF(2^m)$
- Implemented a novel 1-D bit-parallel systolic array for $GF(2^m)$ multiplication, reducing hardware complexity from $O(m^2)$ to O(m) while maintaining speed.
- Proved the new design surpasses previous bit-parallel systolic multipliers in area efficiency and power consumption without compromising speed.
- The results indicate that the proposed design significantly improves AT over the compared parallel designs by at least 99.72% for m = 233 and 99.76% for m = 409, respectively.

Implementation of Partial Reconfiguration for Systolic Array Architecture using FPGA

- Interfaced embedded processor(PS) with programmable logic (PL) unit for partially re-configurable systolic array architecture on the Zedboard, for image processing application.
- Created a custom AXI-Lite memory interface in PL for data sharing between PS and PL.
- Leveraged FPGA's Partial Reconfiguration (PR) capabilities to enable real-time switching between these tasks without reconfiguring the entire fabric.

Analysis of Low-Power Retentive TSPC Flip-Flop With Redundant Precharge Free Operation

- Implemented the paper titled "Low-Power Retentive True Single-Phase-Clocked Flip-Flop With Redundant Precharge Free Operation" using GPDK45nm technology node.
- Optimized transistor sizes and conducted static timing analysis.
- Conducted floating node analysis, simulated the circuits, and analyzed for soft errors.

Publications

Precision and Power Efficient Piece-wise-Linear Implementation of Transcendental Functions

- Accepted to The Euromicro Conference on Digital System Design (DSD) 2024
- We designed a PWL method utilizing the Method of Least Squares to approximate both Sigmoid and Hyperbolic-Tangent functions, achieving a 6.77% improvement in Maximum Absolute Error (MAE) for Sigmoid and a 10.3% enhancement for Tanh, along with 70.6% and 45.3% power savings and 41% and 10.3% less delay.
- Implemented those functions into the AlexNet model and performed Quantization-aware Training and Testing, demonstrating comparable training and validation accuracy to exact functions.
https://ieeexplore.ieee.org/document/10741664

Technical Skills

Languages: Python, C, Verilog
Tools: Yosys, Xilinx Vivado, LTSpice, Cadence Genus, iverilog, Arduino IDE

Relevant Coursework

- System Design Through FPGA
- Digital CMOS VLSI Design
- Hardware Modelling Using Verilog
- Physical Design Using ASIC
- Machine Learning

Achievements

- Recieved Micron's University Research Alliance Scholarship.
- Received Best Outgoing Student Award among 2023 batch from Rajalakshmi Engineering College.
- First in the Excellent Category in Mixed Signal SoC design Marathon using eSim & SKY130 organized by VLSI System Design and eSim,IITB.

Leadership / Extracurricular

MOSFIT, IIITB **July 2024 – Current**

Senior Core Memeber *International Institute of Information Technology Bangalore*

∗ Conduct interactive sessions for college students and organise hackathons.

Designers Consortium **April 2022 – May 2023**

Vice-President *Rajalakshmi Engineering College*

∗ Organized the Product Research and Technical Analysis of Market (PRATAM) 2022 event, a design and product development hackathon that drew over 150 participants from multiple institutions.

∗ Led a team of 10 to create workshops and events focused on design thinking, CAD, and prototyping, fostering technical skills and project-based learning.