DILLI BABU PORLAPOTHULA

International Institute of Information Technology, Bangalore
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Education

International Institute of Information Technology, Banglore **Aug. 2023 – Dec 2025**
MS in VLSI and Embedded Systems *CGPA: 3.48 /4*

SASTRA University, Thanjavur **Aug. 2017 – July 2021**
B.Tech in Electronics and Communication Engineering *CGPA: 8.04/10*

Experience

COMCAST **Jan 2021 – May 2023**
Software Development Engineer *Chennai,Tamil Nadu*

- Part of .net backend team responsible for video processing.
- Automated several manual tasks that team is doing using python.
- Integrated Datadog to improve better insights and debug faster.

Mentorship

Teaching Assistant **Aug 2024 – Dec 2024**
Embedded Systems and Design *IIIT Bangalore*

- Conducted lab sessions for students on PSoC boards, covering various PSoC modules and Embedded C programming.

Projects

Reliability Assessment for 6T SRAM in Aging Environments | *Cadence Virtuoso, 180nm* **November 2023**

- Conducted an in-depth analysis of aging effects on 6T SRAM cells, focusing on performance metrics like read/write latencies, access times, and power consumption.
- Designed and simulated a dual-edge-triggered transition detector and stability-checker-based pulse detector for robust reliability assessment under PVTA degradations.
- Demonstrated the solution's ability to detect signal transitions and maintain stability across diverse operating conditions, paving the way for optimization in advanced memory design.

Carry Disregard Approximate Multiplier Design | *Cadence Genus, 45nm* **April 2024**

- Evaluated a methodology for designing approximate N-bit array multipliers based on carry disregarding, optimizing for error-tolerant applications..
- Achieved significant reductions in critical path delay (up to 35%), power consumption (up to 29%), and area (up to 30%) compared to exact multipliers.
- Demonstrated the practical applicability of the design in image processing, achieving PSNR above 30 dB and SSIM over 94%.

Technical Skills

Languages: Verilog, Python, C
Tools/Technologies: Cadence Virtuoso, Cadence Genus, Xilinx Vivado, LTspice

Relevant Coursework

- Digital CMOS VLSI Design
- System design with FPGA
- Physical Design Of ASICs
- VLSI Architecture Design

Leadership / Extracurricular

- Secured 1st prize in the college hackathon during the 2nd year of B.Tech for developing a line-following robot.
- Volunteered and organized ADCOM 2024, managing food arrangements and registration processes.
- Assisted in organizing the ICVGIP 2024 conference, overseeing tutorial session arrangements.