Pruthvi Parate

International Institute of Information Technology, Bangalore
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Education

International Institute Of Information Technology, Bangalore **Aug 2023 – Present**
MS By Research, Electronics And Communication Engineering; ***CGPA*** *: 3.76/4* *Bengaluru, Karnataka*

L.J Institute Of Engineering And Technology **July 2019 – July 2023**
B.E In Electronics And Communication Engineering; ***CGPA*** *: 9.23/10* *Ahmedabad, Gujarat*

Projects

RISCV-based Social Distance Detection | *RISCV, Openlane, C, Verilog* **November 2023**

- The aim of this project was to develop and implement a flexible social distance detection system controlled by a RISC-V. This system facilitates the measurement of social distance. The user will be alarmed when the distance will be less than 2m and greater than 0.

Displaying Image on the VGA monitor from SD Card | *Verilog, Python, TCL* **November 2023**

- Hardware used: Zedboard evaluation board, SD Card, VGA Monitor and Cable
- Software tools used: Vivado, Vitis
- The implementation integrates Verilog modules for image processing and VGA display., utilizing block RAM for data storage and AXI Lite interface for communication. The Sobel operator is employed for edge detection in image processing. The project was rigorously tested using iverilog, Vivado, and Python scripts.

Compact Bit Parallel Implementation of Systolic Array over $GF(2^m)$ | *Verilog, Python* **November 2023**

- This project re-implements the paper: A. Ibrahim, F. Gebali, Y. Bouteraa, U. Tariq, T. Ahanger and K. Alnowaiser, "Compact Bit-Parallel Systolic Multiplier Over $GF(2^m)$
- Implemented a novel 1-D bit-parallel systolic array for $GF(2^m)$ multiplication, reducing hardware complexity from $O(m^2)$ to O(m) while maintaining speed.
- The results indicate that the proposed design significantly improves AT over the compared parallel designs by at least 99.72% for m = 233 and 99.76% for m = 409, respectively.

Experience

Grownited Private Limited **Jan 2023 – May 2023**
Python/Django Intern *Ahmedabad, Gujarat*

- Utilized Python programming and its framework Django to develop a project.
- Mastered advanced Python programming concepts and developed a project named 'Test Killer'.

Publications

Non-Homogeneous Composite Karatsuba Multipliers Factored Hardware-Efficient ECDSA Generation- and Verification Accelerator Units
Authors: Pruthvi Parate, Madhav Rao et.al

- Accepted to International Symposium on Quality Electronic Design, ISQED 2025

Power and Area-Efficient ECC Processor with Sequential Recursive Polynomial Multiplier Implementation
Authors: Pruthvi Parate, Madhav Rao et.al

- Accepted to International Symposium on Quality Electronic Design, ISQED 2025

A Generalized Hardware-Efficient Gabor Wavelet Architecture for Medical Image Processing
Authors: Priyanka Agarwal, **Pruthvi Parate**, Madhav Rao et.al

- Accepted to International Symposium on Quality Electronic Design, ISQED 2025

Hardware-Efficient ECC Processor Design using Non-Homogeneous Split Hybrid Karatsuba Multiplier
Authors: Pruthvi Parate, Madhav Rao et.al

- Published to IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2024

Technical Skills

Languages: Verilog, Python, C
Technologies/Tools/Framework: Asic, Openlane, Cadence, Xilinx Vivado and Vitis, LTSpice, Linux, RISCV

Relevant Coursework

- Digital CMOS
- System Design With FPGA
- Physical Designs Of ASICs
- VLSI Architecture

Leadership / Extracurricular

VLSI Design Conference **January 2025**
Volunteer *IIITB*

- Assisted in organizing an international conference with 2,700 participants, including semiconductor experts, industry leaders, and government dignitaries. Supported event logistics, participant engagement, and ensured smooth operations.

RISE 2024 Open House **March 2024**
Volunteer *IIITB*

- Coordinated and facilitated the event where research scholars presented their work.