Aashish Tiwary

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Education

International Institute of Information Technology, Bangalore **August 2022 – July 2025**
MS By Research in VLSI *3.36/4*

University Institute Of Engineering and Technology, Panjab University **July 2015 – July 2019**
B.E in Electronics and Communication Engineering *7.44/10*

Technical Skills

Languages: Verilog, C
Technologies/Frameworks: Accelerator, FPGA, Vivado, Vitis IDE, ASIC, AXI, LTSpice, Linux, CDC

Experience

TT Consultants **July 2019 – July 2021**
Patent Research Analyst *Mohali, Punjab*

- Reviewed and analyzed hundreds of patent applications, granted patents, and technical literature for strategic IP management.
- Compiled detailed search reports that identified key trends in technology, leading to tailored recommendations for three successful IP strategies adopted by clients.

Mentorship

Teaching Assistant **August 2024 – November 2024**
System Design with FPGA — Course Instructor: Prof. Nanditha Rao *IIIT Bangalore*

- Delivered tutorials and lab sessions for a class of 120 students, explaining FPGA design principles and Xilinx tools.
- Mentored students in their final project by providing constructive feedback and debugging errors.

Projects

Hardware/Software Co-design of Machsuite Benchmarks | *Vitis, HLS, Zynq-MPSoC* **Jan 2024 - Mar 2024**

- Executed 3 workloads defined in Machsuite Benchmarks using Vitis embedded acceleration flow on ZCU104 board.
- Worked on efficient data transfer between Kernel and DDR Banks on off chip global memory
- Performed code partitioning to offload the compute-intensive part to the hardware kernel.
- Optimized workloads achieving an average of 1000 times reduction in its latency with this method

Hardware Implementation of POSIT Adder | *Xilinx Vivado, SDK, FPGA* **Jan 2023 - Mar 2023**

- Implemented the (32,2) POSIT adder design using verilog in Xilinx vivado .
- Created vivado IP of the design and used Microblaze to run it on Nexys A7 using vivado and xilinx SDK

Hardware modeling of floating point MAC using DSP Packing | *Vivado, Verilog, FPGA* **Sep 2024-Nov 2024**

- Designed a multiply and accumulate unit with BFloat16 precision by using DSP packing technique.
- Optimized the design achieving 50% reduction in DSP usage compared to traditional Bfloat without DSP packing.

Physical Design of an 8-bit ALU using SKY130 Technology PDK | *Openlane, Magic, Yosys* **Oct 2022 - Dec 2022**

- Conducted RTL-to-GDSII flow for the 8-bit ALU design using openlane tool culminating in a successful tapeout.
- Conducted thorough DRC/LVS verification using precheck tools to ensure the IC met all design criteria.
- Acheived an operating frequency of 2.87 GHz and area of 10 mm^2 for the design with the skywater 130nm PDK.

Publications

LUTAccel: Look-up-Table based Vector Systolic Accelerator on FPGAs **July 2024 - Sept 2024**

- Submited to ISQED'25

Relevant Coursework

- Digital CMOS VLSI Design
- System design with FPGA
- Functional Verification of SoCs
- Physical design of ASICs
- VLSI Design FLow:RTL to GDS (NPTEL)

Acheivements

- One of the first recipients of a taped out IC through Google's Open MPW Shuttle Program, for designing an 8-bit ALU using the Open PDK sky130A