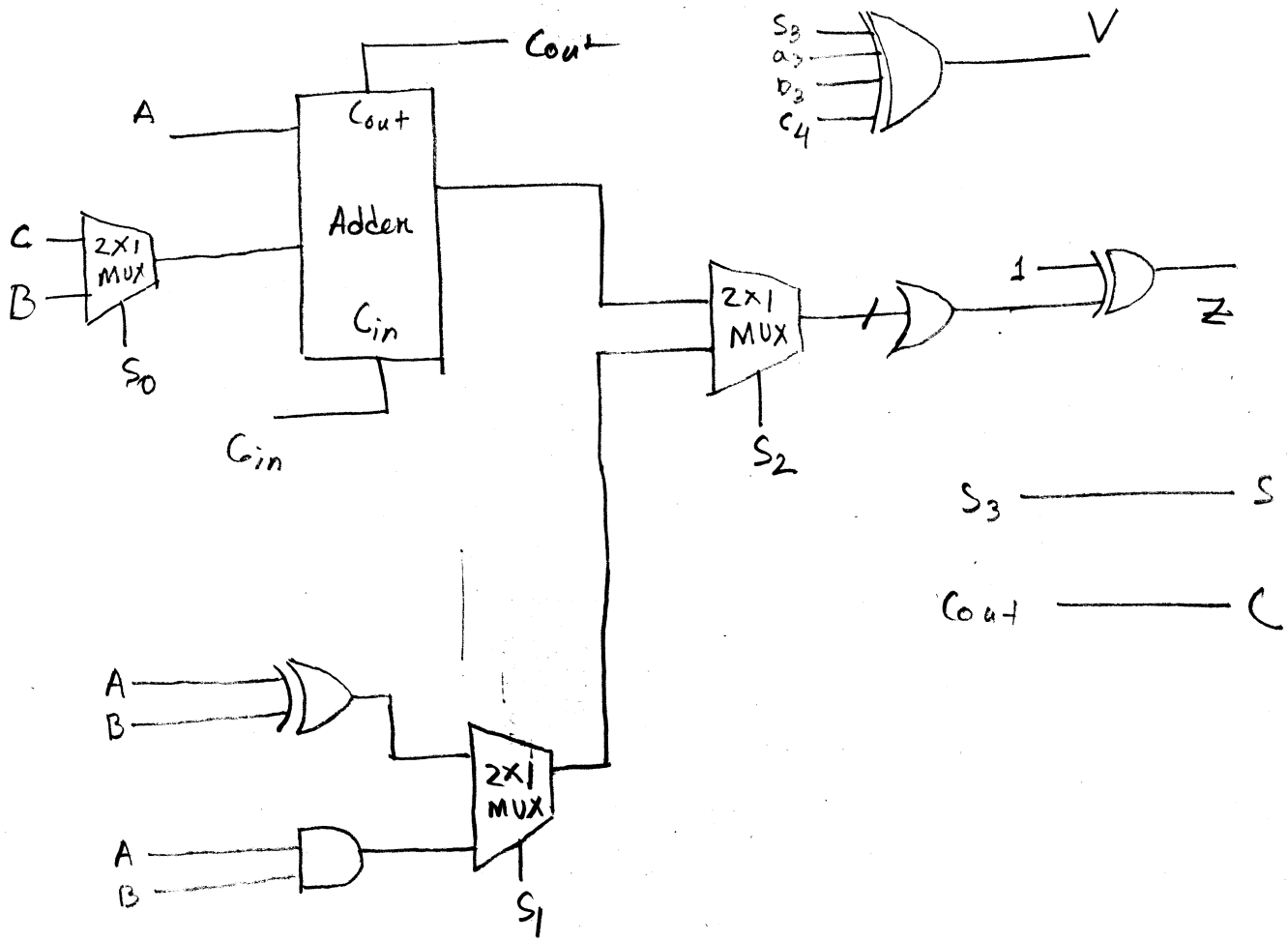

CS_2	CS_1	CS_0	OP	C	C_{in}	S_0	S_1	S_2
0	0	0	Add	X	0	1	X	0
0	0	1	AND	0	0	0	1	1
0	1	0	Add	X	0	1	X	0
0	1	1	Transfer A	0	0	0	X	0
1	0	0	Decrement A	1	0	0	X	0
1	0	1	XOR	0	0	0	0	1
1	1	0	Add with carry	X	1	1	X	0
1	1	1	Add with carry	X	1	1	X	0

K maps:

C

	0	1
00	X	0
01	X	0
11	X	X
10	1	0

$C = \overline{CS_0}$

(1 NAND)

C_{in}

	0	1
00	0	0
01	0	0
11	1	1
10	0	0

$C_{in} = \overline{\overline{D_6}\ \overline{D_7}}$

(1 NAND)

S_0

	0	1
00	1	0
01	1	0
11	1	1
10	0	0

$S_0 = \overline{\overline{D_0}\ \overline{D_2}} + \overline{\overline{D_6}\ \overline{D_7}}$

(1 NAND, 1 OR)

S_1

	0	1
00	X	1
01	X	X
11	X	X
10	X	0

$S_1 = \overline{D_5}$

S_2

	0	1
00	0	1
01	0	0
11	0	0
10	0	1

$S_2 = \overline{\overline{D_1}\ \overline{D_5}}$

(1 NAND)

ICs

1. 1 3-8 Decoder
2. 1 4-bit Full Adder
3. 3 Quad 2x1 MUX
4. 2 Quad XOR
5. 1 Quad AND
6. 1 Quad OR
7. 1 Quad NAND