A Low-Power Efficient Demosaicing Hardware Design : Project Proposal

SAGNIK BASU sbasu24@wisc.edu
JAGDISH MOHAPATRA nmohapatra@wisc.edu
LAMSHE RAJA lraja@wisc.edu
RAHIMULLAH SHAIK rshaik@wisc.edu

***Abstract*— Digital cameras use Color Filter Array (CFA) where the sensor detects only a particular spectral band for each pixel. The unmeasured spectral bands are estimated from the neighborhood pixels. Hence to reconstruct a full representation of the color image, an interpolation of the unmeasured spectral bands is required.This is known as demosaicing Though there are many different demosaicing techniques,there is always a trade-off between dynamic power consumed during computation and quality of the reconstructed image.The proposed scheme is based on the fact that edges have strong luminance components. Hence, we are proposing an gradient-corrected technique by taking the intensity values of critical pixels into consideration.The proposed techniques give a better performance in terms of low dynamic power consumption and improved PSNR when compared to some of the available demosaicing techniques such as Nearest Neighbor interpolation, vector median interpolation, and bilinear interpolation.**

I. INTRODUCTION

Image Signal Processors are integral part of all modern smartphones. From [1],it can be summarized that it consists of several blocks to convert the Bayer pattern from CMOS Sensor to a visually perceptive RGB pattern. With more powerful processors which are available to us, the ISP pipelines are becoming more computationally heavy to support more pixel resolution. We propose a novel design for one of the most important blocks of the ISP – which is Image Demosaicing [2].

Out project considers the ISP to be an important part of embedded system like digital camera, as without it we cannot have an efficient imaging pipeline.More research are being done on efficient ISP designs on modern processors [3].The RGB output pixels computed from the demosaicing from them are an important for computer vision algorithms being run on embedded system. Since the output from demosaicing blocks are being fed to noise reduction blocks , we target generating a more accurate demosaicing hardware in order to reduce dynamic power consumption and improve PSNR.By saving dynamic power on the demosaicing block, we are making ISP pipeline more efficient than before.

II. GOALS

Our goal is to improve any complex ISP design by improving the important beginning block in the ISP pipeline which is “demosaicing”. The line buffers (in memory) will have more accurate data for the subsequent ISP blocks to process, if we make the demosaicing block efficient enough, since it’s the beginning block in every ISP. We are planning to implement a hardware engine capable of doing demosaicing more efficiently than the previously proposed schemes, i.e. bilinear interpolation [2]. In our method, we are planning to optimize the power and improve the PSNR value compared bilinear interpolation method to generate more accurate RGB pixel data.

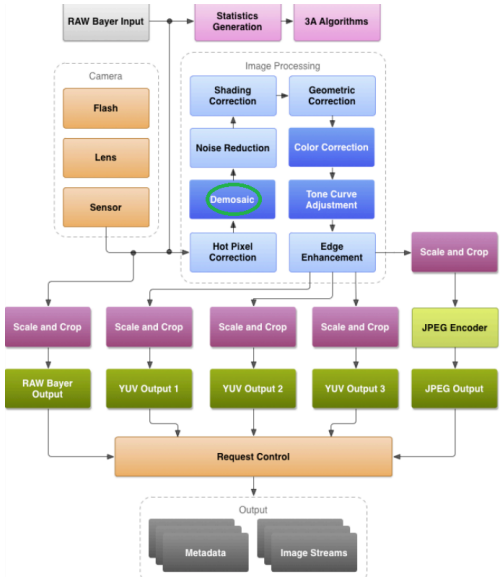

Fig. 1. ISP Full chain

To compare our design, we choose the ASIC implementation of an interpolation processor as discussed here [4]. Since this is pure ASIC implementation, we believe our design on FPGA will match and can even outperform the baseline design.

III. RELATED WORK

First and foremost, we would use [1] to gain understanding of Image Signal Processing blocks and the demosaicing algorithms used.

Further, recent work on efficient mapping of demosaicing algorithms onto FPGA were done in [5] and [6]. Traditional ISP implementations that use bi-linear interpolation for major computations, incurs drain on performance, dynamic power and efficiency due to inefficient filter size and co-efficient. To

overcome this issue, papers like [7] suggest a improvement over bi-linear interpolation.

Further, we also plan to leverage the Approximate techniques mentioned in [8] and [9] to improve the filter design as showed in Fig. 2. This is because the image pipeline is error resilient to the background and other noises of the CMOS sensors.Also, the similar correlation across the Bayer channels will also ensure minimum degradation of PSNR on the output.

.

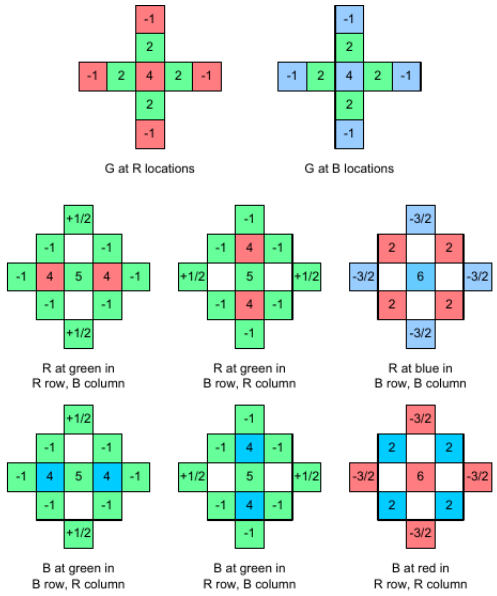

Fig. 2. Filter coefficients of our proposed demosaicing block

IV. EMBEDDED SYSTEM RELEVANCE

A major goal of ECE 751 is to understand the advanced design principles of a power efficient embedded computing system and identify ways to optimize programs using techniques like optimized memory access patterns , approximate computing etc. These are basic building blocks to solve the challenges of designing complex systems like Image Signal Processor.

To tackle the problem of designing a Demosaicing hardware, we consider the functional and non-functional requirements of the design. Some of the important functional requirements are : 1) high input resolution of the image 2) optimal size of the filter coefficients 3) low dynamic power consumption . Since most modern cameras require supporting high input resolution, our demosaicing hardware must process them efficiently to generate the required RGB image without any significant degradation.

The demosaicing hardware block is something which is going to be used in embedded systems that use CMOS camera sensors (ex - DSLR cameras). The work proposed here is based on our learning on embedded system concepts and does not include any topic from other courses taught in UW-Madison.

V. EVALUATION METHODS

Our primary objective is to come up with a synthesizable and verified RTL design of Demosaicing block which will consume less dynamic power while giving almost accurate results with very minimal loss in image information.

A. Resources

We intend to make use of the Xilinx Software Suite (Vivado) to emulate the Demosaicing data flow computations. To calculate the PSNR, we will use the OpenISP [10] output to compare with our proposed mechanism.For power and area measurement, the most accurate analysis requires Ansys Power Artist and PTPX tool suite. However, we will also consider an appropriate theoretical power model design for our experiments.

B. Features

Ultimately our aim is to create a novel Demosaicing engine based on approximate computing techniques which will consume low dynamic power while having PSNR values close to some of the openly available ISP demosaicing algorithms.

VI. PROJECT PLAN

We are assuming the Week 1 to start with proposal submission date.

- Micro-architecture, Block-level and Top-Level RTL design bring up by November 20.
- Verification using Verilog-HDL testbench by November 29.
- Code Coverage, Power estimation either by Ansys Power Artist tool or by theoretical calculations by December 8.
- PSNR improvement comparison by December 18.
- Future Research proposal design by December 22.

Our teamwise task breakdown is as follow :

- Sagnik : research techniques on implementing a hardware efficient demosaicing method. Propose the possible improvements on the said techniques. Design tools for measuring the PSNR. Work with Jagdish in implementing the demosaicing sub-units.
- Jagdish : Coming up with novel demosaicing hardware enginer architecture. Implement it using verilog HDL. Synthesize the netlist with Xilinx Vivado.Will work closely with rest of the team for design improvements on rest of the project.
- Lamshe : Coming up with a self checking testbench to test each unit of design for different corner cases. Give feedback to rest of the team based on testing.
- Rahimullah : Come up with exhaustive testcases to measure all the feature of the top hardware module before it goes to FPGA and test the code coverage for the RTL.

REFERENCES

[1] S.-H. Choi, J. Cho, Y.-M. Tai, and S.-W. Lee, "Implementation of an image signal processor for reconfigurable processors," *2014 IEEE International Conference on Consumer Electronics (ICCE)*, pp. 141–142, 2014.

[2] K. Hirakawa and T. Parks, "Adaptive homogeneity-directed demosaicing algorithm," *IEEE Transactions on Image Processing*, vol. 14, no. 3, pp. 360–369, 2005.

[3] P. Hansen, A. Vilkin, Y. Krustalev, J. Imber, D. Talagala, D. Hanwell, M. Mattina, and P. N. Whatmough, "Isp4ml: The role of image signal processing in efficient deep learning vision systems," *2020 25th International Conference on Pattern Recognition (ICPR)*, pp. 2438–2445, jan 2021. [Online]. Available: https://doi.ieeecomputersociety.org/10.1109/ICPR48806.2021.9411985

[4] S.-C. Hsia, M.-H. Chen, and P.-S. Tsai, "Vlsi implementation of low-power high-quality color interpolation processor for ccd camera," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 4, pp. 361–369, 2006.

[5] W. Hsu and C.-S. Fuh, "Real-time demosaicking for embedded systems," 2007, pp. 1–2.

[6] A. Karloff and R. Muscedere, "A low-cost, real-time, hardware-based image demosaicking algorithm," 2009, pp. 146–150.

[7] H. Malvar, L. wei He, and R. Cutler, "High-quality linear interpolation for demosaicing of bayer-patterned color images," in *2004 IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. 3, 2004, pp. iii–485.

[8] S. De, S. Mohamed, D. Goswami, and H. Corporaal, "Approximation-aware design of an image-based control system," *IEEE Access*, vol. 8, pp. 174 568–174 586, 2020.

[9] X. Li, "Demosaicing by successive approximation," *IEEE Transactions on Image Processing*, vol. 14, no. 3, pp. 370–379, 2005.

[10] H. S. Park, "Architectural analysis of a baseline isp pipeline," *Springer Netherlands*, pp. 21–45, 2016. [Online]. Available: https://doi.org/10.1007/978-94-017-9987-4$_2$