Resolving Timing Violations after APR:

- **To check the timing violations after the post-route optimization stage:**
  - `report_constraint -all_violators -significant_digits 6 > [filename_of_your_choice]`
  - Analyze `[filename_of_your_choice]` to understand the kind of violations in the design

- **To perform post route optimizations to fix setup, hold and other timing DRCs:**
  - `focal_`opt is a procedure provided by Synopsys to perform targeted fixing of timing violations
  - Use the `focal_`opt command with the appropriate options
  - For setup violations: `focal_opt -setup_endpoints all`
  - For hold violations: `focal_opt -hold_endpoints all`
  - For timing DRC violations: `focal_opt -drc_nets all -drc_pins all`

- **Fixing hold violations using route_opt:**
  - Hold violations may also be resolved by increasing the wire lengths
  - Increasing the wire lengths increases the wire delay and helps with resolving hold violations
  - For hold violations: `route_opt -incremental -only_hold_time`

- **Fixing setup or max transition violations:**
  - IF focal_opt does not resolve the transition violations, they can also be fixed manually
  - Setup time violations or max transition violations typically occur because the signal on the data path travels slower than required
  - A common method to fix these type of violations is to upsize the driver cell
  - Let's look at an example (refer to figures below):
  - The net that is causing the violation is `n13249`
  - Net `n13249` is connected to the list of pins showed in the report below
  - The signal on net `n13249` is slow and hence, the transition requirements on these pins are violated
  - The cell that is driving the net is small and hence, its driving strength is not sufficient to drive the signal fast enough
    - We need to get the cell that drives n13429 (refer to figure below)
    - Each net is always driven only by one cell/pin. So, the below commands can be used to get the driver cell

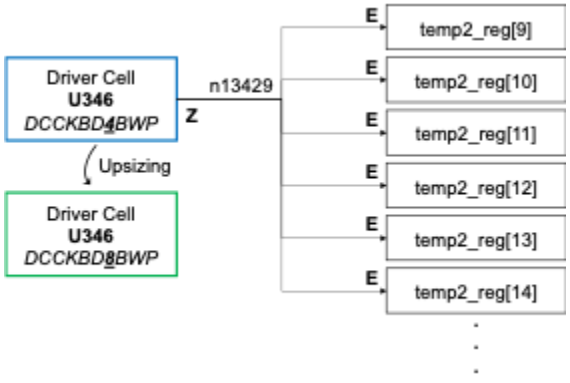
    - ```
      get_pins -of_objects [get_nets n13429] -filter
      "direction==out"
      >> U346/Z
      ```
    - U346 is the name of the cell and Z is the pin name

    - To get the type of library cell:
    - `get_attribute [get_cells U246] ref_name`
    - `>> DCCKBD4BWP`

    - The name of the cell in the library also contains information about its size
    - To change the size of the cell (from 4x to 8x):
    - `size_cell [get_cells U246] DCCKBD8BWP`

  - Follow the other steps below to legalize the cell placement and resolve physical DRC violations
      ```

```
n13429                  0.100000       0.104952       -0.004952 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[9]/E
                        0.100000       0.104952       -0.004952 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[10]/E
                        0.100000       0.104952       -0.004952 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[12]/E
                        0.100000       0.104952       -0.004952 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[11]/E
                        0.100000       0.104952       -0.004952 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[12]/E
                        0.100000       0.104951       -0.004951 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[13]/E
                        0.100000       0.104727       -0.004727 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[14]/E
                        0.100000       0.104761       -0.004761 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[13]/E
                        0.100000       0.104629       -0.004629 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[16]/E
                        0.100000       0.104768       -0.004768 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[15]/E
                        0.100000       0.104760       -0.004760 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[17]/E
                        0.100000       0.104759       -0.004759 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[16]/E
                        0.100000       0.104703       -0.004703 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[19]/E
                        0.100000       0.104551       -0.004551 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[19]/E
                        0.100000       0.104597       -0.004597 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[15]/E
                        0.100000       0.104763       -0.004763 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[20]/E
                        0.100000       0.104544       -0.004544 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[18]/E
                        0.100000       0.104580       -0.004580 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[17]/E
                        0.100000       0.104644       -0.004644 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[18]/E
                        0.100000       0.104648       -0.004648 (VIOLATED)
    PIN :   gnn/n01_node0/temp2_reg[14]/E
                        0.100000       0.104763       -0.004763 (VIOLATED)
    PIN :   gnn/n01_node0/temp0_reg[20]/E
                        0.100000       0.104552       -0.004552 (VIOLATED)
    PIN :   gnn/n01_node0/temp1_reg[19]/E
                        0.100000       0.104434       -0.004434 (VIOLATED)
    PIN :   gnn/n01_node0/temp1_reg[16]/E
```



- **Legalizing placement after focal_opt or other manual fixes:**
  - Some cells might be out of their legal positions after using `focal_opt` or after performing manual fixes
  - The legal placement of cells can be checked with `check_legality` command
  - There are one of two ways to resolve this
    - `legalize_placement -incremental`

        - `place_eco_cells -legalize_only -eco_changed_cells`

- **Resolving physical DRC violations:**
    - Nets in the design may suffer from DRC violations (shorts, open nets, etc.)
    - The `verify_zrt_route` command can be used to check the physical DRC status
    - To route open nets:
        - route_zrt_eco -open_net_driven true -reuse_existing_global_route true
    - To fix only DRC violations (no open nets):
        - route_zrt_detail -incremental true