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DS-A

Assignment (1)

(1) Explain about 8086 microprocessor Architecture.

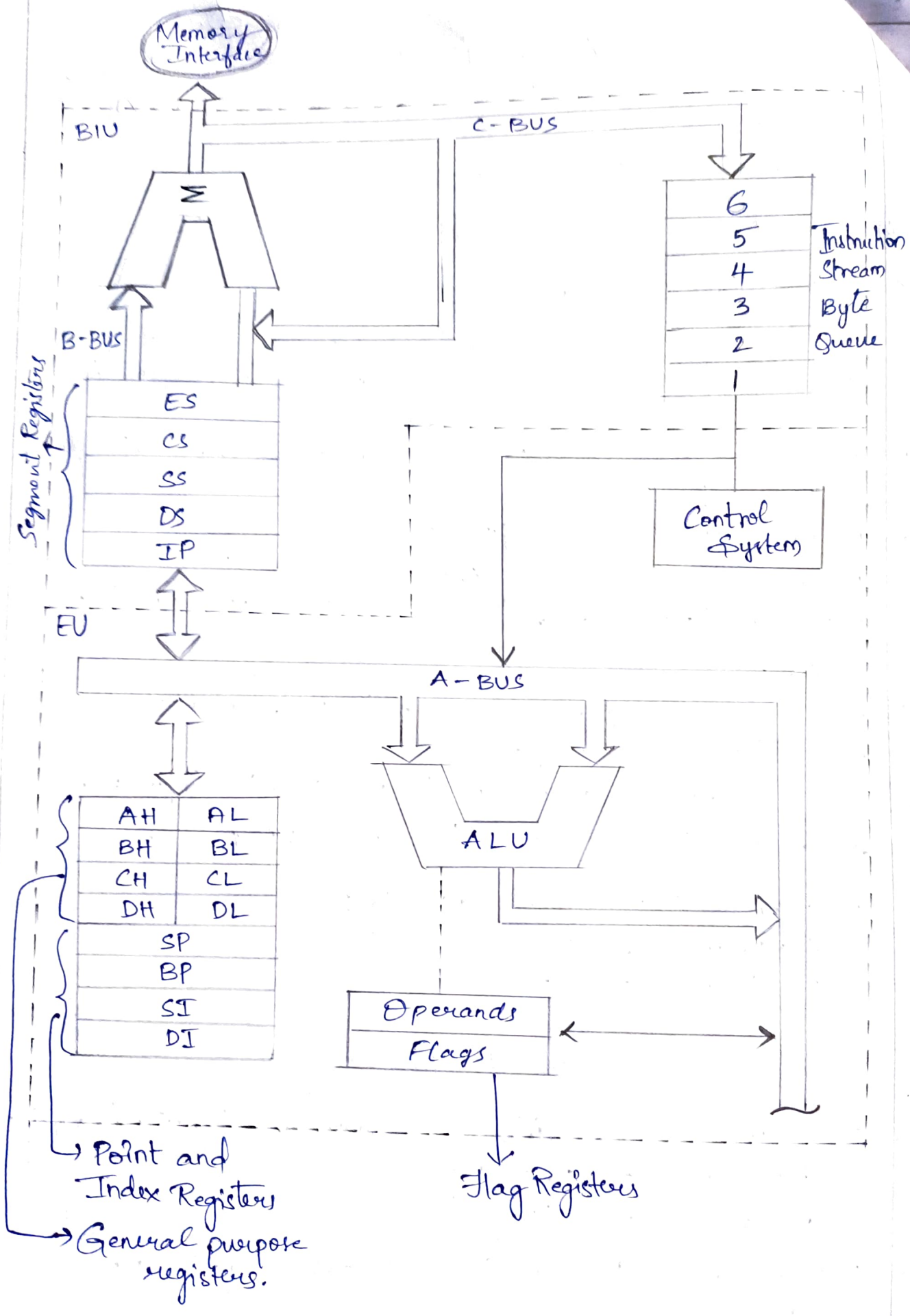
Ans: 8086 Microprocessor Architecture :-

* It is a 16 bit microprocessor
* It has a 16 bit data bus, so it can read data from or write data to memory and ports either 16 bit or 8 bit at a time.
* It has 20 bit address bus and can acess upto 2^{20} memory locations.
* It can support upto 64 KB I/O ports
* It provides 14, 16 bit registers
* It has multiplexed address & data bus AD_0-AD_{15} and A_{16}-A_{19}
* It requires single phase clock with 33% duty cycle to provide internal timing.
* Prefetches upto 6 instruction bytes (48 bits) from memory & queues them in order to speed up processing.
* It supports 2 modes of operation:
  (1) Maximum mode
  (2) Minimum mode.

Architecture of 8086 Microprocessor :-

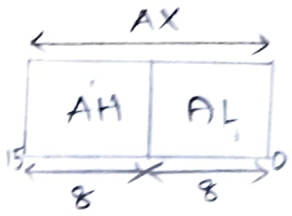
→ 8086 CPU is divided into 2 independent functional parts:
  1) Bus Interface Unit (BIU)
  2) Execution unit (EU)

→ Dividing work between these 2 units speeds up processing.


Memory Interface
BIU
C-BUS
Σ
B-BUS
6
5
4
3
2
1
Instruction Stream Byte Queue
Segment Registers
ES
CS
SS
DS
IP
Control System
EU
A-BUS
ALU
AH
AL
BH
BL
CH
CL
DH
DL
SP
BP
SI
DI
Operands
Flags
Point and Index Registers
General purpose registers.
Flag Registers

8086 Micro-processor has 4 types of Registers:-
(1) General purpose registers (AX, BX, CX, DX)
(2) Point and Index registers (SP, BP, SI, DI, IP)
(3) Flag Registers (conditional & control)
(4) Segment Registers (CS, SS, DS, ES)

⇒ General purpose Register: It stores 16 bit data, the valid registers face are AH, AL, BH, BL, CH, CL, DH, DL. It refers to the AX, BX, CX, DX respectively.



- AX Register: It is also known as accumulator register. It is used to store Operands.
- BX Register: It is used as a base register. It is used to store the starting base address.
- CX: It is referred to as counter. It is used in loop instruction to store the loop counter
- DX (Device I/O) :- This register used to hold I/O port address for I/O instructions.

⇒ Pointer and Index Register :-

- SP: It is a 16 bit register pointing to program stack in stack segment.
- BP: It is also 16 bit register pointing to data in stack segment.
- IP: It is a 16 bit register used to hold the address of next instruction.
- SI: It is a 16 bit register used for indexed base indexed & register indirect addressing as well as source data addresses in string manipulation instructions.

- DI : It is also 16 bit registers, DI used for Indexed, base Indexed and register indirect addressing as well as destination data addresses in string manupulation instruction.

Execution Instructions major function is :-
1) Decode the Instructions
2) Execute the Instructions.

* IP register which tests the next instruction
IP is in BIU why because instructions are fetches from memory to BIU.

⇒ Flag Register :- It is a 16 bit register which is works like a flip-flop.
In this 9 active flags and 7 unused flags. These flags are olivided into 2 parts.
(1) conditional flags
(2) control flags.

				Overflow	Direction	Interrupt	Trap	Sign	Zero		Auxillary		Parity		Carry Flag
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AX	U	PF	U	CY
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

* Conditional Flag:
- CF - This flag indicates an overflow condition for arthematic operations.
- AX - When an operation is performed by ALU it result in a carry / borrow from lower nibble and upper nibble (D_4-D_7) then the flag is set carry given by D_3 bit (or) D_4 bit. This flag works in BCD conversions.

- PF : This flag is used to indicate the parity of the result where the lower order 8 bits. The result contains even number of 1's then the parity flag is set.
  For odd no of 1's the flag is reset.
- ZF - The flag is set to 1 when the result when the result of the operation is negative it is set 1 arithematic or logical operation is 0 or else it is set to zero.
- SF - This flag holds the sign of the result when the result of the operation is negative it is set 1 or else it is 0
- OF - This flag represents the result when the system capacity is exceeded.

⇒ Control flags :-

1) Trap flag : It returns single step controls and allows the user to execute one instruction at a time for debugging.

2) IF : It is an Interrupt unable - disable flag. This flag is used to allow the insterruption of a program it is set to 1 for interrupt enable condition and set to zero for interrupt disable.

3) DF : It is used in string operation as the name suggest string bytes are accessed from higher memory address to the lower memory address and vice-versa.

BIU (Bus Interface Unit) :-

In this block 3 major components

(i) Instruction queue
(ii) Segment registers (CS, DS, SS, ES) with 1 Instruction pointer
(iii) Control unit

→ **Instruction queue:**

① BIU gets upto 6 bytes of instruction queue when EU executes instructions and is ready for next instruction then it simply reads the instructions from instructions queue.

② Fetching the next instruction while the current instruction executes is called pipelining.

* **Segment Registers:**

(1) Code Segment (CS): Size of this register is 16 bit register. It is used for addressing a memory location is code segment of the memory, where the executable prog is stored.

(2) Data Segment (DS): It consists of data used by the program. And it is accessed in the data segment by an offset addresses.

(3) Stack segment (SS): It handles memory to store data data and address during execution.

(4) Extra segment (ES): ES majorly additional to data segment which is used by the string to hold the extra destination data.

Control Unit :-

1) It controls that all operations within the processor BIU and EU
2) The control unit which has special register i.e, PC is a special register. It counts how many instructions in a program & it sends the instructions one by one.

40 pin diagram :-