PSW register is 8-bit register, also called flag register. These flags eindicate status of the current result. They are changed by the ALV after every arithmetric and logic operations. There flags can also be logic operations. There flags can also be changed by programmer. PSW is a bit-changed by programmer. PSW is a bit-addressable register. Fach bit can addressable register. Fach bit can be individually changed by the programmer. The 8-bits of PSW register are as follows:

PSW-7 PSW-6 PSW-5 PSW-4 PSW-3 PSW-2 PSW-1 PSW-0

CY AC FO RS1 RSO OVR — P

1) CY - CARRY FLAGT: (PSW.7)

2+ indicates the carry out of the MSB

(most significant bit) after any authoritic

operation.

out of MSB

2) AC - AUXILIARY CARRY FLAG: (PSW.6) 2+ indicates the carry from lower

nibble to higher nibble. In other words, it is carry from bit 3 to bit 4 (-- 654/3 2 1 -), Bito Bil 7 Higher hower nibble nibble If there is a carry from lower Nibble to higher nibble, AC = 1, otherwise AC flag = O. James OJA inside operations as a continue 4 0 0 0 0 0 0 0 0 0 0 0 ~0000,0000 mbin operation . Therefore ING TENET TO A The a carry afrom lower nibble Aux Carry flag higher nibble AC(=14129); MAIR YARAD - Y PARITY FLAG (P): PSW.O It, for checking the painty of the is determined by the number of 1's in the result. If number of 1's are odd, Parity flag = 1

: ODD Parity & 24 neumber of 1" in the

sesult is even, then Parity flag=0,
The result has even parity.

- 4) PSW-1 => 2+ is a user definable flag. It can be zero or one.
- 5) PSW-5 (FO) => 2+ is also user definable flag. Processor neither read-luis flag, nor it changes this flag. using the simple commands, it kan be made 0 or 1. for eg: = makes PSW.5 = 1 PSW.5 SET B

=> Makes PSW. 5 = 0 PSW.5 CLR

6) OVER FLOW FLAG (OVR): PSW.2

It indicates if there was on overflow during a signed operation. An S-bit signed number has the sange -80H.... OOH --- +7FH. Any result! out of this sange icauses an overflow.

If OVR = 1: There was an overflow in the sexult. If OVR = 0: There was no overflow in the result. overflow is determined by doing an

Fx-or between the 2nd last carry (6).

and the last carry (C7). After an overflow, the sign (MSB) of the secult overflow, the sign (MSB) of the secult becomes wrong.

Note: To renderstand this flag, we must know that what are signed 2 unsigned Number, only then

-> So let's learn, what are signed and censigned numbers first.

we can renderstand overflow event.