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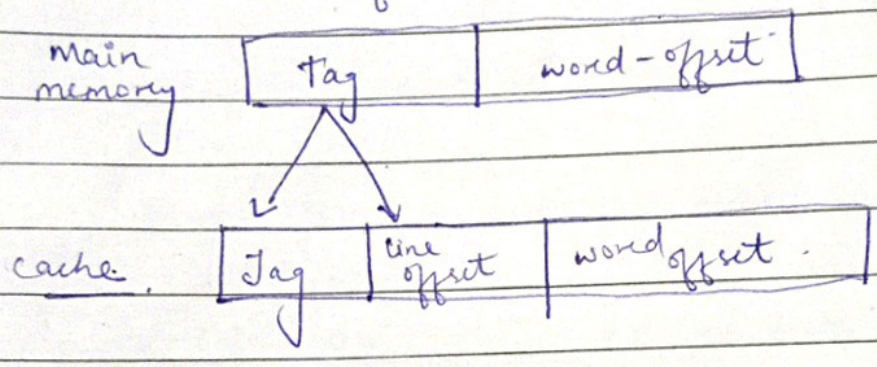
COA Assignment

Q1). The following are the different types of cache mapping mechanism :

1) Direct Mapping :

In direct mapping, each block of the main memory is mapped into one possible line with the location predefined.

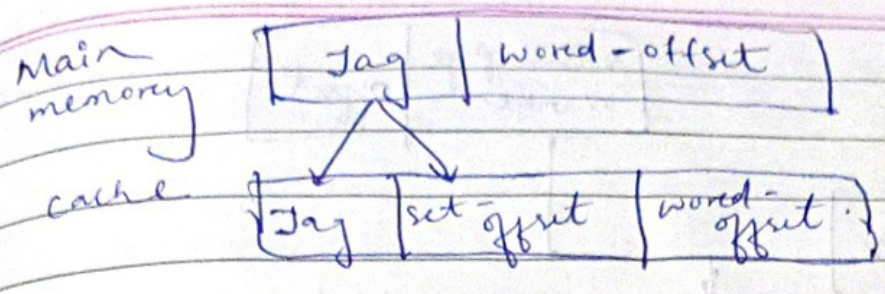


2) Associative Mapping :

In this type of mapping, the associative memory is used to store content & address of memory word. The location is not predefined hence can be stored anywhere.

3) SET- associative mapping :

This mapping combined the best of direct and associative mapping. It does this by saying that instead of having exactly one line that a block can map to in cache, then group a few lines together creating a set.
Then a block in memory can map to any one of the lines of a specific set.



Q2) (b) Assuming 32-bit address

1 word = 1 byte

Data cache = 128 kb

Block size = 32 words = 2^5.

Block offset = 5 bit.

4k memory block = 4 × 1024 = 4096.

∴ size of main memory = 4096 × 32 bytes.

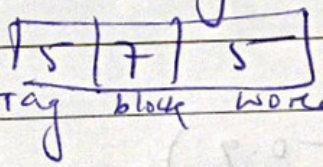
= 2^{17} bytes.

No of bits required in address field to access main memory = 17 bits.

(2) cache memory size

= 32 × 128 = 4096 bytes

(3) Direct mapping.

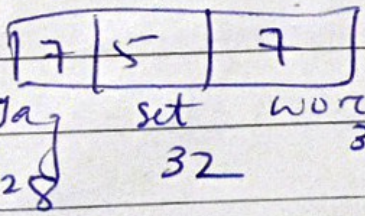


$32 = 2^5$

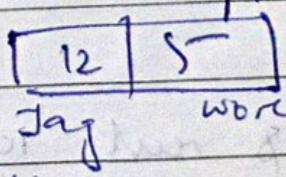
$128 = 2^7$

$2^5 = 32$

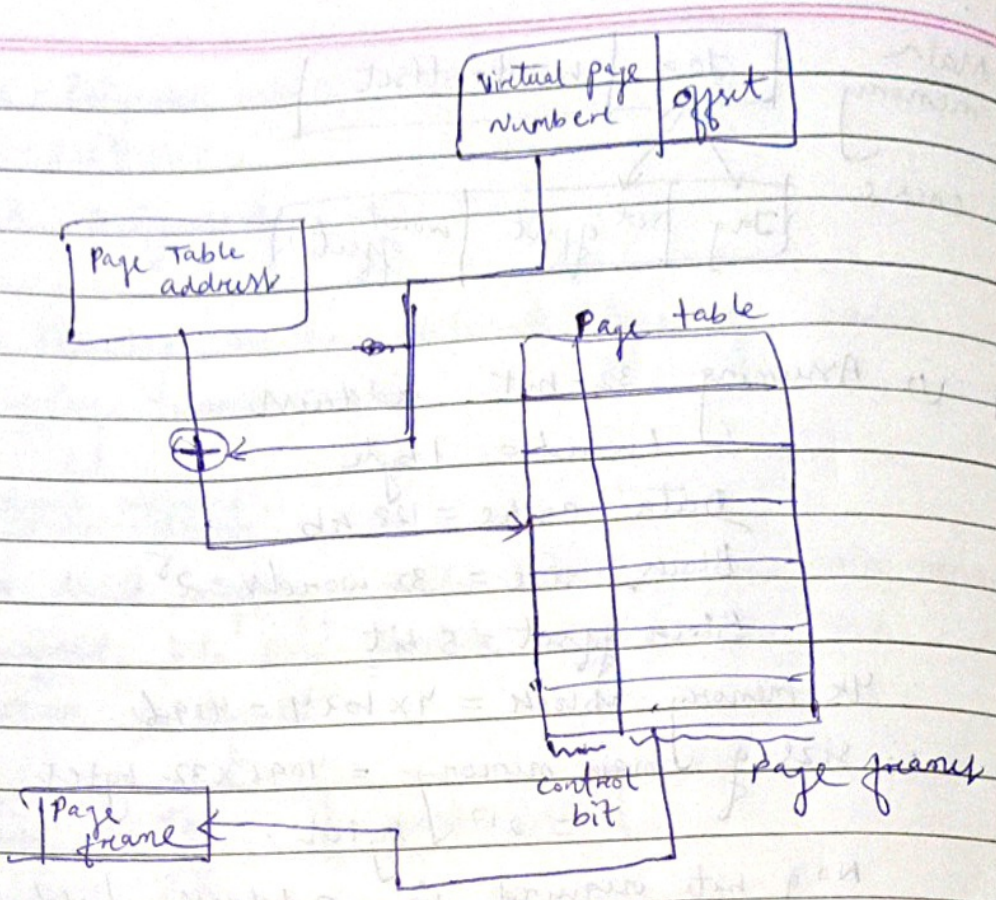
(4) set associative



(5) Associative mapping



(3)



Physical address in main memory.

(4) · Minimum refresh time

$a = w$

$it = cv \qquad t = \frac{cv}{i}$

$c = 30 \times 10^{-15} f$

$i = 0.25 \times 10^{-12} A$ ·

$$M.R.T = \frac{30 \times 10^{-15} \times (1.5 - 0.9)}{0.25 \times 10^{-12}}$$

$= 72$ ns.

(5) ·

Word size = 32 bits.

Cache base size = 512 bytes.

hit rate = 0.85

Accordingly,

1st word taken 30 ns & rest 10 ns.

$T_{avg} = h \times T_c + (1-h) \times [T_c + T_m]$

$= 0.85 + [(1-0.85)(3-(30 + (127 \times 10)]$

$= 198$ ns.

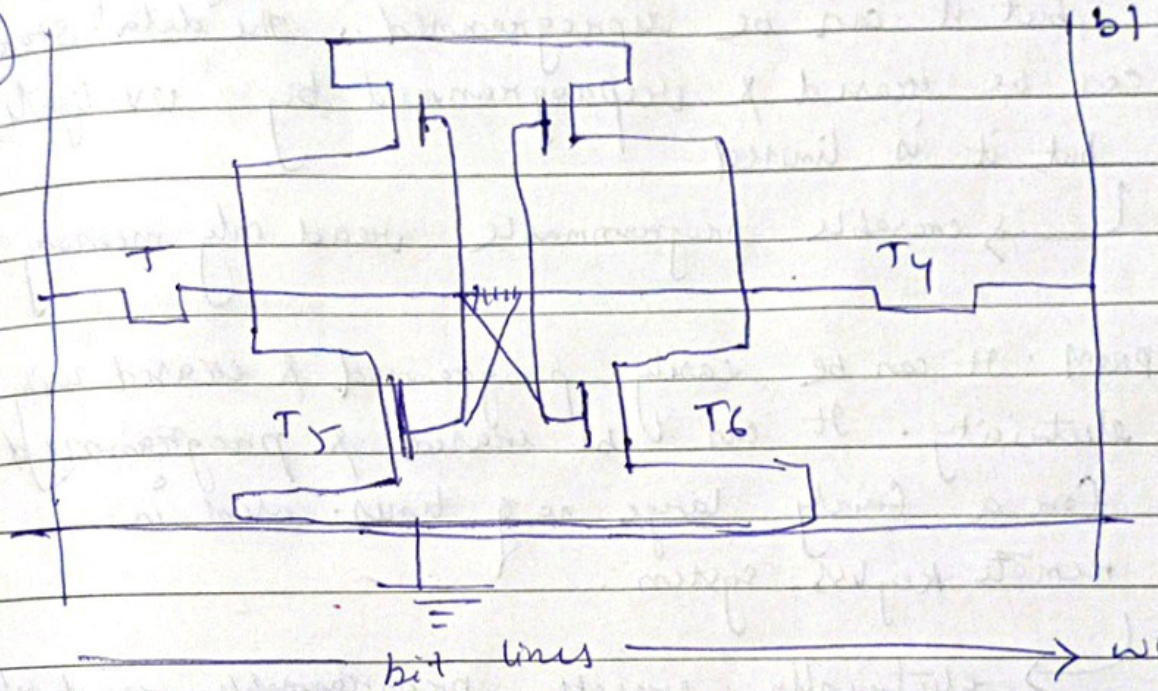
(6) Total time taken to perform refresh operation
$= 2^{14} \times 25$ ms
$= 409600$ ms $= 0.4096$ ms.

Refresh period = 3 ms.

∴ Time spent in refresh period in %
$= \frac{0.409600}{3} \times 100 = 13.66\%$.

Time spent in read/write = 100% − 13.66%
= 86.34%.

(7)



1 bit SRAM memory cell using 6T CMOS transistors.

(8) ROMs are of 4 types :-

1) MROM : The first ROM that consist of a grid of word lines & bit lines joined together transistor switches. It is physically encoded in the circuit & can only be programmed during fabrication. It was not so expensive.
↳ masked read only memory.

2) PROM: It is a kind of digital memory. Each bit is locked by a fuse or anti-fuse. The data is stored permanently & thus, cannot be changed or erased. It is used in low-level programs such as microcode.

↳ programmable read-only memory.

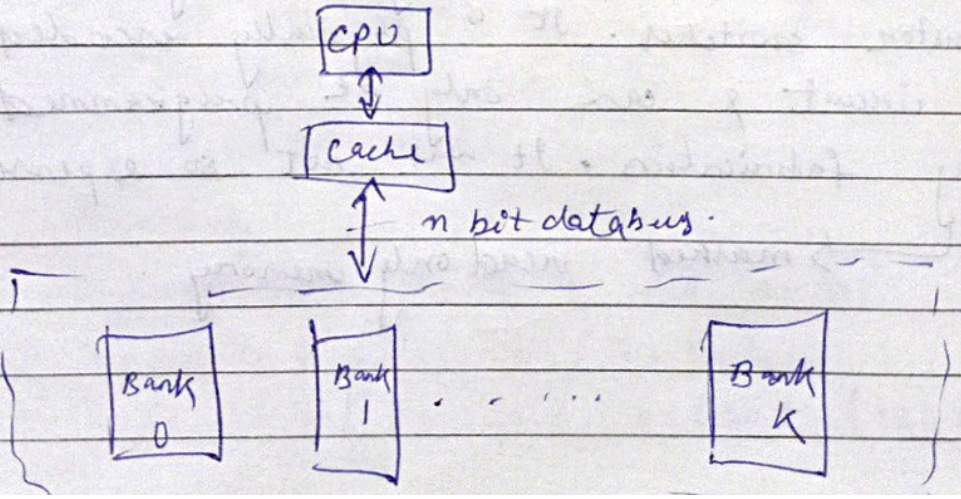
3) EPROM: EPROM also called EROM, is a type of PROM but it can be reprogrammed. The data stored can be erased & reprogrammed by UV lights, but it is limited.

↳ erasable programmable read only memory.

4) EEPROM: It can be easily programmed & erased using electricity. It can be erased & programmed for a fairly large no of times. used in remote keyless system.

↳ electrically erasable programmable read only memory.

(9) Memory interleaving is an abstraction technique which divides memory into a no of modules such that successive words in the address space are placed in different modules.



(10) (i) It is a region of memory, used to temporarily hold data which it is being moved from one place to another. Data is first stored in buffer then it gets copied to cache & main memory.

(ii) It is mostly used through softwares like compiler. It refers to the retrieving & storing data into the cache before the processor requires the data, thus this increases the speed of the process.

(iii) During prefetching, if cache is performing prefetching from main memory, it might not be able to listen to processor. So cache needs a different storage space to keep a count of the miss rates.