Assignment # 2
(Solution)

Problem 1:

Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

Solution:

Design procedure:

1. Derive the truth table that defines the required relationship between inputs and outputs.

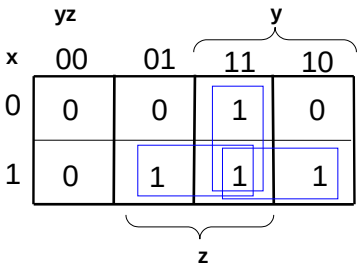
x	Y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

2. Obtain the simplified Boolean functions for each output as a function of the input variables.

Map for output A:

The simplified expression from the map is:

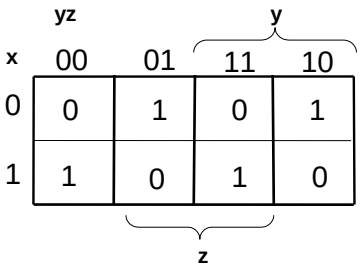
$A = xz + xy + yz$



Map for output B:

The simplified expression from the map is:

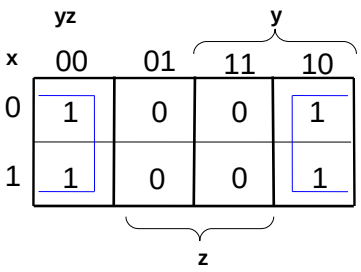
$B = x'y'z + x'yz' + xy'z' + xyz$



Map for output C:

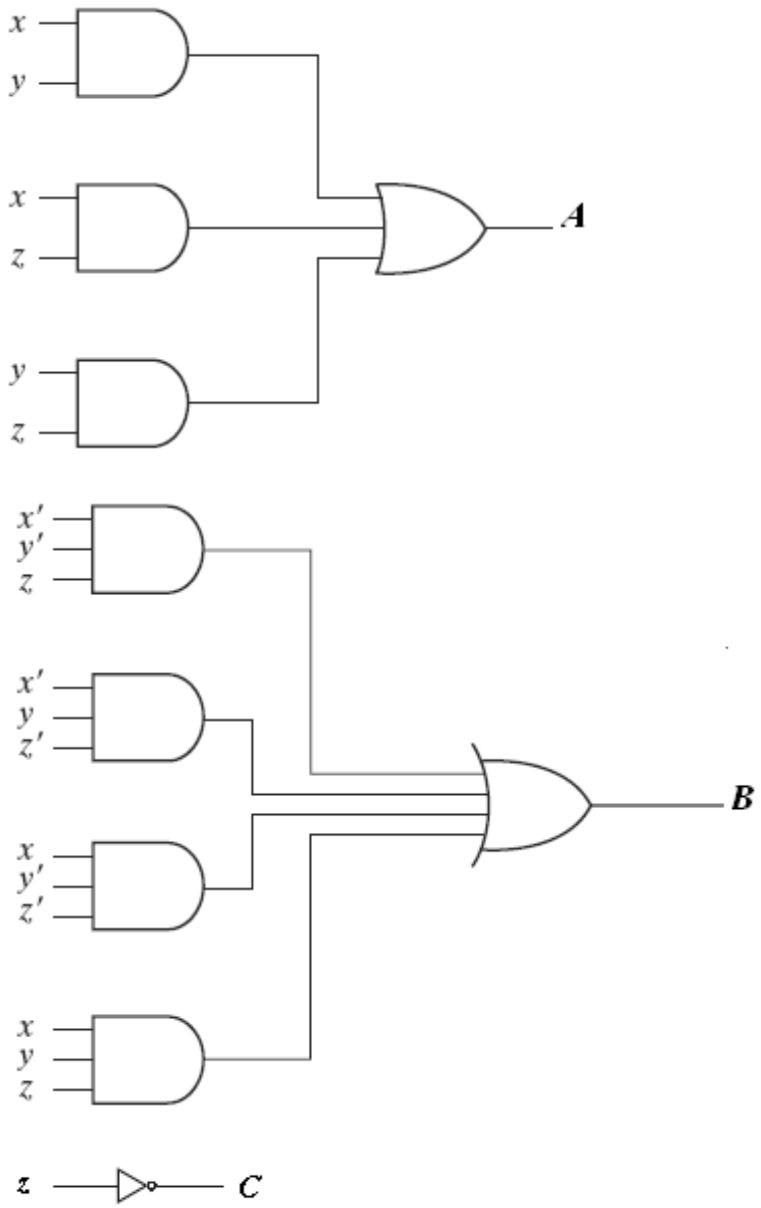
The simplified expression from the map is:

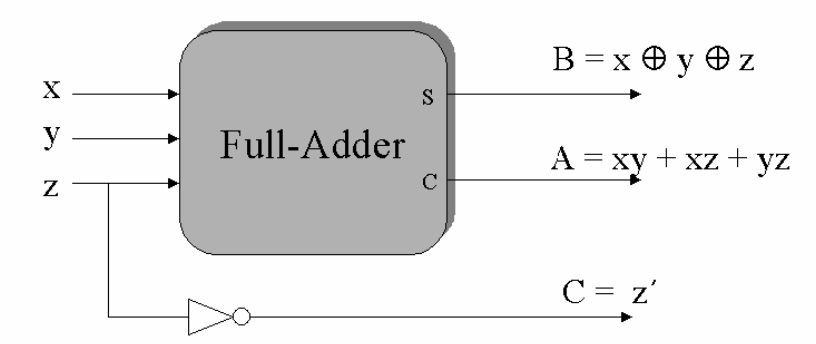
$C = z'$



3. Draw the logic diagram.

$A = xy + xz + yz$
$B = x'y'z + x'yz' + xy'z' + xyz$
$C = z'$





Problem 2:

Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable input.

Solution:

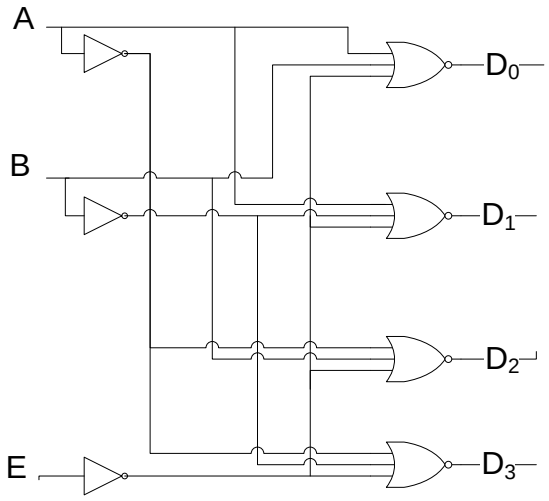
Design procedure:

1. The truth table for the circuit.

E	A	B	D_0	D_1	D_2	D_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

D_0= EA'B'=(E'+A+B)'
D_1= EA'B =(E'+A+B')'
D_2= EAB' =(E'+A'+B)'
D_3= EAB =(E'+A'+B')'

2. The logic diagram



Problem 3:

Implement a full adder with two 4 x 1 multiplexers.

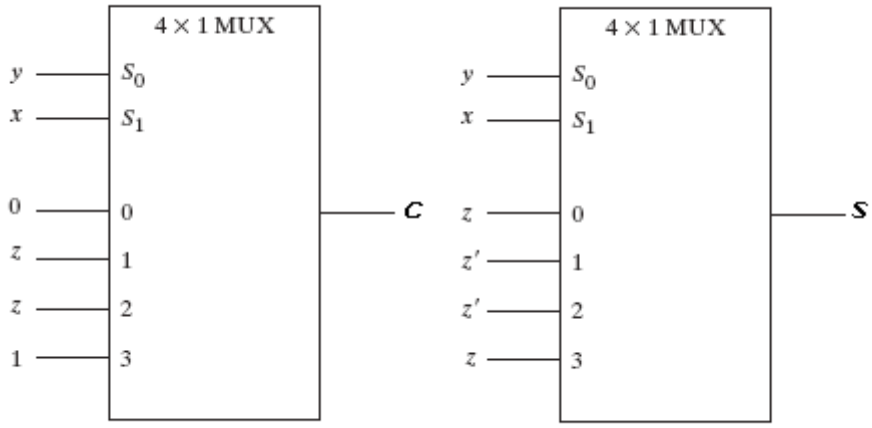
Solution:

Design procedure:

1. Derive the truth table that defines the required relationship between inputs and outputs.

X	Y	Z	C	C	S	S
0	0	0	0	C=0	0	S=Z
0	0	1	0		1	
0	1	0	0	C=Z	1	S=Z′
0	1	1	1		0	
1	0	0	0	C=Z	1	S=Z′
1	0	1	1		0	
1	1	0	1	C=1	0	S=Z
1	1	1	1		1	

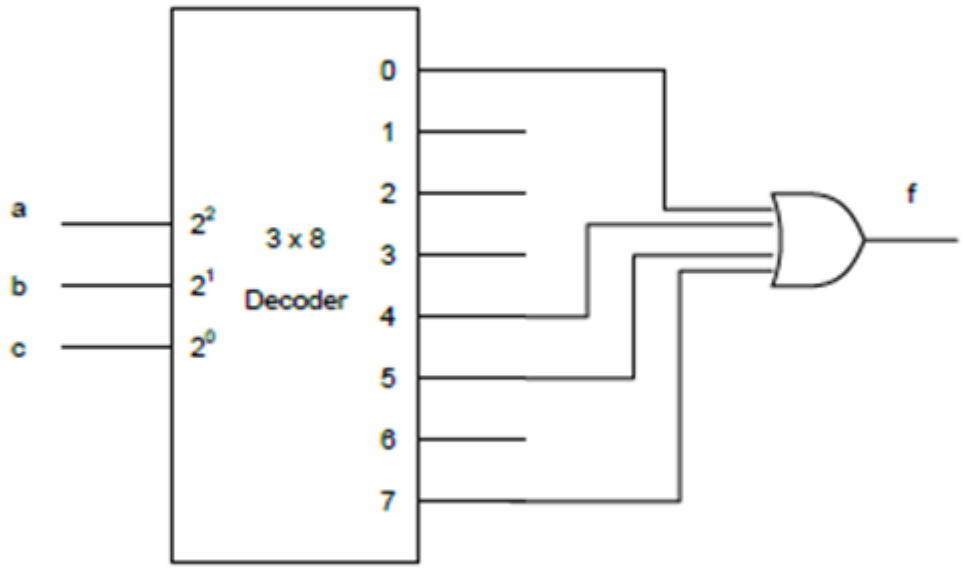
2. We connect the first two variables of the functions to the selection inputs of the multiplexer. The remaining single variable of the function is used for the data inputs.



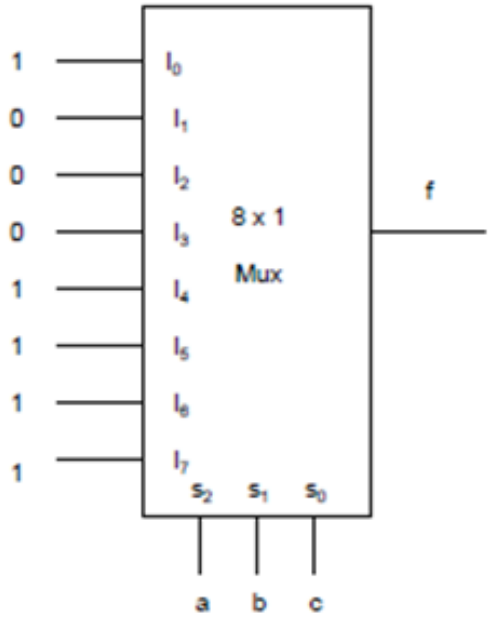
Problem 4:
Implement the truth table given below using

input			output
a	b	c	f
0	0	0	1
0	0	1	0
0	1	0	Don't care
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Don't care
1	1	1	1

a) A single 3-to-8 Decoder and any simple logic (e.g AND / OR / INV) .

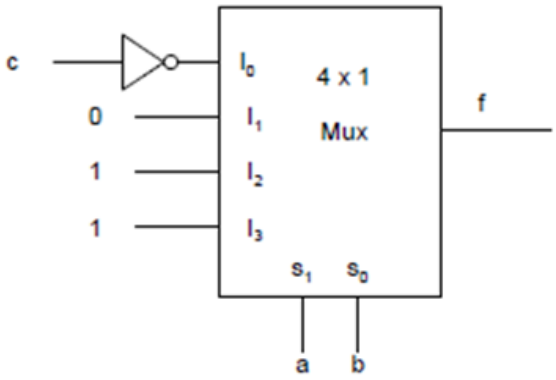


b) A single 8-to-1 Multiplexer and any simple logic (e.g AND / OR / INV) .

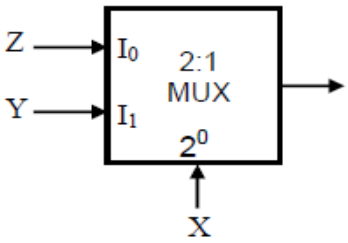


c) A single 4-to-1 Multiplexer and any simple logic (e.g AND / OR / INV) .

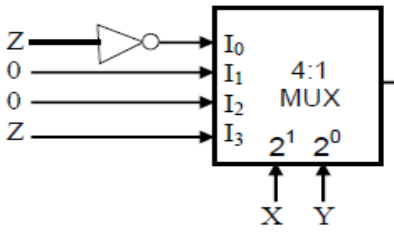
Inputs			Output
a	b	C	f
0	0	0	1
0	0	1	0
0	1	0	Don't care
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Don't care
1	1	1	1



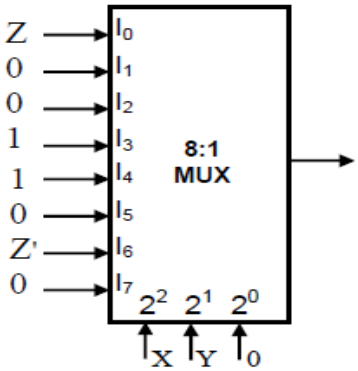
Problem 5:
Given the Boolean functions (F1,F2,F3,F4) . determine the Boolean expression of each one.



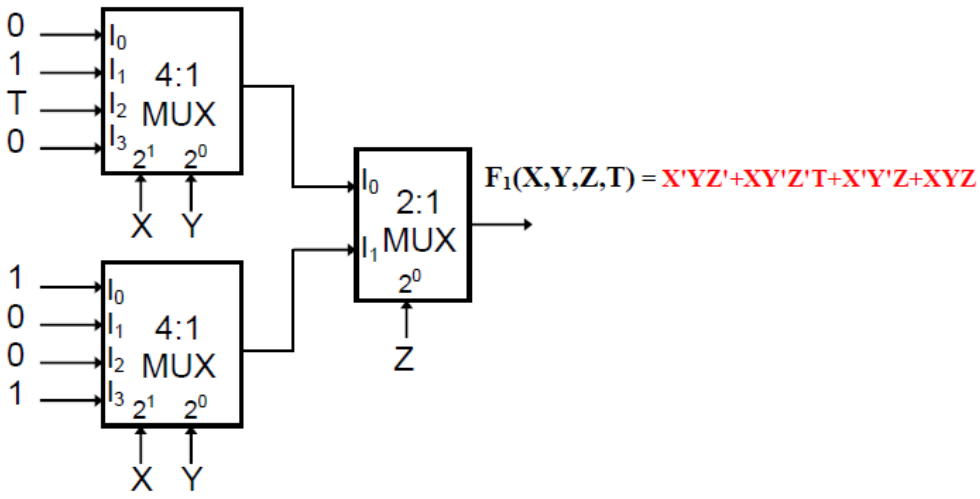
F1(X, Y, Z) = …**X'Z + XY**…



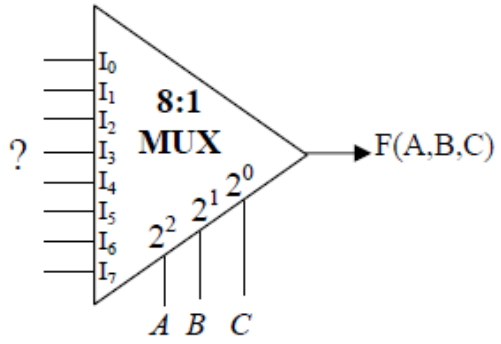
F2(X, Y, Z) = **X'Y'Z' + XYZ**…



F3(X, Y, Z) = ∑(1,4,5,6) …

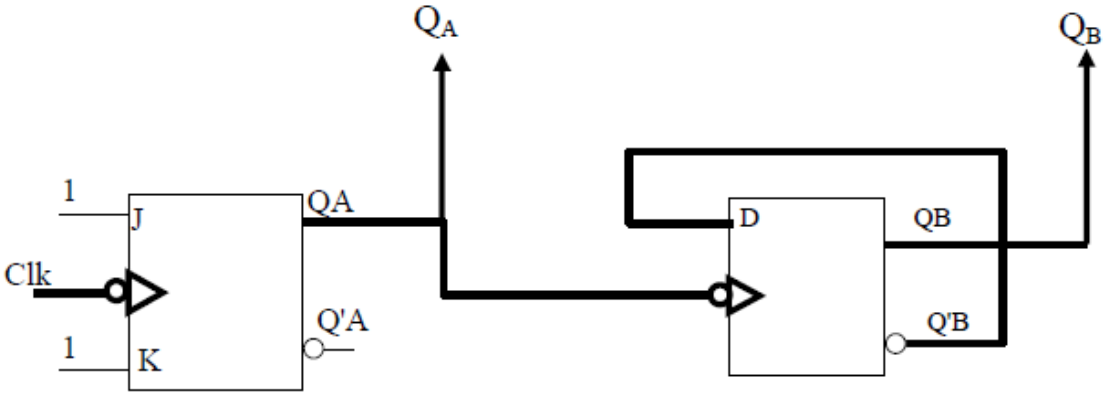


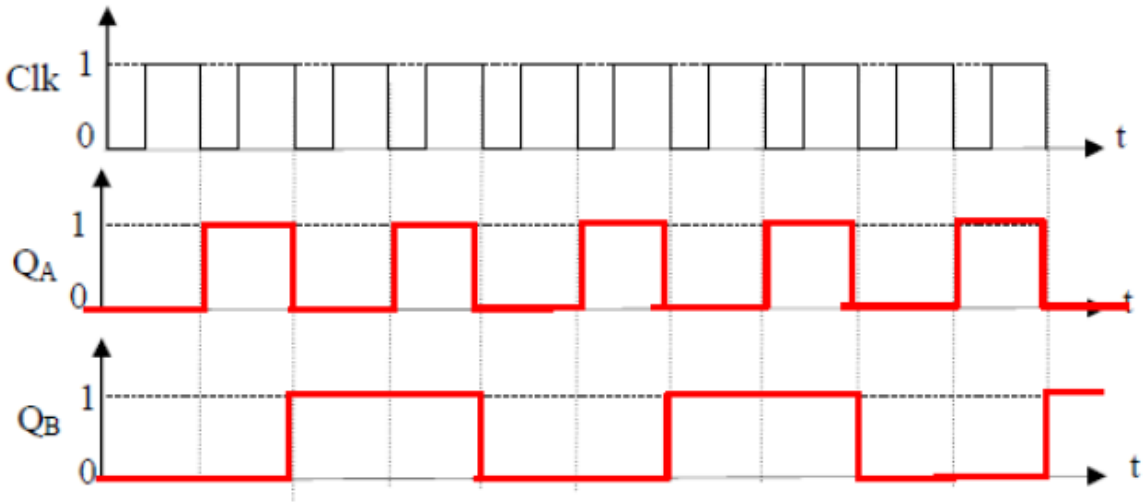
Problem 6:
Given the four-variable Boolean function
F(A,B,C,D) = AB'C+A'B'CD+A'BCD'+ABC.
What are the multiplexer's inputs (I0,…,I7) for the multiplexer ?



I0 = 0
I1 = D
I2 = 0
I3 = D'
I4 = 0
I5= 1
I6 = 0
I7 = 1

Problem 7:
A D flip-flop, and a JK flip-flop are connected as shown below .
Complete the timing diagram (note that Q_A and Q_B are initially low (0))





Problem 8:

1) Convert a T-FF to a JK-FF.

2) Convert a T-FF to a D-FF.

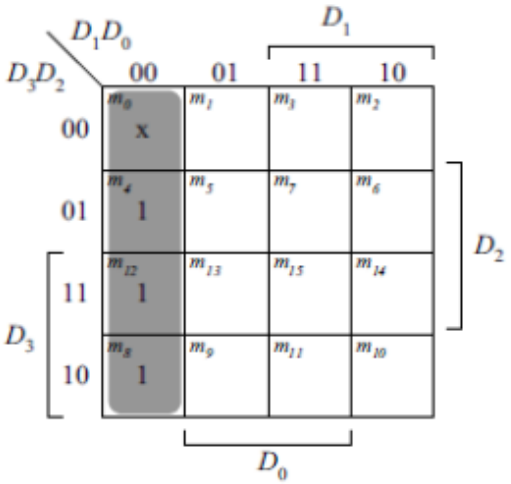
3) Convert a JK-FF to a D-FF.

4) Convert a JK-FF to a T-FF.

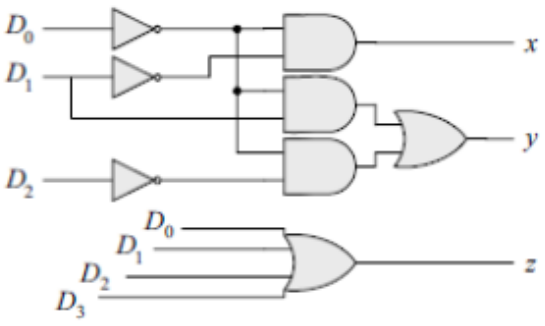
Problem 9:

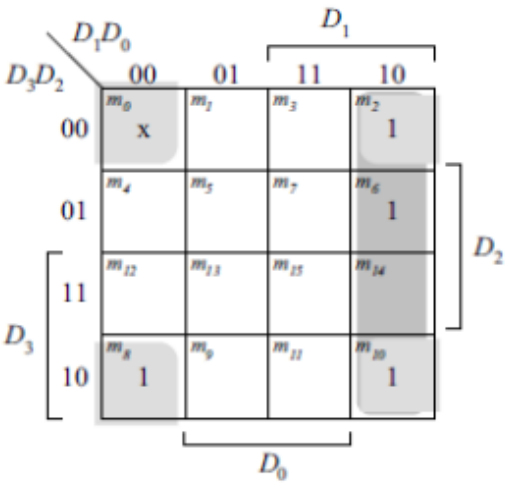
Design a four-input priority encoder , with input D 0 having the highest priority and input D 3 the lowest priority.

Inputs $D_3\ D_2\ D_1\ D_0$	Outputs $X\ Y\ Z$
0 0 0 0	x x 0
x x x 1	0 0 1
x x 1 0	0 1 1
x 1 0 0	1 0 1
1 0 0 0	1 1 1



$$v = D_0 + D_1 + D_2 + D_3$$





$$y = D'_0D_1 + D'_0D'_2$$

Problem 10:
Implement the function F= Σ(0,2,4,5,7,8,10,11,15) using MUX .

A	B	C	D	F	
0	0	0	0	1	F = D'
0	0	0	1	0	
0	0	1	0	1	F = D'
0	0	1	1	0	
0	1	0	0	1	F = 1
0	1	0	1	1	
0	1	1	0	0	F = D
0	1	1	1	1	
1	0	0	0	1	F = D'
1	0	0	1	0	
1	0	1	0	1	F = 1
1	0	1	1	1	
1	1	0	0	0	F = 0
1	1	0	1	0	
1	1	1	0	0	F = D
1	1	1	1	1