



Rishabh Srikrishnan Chitoor

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EDUCATION

- ◆ **University of Texas at Austin**
 - Incoming MSc + PhD student in ECE, Computer Architecture Track
- ◆ **Indian Institute of Technology Madras**
 - B.Tech in Electrical Engineering; GPA 8.51/10

Fall 2021 Intake

Expected Graduation: May '21

SCHOLASTIC ACHIEVEMENTS

- ◆ Did **Branch Change** from B.Tech Metallurgy to B.Tech Electrical in Sem 1 with a **GPA of 9.70**.
- ◆ Won **Gold Medal** for Zonal Excellence at SOF Mathematics Olympiad (IMO) 2015, *among 10,000 students*.
- ◆ Secured **Rank 1** in South India Region at Ahaguru Physics Challenge - 2015, *among 15,000 students*.
- ◆ **Ranked 4329 (General)** in JEE Advanced 2017 (of 175,000 applicants)
- ◆ **Ranked top 0.5% (General)** in JEE Mains 2017 (of 1.3 million applicants)

RESEARCH PROJECTS

- ◆ **Novel 4-stage Cache Coherence Protocol**, towards B.Tech Thesis | *Prof. Madhu Mutyam* *(Oct 2020 - Ongoing)*
 - The new Cache Coherence Protocol is designed to reduce the number of **write-backs** to LLC.
 - Built a **local Cache Coherence simulator** which supports MSI, MESI, MESIF, MOESI & the new Cache coherence protocol.
 - Current work - modelling and simulating the new 4-stage coherency protocol using **gem5 simulator**
 - Future goals - analyzing performance metrics for varied workloads, and benchmarking against the existing protocols.
- ◆ **Custom Soft Processor Core**, for the IITM 5G Radio Testbed Project | *Prof. Nitin Chandrachoodan* *(Sep 2020 - Ongoing)*
 - The "Physical Layer Controller" of the 5G Testbed gets data through **AXI Stream**, based on which it sends control information to the various modules of the **Physical Layer system**, such as modulation, error control coding, FFTs, etc.
 - The soft processor core is optimized resource and timing-wise to run this "**Physical Layer Controller**" of the 5G testbed.
 - Processor based on **RISC V ISA** | **AXI Stream interfaces** done using dedicated memory-mapped peripherals
 - Achieved substantially lesser resource utilization compared to Microblaze | [Link to detailed and most recent report](#)
 - Current work - improving the frequency of operation from the current value of **120MHz** and validating the processor
- ◆ **SHAKTI**, India's first indigenously designed & manufactured microprocessor | *Prof. Kamakoti V* *(Sep 2019 - Dec 2019)*
 - Built **Macro-Operation Fusion** feature in the Decode stage for the **RISC-V SHAKTI F Class Microprocessor** prototype.
 - Involved fusing RISC-V instructions in the front-end of the pipeline | reduced total dynamic instruction count by **0.6%**.
 - Examples of macro-fused instructions implemented include Load Effective Address, Wide Multiply/Divide, Load Upper Immediate, etc.
 - Coded in **Blue-Spec Verilog** | In an overall team size of 25, solely responsible for the Macro-Operation Fusion module.

TECHNICAL PROFESSIONAL EXPERIENCE

- ◆ Intern at Data Centre Group, **Xilinx, India** *(May 2020 - Jul 2020)*
 - Built a **power throttling algorithm** for the **Samsung U.2 SmartSSD**; controls the power by modifying bandwidth & frequency
 - Provided the insight to shift from SSD controlled throttling to **FPGA controlled throttling** for higher response speed.
 - 2 different project implementations for the dynamic power throttling requirement;
 - High-level approach; used Python, NVMe commands and BASH to dynamically adjust the SSD bandwidth.
 - Switch-level approach; built an **IP Module** to control the bandwidth at a packet level, coded entirely in RTL Verilog.
 - Improved the bandwidth **by 10x** and power throttling performance **by 3x** compared to the existing algorithm.
 - Module runs **at 250MHz** | Verified and validated at the synthesis level
- ◆ Intern at Data Centre Group, **Xilinx, India** *(May 2019 - Jul 2019)*
 - Built a Hardware Accelerator IP for **RAID6 Disk Storage System**, using RTL Verilog.
 - Also responsible for the **AXI Stream and AXI Lite** interfaces for data transfer to the RAID6 core.
 - Module runs at **maximum of 300MHz** | Additionally assisted with validation and configuration of the IP Module
- ◆ Intern at **Carizen Software Pvt. Ltd., Chennai** *(Jun 2018 - Jul 2018)*
 - **Teaching Assistant** to an Employee Training course on the Linux OS (**CentOS 7**), Linux terminal commands, Bash script, and computer networking.
 - Helped the trainees better grasp the concepts taught during the course through innovative and interactive exercises.

- ◆ **Designing a pipelined signed 8-bit Multiplier**, EE5311:Digital IC Design (Aug 2020 - Dec 2020)
 - Used Electric to design the layout, transistor level circuit and icon for the signed 8-bit Multiplier | Simulated using LTSpice
- ◆ **Implementation of a Cross-Core Covert Channel**, CS6330:Secure Processor Microarchitecture (Feb 2020 - May 2020)
 - Uses Flush+Reload in L1 Cache to establish a Cross-Core Covert Channel, achieving average bandwidth of **100 MB/s**.
 - https://github.com/rishabh-c-s/Cross_Core_Covert_Channel
- ◆ **Implementation of a 5-stage pipelined RISC-V processor**, EE2003:Computer Organization (Aug 2019 - Nov 2019)
 - Added Multiply operations from RV-32M ISA using a dedicated memory-mapped peripheral.
 - Processor includes error-handling | runs at **peak 250MHz** | <https://github.com/rishabh-c-s/RISC-V-Processor>
- ◆ **An Arcade of Video Games**, for a School Tech Innovation Exhibition (Jul 2016 - Dec 2016)
 - An integrated gaming platform which allows the user to play multiple games, won **Best High School Project**.
 - Coded in C++, utilized Object Oriented Programming, Dynamic Memory, Arrays and other programming concepts.
 - https://github.com/rishabh-c-s/gaming_arcade_LALABOTS

RELEVANT COURSEWORK AND LABS

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|--|---|
| ◆ Computer Architecture (G) | ◆ Mapping Signal Processing Algorithms to DSP Architectures (G) |
| ◆ Digital IC Design (G) | ◆ Digital Signal Processing |
| ◆ Secure Processor Microarchitecture & Lab (G) | ◆ Microprocessor Theory & Lab |
| ◆ Digital System Testing & Testable Design (G) | ◆ Computer Organization & Lab |
| ◆ GPU Programming (Ongoing) (G) | ◆ Parallel Programming using OpenMP (Ongoing) |

*G - Graduate Level Courses, level 5000 or higher

SKILLS

- ◆ **Programming languages (Advanced):** C, C++, Python, Verilog, Bluespec Verilog, BASH, CUDA, OpenMP
- ◆ **Programming languages (Intermediate):** JavaScript, MATLAB, GNU Octave, x86 Assembly Language
- ◆ **Tools:** Vivado, Vivado HLS, ISE, iVerilog, SpyGlass, LTSpice, Electric, Cachegrind, gem5, Autodesk

CO-CURRICULAR EXPERIENCES

- ◆ **Teaching Assistant**, EE2003:Computer Organization course, for Prof. Nitin Chandrachoodan (Aug 2020 - Dec 2020)
 - Classroom Responsibilities – Weekly sessions for review of material covered in lecture, assisting during lab sessions
 - Assignment Responsibilities – Making test benches, Grading the assignments, Addressing students' doubts
- ◆ **Social Volunteer at Avanti Fellows**, Pondicherry (Jul 2017 - May 2018)
 - Mentor for grade 11 and grade 12 under-privileged students in JNV Puducherry School, guiding them for IIT-JEE.
 - **30 students** cleared JEE Mains 2018 | **7 students** secured admissions in top 5 IITs, joined 2018 | Class strength: **40**

LEADERSHIP

- ◆ **Literary Secretary**, Saraswathi Hostel IIT Madras, 2019-20 term (Aug 2019 - Apr 2020)
 - **Elected** to the **hostel executive council** by an electorate of **400 students** to manage all hostel cultural activities.
 - Envisioned and built the Saraswathi Library from scratch, currently the biggest hostel library of IIT Madras
 - Supervised a budget of **Rs. 1 Lakh** over the academic year 2019-20.
- ◆ **Convener & Club Captain**, Oratory and Comedy Club, IIT Madras, 2019-20 term (Aug 2019 - Apr 2020)
 - Responsible for cultivating the Speaking Arts Cultural Community of IITM through workshops and competitions
 - Organized the Oratory & Comedy events at **Saarang 2020**, attracted total participation of **~300 students** in the events.
 - Lead the IIT Madras Oratory and Comedy Contingent in **"Inter-IIT Culturals 2019"** and other cultural festivals.

EXTRACURRICULAR ACHIEVEMENTS AND ACTIVITIES

- ◆ **Literary & Arts;**
 - **MVP Award**, LitSoc 2019-20, for accumulating the most points in cultural events as an individual among 8000+ students.
 - **Winner, Debate**, Festember, NIT Trichy 2019 (among 40 teams) | **Winner, Debate**, LitSoc 2018-19 (among 22 participants)
 - **3rd place, Improv Comedy**, Saarang 2020, India's biggest cultural festival (among ~50 teams)
 - **Best Director and Winning Drama**, Stage Play (Dramatics), LitSoc 2018-19, (among 15 participating hostel teams)
- ◆ **Sports;**
 - District-level Badminton player; **Winner, Chengalpattu District Badminton Tournament 2012**
 - Member of the **hostel football & hockey team** from 2018-20; **Champions, Dean's Trophy Football, 2020**
- ◆ **Music;**
 - Trained in Piano for **8 years** | **Winner**, the esteemed Sumukhi Rajasekharan Foundation Piano competition