EXPERIMENT NUMBER: 7

EXPERIMENT NAME: Construction and verification of Flip-Flops

AIM: Construct (i) SR Flip Flop
(ii) D Flip Flop
(iii) JK Flip Flop
(iv) T Flip Flop
using logic gates and verify them.

APPARATUS REQUIRED:

SL. NO.	COMPONENT	SPECIFICATION	QUANTITY
1.	NOR gate	IC 7402	1
2.	NOT gate	IC 7404	1
3.	AND gate	IC 7408	1
4.	IC trainer kit	-	1
5.	Connecting Wires	-	As required

THEORY:

Flip-flop is a basic storage element (memory cell) used to store data (information). A flip-flop can store a single bit of data. It is a bi-stable device and can be used as a multivibrator. A flip-flop has two outputs. Flip-flops and latches are fundamental building blocks of any sequential logic circuits. Flip-flops are used in counters, registers (RAM), sequence generators and any other sequential logic circuit.

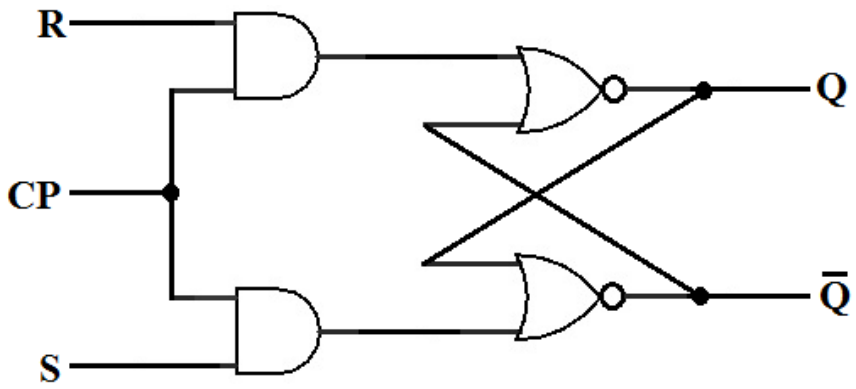
There are four types of flip-flops: (i) SR Flip Flop, (ii) D Flip Flop, (iii) JK Flip Flop and (iv) T Flip Flop. Flip-flops are edge-sensitive. Thus they change output as per the applied input only when the positive edge (for positive edge triggered flip-flops) or the negative edge (for negative edge triggered flip-flops) arrives. For the other parts of the clock pulse, the flip-flops remain insensitive to the inputs.

(i) SR FLIP-FLOP:

CHARACTERISTIC TABLE OF AN SR FLIP-FLOP:

Input			Output
Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

CIRCUIT DIAGRAM OF AN SR FLIP-FLOP:

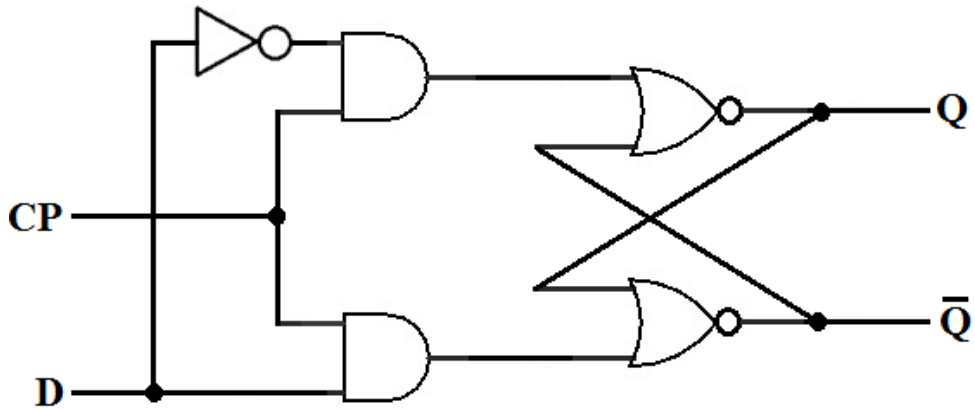


(ii) D FLIP-FLOP:

CHARACTERISTIC TABLE OF A D FLIP-FLOP:

Input		Output
Q_t	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

CIRCUIT DIAGRAM OF A D FLIP-FLOP:

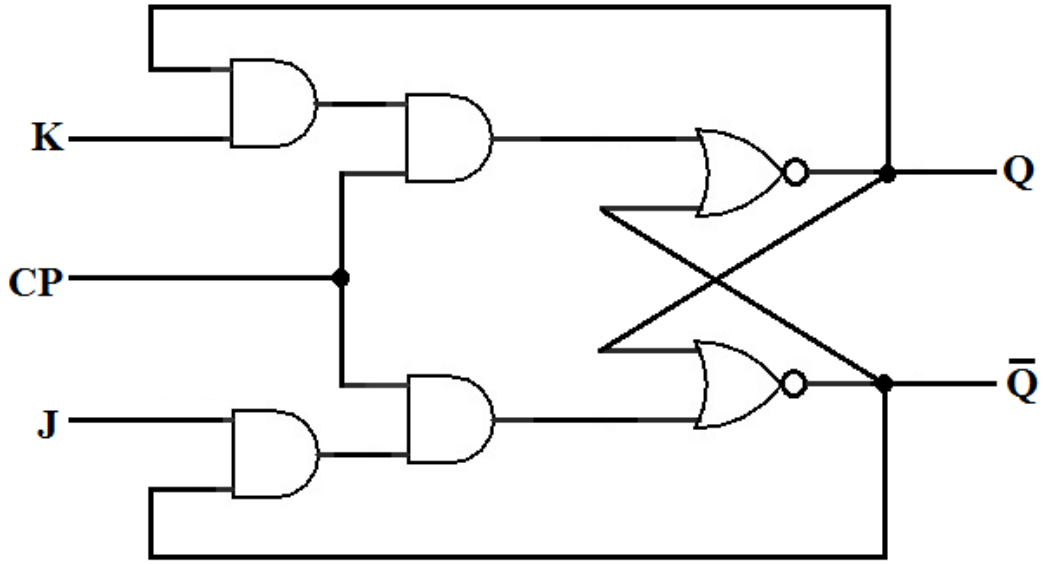


(iii) JK FLIP-FLOP:

CHARACTERISTIC TABLE OF A JK FLIP-FLOP:

Input			Output
Q_t	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

CIRCUIT DIAGRAM OF A JK FLIP-FLOP:

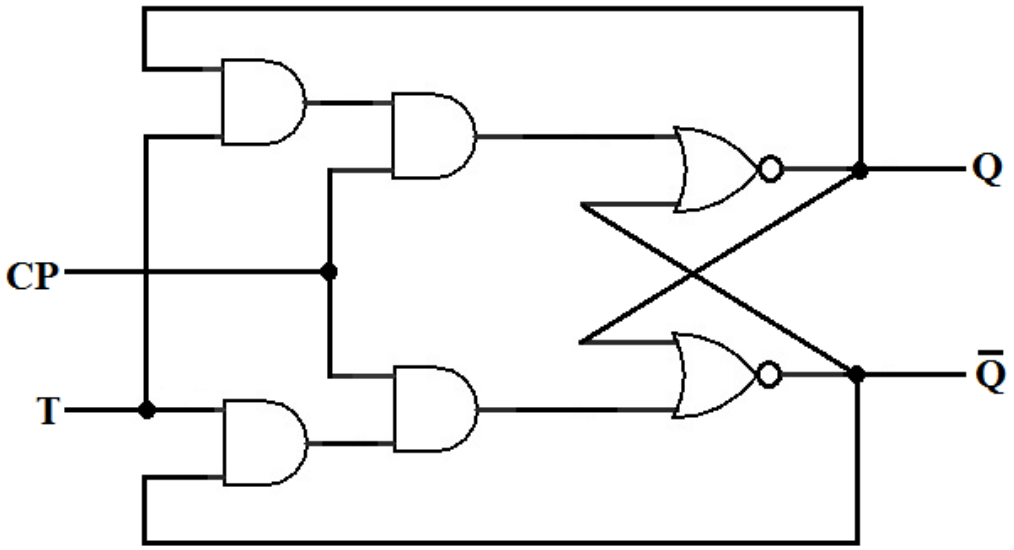


(iv) T FLIP-FLOP:

CHARACTERISTIC TABLE OF A T FLIP-FLOP:

Input		Output
Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0

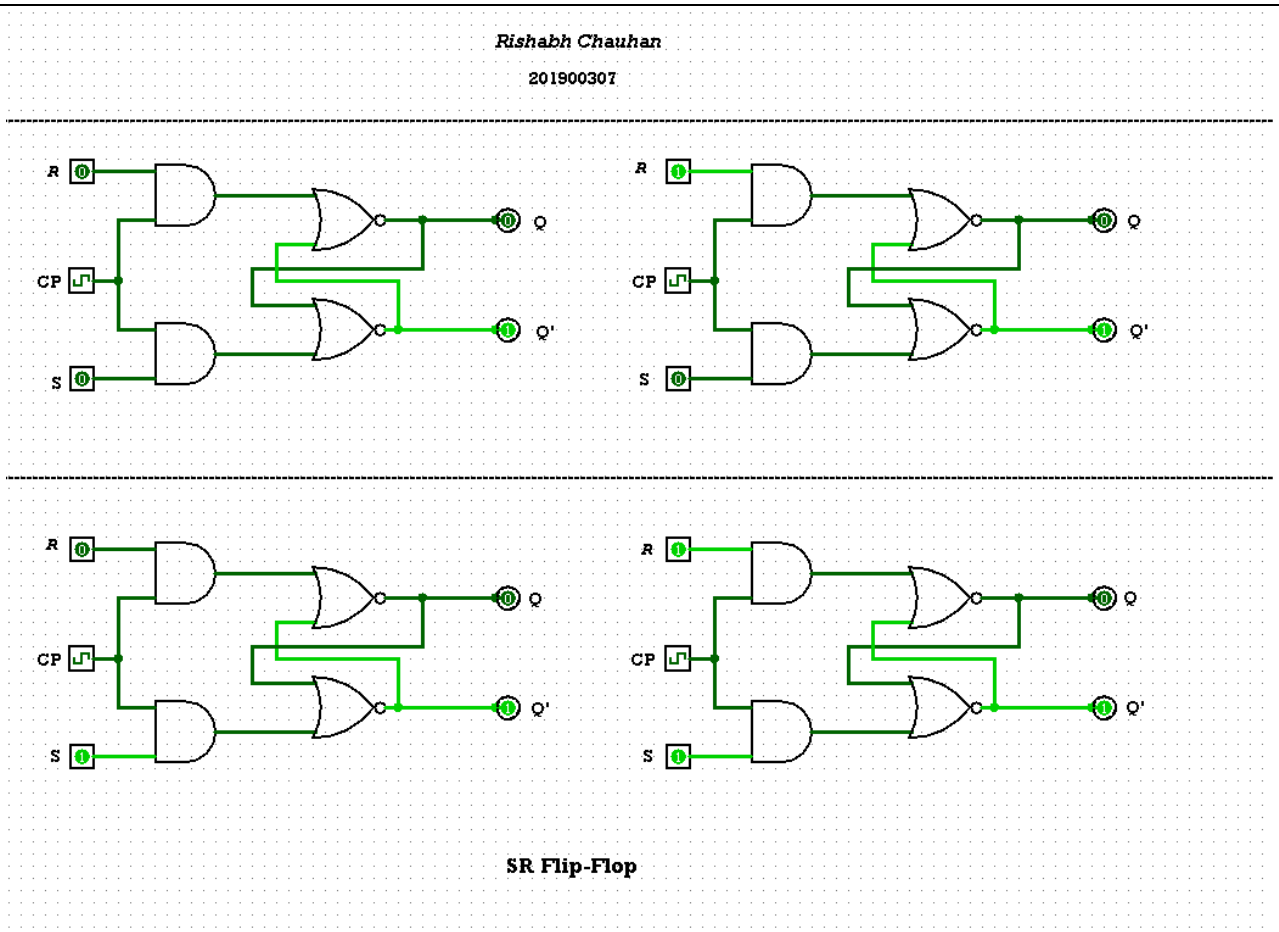
CIRCUIT DIAGRAM OF A T FLIP-FLOP:



PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the characteristic table of the circuits.

Student's worksheet-1



Student's observation and conclusion:

SR FLIP FLOP: **In SR flip flop, with the help of logic circuits when the power is Switched ON, the circuit keeps on changing. i.e. it is uncertain. It may come to Set (Q = 1) or Reset (Q' = 0) state (vice-versa).**

IN SR FLIP FLOP S MEANS SET AND R MEANS RESET.IT STORS DATA 0 OR 1. IN THIS OUTPUT IS INTERMEDIATE.

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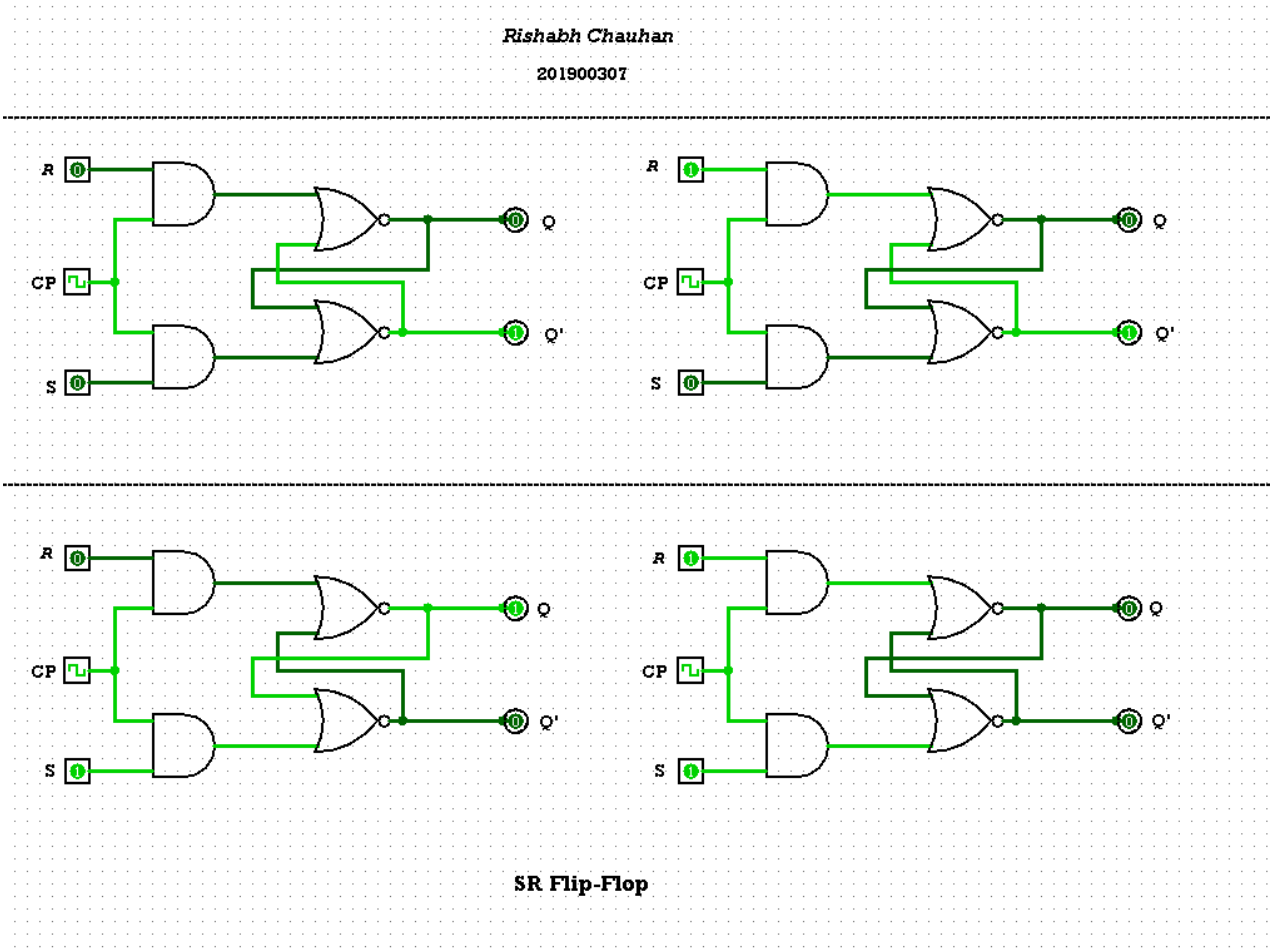
Date: 22/09/2020

Student's worksheet-2



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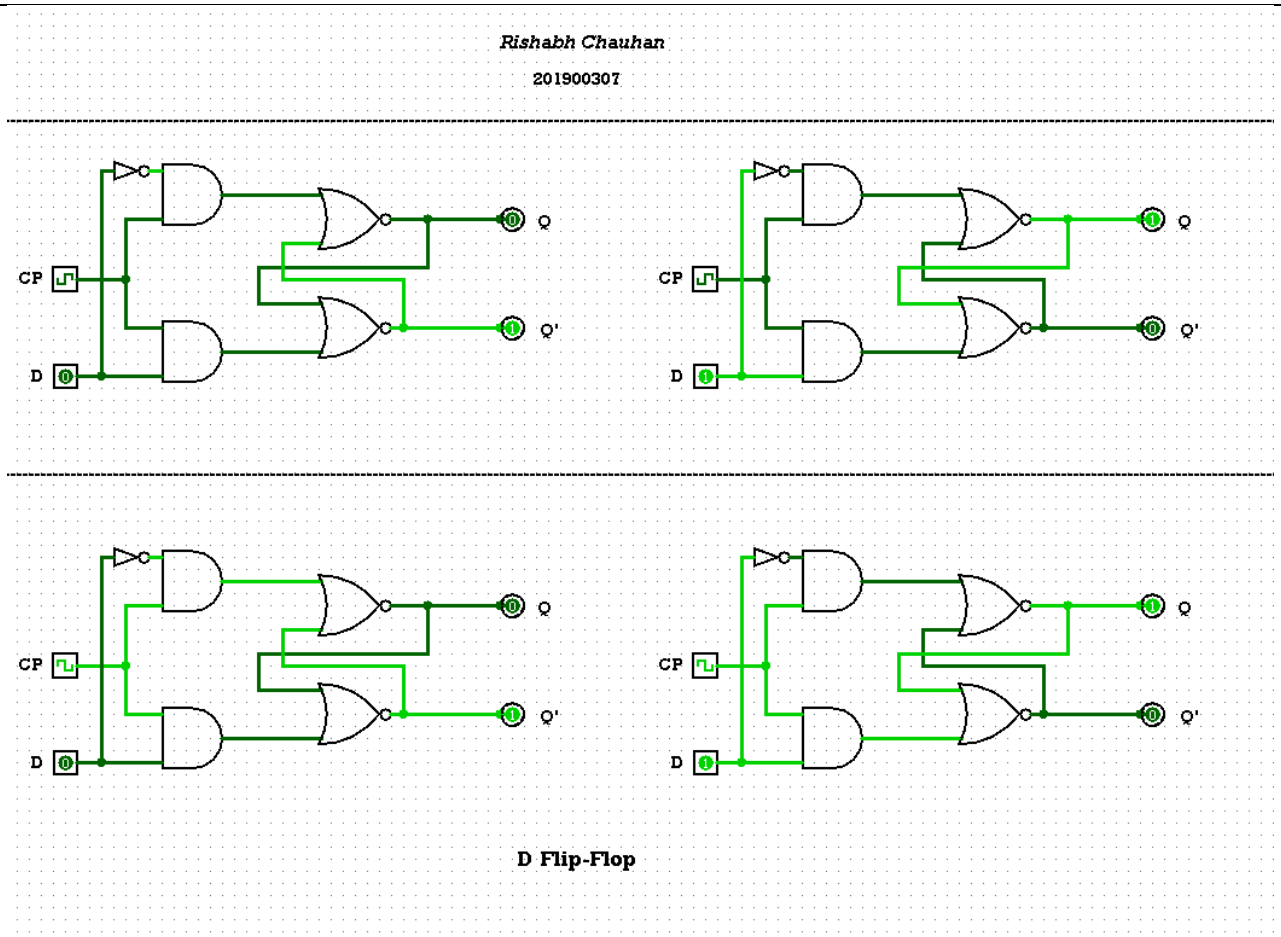
Student's worksheet-3



Student's observation and conclusion:

D FLIP FLOP: **The output changes state by signals applied to one or more control inputs. The basic here D Flip flop has a D input and a clock input and outputs Q and Q'. this means that the flip flop changes output value only when the clock is at a positive edge. There is also a negative edge triggered flip flop, which changes on a negative clock edge.**

IN D FLIP FLOP IT IS CONCLUDED THAT THE INPUT D IS ONLY COPIED TO THE OUTPUT Q.

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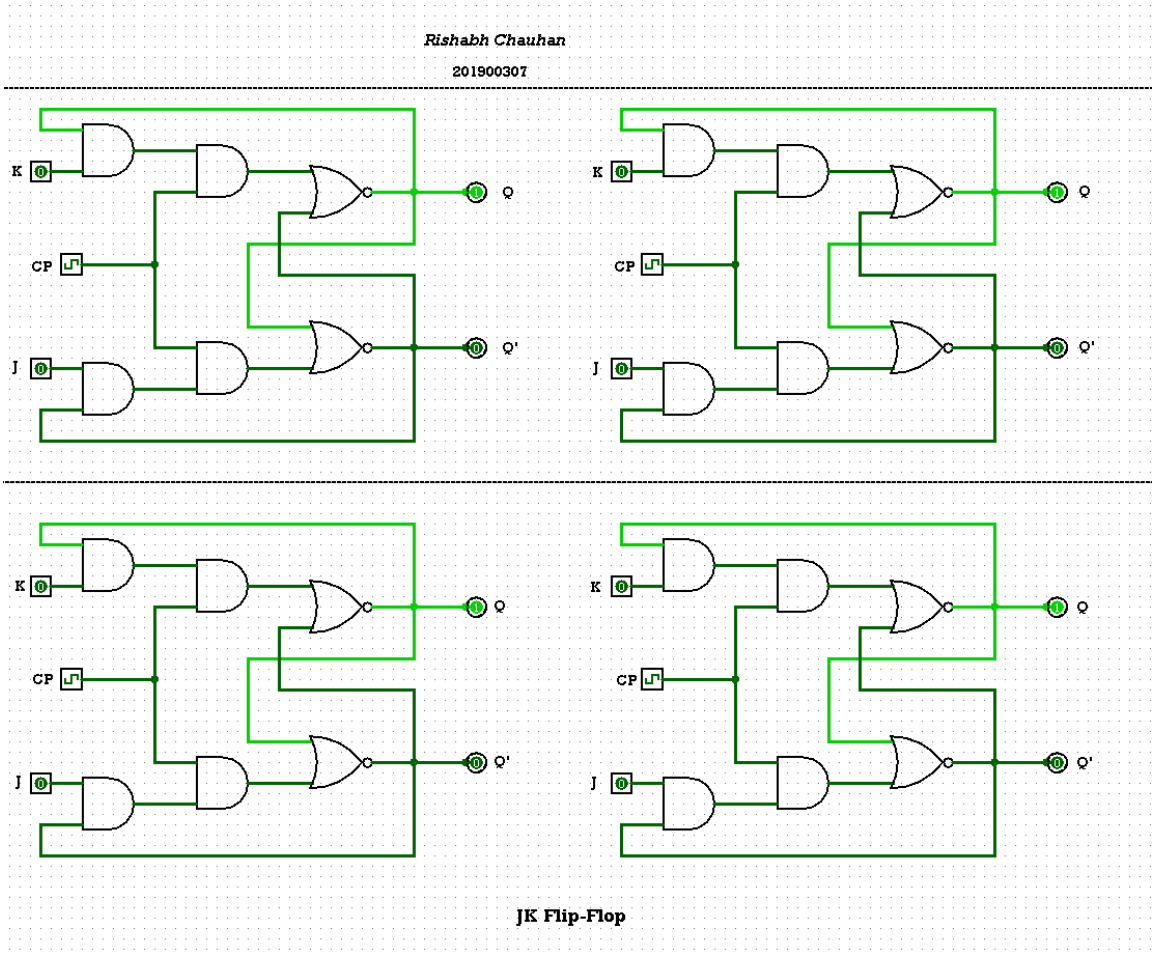
Student's worksheet-4



Student's observation and conclusion:

JK FLIP FLOP: **When J and K both are set to 1, the inputs remains high for some period, then the output keeps on toggling. Toggle means switching in the output instantly i.e. Q = 0, Q' = 1 will immediately change to Q = 1 and Q' = 0 and this keeps on changing continuously. And, in the rest of the conditions as shown in the above logic circuits.**

IN JK FLIP FLOP HAS TWO SATBLE STATE IN WHICH IT STORES DATA EITHER 0 OR 1 ITS OPERATION IS AS SAME AS THE S-R FLIP FLOP WITH SET AND RESET INPUTS. BUT THEIR WILL BE NO INTERMEDIATE OUTPUT ON J=1 AND K=1.

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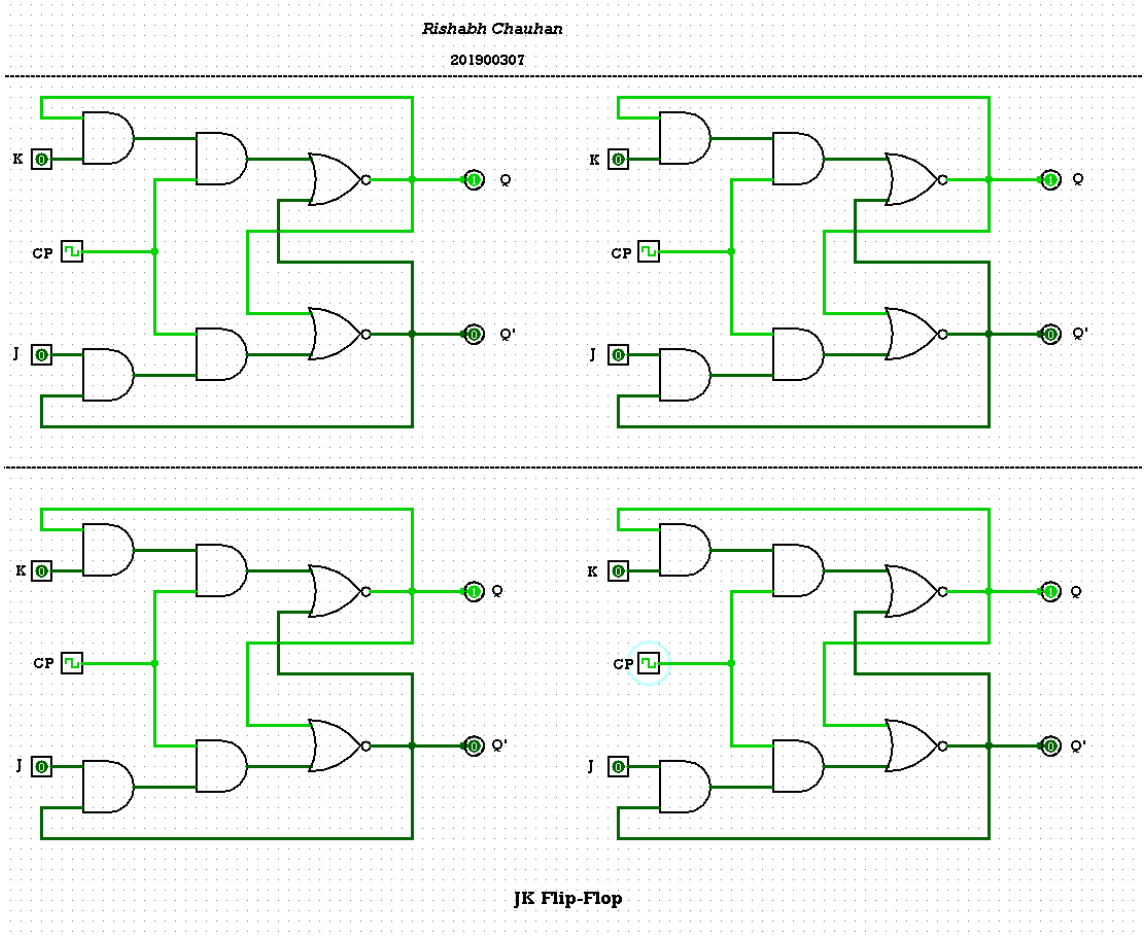
Student's worksheet-5



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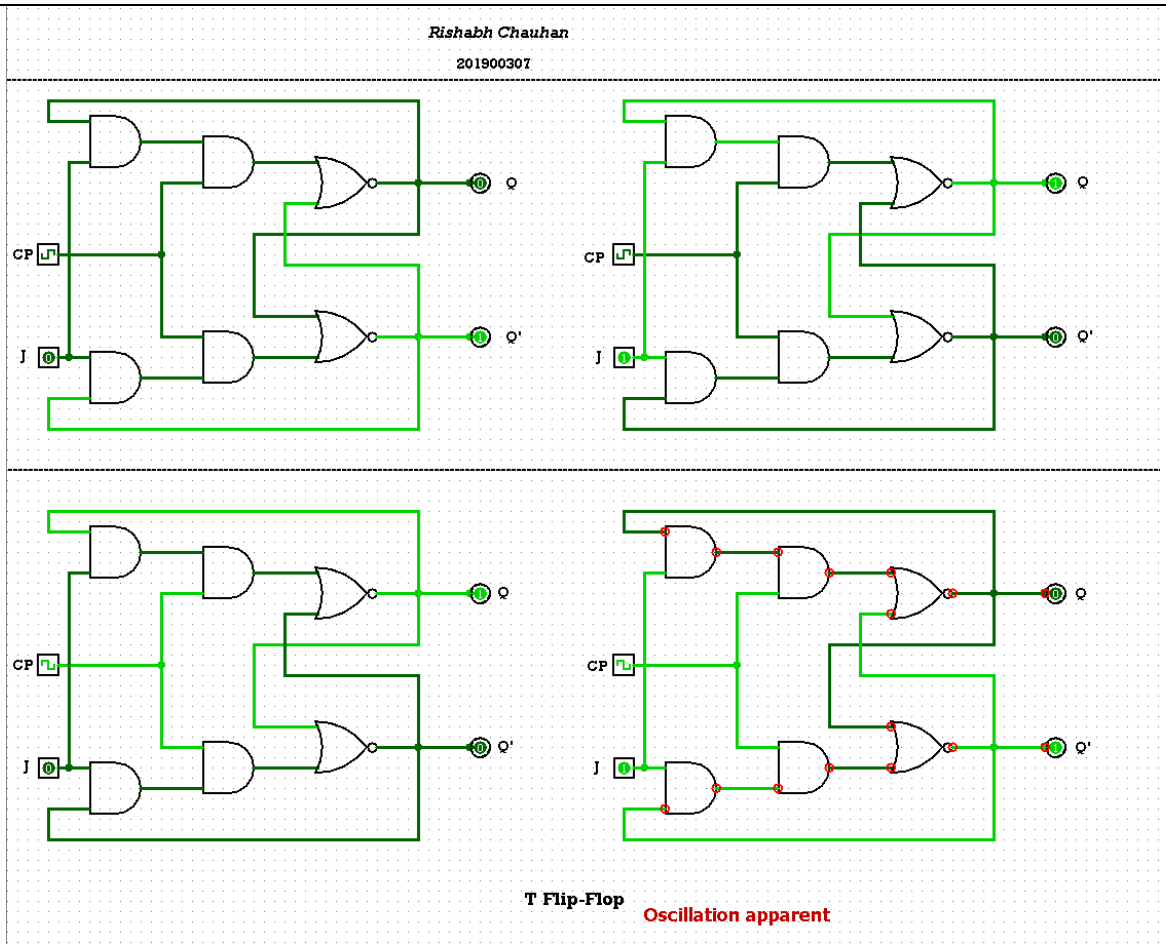
Student's worksheet-6



Student's observation and conclusion:

T FLIP FLOP: **In T Flip Flop, the upper gate is enabled, and the lower NAND gate is disabled. When the output Q is set to 0. The upper NAND gate is disabled, and the lower NAND gate is enabled when the output Q is set to 1.**

IN T FLIP FLOP, T STANTS FOR TOGGLE. IT IS CONSIDERED THAT OUTPUT Q VALUE BECOMES OPPOSITE TO INPUT T.

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