EXPERIMENT NUMBER: 9

EXPERIMENT NAME: Design of a mod 16 asynchronous down counter

AIM: Design a mod 16 asynchronous down counter.

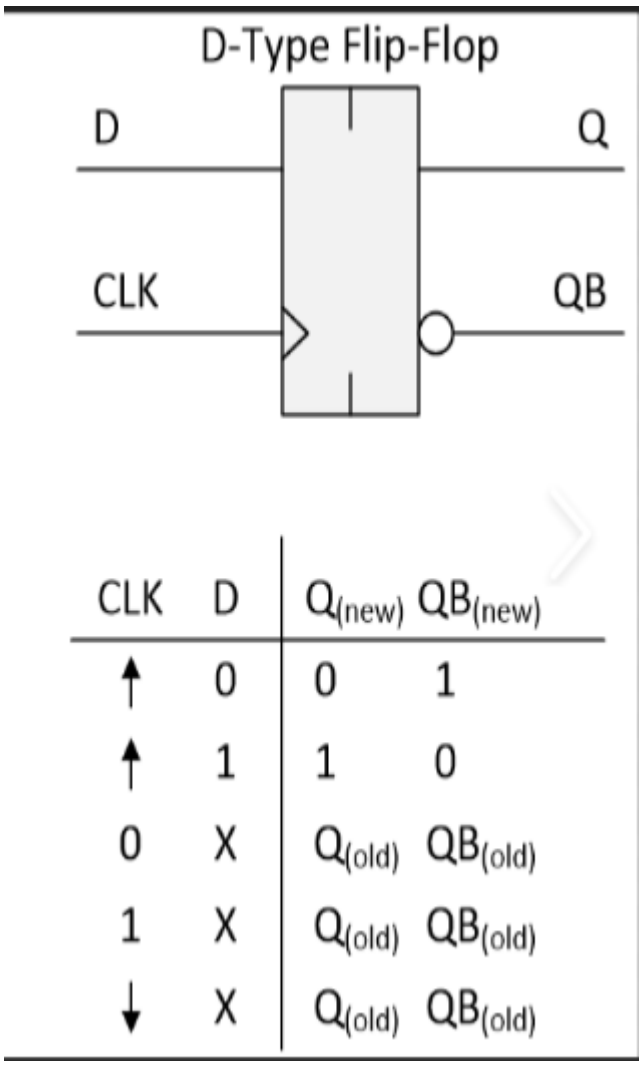
APPARATUS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	D Flip-flop	IC 7473/IC 7476	2
2.	IC TRAINER KIT	-	1
3.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

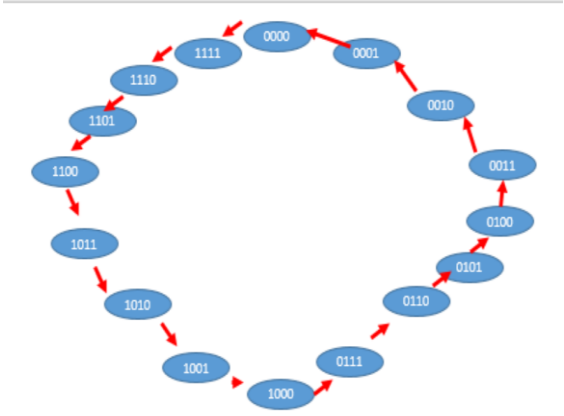
A *4-bit down counter* is a digital counter circuit, which provides a binary countdown from binary 1111 to 0000. This circuit uses four D-type flip-flops, which are *positive edge triggered*. At each stage, the flip-flop feeds its inverted output (/Q) back into its own data input (D). However, it feeds its non-inverted output (Q) to the clock input (CK) of the following stage. This type of circuit operates in an *asynchronous* (ripple) manner because the flip-flop stages do not rely on a common clock pulse for timing. The operational speed of the counter depends upon the *signal propagation* through successive stages, rather than a common clock pulse as in synchronous circuits.

When RESET is applied on all the flip-flops simultaneously, their Q outputs become logic 0 state, and /Q outputs becomes logic 1 state. The /Q outputs are fed back into their own data inputs (D) and therefore all that they require is the rising edge of a clock pulse to transfer the data at input (D) to output Q.

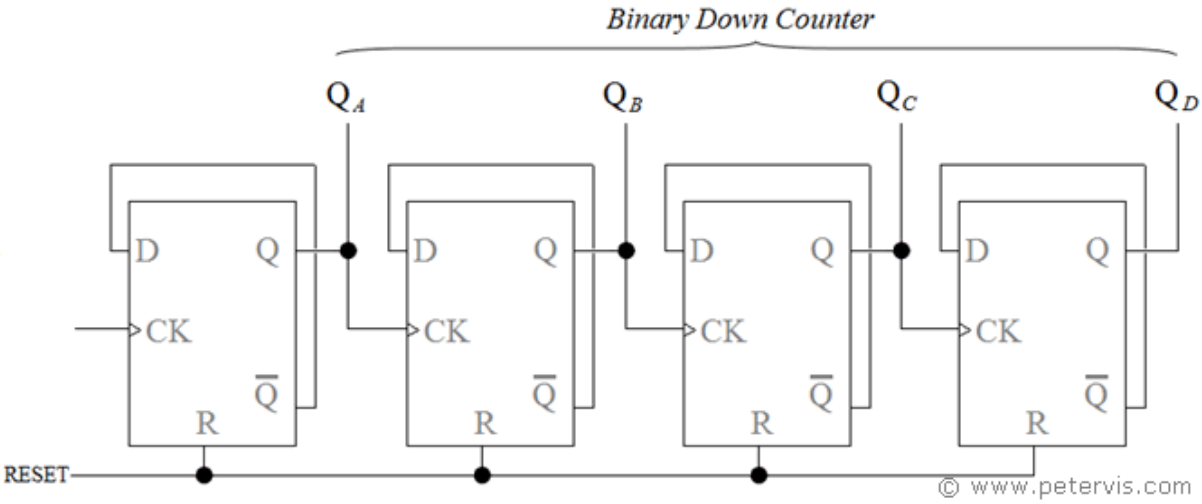


CLK	D	$Q_{(new)}$	$QB_{(new)}$
↑	0	0	1
↑	1	1	0
0	X	$Q_{(old)}$	$QB_{(old)}$
1	X	$Q_{(old)}$	$QB_{(old)}$
↓	X	$Q_{(old)}$	$QB_{(old)}$

STATE DIAGRAM:



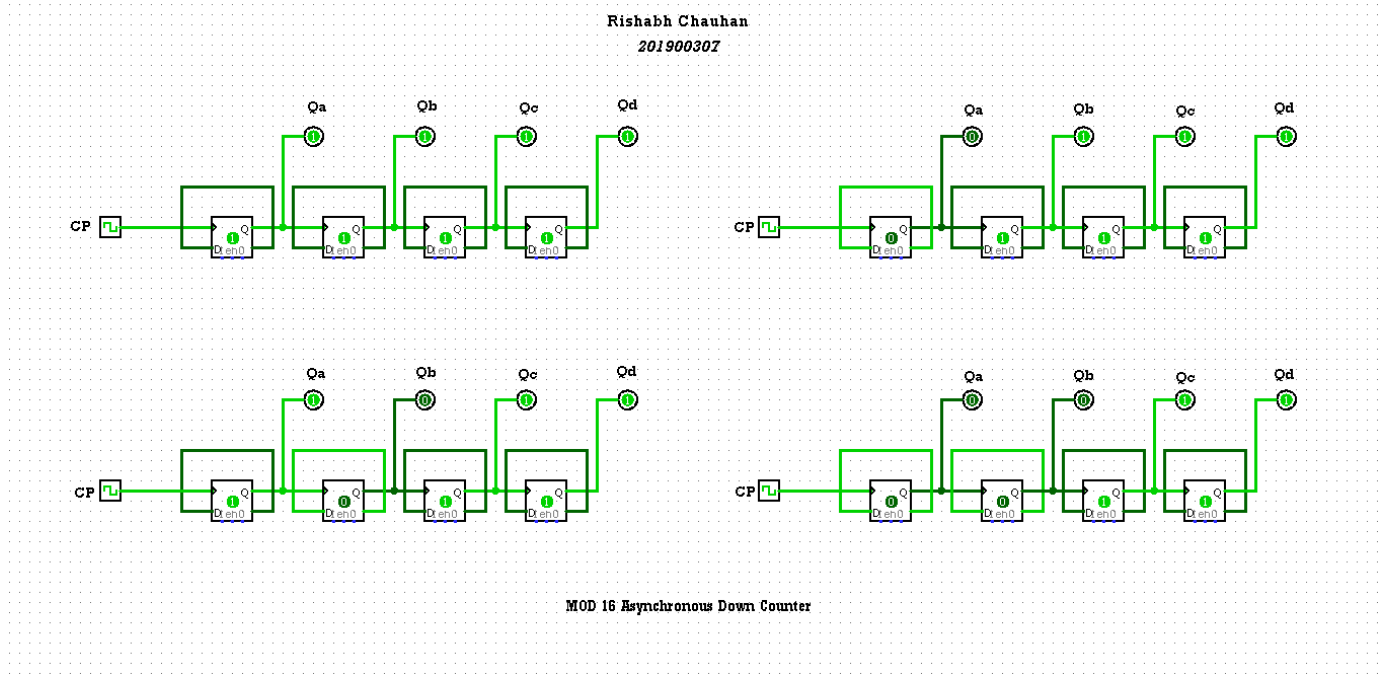
CIRCUIT DIAGRAM OF A MOD 16 ASYNCHRONOUS UP COUNTER:



PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet-1



Student's observation and conclusion:

- **A mod 16 asynchronous down counter is a sequential circuit as it depends on its previous output. It is made up of four D Flip-flop which is toggled as the complement output of each individual D flip-flop is connected to its input(D), it gives 16 outputs in a descending sequence(in its binary form) as shown in the above attached circuits, therefore the truth table is verified.**

•Initially, output of all the flip flops is 0.

•When the clock pulse is rising edge for the first time, Qa, Qb, Qc, Qd change to 1.

• Qd acts as Most Significant Bit (MSB) and Qa acts as Least Significant Bit (LSB).

•Qa toggles every time as it depends on the rising edge of the clock pulse whereas, Qc, Qd remains 1 throughout. Qb changes during the rising edge of Qa. Hence in the first four cycles we get the values from 1111 to 1100.

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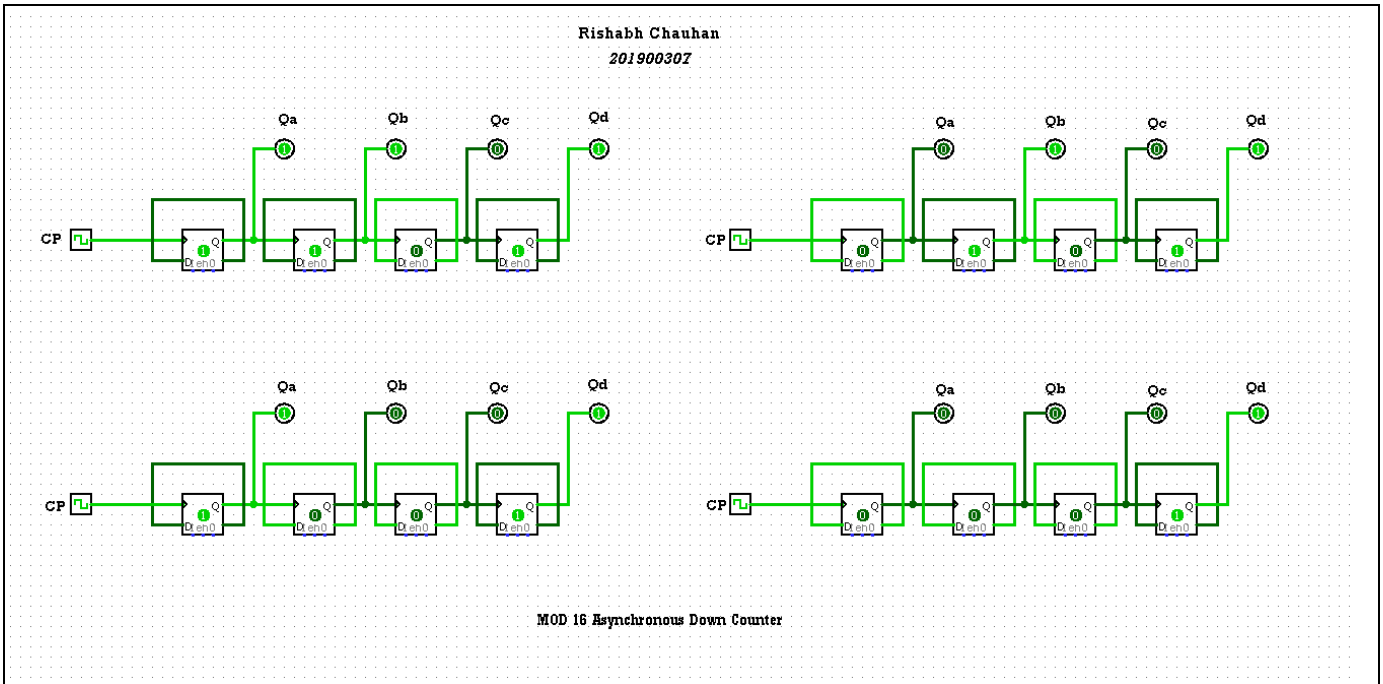
Student's worksheet-2



Student's observation and conclusion:

• Qa toggles during every pulse of the clock as it depends on the rising edge of the clock.

•Qb changes only during the rising edge of Qa. Hence, it becomes 0 in seventh cycle.

•Qc depends on the rising edge of Qb. Since rising edge of Qb is never encountered in this cycle hence, Qc holds its previous vale of 0.

•Qd changes with the rising edge of Qc. Hence, Qd remains 1 throughout. Hence, we get values from 1011 to 1000 in fifth to eighth cycle.

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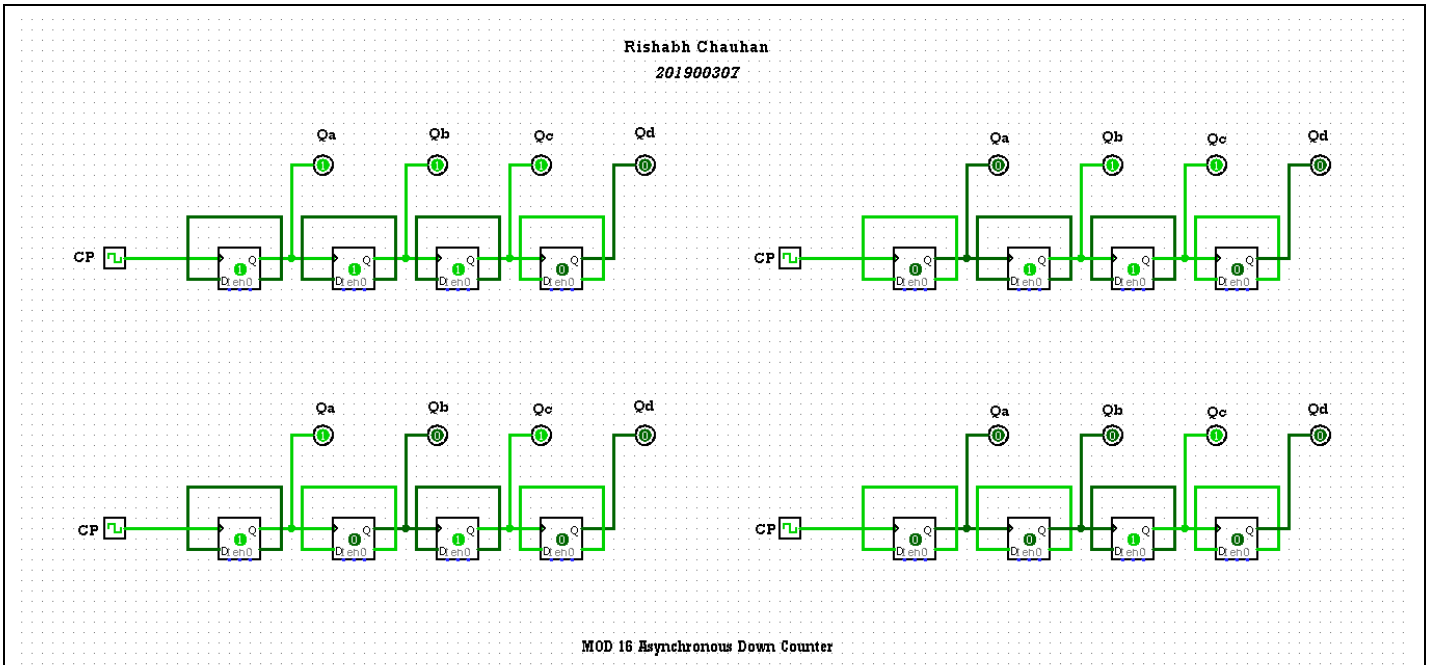
Student's worksheet-3



Student's observation and conclusion:

•Qa depends on clock pulse. Hence it changes throughout.

•Qb becomes 1 when Qa becomes 1, retains its value till rising edge of Qa is encountered again eleventh cycle and remains 0 from then.

•Qc and Qd stay 1 and 0 respectively during these four cycles.

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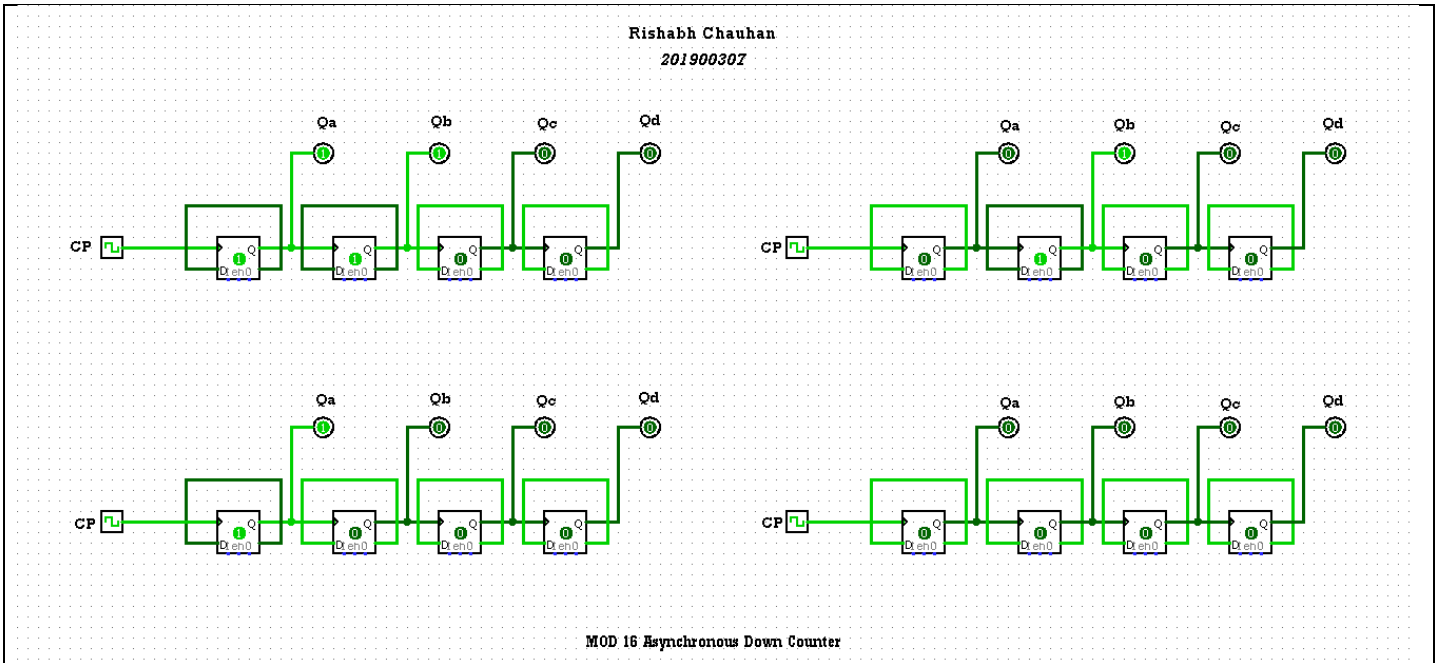
Student's worksheet-4



Student's observation and conclusion:

•In thirteenth cycle, Qa becomes 1 hence, Qb also becomes 1. Qc toggles to 0 due to rising edge of Qb. Qd does not change.

•In fourteenth cycle, Qa becomes 0. Qb, Qc, Qd remains unchanged.

•In fifteenth cycle, Qa becomes 1. So Qb toggles to 0. Since rising edge of Qb is not encountered hence, Qc and therefore Qd retains its past values. •In sixteenth cycle, Qa, Qb, Qc, Qd are 0.

- **In the given worksheet 1,2,3,4, the circuit diagram is of 16-mod asynchronous down counter. In this circuit we use D FLIP FLOP and CLOCK and it provides a binary conversion from binary 1111 to 0000.**

- **In the given 16 circuit when RESET is applied on all the flip-flops simultaneously, their Q output shows 0, and Q' outputs shows 1. The Q' outputs are then connected to D and therefore all that they require is the rising edge of clock to transfer the data at input D to output Q.**

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