EXPERIMENT NUMBER: 5

EXPERIMENT NAME: Design of a 2 to 4 line active HIGH outputs Decoder.

AIM: To design a 2 to 4 line Decoder with active HIGH outputs using logic gates and verify it.

APPARATUS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	AND GATE	IC 7408	1
2.	NOT GATE	IC 7404	1
3.	IC TRAINER KIT	-	1
4.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

A decoder is a combinational circuit that connects the binary information from 'n' number of input lines to a maximum of 2n unique output lines. Decoder is also called a minterm generator/Maxterm generator. A minterm generator is a decoder with active HIGH outputs and is constructed using AND and NOT gates. Maxterm generator is designed with OR and NOT gates and has active LOW outputs.

TRUTH TABLE:

INPUT		OUTPUT			
A	**B**	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

From the truth table, we get the output expressions as:

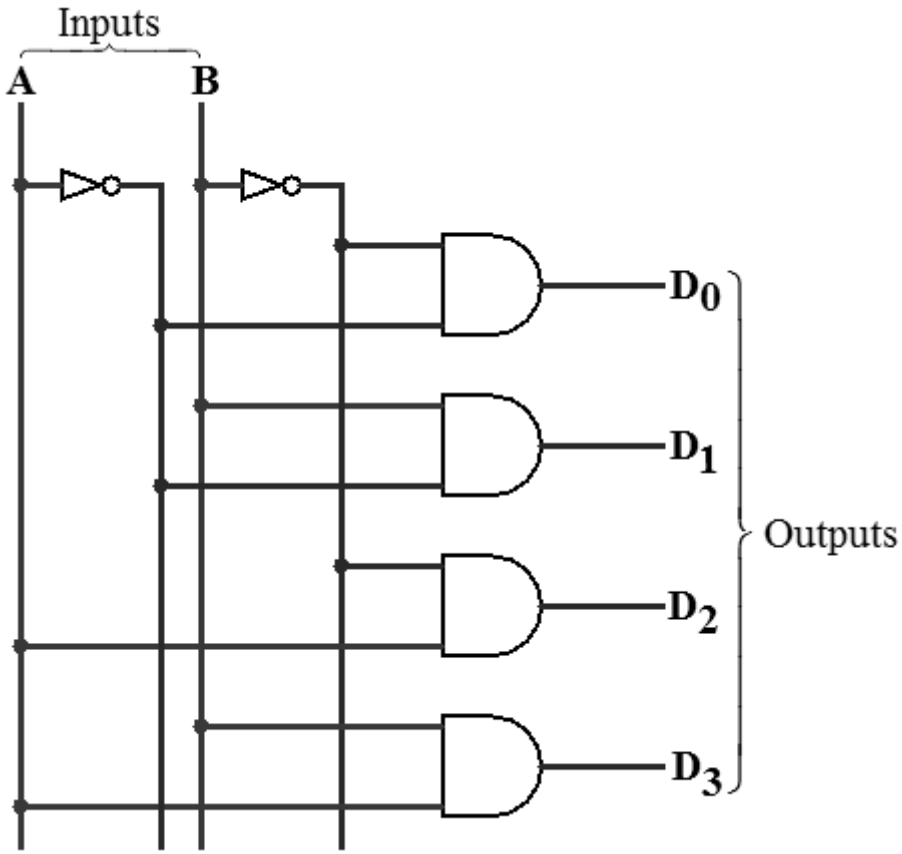
$D_0 = \overline{A}\ \overline{B}$

$D_1 = \overline{A}\ B$

$D_2 = A\ \overline{B}$

$D_3 = A\ B$

CIRCUIT DIAGRAM OF A 2 TO 4 LINE DECODER WITH ACTIVE HIGH OUTPUTS:



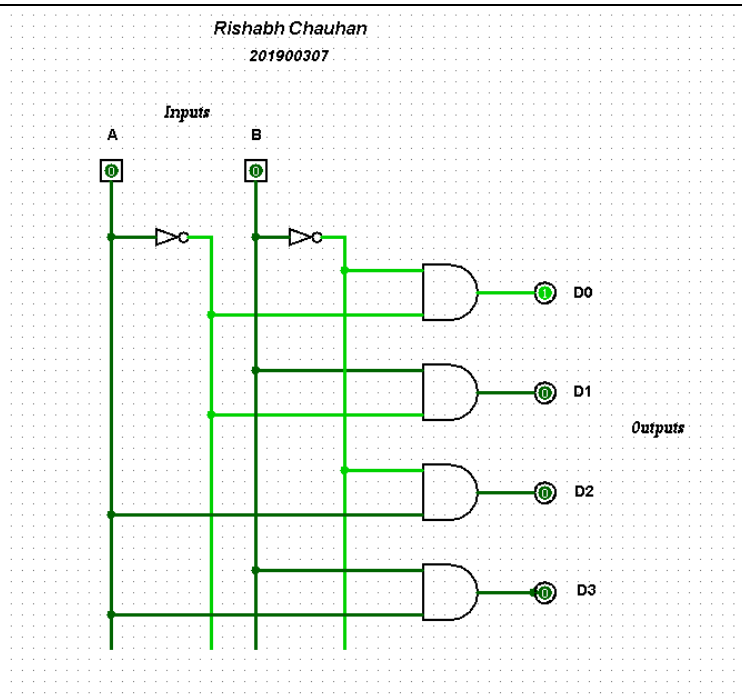
DESIGN PROCEDURE:

1. Truth table of 2 to 4 line decoder with active HIGH outputs is prepared.
2. K-maps for all the output variables (D_0, D_1, D_2 and D_3) are drawn.
3. Simplified expressions for the output variables are obtained using manual simplification.
4. Circuit diagram is drawn as per the simplified expressions of the output variables obtained in step 3.

PRACTICAL PROCEDURE:

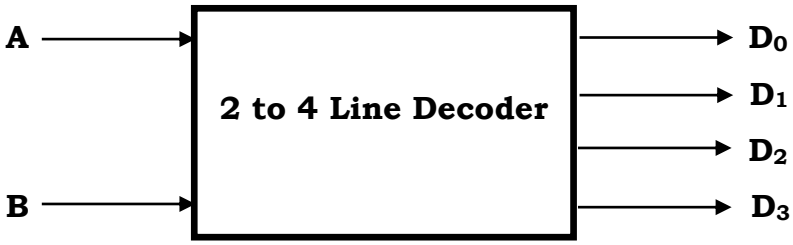
1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet 1



INPUT		OUTPUT			
A	**B**	**D_0**	**D_1**	**D_2**	**D_3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Student 's observation and conclusion:



- **The 2 binary inputs labelled A and B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the minterms of the 2 input variables, (each output = a minterm).**
- **The binary inputs A and B determine which output line from D_0 to D_3 is "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic "0" so only one output can be active (HIGH) at any given point of time. Here, D_0 is kept "HIGH" since $D_0 = \overline{A} \cdot \overline{B}$ ($\overline{A} = \overline{B} = 1$).**

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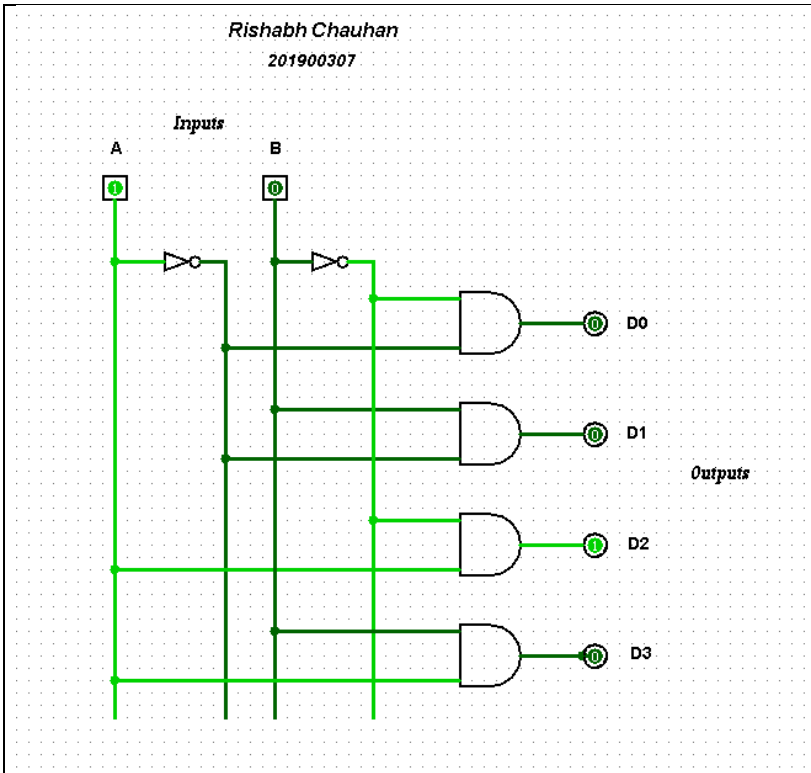
Student's worksheet 2



INPUT		OUTPUT			
A	**B**	**D_0**	**D_1**	**D_2**	**D_3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Student's observation and conclusion:

- **Here D_2 is held "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic level "0", since $D_2 = A \cdot \overline{B}$ ($A = \overline{B} = 1$).**
- **The 2 binary inputs labelled A and B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the minterms of the 2 input variables, (each output = a minterm).**
- **If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2^n outputs based on that input with all other outputs deactivated.**

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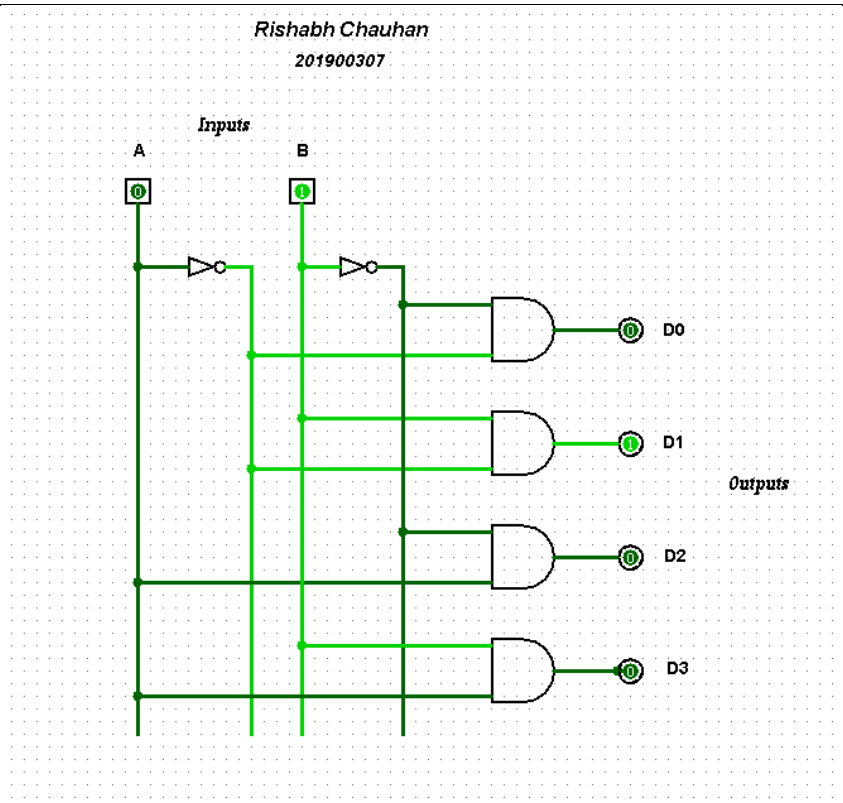
Student's worksheet 3



INPUT		OUTPUT			
A	**B**	**D_0**	**D_1**	**D_2**	**D_3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Student's observation and conclusion:

- **Here D_1 is held "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic level "0", since $D_1 = \overline{A}.B$ ($\overline{A} = B = 1$).**
- **The 2 binary inputs labelled A and B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the minterms of the 2 input variables, (each output = a minterm).**
- **If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2^n outputs based on that input with all other outputs deactivated.**

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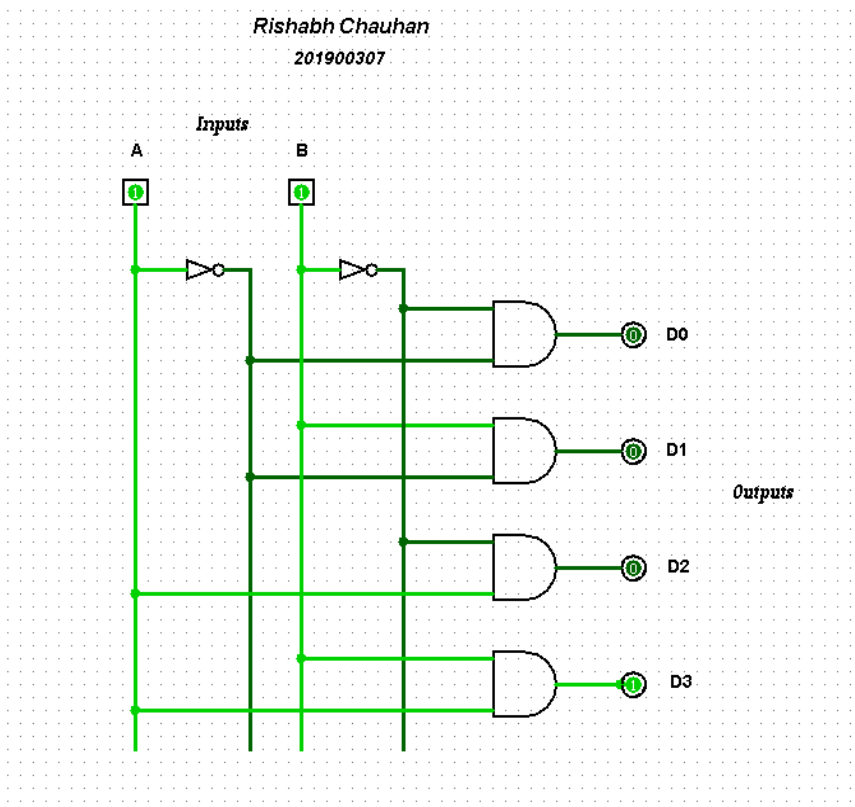
Student's worksheet-4



INPUT		OUTPUT			
A	**B**	**D_0**	**D_1**	**D_2**	**D_3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Student's observation and conclusion:

- **Here D_3 is held "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic level "0", since $D_3 = A \,.\, B$ $(A = B = 1)$.**
- **The 2 binary inputs labelled A and B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the minterms of the 2 input variables, (each output = a minterm).**
- **If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2 outputs based on that input with all other outputs deactivated.**

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