EXPERIMENT NUMBER: 12

EXPERIMENT NAME: Verification of registers.

AIM: To realize and study of Shift Register in

(i) SISO (Serial in Serial out) mode

(ii) SIPO (Serial in Parallel out) mode

(iii) PIPO (Parallel in Parallel out) mode

(iv) PISO (Parallel in Serial out) mode

APPARATUS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	D Flip-flop	IC 7474	2
2.	2:1 MUX	-	3
3.	IC TRAINER KIT	-	1
4.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

Flip flops can be used to store a single bit of binary data (1or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in order to store n bits of data. A **Register** is a device which is used to store such information. It is a group of flip flops connected to series used to store multiple bits of data.

The information stored within these registers can be transferred with the help of **shift registers**. The Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.

The registers which will shift the bits to left are called “Shift left registers”.

The registers which will shift the bits to right are called “Shift right registers”.

Shift registers are basically 4 types. These are:

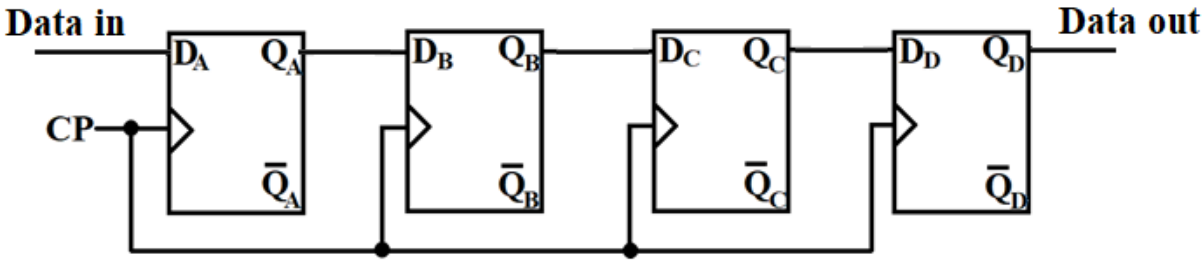
- **Serial-in to Parallel-out (SIPO)** - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

- **Serial-in to Serial-out (SISO)** - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

- **Parallel-in to Serial-out (PISO)** - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

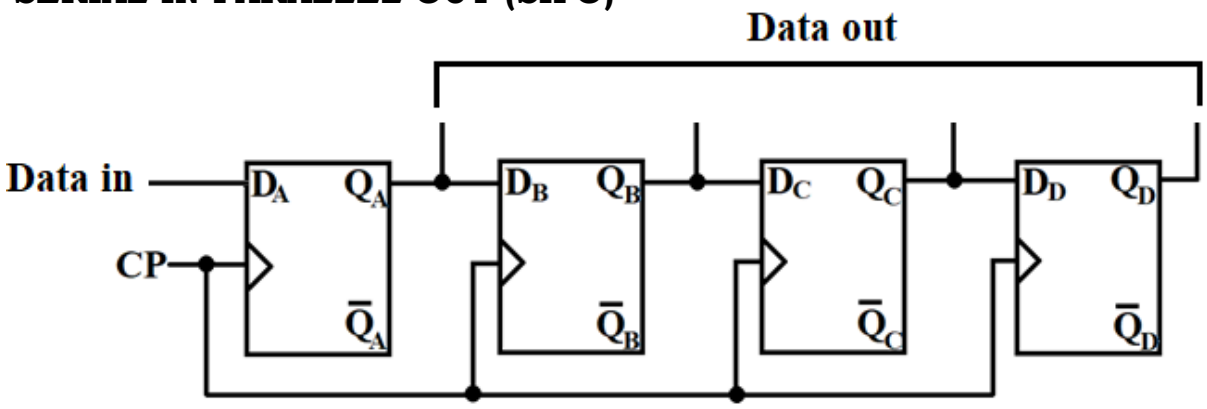
- **Parallel-in to Parallel-out (PIPO)** - the parallel data is loaded simultaneously into the register and transferred together to their respective outputs by the same clock pulse.

(i) SERIAL IN SERIAL OUT (SISO)(Right Shift)



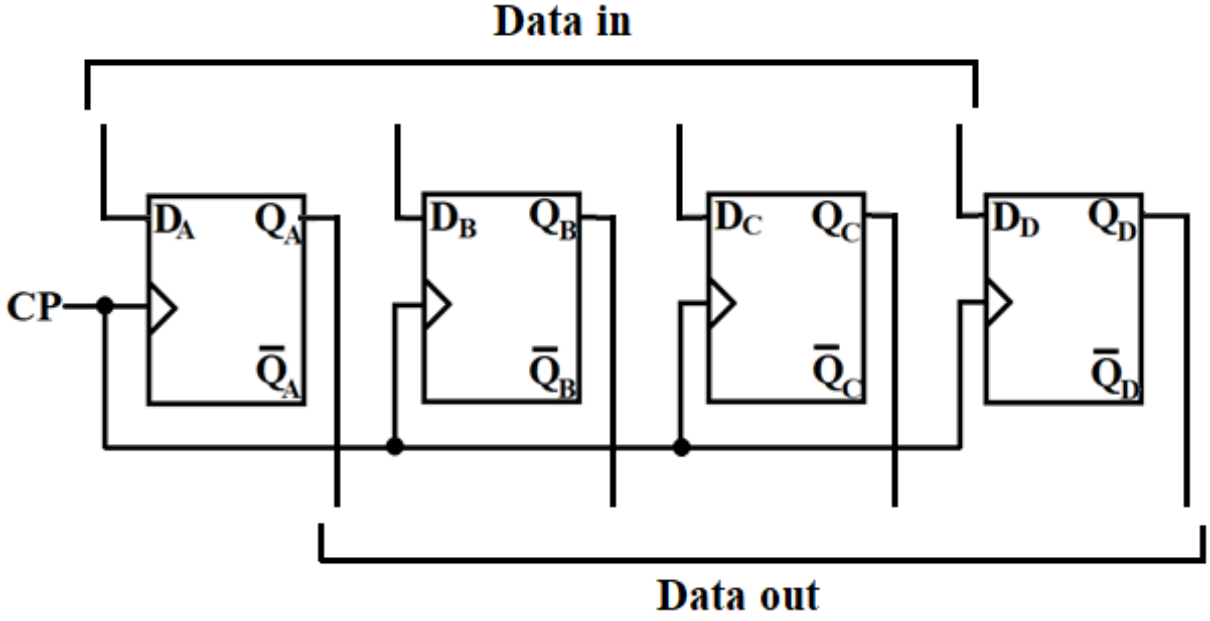
CP	Data input	Q_D
0	1	x
1	0	x
2	1	x
3	0	x
4	1	1
5	0	0

(ii) SERIAL IN PARALLEL OUT (SIPO)



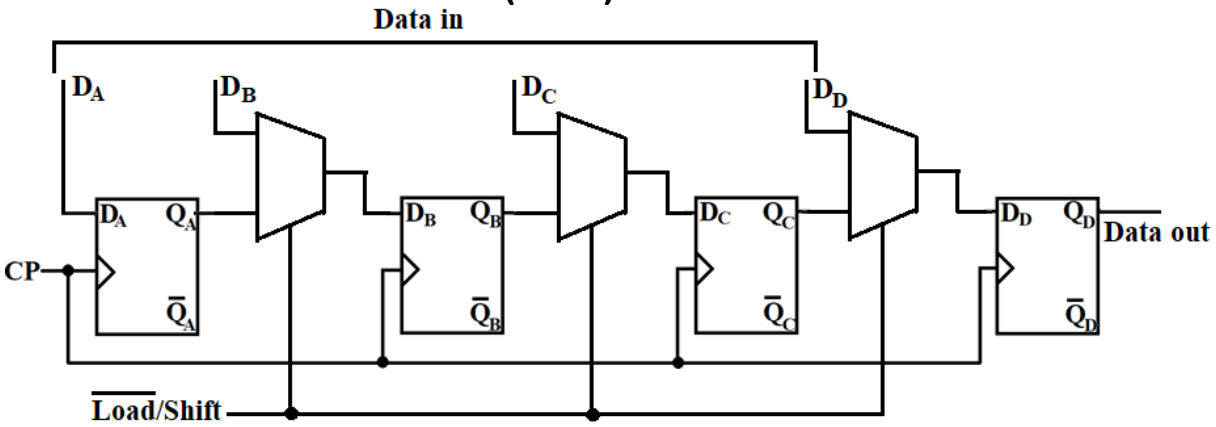
CP	Data input	Q_A	Q_B	Q_C	Q_D
0	1	x	x	x	x
1	0	1	x	x	x
2	1	0	1	x	x
3	0	1	0	1	x
4	1	0	1	0	1

(iii) PARALLEL IN PARALLEL OUT (PIPO)



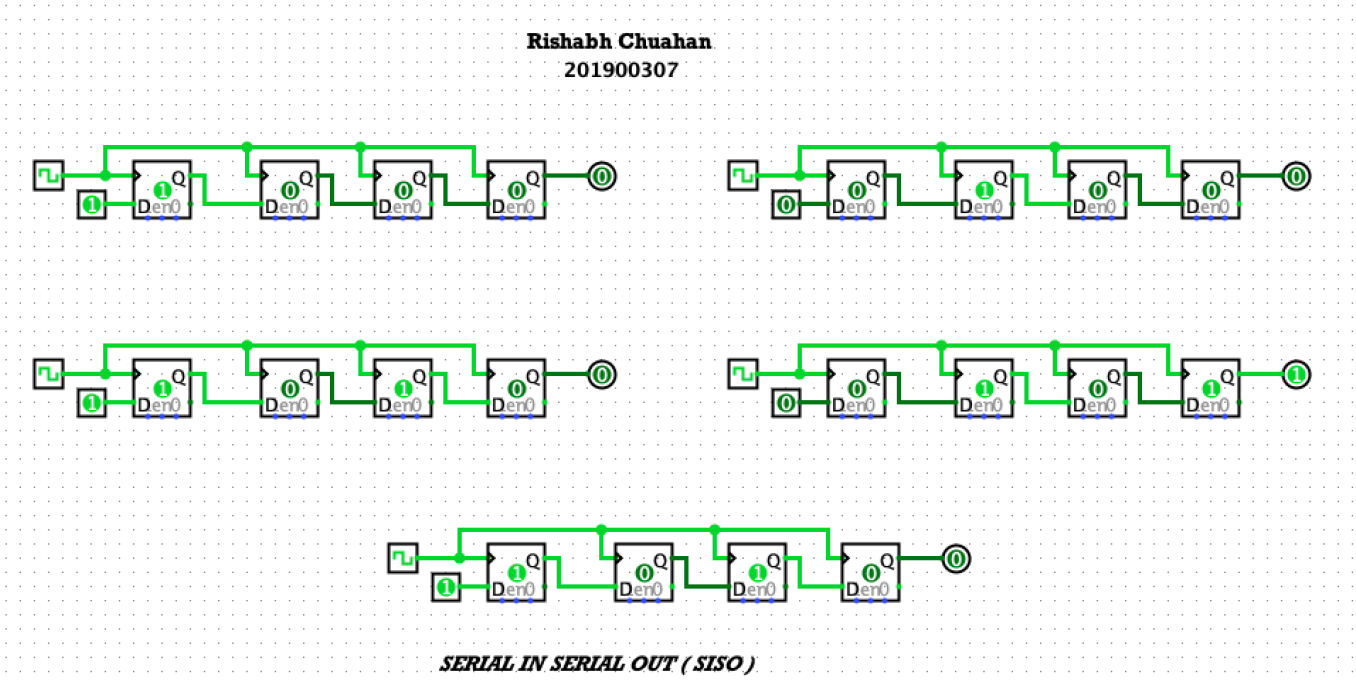
CP	Data input				Q_A	Q_B	Q_C	Q_D
	D_A	D_B	D_C	D_D				
0	1	0	1	0	x	x	x	x
1	x	x	x	x	1	0	1	0

(iv) PARALLEL IN SERIAL OUT (PISO)



CP	Load/ Shift	Data input				Q_D
		D_A	D_B	D_C	D_D	
0	0	1	0	1	0	x
1	0	1	0	1	0	0
2	1	1	0	1	0	1
3	1	1	0	1	0	0
4	1	1	0	1	0	1

Student's worksheet 1



Students' observations and conclusions:

The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register.

The logic circuit given below shows a serial-in serial-out shift register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

The above circuit is an example of a shift right register, taking the serial data input from the left side of the flip flop. The main use of a SISO is to act as a delay element.

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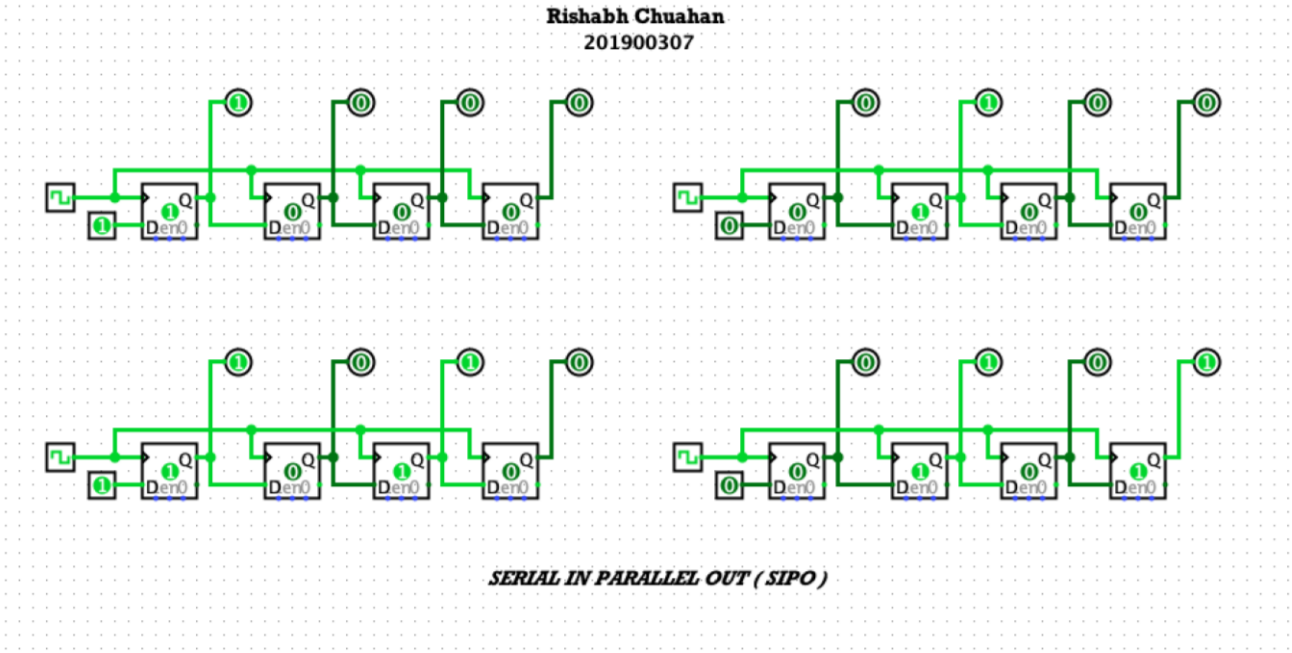
Student's worksheet-2



Students' observations and conclusions:

This circuit consists of three D flip-flops, which are cascaded. That means, the output of one D flip-flop is connected as the input of the next D flip-flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each one.

In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**. For every positive edge triggering of clock signal, the data shifts from one stage to the next. In this case, we can access the outputs of each D flip-flop in parallel. So, we will get **parallel outputs** from this shift register.

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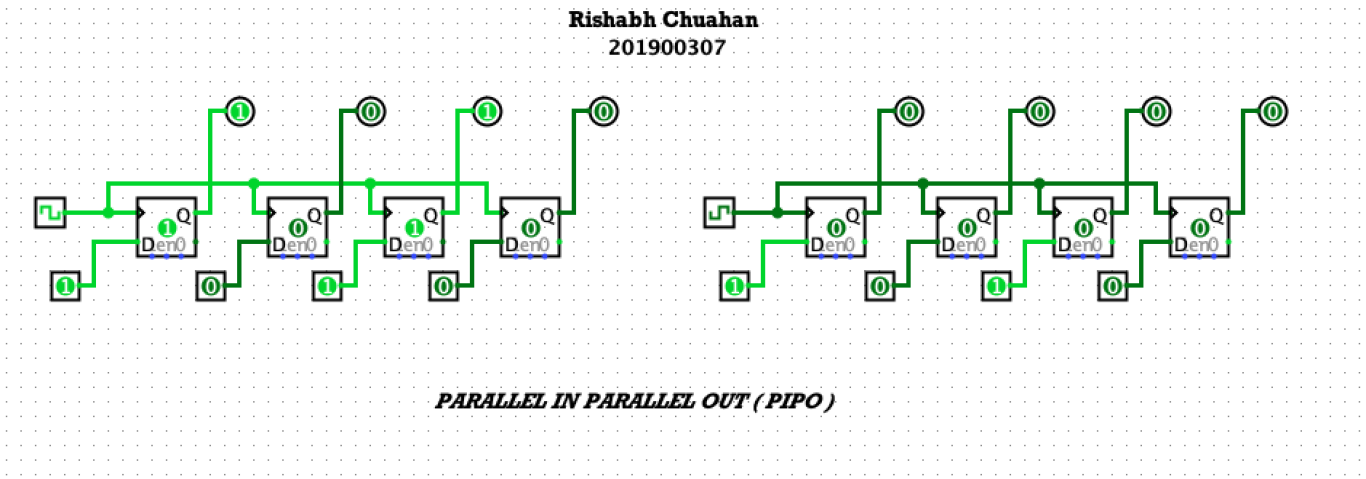
Student's worksheet 3



Students' observations and conclusions:

This circuit consists of three D flip-flops, which are cascaded. That means, the output of one D flip-flop is connected to the input of the next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can apply the **parallel inputs** to each D flip-flop by making Preset Enable to 1. We can apply the parallel inputs through preset or clear. These two are asynchronous inputs. That means, the flip-flops produce the corresponding outputs, based on the values of asynchronous inputs. In this case, the effect of output is independent of clock transition. So, we will get parallel **outputs** from each D flip-flop.

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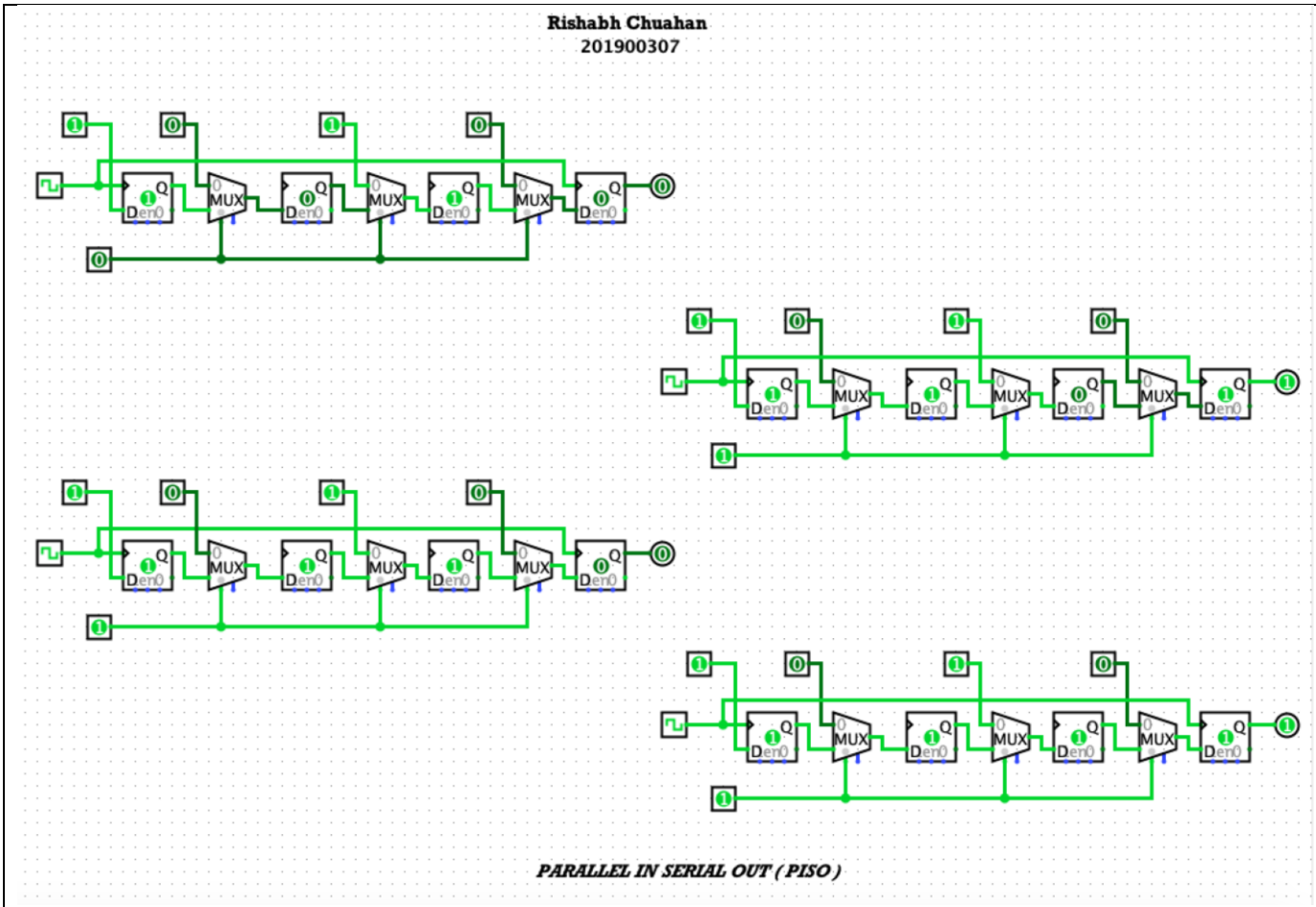
Student's worksheet-4



Students' observations and conclusions:

This circuit consists of three D flip-flops, which are cascaded. That means, the output of one D flip-flop is connected as the input of the next D flip-flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each one.

In this shift register, we can apply the **parallel inputs** to each D flip-flop by making Preset Enable to 1. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we will get the **serial output** from the right most D flip-flop.

In Parallel in Serial out, the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

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