EXPERIMENT NUMBER: 11

EXPERIMENT NAME: Design of a 4-bit ring counter and Johnson counter.

AIM: To design a (i) 4-bit ring counter and (ii) 4-bit Johnson counter using D flip-flops and verify their state diagrams.

(i) 4-bit ring counter

APPARATUS REQUIRED:

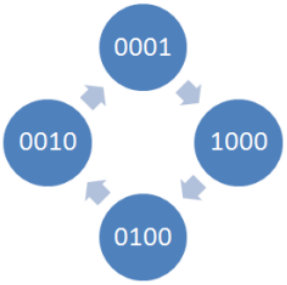
Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	D Flip-flop	IC 7474	2
2.	IC TRAINER KIT	-	1
3.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

Ring counter is a sequential logic circuit that is constructed using shift register. Same data recirculates in the counter depending on the clock pulse.

The ring counter is a cascaded connection of flip flops, in which the output of last flip flop is connected to input of first flip flop. In ring counter if the output of any stage is 1, then its reminder is 0. The Ring counters transfers the same output throughout the circuit.

That means if the output of the first flip flop is 1, then this is transferred to its next stage i.e. 2nd flip flop. By transferring the output to its next stage, the output of first flip flop becomes 0. And this process continues for all the stages of a ring counter. If we use n flip flops in the ring counter, the '1' is circulated for every n clock cycles.



State Diagram:

The state diagram of the 4-bit ring counter is shown in above picture. It denotes that the position of the preset digit (in this case preset digit is 1) is changing its position from LSB to MSB, for one clock signal.

STATE TABLE:

Present State				**Next State**				**Excitation table of D flip-flops**			
Q_A	Q_B	Q_C	Q_D	Q_{AN}	Q_{BN}	Q_{CN}	Q_{DN}	D_A	D_B	D_C	D_D
0	0	0	0	×	×	×	×	×	×	×	×
0	0	0	1	1	0	0	0	1	0	0	0
0	0	1	0	0	0	0	1	0	0	0	1
0	0	1	1	×	×	×	×	×	×	×	×
0	1	0	0	0	0	1	0	0	0	1	0
0	1	0	1	×	×	×	×	×	×	×	×
0	1	1	0	×	×	×	×	×	×	×	×
0	1	1	1	×	×	×	×	×	×	×	×
1	0	0	0	0	1	0	0	0	1	0	0
1	0	0	1	×	×	×	×	×	×	×	×
1	0	1	0	×	×	×	×	×	×	×	×
1	0	1	1	×	×	×	×	×	×	×	×
1	1	0	0	×	×	×	×	×	×	×	×
1	1	0	1	×	×	×	×	×	×	×	×
1	1	1	0	×	×	×	×	×	×	×	×
1	1	1	1	×	×	×	×	×	×	×	×

K-Map for D_A:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	1	X	0
01	0	X	X	X
11	X	X	X	X
10	0	X	X	X

K-Map for D_B:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	0	X	0
01	0	X	X	X
11	X	X	X	X
10	1	X	X	X

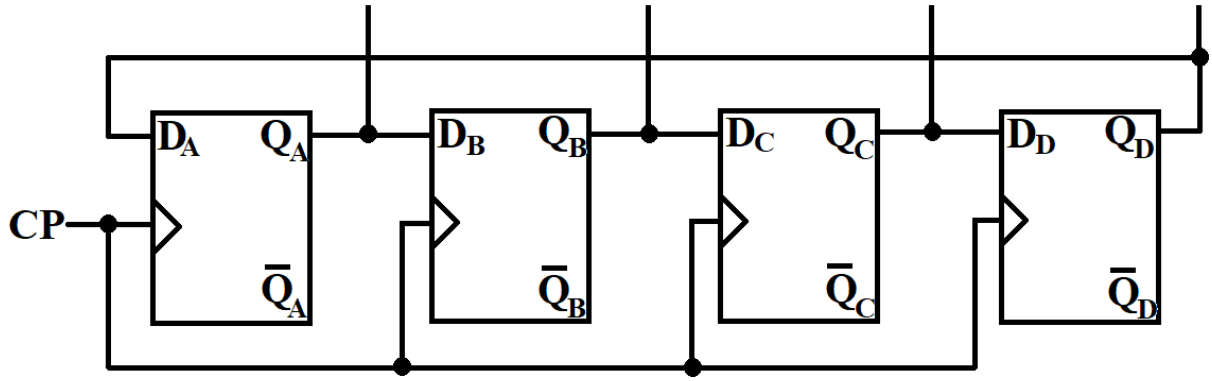
K-Map for D_C:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	0	X	0
01	1	X	X	X
11	X	X	X	X
10	0	X	X	X

K-Map for D_D:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	0	X	1
01	0	X	X	X
11	X	X	X	X
10	0	X	X	X

CIRCUIT DIAGRAM OF 4-BIT RING COUNTER:



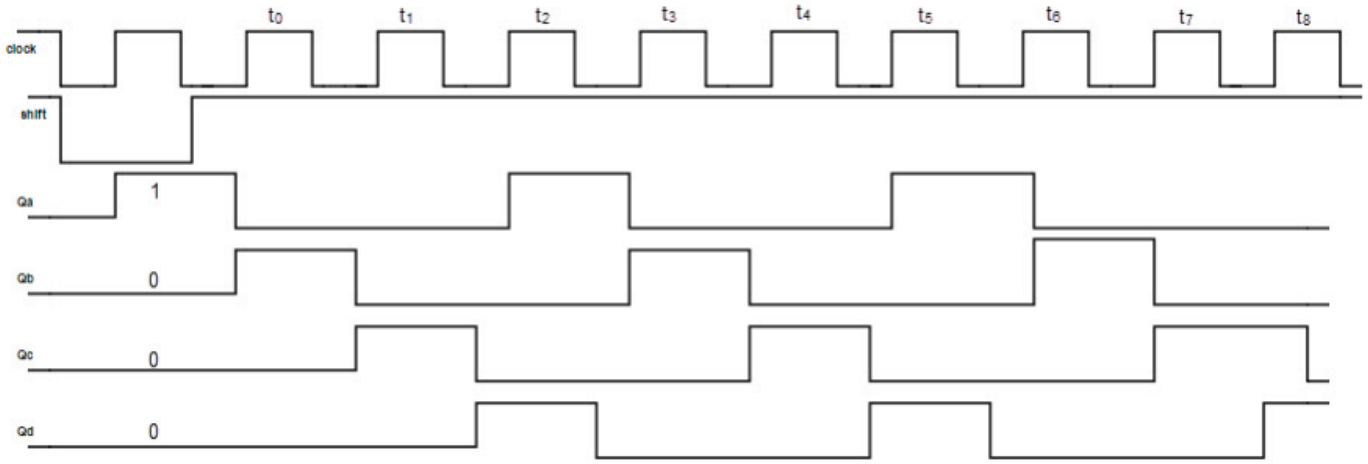
DESIGN PROCEDURE:

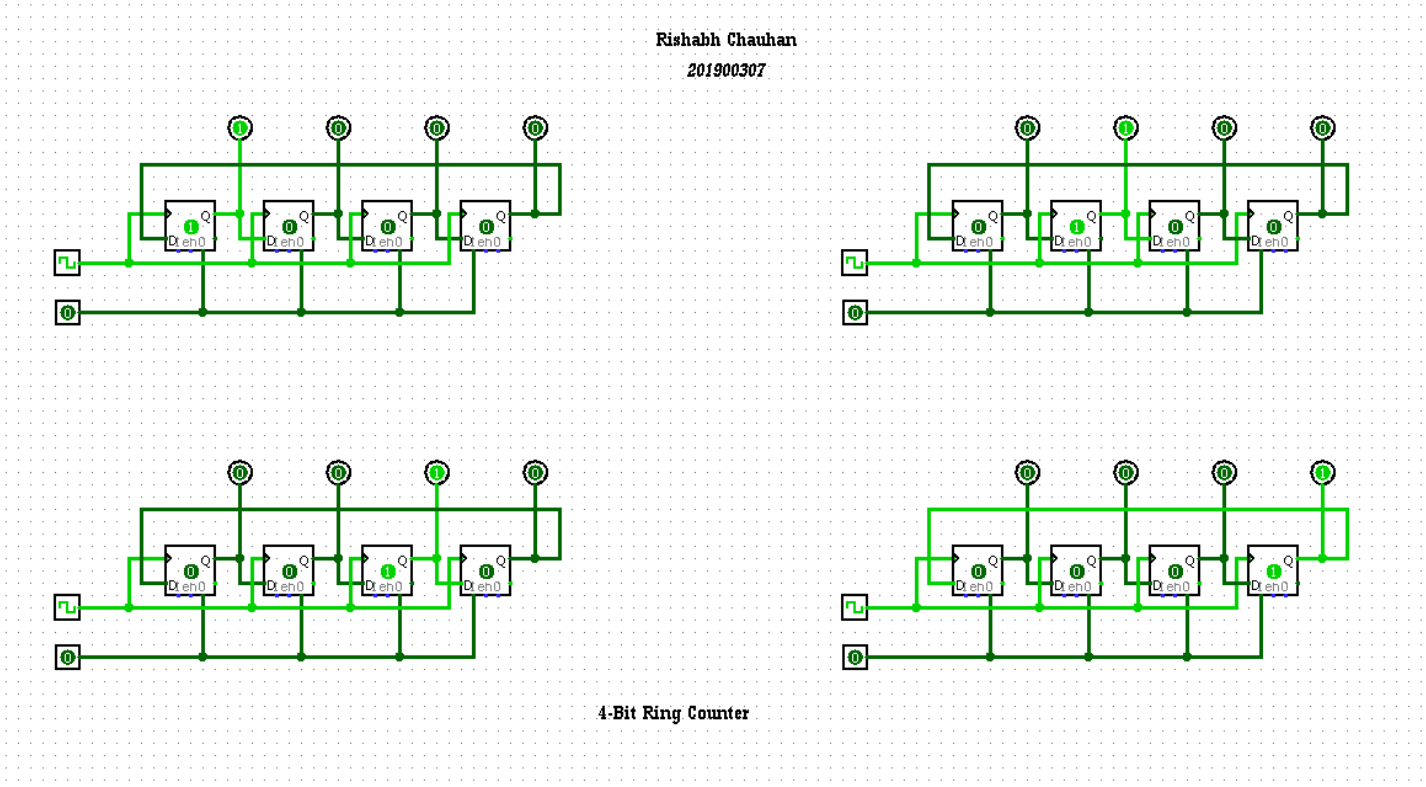
1. State diagram of the counter is prepared.
2. State table is prepared
3. K-maps for all the flip-flip inputs (D_A, D_B, D_C and D_D) are drawn.
4. Circuit diagram is drawn as per the simplified expressions obtained in step 3.

PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Clock pulses were applied and state diagram was is verified.

Student's worksheet-1





Student's observation and conclusion:

- **Here we design the ring counter by using D flip flop. This is a Mod 4 ring counter which has 4 D flip flops connected in series. The clock signal is applied to clock input of each flip flop, simultaneously and the RESET pulse is applied to the CLR inputs of all the flip flops.**

- **Initially, all the flip flops in ring counter are reset to 0 by applying CLEAR signal. Before applying the clock pulse, we apply the PRESET pulse to the flip flops which assigns the value '1' to the ring counter circuit. For each clock signal, the data circulates among all the 4 flip flop stages of ring counter.**

- **These 4 staged ring counters is called Mod 4 ring counter or 4-bit ring counter. To circulate the data correctly in the ring counter, we must load the counter with required values like all 0's or all 1's.**

- **The timing diagram of the Ring counter will explain that the clock signal changes the output of every stage of the counter, so that CLK signal will help the data to circulate from one flip flop to another. As the 4-bit ring counter (4 stages or 4 flip flops) circulates the preset digit within one clock signal, the output frequency of each flip flop is ¼ th of the main clock frequency.**

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(ii) 4-bit Johnson counter

APPARATUS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	D Flip-flop	IC 7474	2
2.	IC TRAINER KIT	-	1
3.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

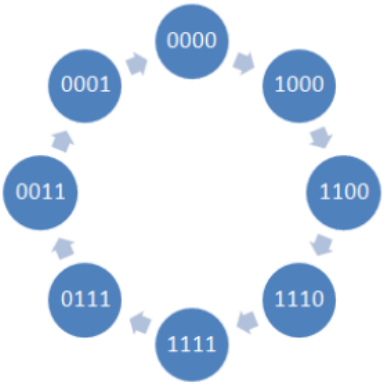
The Johnson counter is a modification of ring counter. In this the inverted output of the last stage flip flop is connected to the input of first flip flop. If we use n flip flops to design the Johnson counter, it is known as 2n bit Johnson counter or Mod 2n Johnson counter.

This is an advantage of the Johnson counter that it requires only half number of flip flops that of a ring counter uses, to design the same Mod.

The main difference between the 4 bit ring counter and the Johnson counter is that, in ring counter , we connect the output of last flip flop directly to the input of first flip flop. But in Johnson counter, we connect the inverted output of last stage to the first stage input.

The Johnson counter is also known as Twisted Ring Counter, with a feedback. In Johnson counter the input of the first flip flop is connected from the inverted output of the last flip flop.

The Johnson counter or switch trail ring counter is designed in such a way that it overcomes the limitations of ring counter. Mainly it reduces the number of flip flops required for designing the circuit.



State Diagram:

STATE TABLE:

Present State				Next State				Excitation table of D flip-flops			
Q_A	Q_B	Q_C	Q_D	Q_{AN}	Q_{BN}	Q_{CN}	Q_{DN}	D_A	D_B	D_C	D_D
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0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	×	×	×	×	×	×	×	×
0	0	1	1	0	0	0	1	0	0	0	1
0	1	0	0	×	×	×	×	×	×	×	×
0	1	0	1	×	×	×	×	×	×	×	×
0	1	1	0	×	×	×	×	×	×	×	×
0	1	1	1	0	0	1	1	0	0	1	1
1	0	0	0	1	1	0	0	1	1	0	0
1	0	0	1	×	×	×	×	×	×	×	×
1	0	1	0	×	×	×	×	×	×	×	×
1	0	1	1	×	×	×	×	×	×	×	×
1	1	0	0	1	1	1	0	1	1	1	0
1	1	0	1	×	×	×	×	×	×	×	×
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	0	1	1	1

K-Map for D_A:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	1	0	0	X
01	X	X	0	X
11	1	X	0	1
10	1	X	X	X

K-Map for D_B:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	X
01	X	X	0	X
11	1	X	1	1
10	1	X	X	X

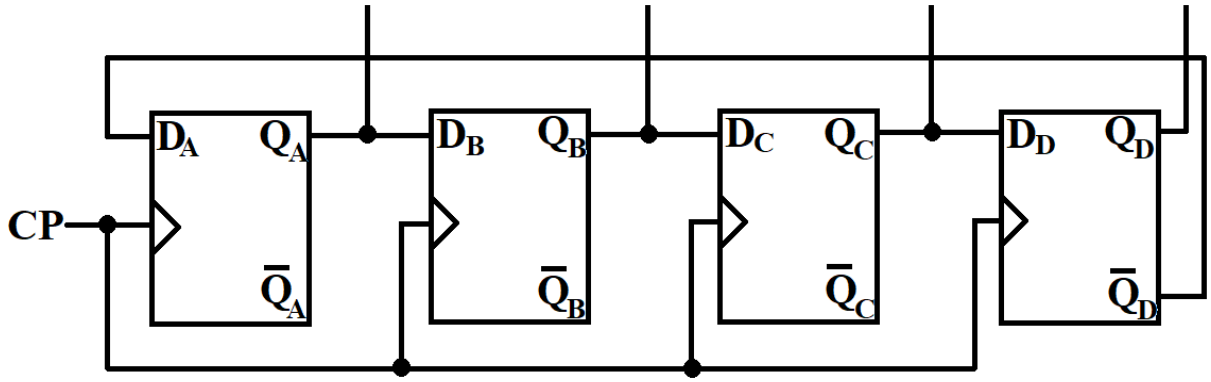
K-Map for D_C:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	X
01	X	X	1	X
11	1	X	1	1
10	0	X	X	X

K-Map for D_D:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	1	X
01	X	X	1	X
11	0	X	1	1
10	0	X	X	X

CIRCUIT DIAGRAM OF 4-BIT RING COUNTER:



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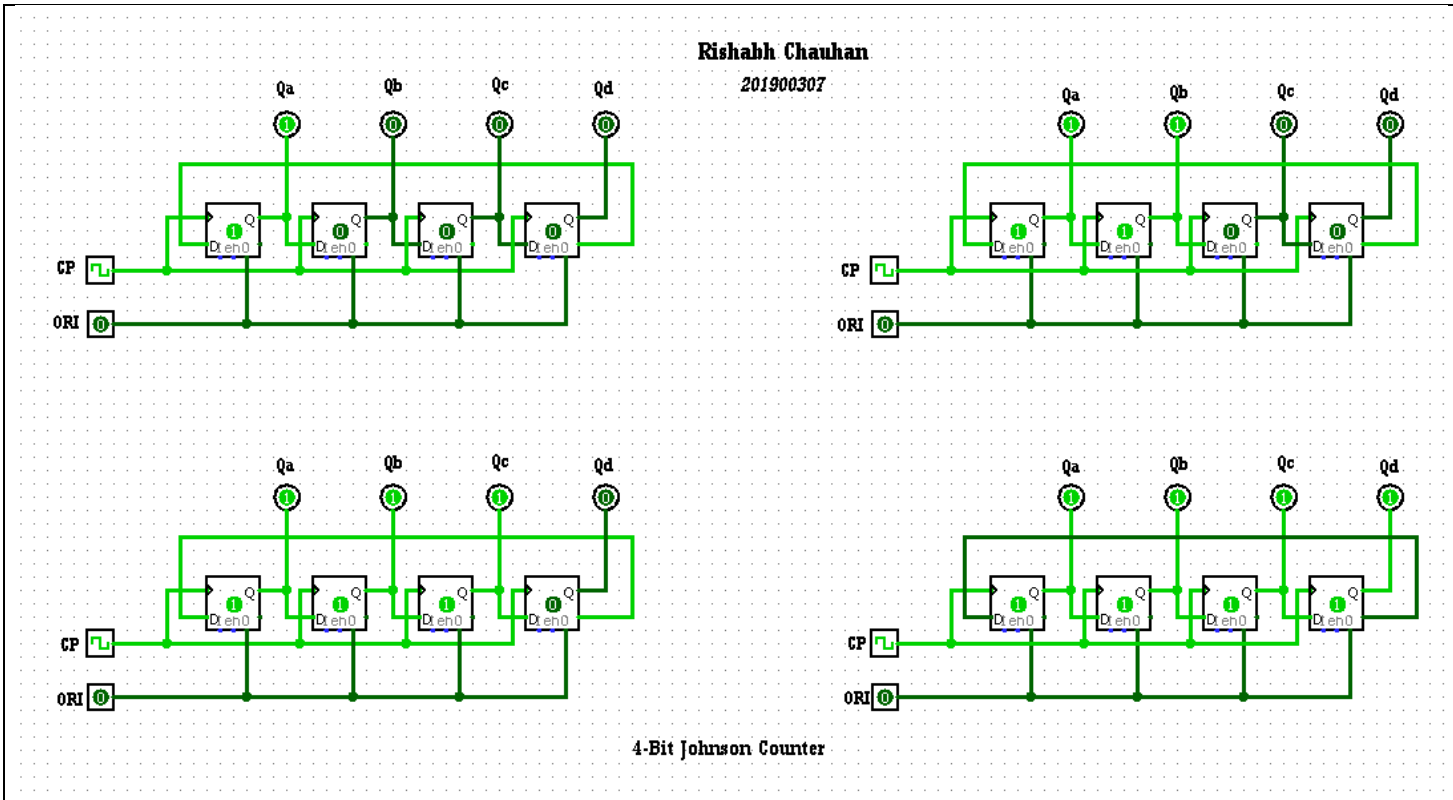
Student's worksheet-1



Student's observation and conclusion:

The Johnson counter is also known as Twisted Ring Counter, with a feedback. In Johnson counter the input of the first flip flop is connected from the inverted output of the last flip flop.

The Johnson counter or switch trail ring counter is designed in such a way that it overcomes the limitations of ring counter. Mainly it reduces the number of flip flops required for designing the circuit.
Like the ring counter, the clock signal in Johnson counter is connected to the clock input of each flip flop simultaneously.

<u>Operation of Johnson counter</u>

- **The Johnson counter designed with D flip flop is shown below. It has four stages i.e. four flip flops connected in series type or cascaded. Initially zero / Null is fed to the Johnson counter and on applying the clock signal, outputs will change to "1000", "1100", "1110", "1111", "0111", "0011", "0001", "0000" in a sequence and the sequence will repeat for next clock signal.**

- **The Johnson counter produces a special pattern by passing four 0's and then four 1's and thus it produces a special pattern by counting down.**

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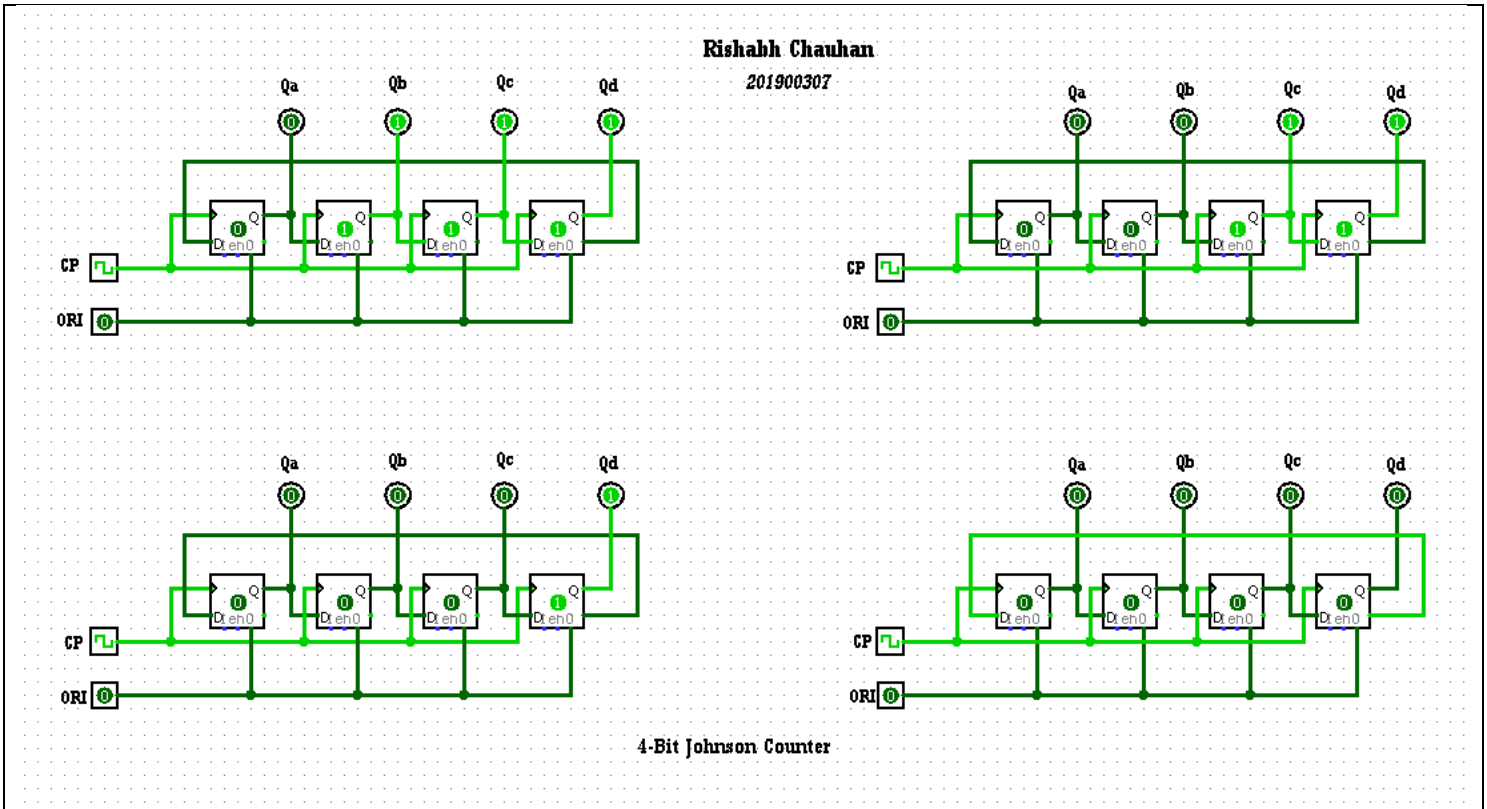
Student's worksheet-2



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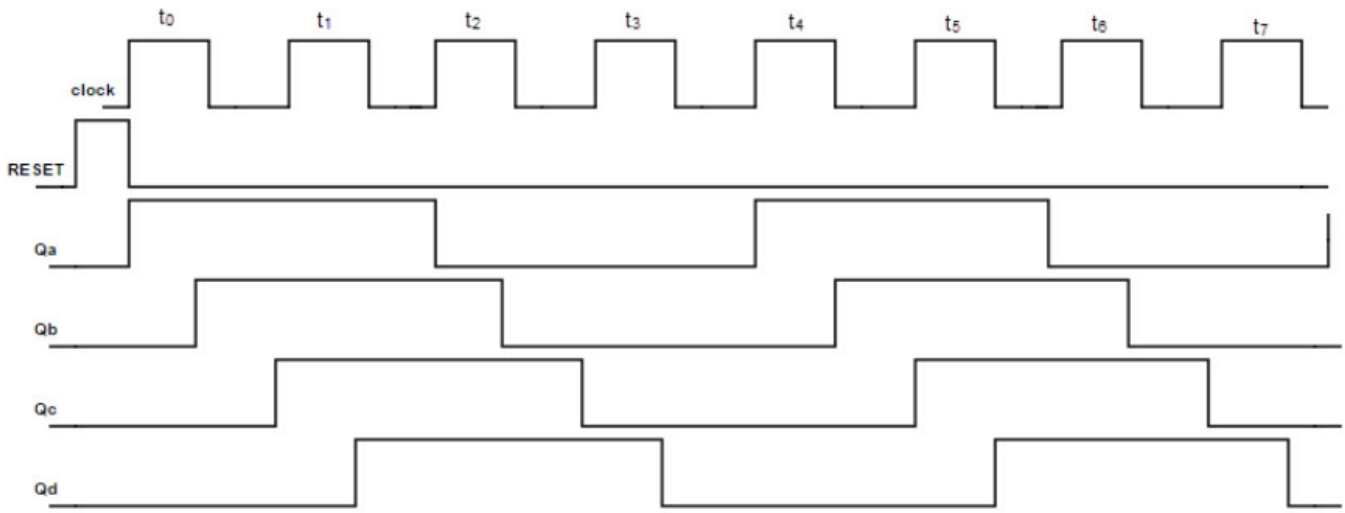
Student's worksheet-3



Student's observation and conclusion:

The timing diagram of the Johnson counter will explain that the clock signal changes the output of every stage of the counter, so that CLK signal will help the data to circulate from one flip flop to another.

When CLR = 0, all outputs and inputs of flip flops are present to 0 (cleared) except the data input of right most FF which sets to 1.

When CLR = 1, Johnson counter starts its operation. On every clock edge, the output of last flip flop (1) shifts left to the third flip flop. As the first flip flop is connected to serial input i.e. 1, the input of third flip flop is 1.

In next cycle, QA = 0 so 0 rotates in ring form in second half cycle. Johnson counter has 8 sequences: 0001, 0011, 0111, 1111, 1110, 1100, 1000, and 0000.

Advantage **of Johnson counter is that, it has more outputs than ring counter.**

Disadvantage **of Johnson counter is that, only out of 15 states are only 8 are used.**

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