EXPERIMENT NUMBER: 10

EXPERIMENT NAME: Design of a mod 16 synchronous up counter using JK FFs.

AIM: To design a mod 16 synchronous up counter using JK FFs and verify its state diagram.

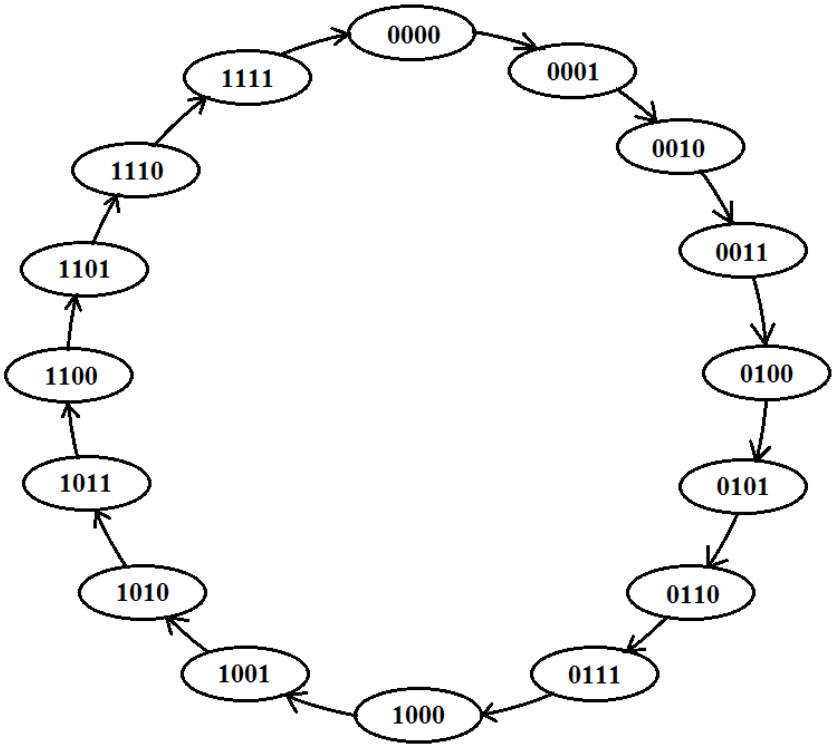
APPARATUS REQUIRED:

Sl. No.	**COMPONENT**	**SPECIFICATION**	**QUANTITY**
1.	AND GATE	IC 7408	1
2.	JK Flip-flop	IC 7473/IC 7476	2
3.	IC TRAINER KIT	-	1
4.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

.

STATE DIAGRAM:


0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

STATE TABLE:

Present State				Next State				Excitation table of JK flip-flop							
Q_A	Q_B	Q_C	Q_D	Q_{AN}	Q_{BN}	Q_{CN}	Q_{DN}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

K-Map for J_A:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

K-Map for K_A:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

K-Map for J_B:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

K-Map for K_B:

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	0	1	0
10	0	X	X	X

K-Map for J_C:

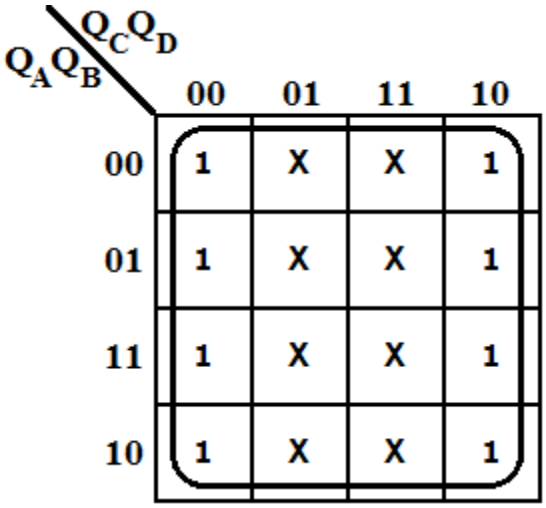
Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	1	X	X
10	0	1	X	X

K-Map for K_C:

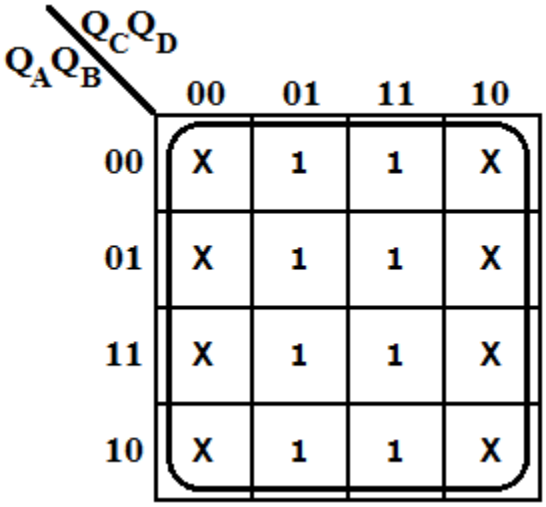
Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	0
10	X	X	1	0

K-Map for J_D:

K-Map for K_D:



Q_AQ_B \ Q_CQ_D	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1



Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

CIRCUIT DIAGRAM OF A MOD 16 SYNCHRONOUS UP COUNTER USING JK FFS:

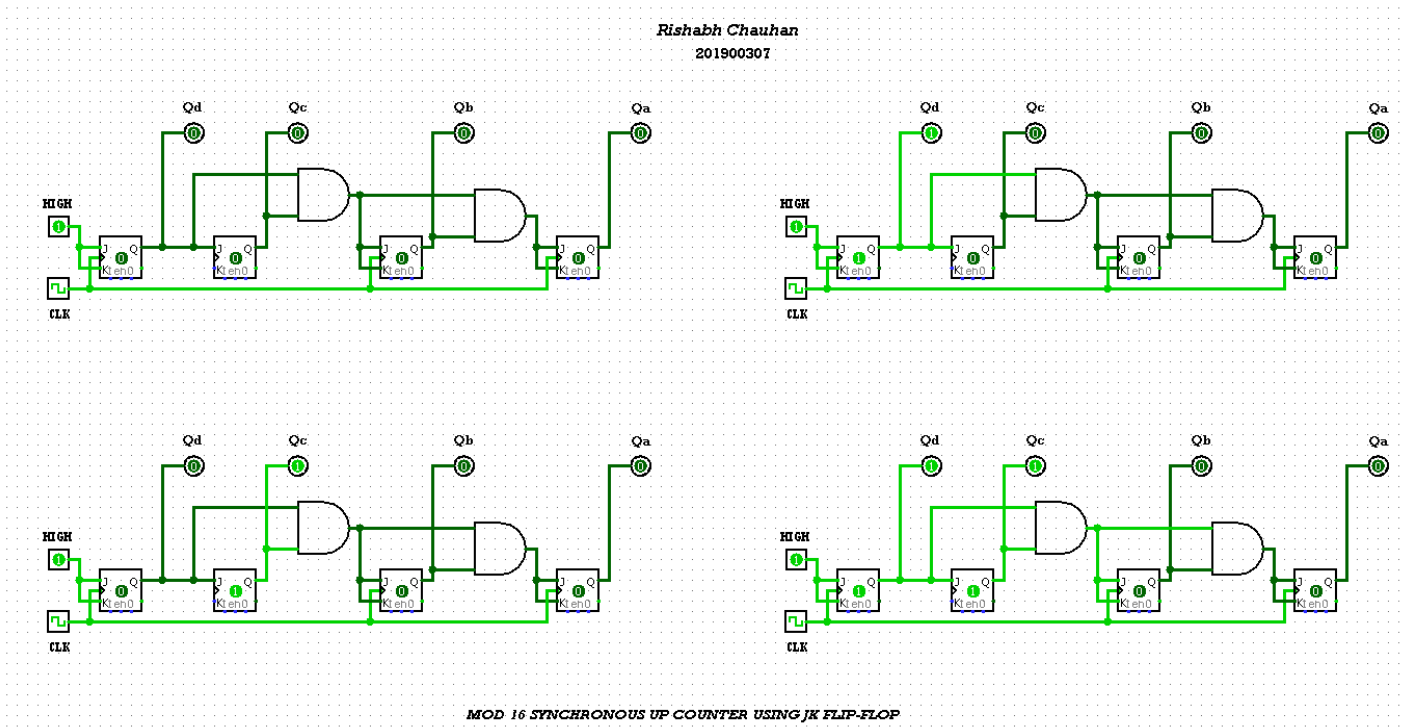
DESIGN PROCEDURE:

1. Truth table of the 4 bit binary to gray code converter is prepared.
2. K-maps for all the output variables (A, B, C and D) are drawn.
3. Simplified expressions for the output variables are obtained using manual simplification.
4. Circuit diagram is drawn as per the simplified expressions of the output variables obtained in step 3.

PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet-1



Student's observation and conclusion:

A MOD 16 Synchronous UP Counter (also known as Parallel Counter) was constructed using JK Flip-Flop. A constant input (1) is provided while the clock is toggled. D is assumed to be the Least Significant Bit (LSB) while A is assumed to be the Most Significant Bit (MSB).

Toggling the clock from ON (1) to OFF (0) to ON (1) changes the result. The obtained result cycles through the various stages in accordance to the theory.

In this case, the initial result is 0000. Toggling the clock has the same effect as "adding" one. So, result changes to 0001.

<u>CONVERSIONS:</u>

- **0000-0001**
- **0001-0010**
- **0010-0011**
- **0011-0100**

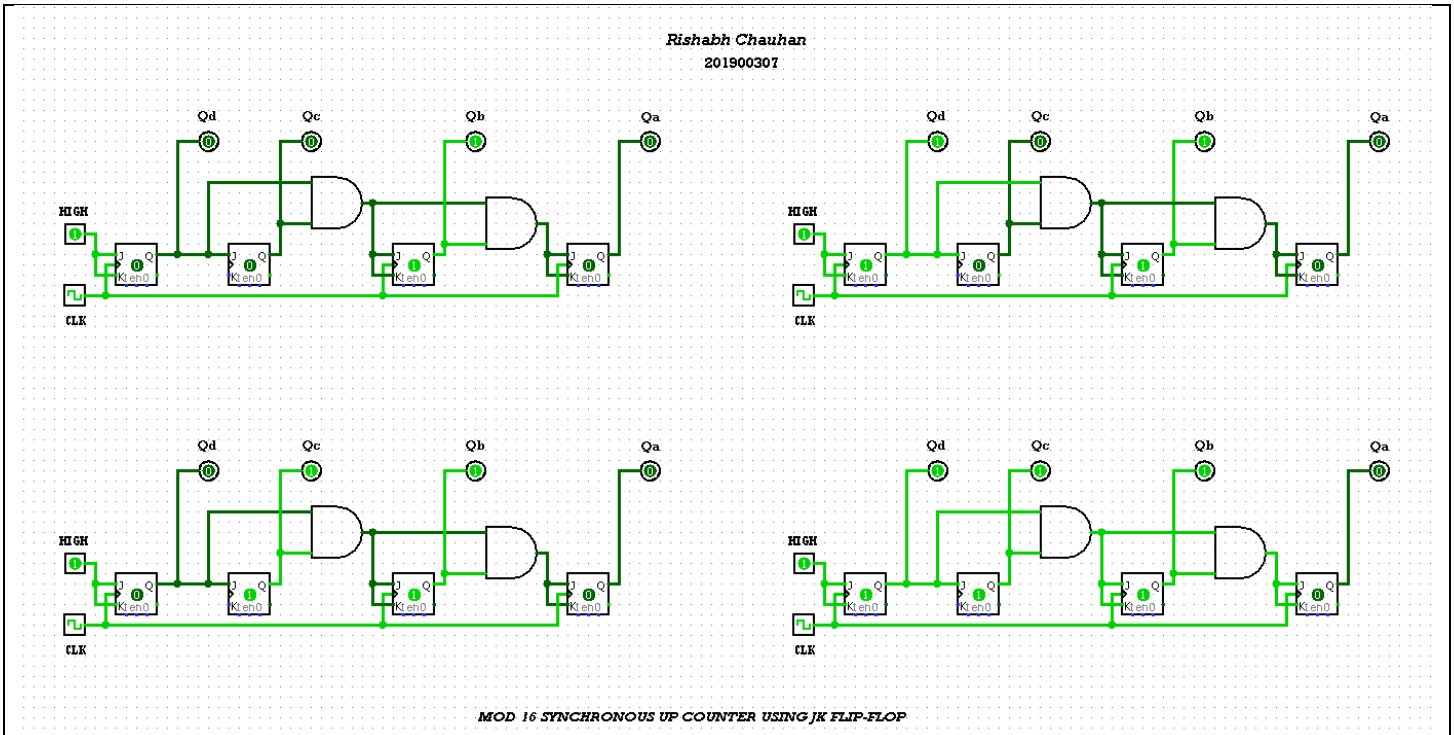
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: *Rishabh*

Date: 20/10/2020

Student's worksheet-2



Student's observation and conclusion:

A MOD 16 Synchronous UP Counter (also known as Parallel Counter) was constructed using JK Flip-Flop. A constant input (1) is provided while the clock is toggled. D is assumed to be the Least Significant Bit (LSB) while A is assumed to be the Most Significant Bit (MSB).

Toggling the clock from ON (1) to OFF (0) to ON (1) changes the result. The obtained result cycles through the various stages in accordance to the theory.

Conversions:

- **0100-0101**
- **0101-0110**
- **0110-0111**
- **0111-1000**

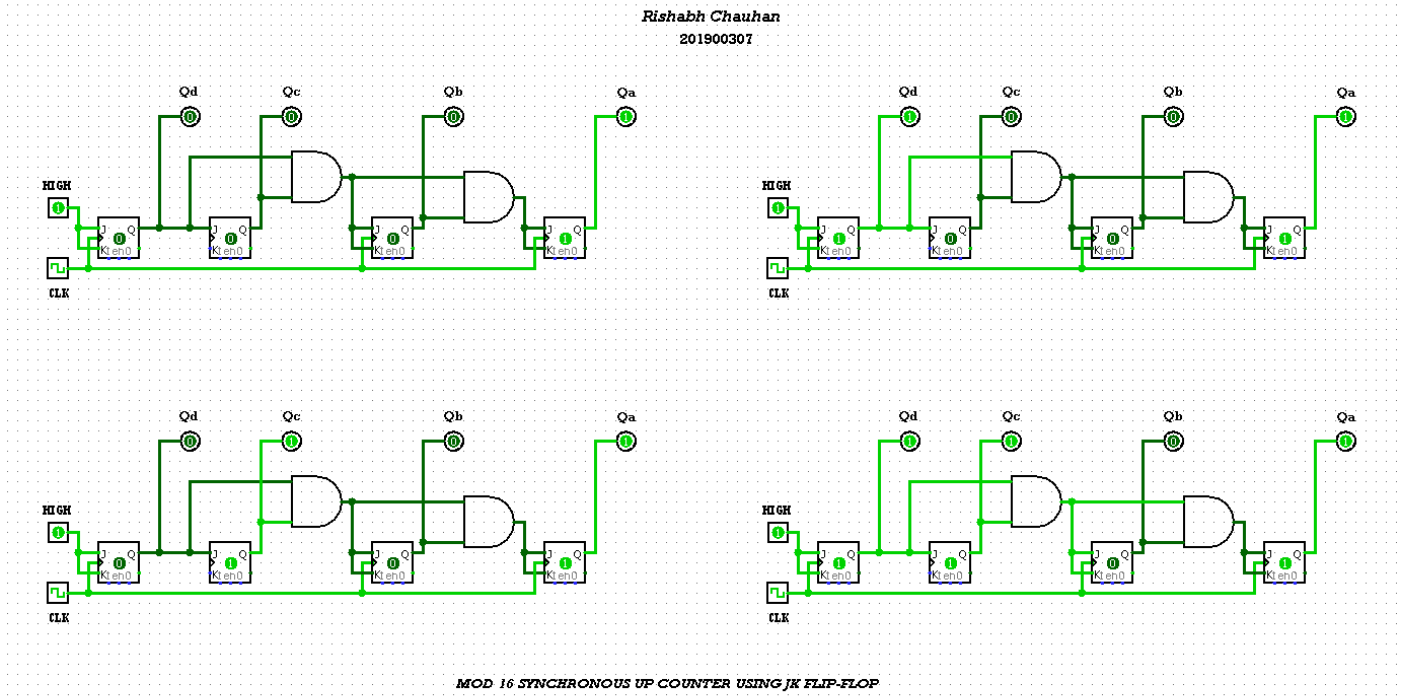
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: Rishabh

Date: 20/10/2020

Student's worksheet-3



Student's observation and conclusion:

A MOD 16 Synchronous UP Counter (also known as Parallel Counter) was constructed using JK Flip-Flop. A constant input (1) is provided while the clock is toggled. D is assumed to be the Least Significant Bit (LSB) while A is assumed to be the Most Significant Bit (MSB).

Toggling the clock from ON (1) to OFF (0) to ON (1) changes the result. The obtained result cycles through the various stages in accordance to the theory.

Conversions:

- **1000-1001**
- **1001-1010**
- **1010-1011**
- **1011-1100**

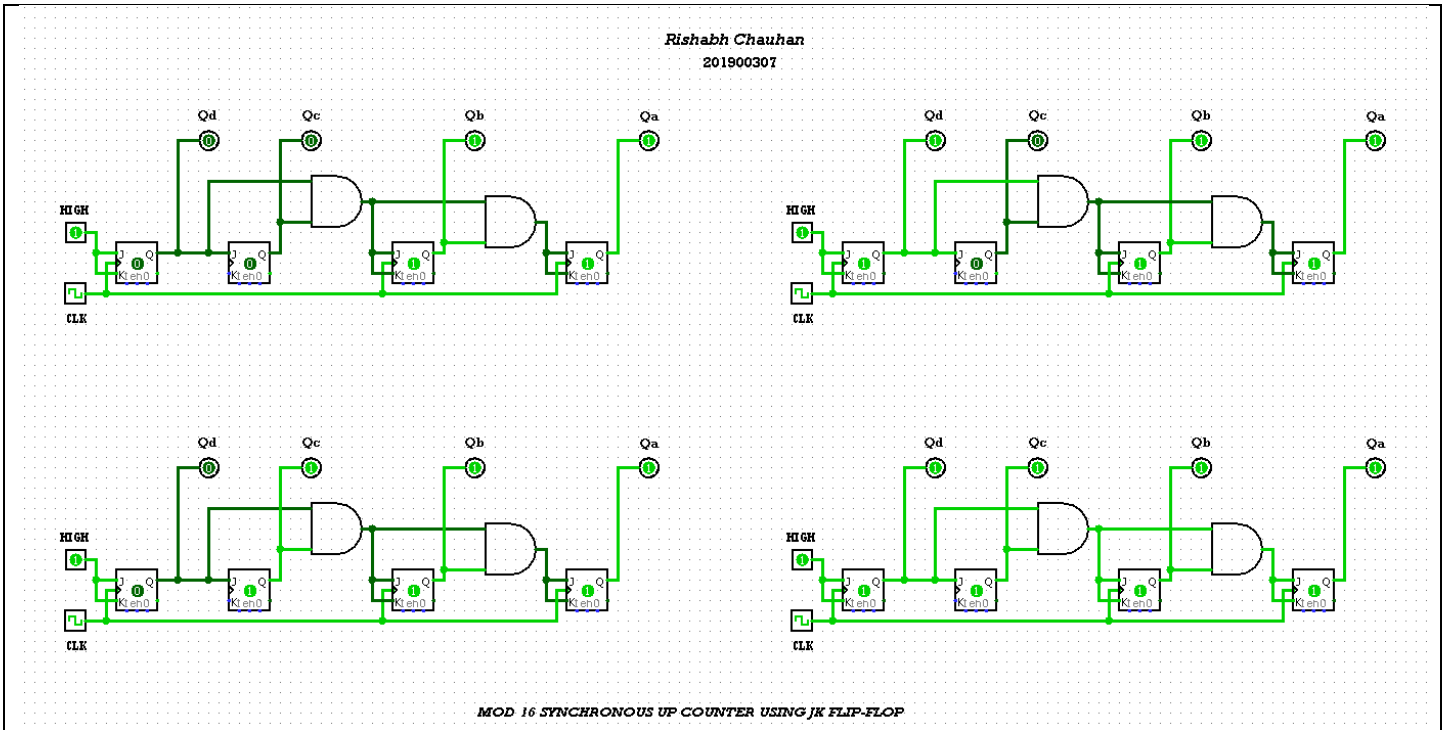
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: *Rishabh*

Date: 20/10/2020

Student's worksheet-4



Student's observation and conclusion:

A MOD 16 Synchronous UP Counter (also known as Parallel Counter) was constructed using JK Flip-Flop. A constant input (1) is provided while the clock is toggled. D is assumed to be the Least Significant Bit (LSB) while A is assumed to be the Most Significant Bit (MSB).

Toggling the clock from ON (1) to OFF (0) to ON (1) changes the result. The obtained result cycles through the various stages in accordance to the theory.

Conversions:

- **1100-1101**
- **1101-1110**
- **1110-1111**
- **1111-0000 (CONTINUES THE FIRST CASE AGAIN.)**

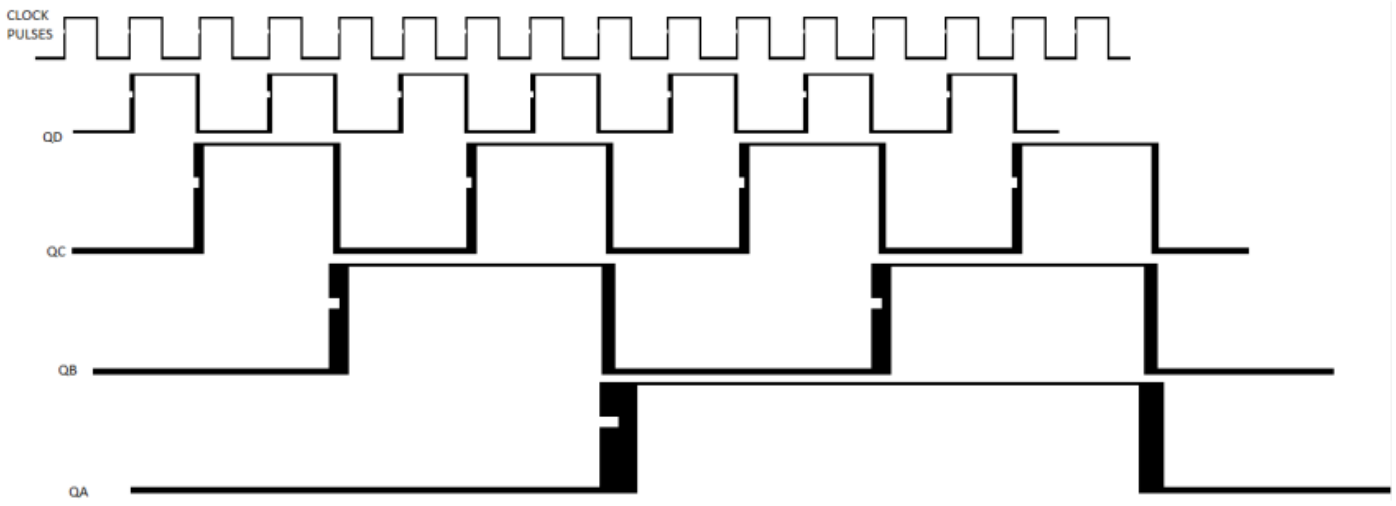
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: *Rishabh*

Date: 20/10/2020

Student's worksheet-5



Student's observation and conclusion:

•This is a timing diagram of a 4-bit synchronous counter.

•It counts sequentially on every clock pulse the resulting outputs count upwards from 0 (0000) to 15 (1111).

•Therefore, this type of counter is also known as a 4-bit Synchronous Up Counter.

•From the timing diagram it is evident that the first flip flop toggle on every clock pulse.

•Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.

THIS 4-BIT SYNCHRONOUS COUNTER COUNTS SEQUENTIALLY ON EVERY CLOCK PULSE THE RESULTING OUTPUTS COUNT UPWARDS FROM 1 (0000) TO 16 (1111). THEREFORE, THIS TYPE OF COUNTER IS ALSO KNOWN AS A 4-BIT SYNCHRONOUS UP COUNTER.

Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: *Rishabh*

Date: 20/10/2020