EXPERIMENT NUMBER: 8

EXPERIMENT NAME: Design of a mod 16 asynchronous counter

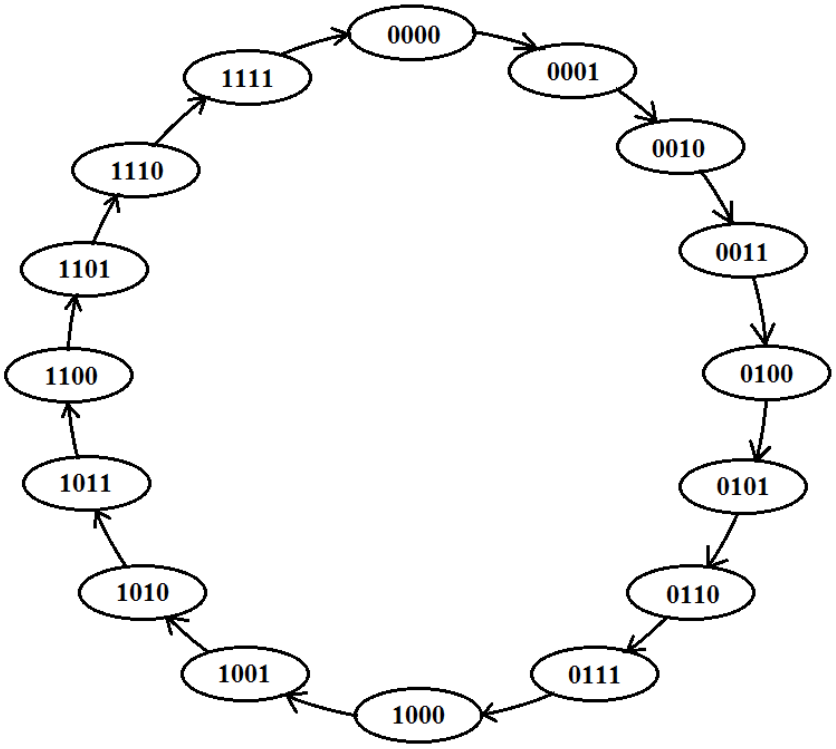
AIM: Design a mod 16 asynchronous up counter.

APPARATUS REQUIRED:

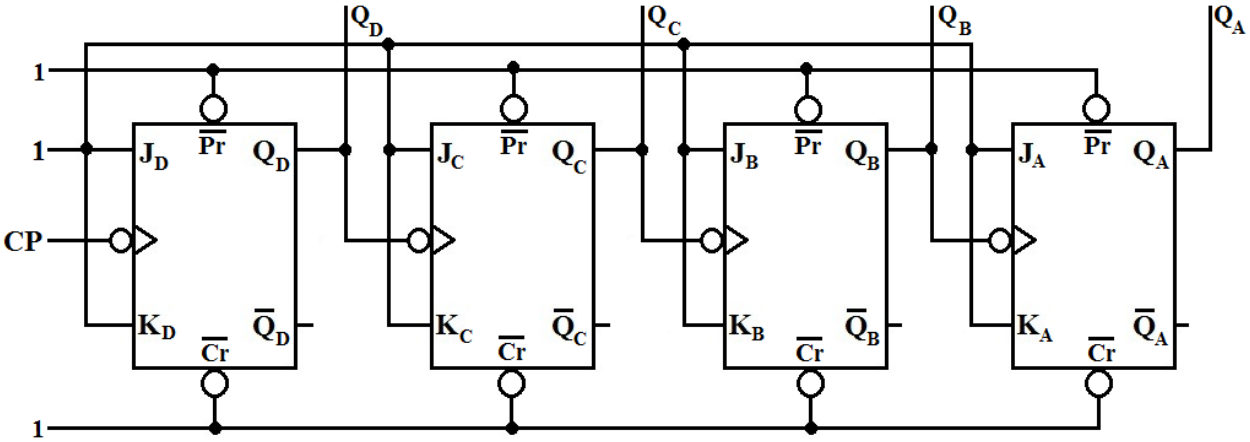
Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	JK Flip-flop	IC 7473/IC 7476	2
2.	IC TRAINER KIT	-	1
3.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

STATE DIAGRAM:



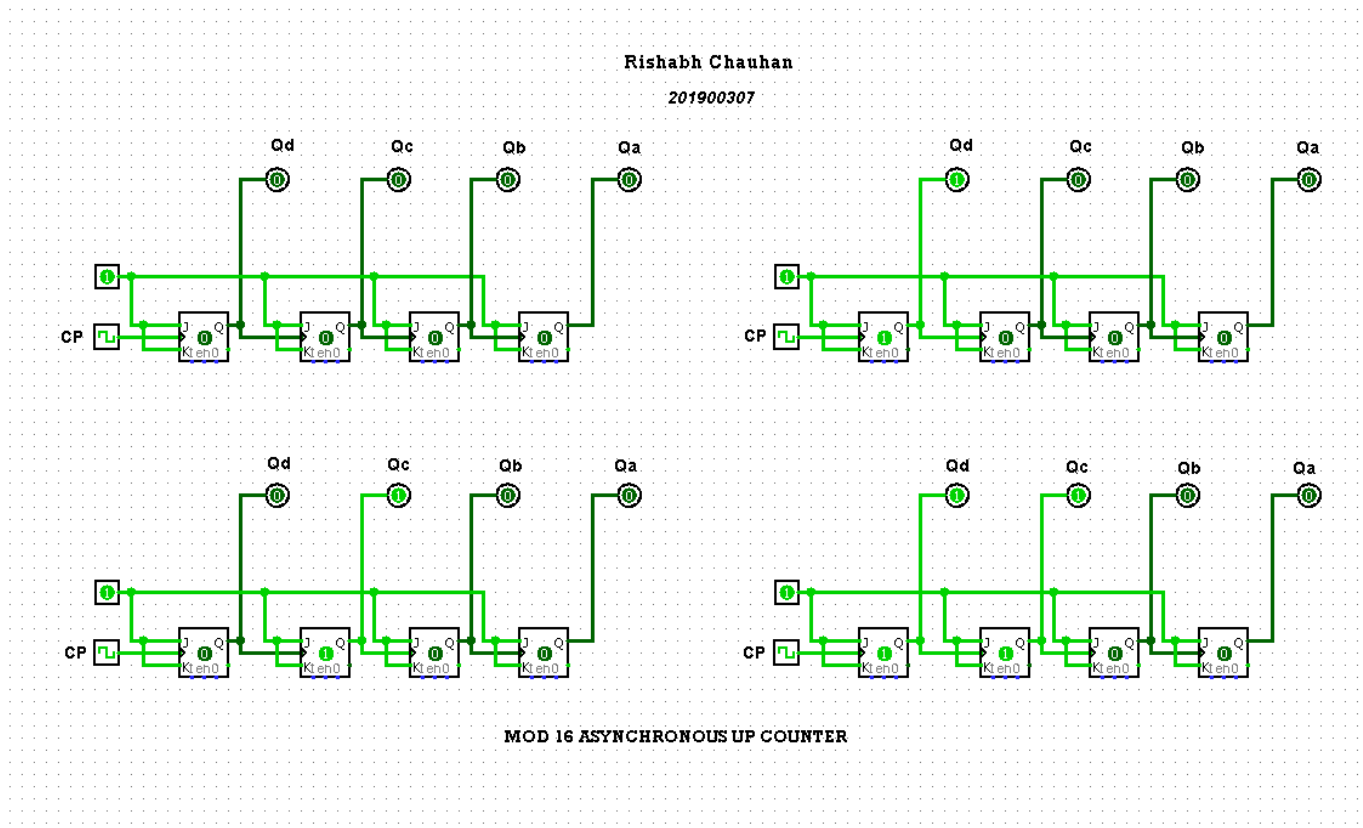
CIRCUIT DIAGRAM OF A MOD 16 ASYNCHRONOUS UP COUNTER:



PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet-1



Student's observation and conclusion:

We simply connect the clock input of each flip-flop to the Q output of the flip-flop before it, so that when the bit before it changes from 1 to 0, the "falling edge" of that signal would "clock" the next flip-flop to toggle the next bit.

The figures above represent the circuit diagram of a mod 16 asynchronous up counter made with JK flip-flop. A counter is used to count specific events in the circuit. Here we have four outputs Q_A, Q_B, Q_C, Q_D.
With Q_D being the most significant bit in the circuits. And in the following circuit these conversions happen:
0000-1000 1000-0100
0100-1100

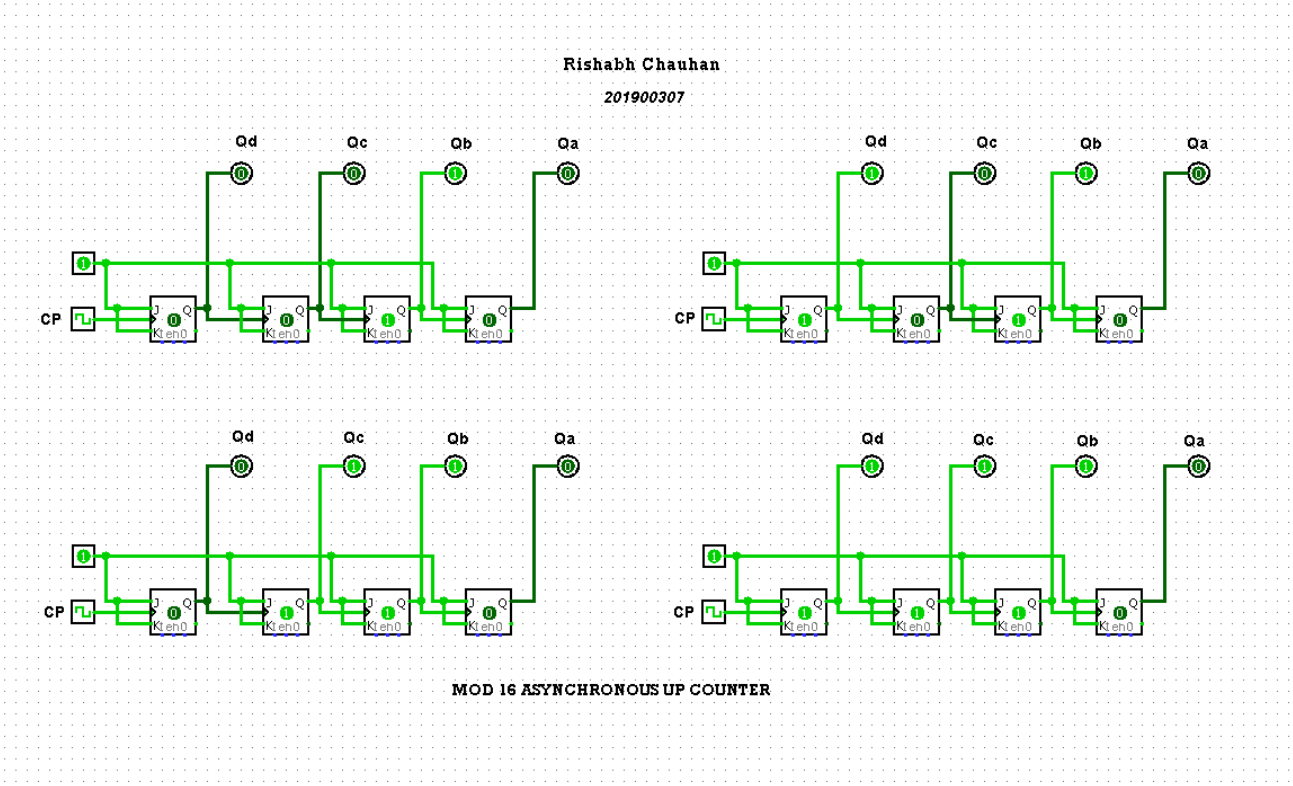
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: *Rishabh*

Date: 29/09/2020

Student's worksheet-2



Student's observation and conclusion:

We simply connect the clock input of each flip-flop to the Q output of the flip-flop before it, so that when the bit before it changes from 1 to 0, the "falling edge" of that signal would "clock" the next flip-flop to toggle the next bit.

The figures above represent the circuit diagram of a mod 16 asynchronous up counter made with JK flip-flop. A counter is used to count specific events in the circuit. Here we have four outputs Q_A, Q_B, Q_C, Q_D.
With Q_D being the most significant bit in the circuits. And in the following circuit these conversions happen:
1100-0010 0010-1010
1010-0110 0110-1110

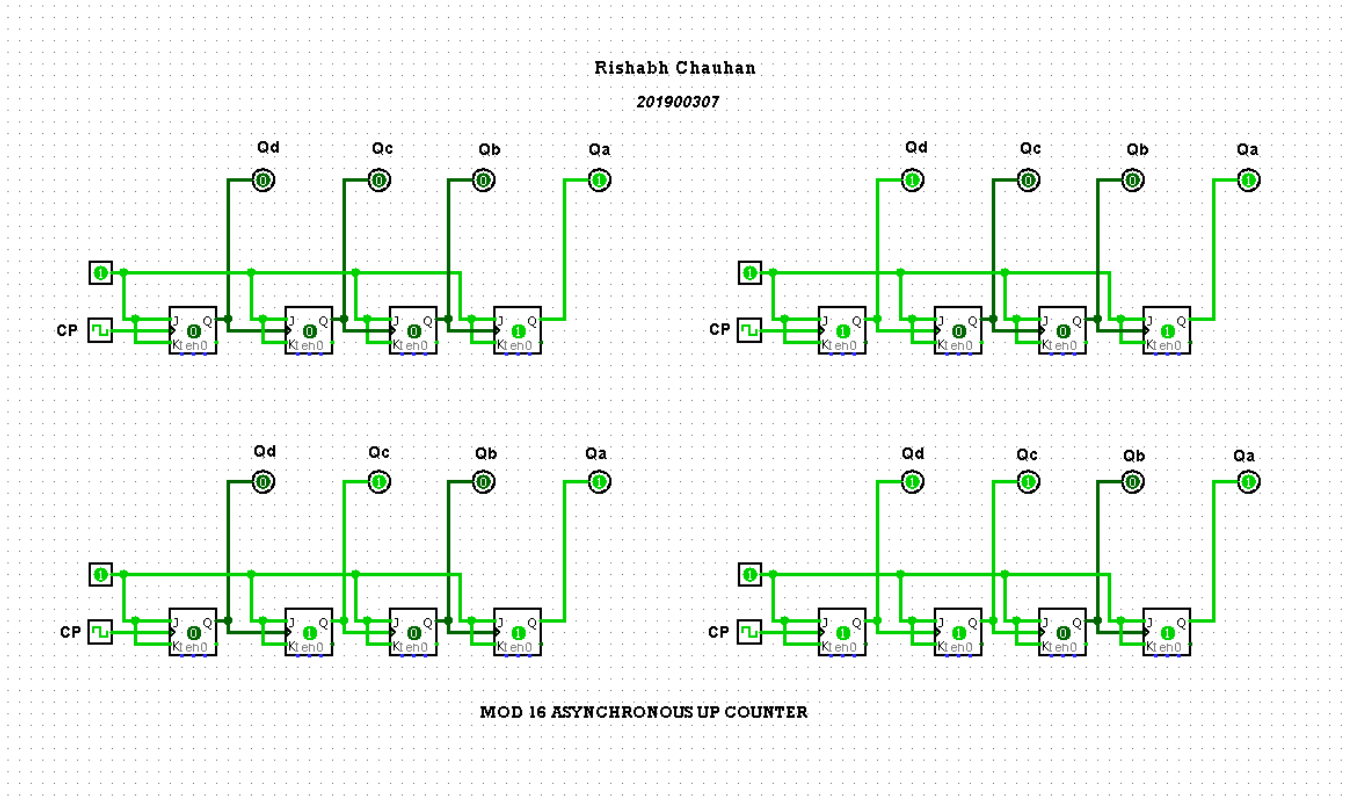
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: Rishabh

Date: 29/09/2020

Student's worksheet-3



Student's observation and conclusion:

We simply connect the clock input of each flip-flop to the Q output of the flip-flop before it, so that when the bit before it changes from 1 to 0, the "falling edge" of that signal would "clock" the next flip-flop to toggle the next bit.

The figures above represent the circuit diagram of a mod 16 asynchronous up counter made with JK flip-flop. A counter is used to count specific events in the circuit. Here we have four outputs Q_A, Q_B, Q_C, Q_D.
With Q_D being the most significant bit in the circuits. And in the following circuit these conversions happen:
1110-0001 0001-1001
1001-0101 0101-1101

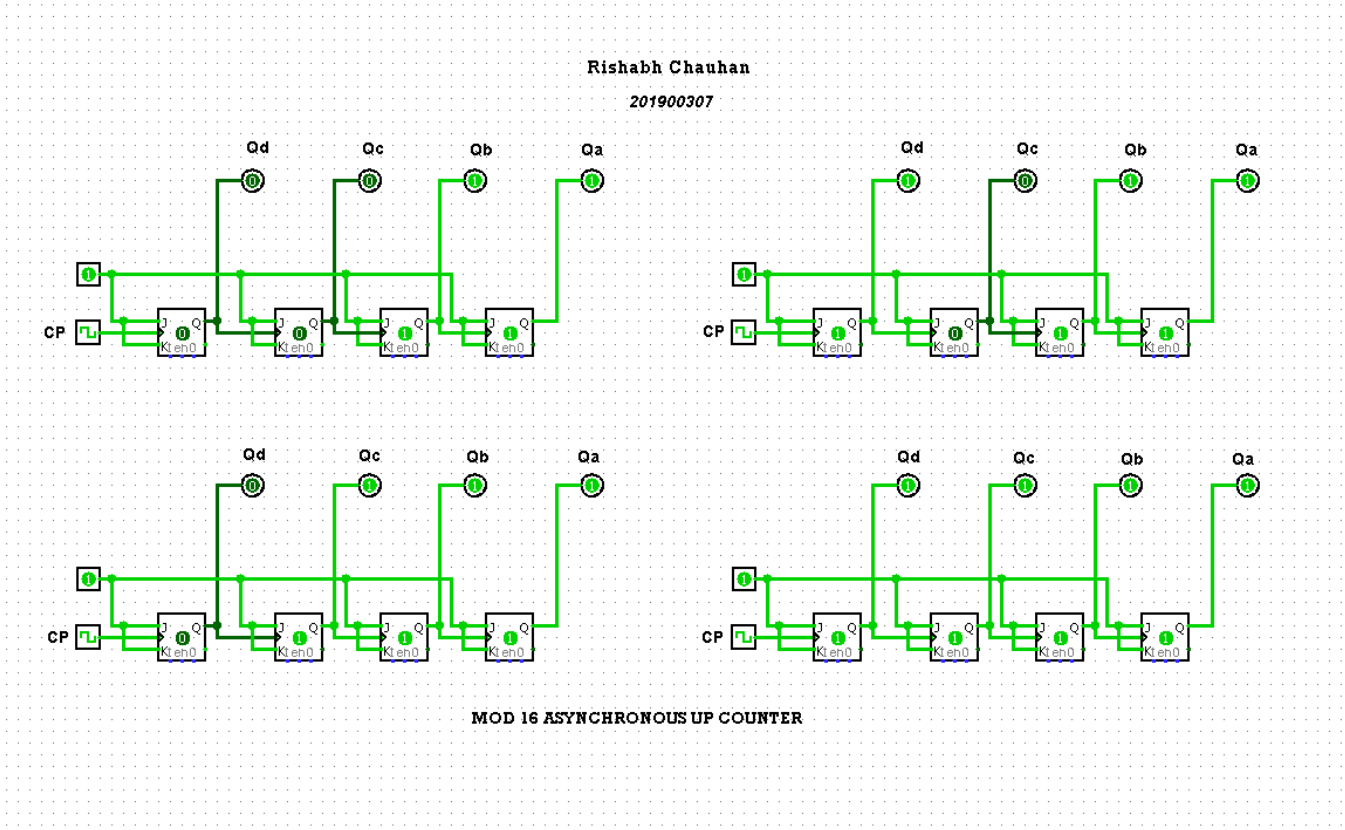
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: Rishabh

Date: 29/09/2020

Student's worksheet-4



Student's observation and conclusion:

We simply connect the clock input of each flip-flop to the Q output of the flip-flop before it, so that when the bit before it changes from 1 to 0, the "falling edge" of that signal would "clock" the next flip-flop to toggle the next bit.

The figures above represent the circuit diagram of a mod 16 asynchronous up counter made with JK flip-flop. A counter is used to count specific events in the circuit. Here we have four outputs Q_A, Q_B, Q_C, Q_D.
With Q_D being the most significant bit in the circuits. And in the following circuit these conversions happen:
1101-0011 0011-1011
1011-0111 0111-1111

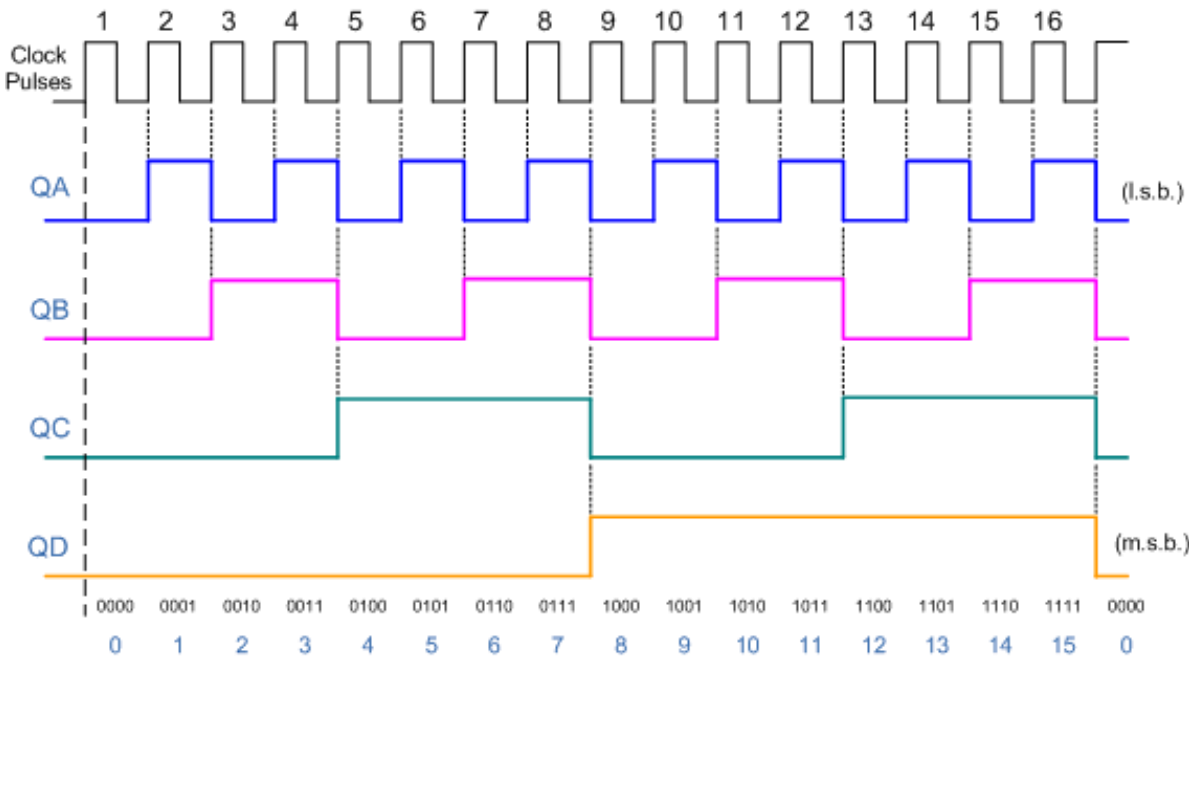
Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: Rishabh

Date: 29/09/2020

Student's worksheet-5



Student's observation and conclusion:

Each bit in this four-bit sequence toggles when the bit before it (the bit having a lesser significance, or place-weight), toggles in a particular direction: from 1 to 0.

Small arrows indicate those points in the sequence where a bit toggles, the head of the arrow pointing to the previous bit transitioning from a "high" (1) state to a "low" (0) state.

In the 4-bit counter above the output of each flip-flop changes state on the falling edge (1-to-0 transition) of the CLK input which is triggered by the Q output of the previous flip-flop, rather than by the Q output as in the up counter configuration. As a result, each flip-flop will change state when the previous one changes from 0 to 1 at its output, instead of changing from 1 to 0.

Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: *Rishabh*

Date: 29/09/2020