EXPERIMENT NUMBER: 3

EXPERIMENT NAME: Design of a (i) Half adder and (ii) Half subtractor

AIM: To design a Half Adder and Half subtractor circuit using logic gates and to verify them using truth tables.

APPARATUS REQUIRED:

SL. NO.	COMPONENT	SPECIFICATION	QUANTITY
1.	AND gate	IC 7408	1
2.	X-OR gate	IC 7486	1
3.	NOT gate	IC 7404	1
4.	OR gate	IC 7432	1
5.	IC trainer kit	-	1
6.	Connecting Wires	-	As required

THEORY:

HALF ADDER:

A half adder is a combinational circuit that can add two bits and produces the sum of the input bits as the result or output. A half adder has two inputs for the two bits to be added and two outputs - one is the sum 'S' and other one is the carry 'C'. A half adder cannot consider a previous carry (third input bit). Due to this limitation, a half adder circuit can't be used in cascade adder. Two half adders can be combined together to form a full adder.

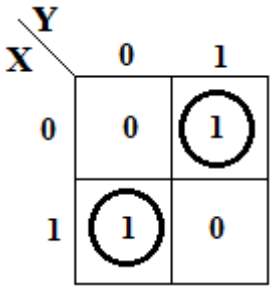
HALF SUBTRACTOR:

The half subtractor is a combinational circuit that takes two input bits and subtracts one bit from the other. Half subtractor produces the result of the subtraction of the two bits through the two outputs – the Borrow 'B' and the Difference 'D'.

TRUTH TABLE OF A HALF ADDER:

Input		Output	
X	Y	C (Carry)	S (Sum)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

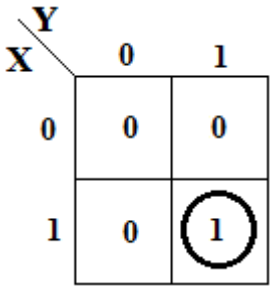
K-Map for S (Sum)



$S = X\overline{Y} + \overline{X}Y$

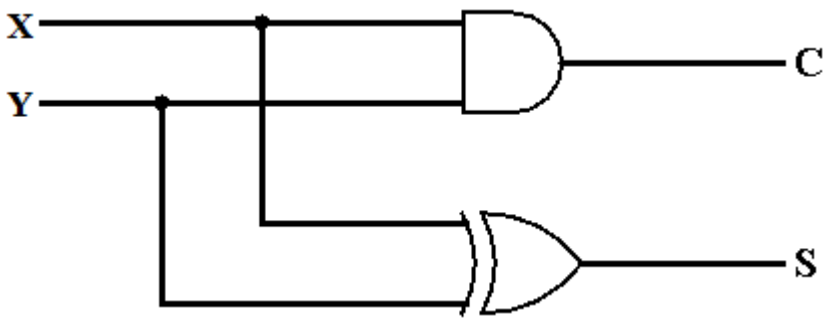
$S = X \oplus Y$

K-Map for C (Carry)



C=AB

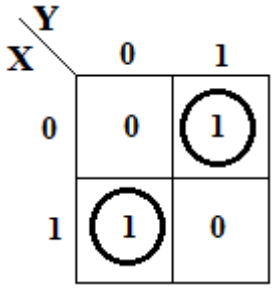
CIRCUIT DIAGRAM OF A HALF ADDER:



TRUTH TABLE OF A HALF SUBTRACTOR:

Input		Output	
X	**Y**	**B (Borrow)**	**D (Difference)**
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

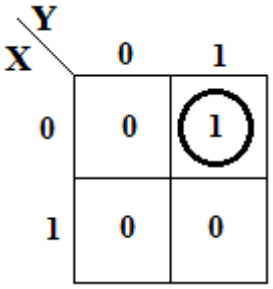
K-Map for D (Difference):



$D = X\overline{Y} + \overline{X}Y$

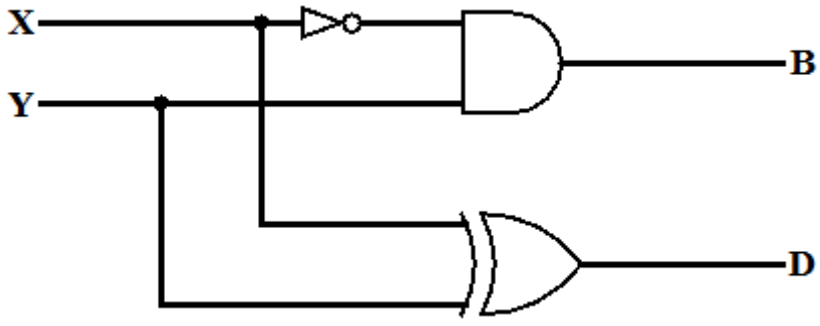
$D = X \oplus Y$

K-Map for B (Borrow):



$B = \overline{X}Y$

CIRCUIT DIAGRAM OF A HALF SUBTRACTOR:



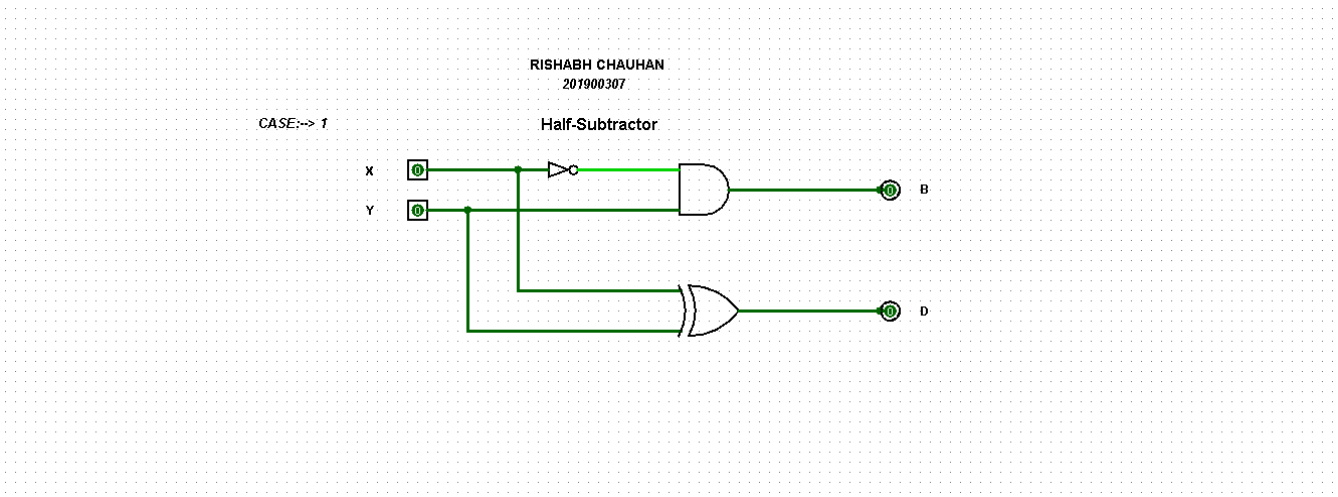
DESIGN PROCEDURE:

1. Truth tables of the (i) Half adder and (ii) Half subtractor are prepared.
2. K-map for each output variable present in the truth tables is drawn.
3. Simplified expression for each output variable is obtained.
4. Circuit diagram is drawn as per the simplified expressions of the output variables obtained in step 3.

PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet-1



Student's observation and conclusion:

- If we subtract two zeroes' [0-0]. Then the DIFFERENCE(D) = 0
- In this case no BORROW(B) is required, so (B) = 0.

- It is the combination of two gates [XOR and NAND] gate. And it performs subtraction of two digits in the binary system.

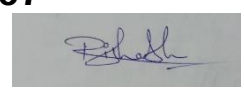
- DIFFERENCE (D) is the output of XOR gate. **D =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And BORROW (B) is the output of NAND gate. **B =** $\overline{X}.Y$

- In this **"HALF SUBTRACTER"** if we do SUBSTRACTION of two binary digits. The output will show two sub outputs in which one is DIFFERENCE(D) and the other is BORROW(B).

Name: Rishabh Chauhan

Reg. No.: 201900307

Digital Signature: 

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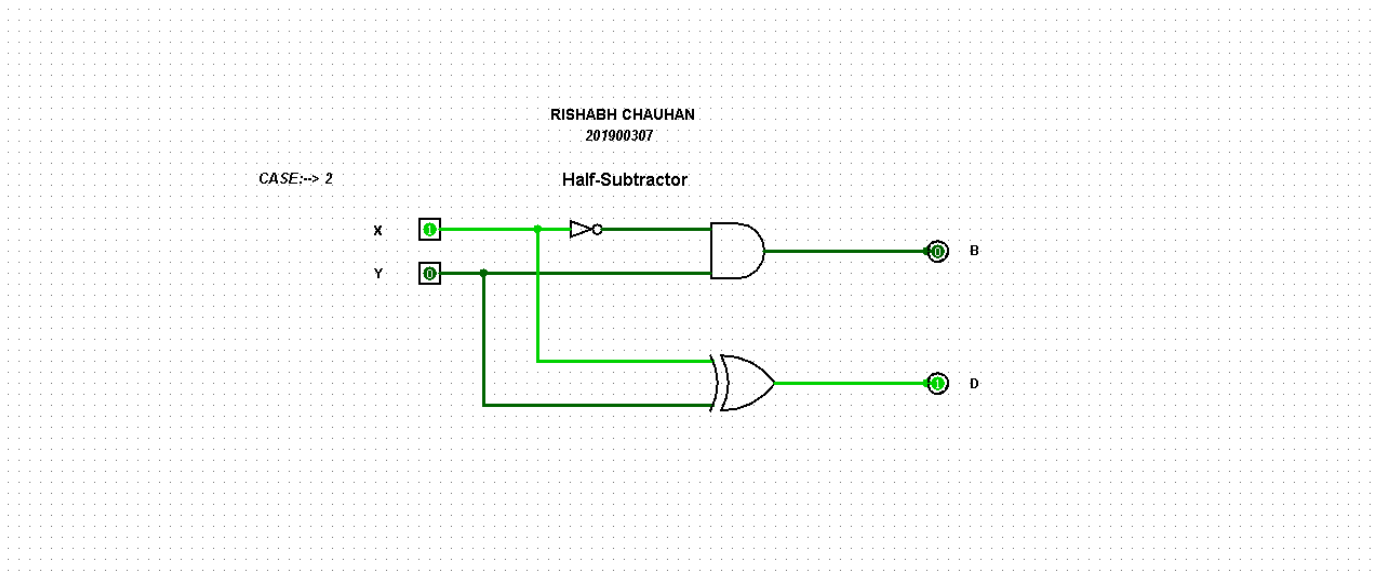
Student's worksheet-2



Student's observation and conclusion:

- If we subtract 1 and 0 [1-0]. The DIFFERENCE(D) = 1. And in this case no BORROW(B) is needed.
- And we get the equation as E = {**D =** $\overline{X+Y}$} i.e. ($\overline{X}Y + X\overline{Y}$).

- It is the combination of two gates [XOR and NAND] gate. And it performs subtraction of two digits in the binary system.

- DIFFERENCE (D) is the output of XOR gate. **D =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And BORROW (B) is the output of NAND gate. **B =** $\overline{X}.Y$

- In this **"HALF SUBTRACTER"** if we do SUBSTRACTION of two binary digits. The output will show two sub outputs in which one is DIFFERENCE(D) and the other is BORROW(B).

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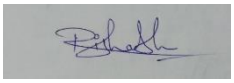
Digital Signature: 

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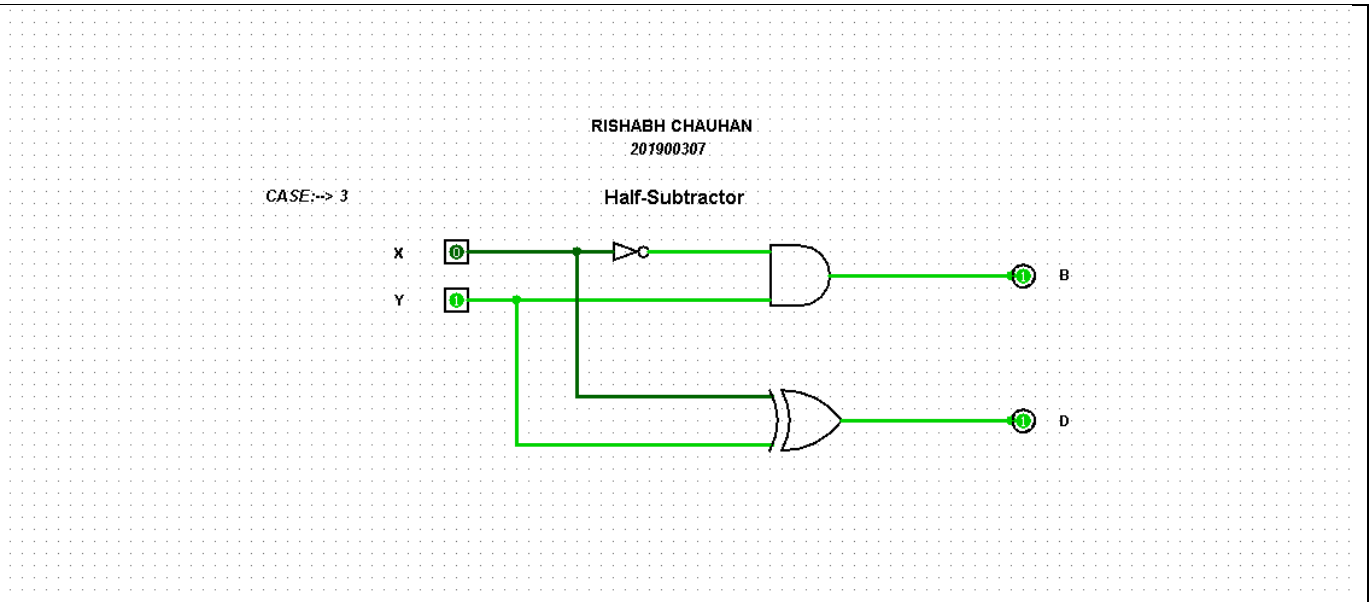
Student's worksheet-3



Student's observation and conclusion:

- If we subtract 0 and 1 [0-1], which is not possible, so we BORROW(B) = 1. And now it becomes 1 0 which is the binary form of 2 now we subtract 2 from 1 [2-1]. And the DIFFERENCE(D) = 1.
- So, BORROW B = $\overline{X}.Y$

- It is the combination of two gates [XOR and NAND] gate. And it performs subtraction of two digits in the binary system.

- DIFFERENCE (D) is the output of XOR gate. **D =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And BORROW (B) is the output of NAND gate. **B =** $\overline{X}.Y$

- In this **"HALF SUBTRACTER"** if we do SUBSTRACTION of two binary digits. The output will show two sub outputs in which one is DIFFERENCE(D) and the other is BORROW(B).

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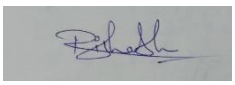
Digital Signature: 

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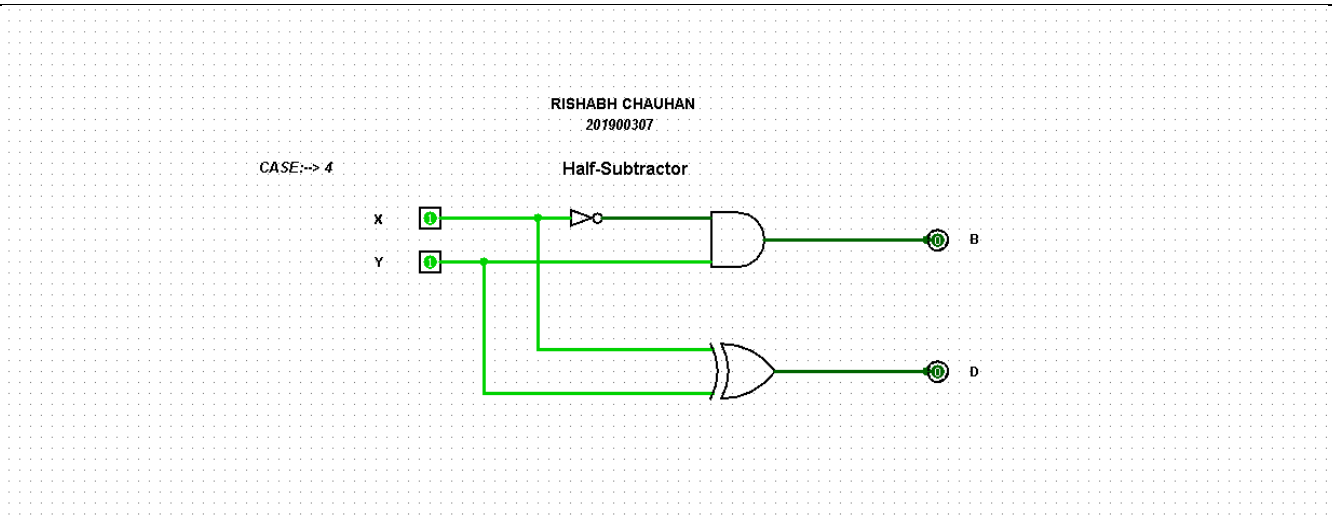
Student's worksheet-4



Student's observation and conclusion:

- If we subtract two one's [1-1]. The DIFFERENCE(D) is 0.
- In this case no BORROW (B) is required B = 0.

- It is the combination of two gates [XOR and NAND] gate. And it performs subtraction of two digits in the binary system.

- DIFFERENCE (D) is the output of XOR gate. **D =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And BORROW (B) is the output of NAND gate. **B =** $\overline{X}.Y$

- In this **"HALF SUBTRACTER"** if we do SUBSTRACTION of two binary digits. The output will show two sub outputs in which one is DIFFERENCE(D) and the other is BORROW(B).

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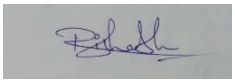
Digital Signature: 

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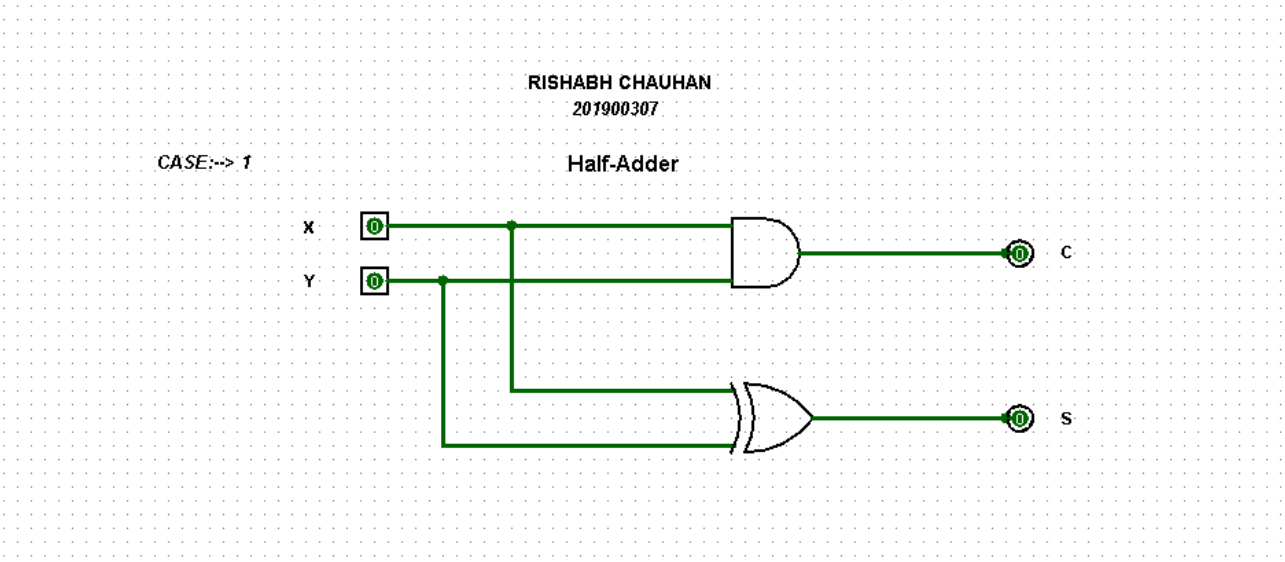
Student's worksheet-5



Student's observation and conclusion:

- If we add two binary zeroes' [0+0]. The SUM(S) = 0, in the binary system.
- And in this case CARRY(C) = 0. To the next significant bit. As no carry is needed.

- It is the combination of two gates [XOR and AND] gate. And it performs addition of two digits in the binary system.

- Binary SUM(S) is the output of XOR gate, **S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And CARRY(C) is the output of AND gate, **C =** $X.Y$

- In this **"HALF ADDER"** if we do addition of two binary digits. The output will show two sub outputs in which one is SUM(S) and the other is CARRY(C).

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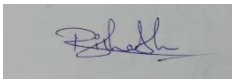
Digital Signature: 

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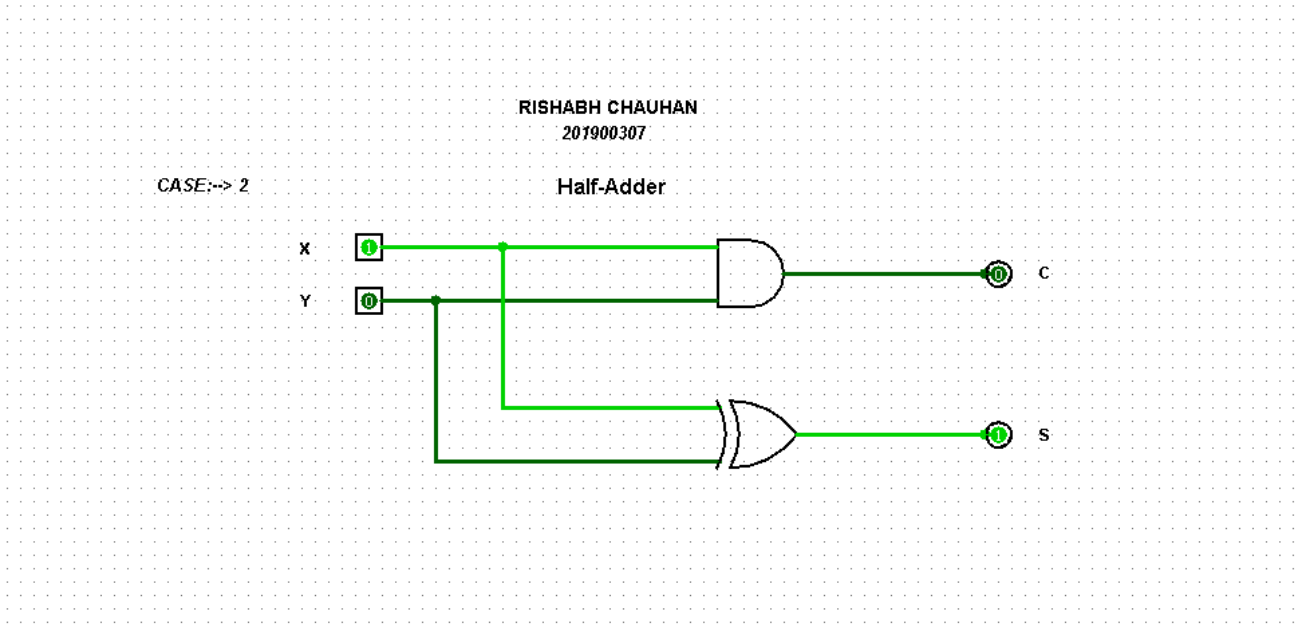
Student's worksheet-6



Student's observation and conclusion:

- If we add 1 and 0 [1+0]. The SUM(S) = 1, in the binary system.
- And in this case CARRY(C) = 0. To the next significant bit. As no carry is needed.
- And the equation (E) = {**S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$)}.

- It is the combination of two gates [XOR and AND] gate. And it performs addition of two digits in the binary system.

- Binary SUM(S) is the output of XOR gate, **S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And CARRY(C) is the output of AND gate, **C =** $X.Y$

- In this **"HALF ADDER"** if we do addition of two binary digits. The output will show two sub outputs in which one is SUM(S) and the other is CARRY(C).

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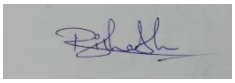
Digital Signature: 

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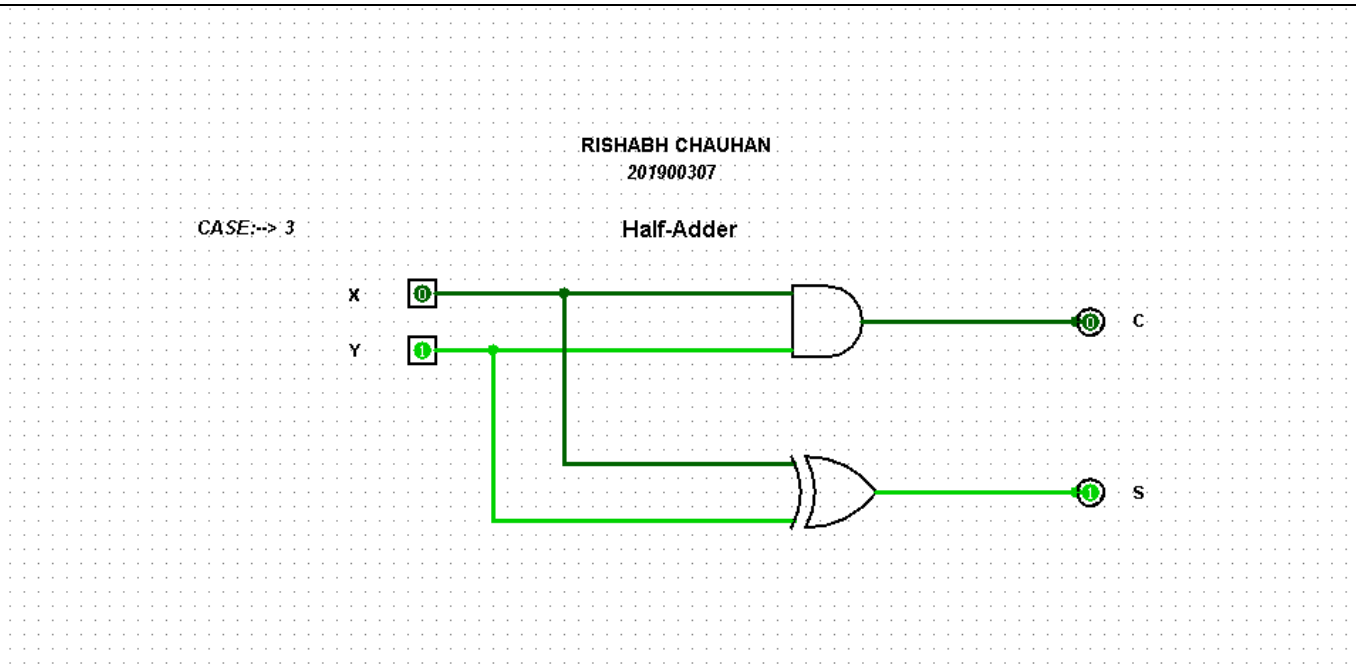
Student's worksheet-7



Student's observation and conclusion:

- If we add 0 and 1 [0+1]. The SUM(S) = 1, in the binary system.
- And in this case CARRY(C) = 0. To the next significant bit. As no carry is needed.
- And the equation (E) = {**S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$)}.

- It is the combination of two gates [XOR and AND] gate. And it performs addition of two digits in the binary system.

- Binary SUM(S) is the output of XOR gate, **S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And CARRY(C) is the output of AND gate, **C =** $X.Y$

- In this **"HALF ADDER"** if we do addition of two binary digits. The output will show two sub outputs in which one is SUM(S) and the other is CARRY(C).

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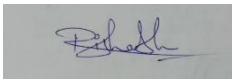
Digital Signature: 

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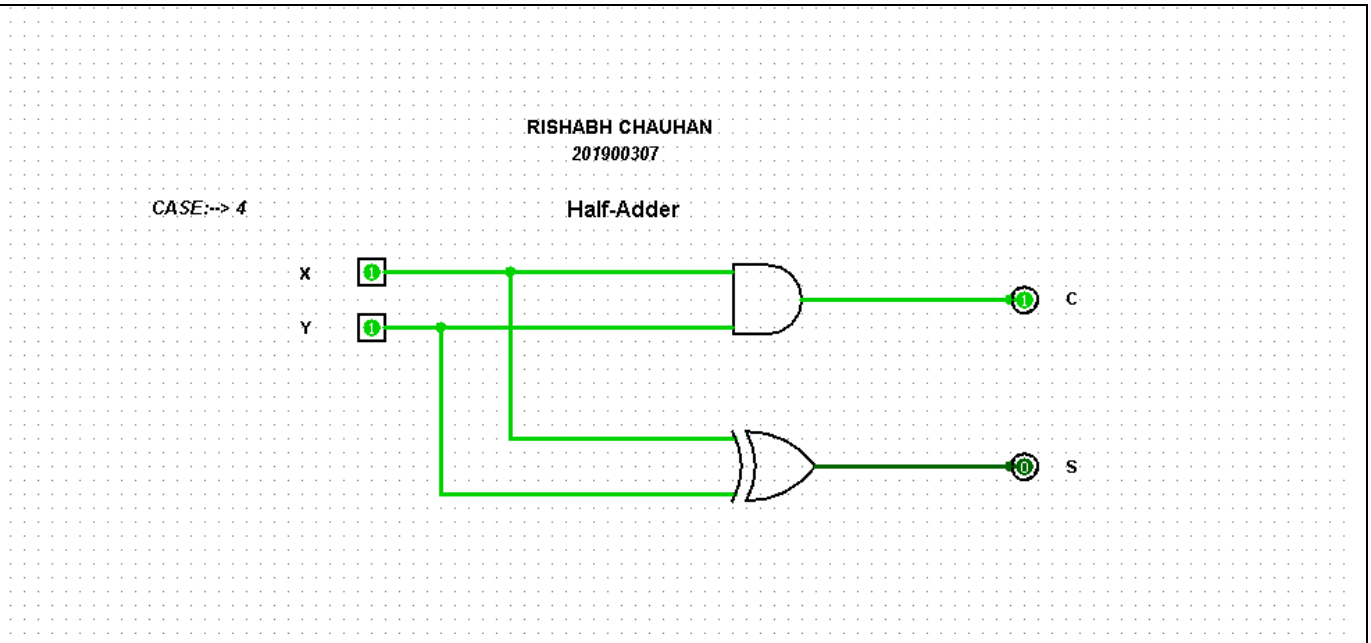
Student's worksheet-8



Student's observation and conclusion:

- If we add 1 and 1 [1+1]. The SUM(S) = 0, in the binary system.
- When 1 and 1 are added the SUM(S) = 0 and 1 is carried [CARRY(C) = 1] to the next bit.
- Thus, we get the equation (E) = {**S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$)}.

- It is the combination of two gates [XOR and AND] gate. And it performs addition of two digits in the binary system.

- Binary SUM(S) is the output of XOR gate, **S =** $\overline{X+Y}$ i.e. ($\overline{X}Y + X\overline{Y}$).

- And CARRY(C) is the output of AND gate, **C =** $X.Y$

- In this **"HALF ADDER"** if we do addition of two binary digits. The output will show two sub outputs in which one is SUM(S) and the other is CARRY(C).

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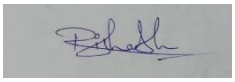
Digital Signature: 

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