EXPERIMENT NUMBER: 6

EXPERIMENT NAME: Design of a 4:1 Multiplexer.

AIM: To design a 4:1 Multiplexer using logic gates and to verify its operation.

APPARATUS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	AND GATE	IC 7408	2
2.	NOT GATE	IC 7404	1
3.	OR GATE	IC 7432	1
4.	IC TRAINER KIT	-	1
5.	CONNECTING WIRES	-	AS REQUIRED

THEORY:

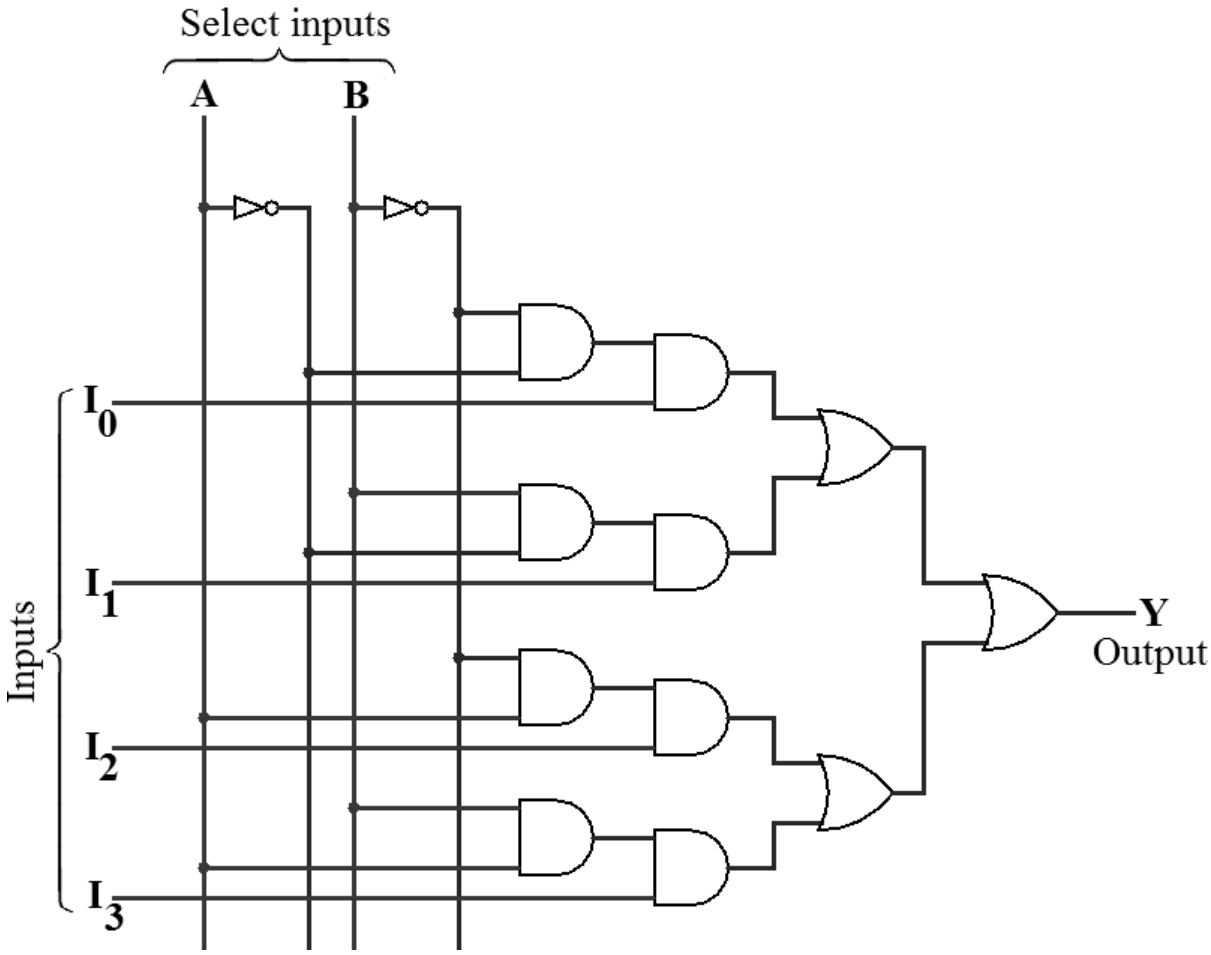
A digital multiplexer is a combinational circuit that receives binary information from many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. A multiplexer has n number of select lines, 2^n number of input lines and a single output line. At a time, any one of the inputs is connected with the output line through the multiplexer. Combination in the select input determines the input which will be connected with the output.

FUNCTION TABLE:

SELECT INPUTS		OUTPUT
A	**B**	**Y**
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = I_0 \overline{A}\,\overline{B} + I_1 \overline{A}\,B + I_2 A\,\overline{B} + I_3 A\,B$$

CIRCUIT DIAGRAM OF A 4:1 MULTIPLEXER:



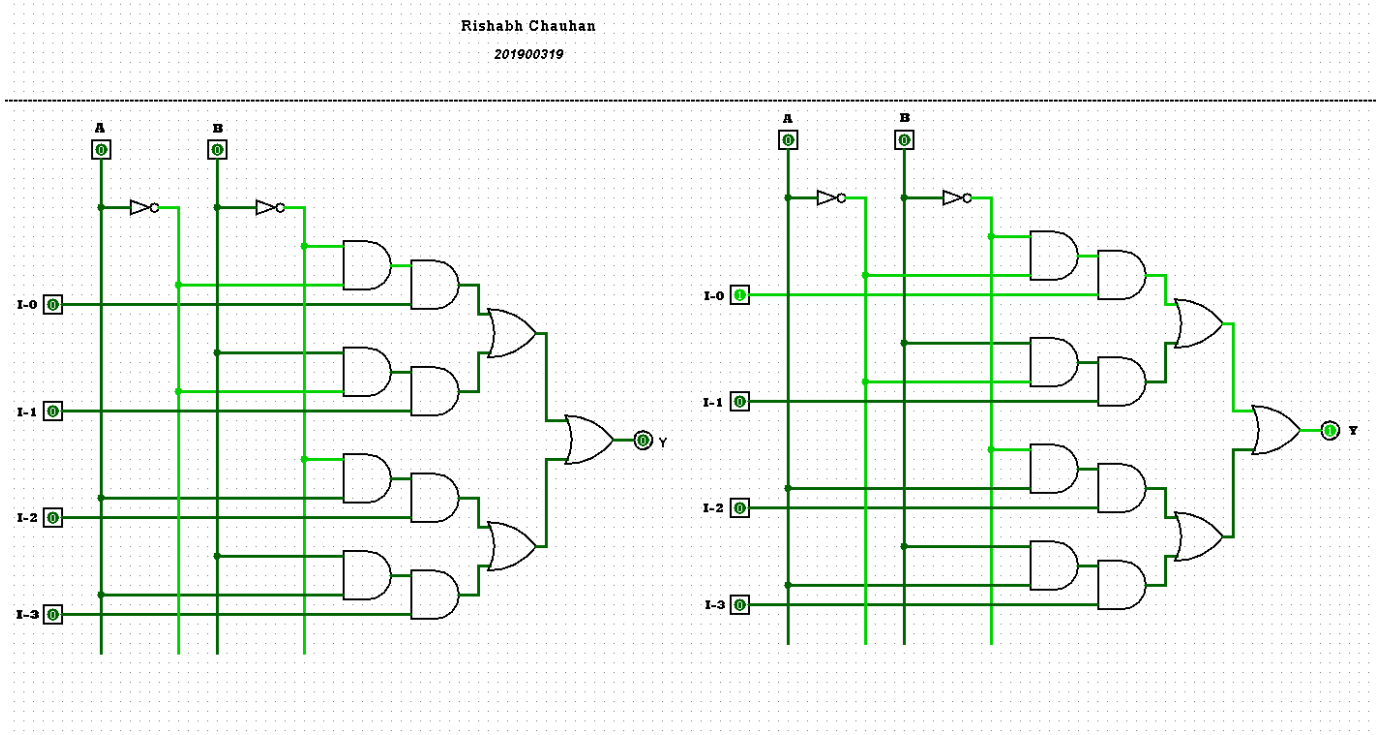
DESIGN PROCEDURE:

1. Function table of 4:1 multiplexer is prepared.
2. From the function table, output expression of the multiplexer is found.
3. Circuit diagram is drawn as per the output expression obtained in step 2.

PRACTICAL PROCEDURE:

1. ICs are placed properly on the bread board of the IC trainer kit.
2. Connections are made as per the designed circuit diagram.
3. Power supply to the board is turned ON.
4. Circuit is verified as per the truth table of the circuit.

Student's worksheet-1



Student's observation and conclusion:

- **A 4-to-1 multiplexer consists of four data input lines marked as I_0 to I_3, two select input lines, marked as A, B and a single output line Y.**

- **The input combination on select input line (A & B) selects one of input (I_0 to I_3) to the output.**

- **When the selection line A represents 0 and selection line B also represents 0 then the input line which will be selected to pass from multiplexer will be I_0. Thus, MUX will be a short circuit for input line I_0 and will be open circuited for other input lines.**

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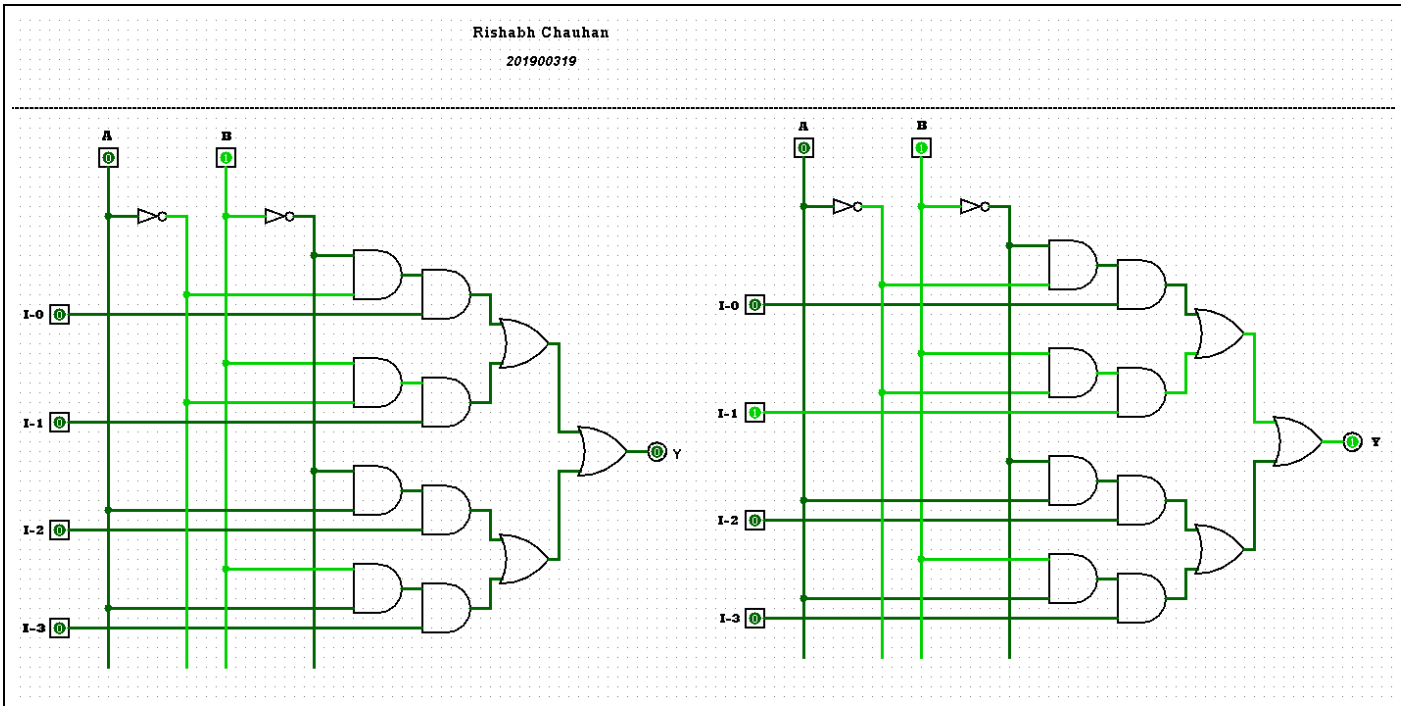
Student's worksheet-2



Student's observation and conclusion:

- **A 4-to-1 multiplexer consists of four data input lines marked as I_0 to I_3, two select input lines, marked as A, B and a single output line Y.**

- **The input combination on select input line (A & B) selects one of input (I_0 to I_3) to the output.**

- **When the selection line A represents 0 while selection line B represents 1, then the input line which will be selected will be I_1. In this case, MUX will behave as a short circuit for input line I_1 while it will behave as an open circuit for other input lines.**

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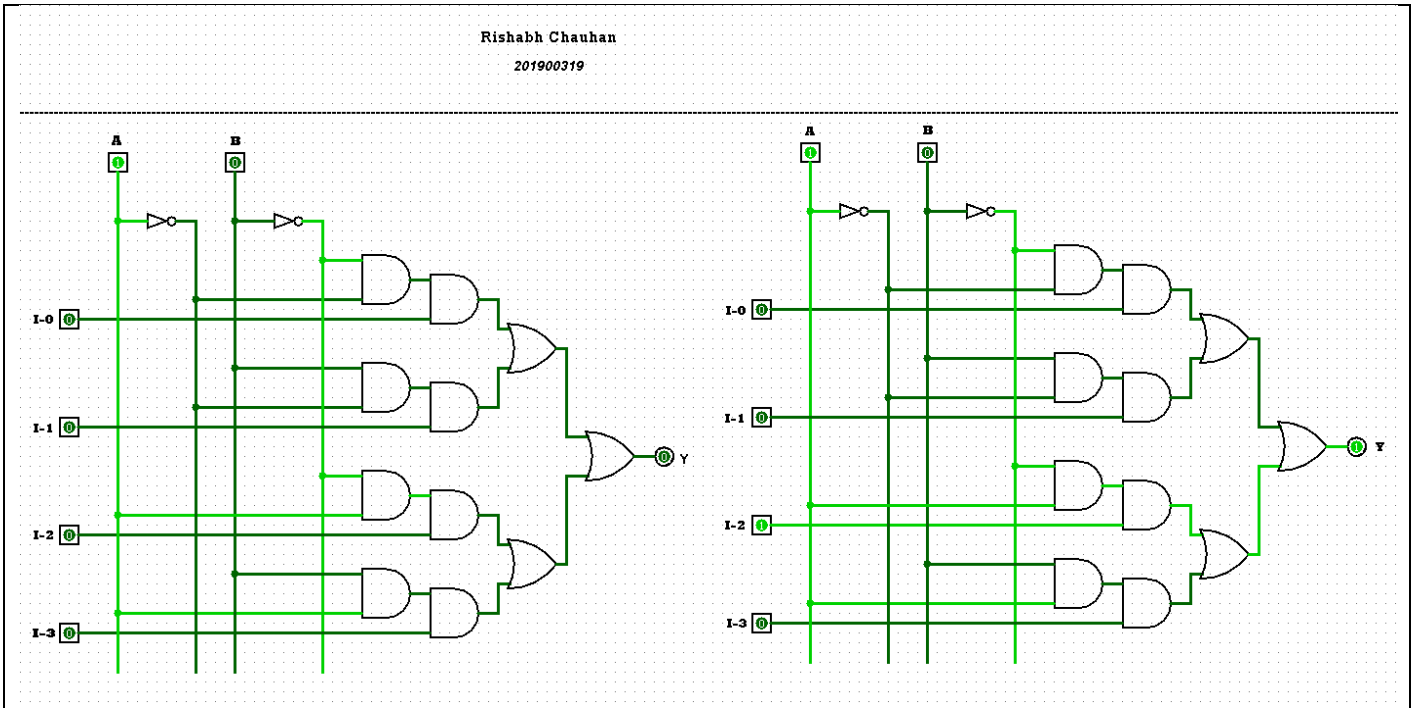
Student's worksheet-3



Student's observation and conclusion:

- **A 4-to-1 multiplexer consists of four data input lines marked as I_0 to I_3, two select input lines, marked as A, B and a single output line Y.**

- **The input combination on select input line (A & B) selects one of input (I_0 to I_3) to the output.**

- **When the selection line A is 1 and B is 0 then the input line I_2 will be generated at the output. In this scenario, the MUX will allow only I_2 to pass through it and other input will be blocked.**

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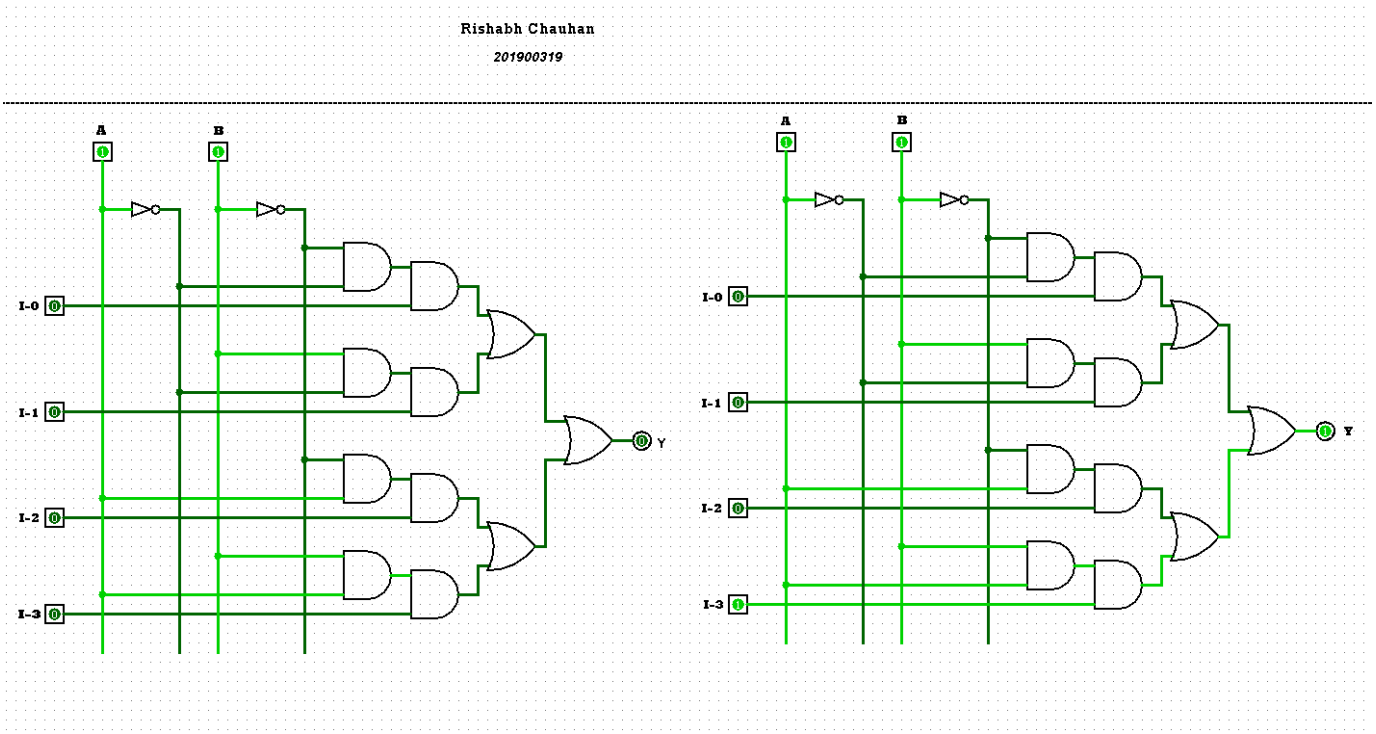
Student's worksheet-4



Student's observation and conclusion:

- **A 4-to-1 multiplexer consists of four data input lines marked as I_0 to I_3, two select input lines, marked as A, B and a single output line Y.**

- **The input combination on select input line (A & B) selects one of input (I_0 to I_3) to the output.**

- **When both the selection line represents 1, then the last input line will be selected i.e. I_3. In this case, the MUX will allow the only I_3 to pass through it and other input lines get blocked from passing through MUX.**

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