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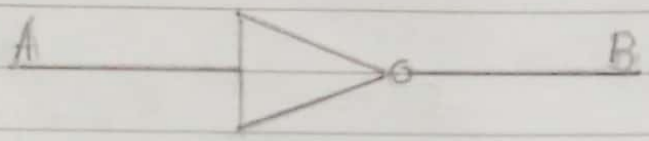
Department of Computer Science

Practical - 01

AIM: Draw symbol and circuit diagram of all logic gates and verify its truth table.

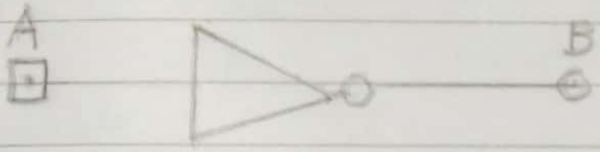
1. NOT GATE

Symbol :-



□ → input
○ → output

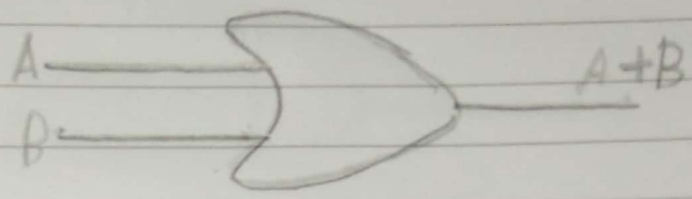
Circuit Diagram :-



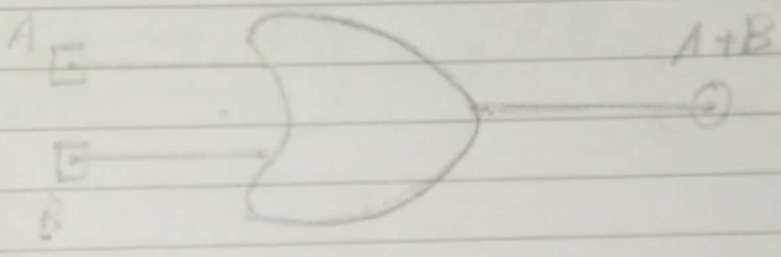
Truth Table :-

OR Gate :-

Symbol :-



Circuit Diagram



Truth Table

Input		Output
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Hence the truth table of Or gate is verified.

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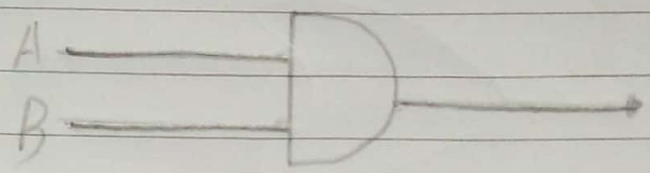
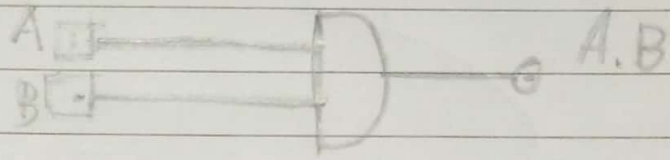
AND Gate

Symbol :

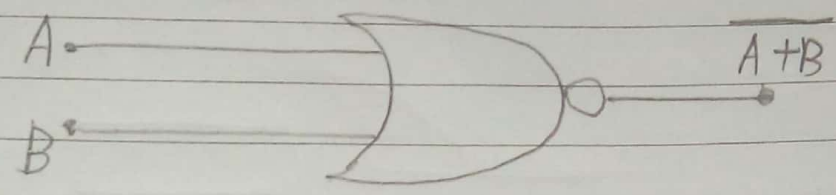


CIRCUIT Diagram :-

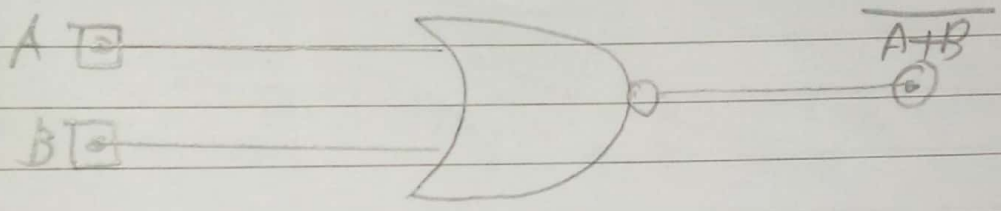


4. NOR Gate

Symbol :-



Circuit Diagram :-



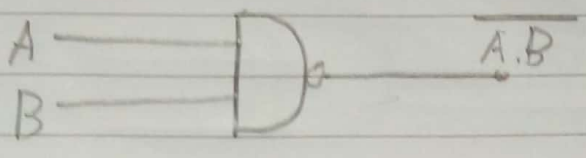
Truth Table :-

Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

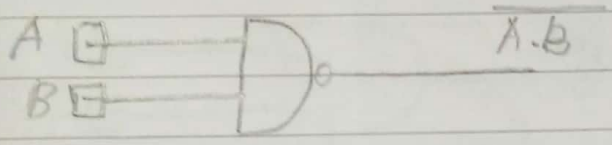
Hence :- The truth table of NOR Gate is verified.

NAND Gate

Symbol :-



Circuit Diagram :-



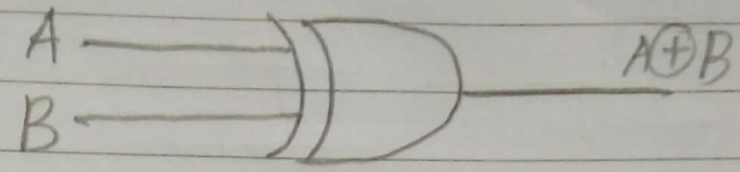
Truth Table :-

Input		Output
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

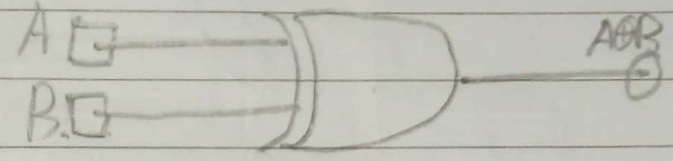
Hence The truth table of NAND Gate is verified.

EXOR Gate :-

Symbolic :-



CIRCUIT Diagram :-



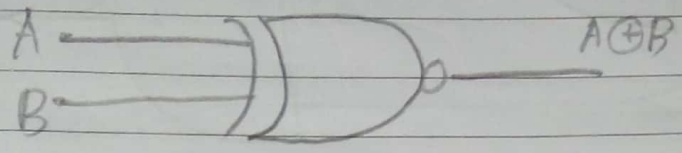
Truth Table :-

Input		Output
A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

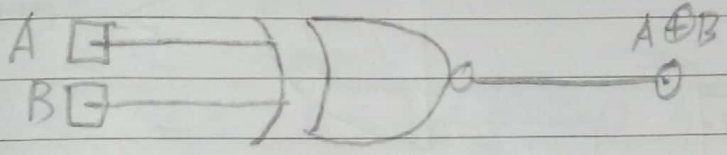
Hence :- The truth table of Exor Gate is verified.

7. Ex-NOR Gate

Symbol :-



Circuit Diagram :-



Truth table :-

Input		Output
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Hence the truth table of Ex-Nor Gate is verified.

A	B	C	A.B	B.C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

2) $(A+B)+C = A+(B+C)$

Truth table :—

A	B	C	A+B	B+C	(A+B)+C	A+(B+C)
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	0	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

Distributive law :-

1) $A.(B+C) = (A.B)+(A.C)$

Truth table :-

A	B	C	A.B	A.C	B+C	A.(B+C)	(A.B)+(A.C)
0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0
0	1	0	0	0	1	0	0
0	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0
1	0	1	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	1	1	1	1	1	1

$\therefore A.(B+C) = (A.B)+(A.C)$

∴ The truth table is verified.

2) $A+(B.C) = (A+B).(A+C)$

Truth table :-

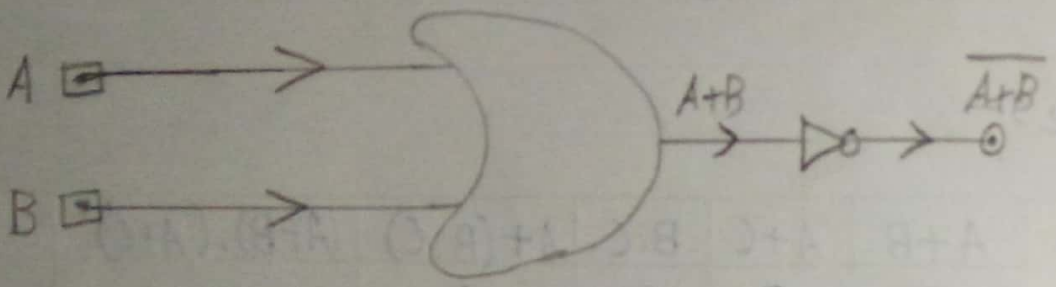
A	B	C	A+B	A+C	B.C	A+(B.C)	(A+B).(A+C)
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1
1	0	1	1	1	0	1	1
1	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1

$\therefore A+(B.C) = (A+B).(A+C)$

$\therefore$ Hence truth table is verified.

Diagram :-

$\overline{A+B}$



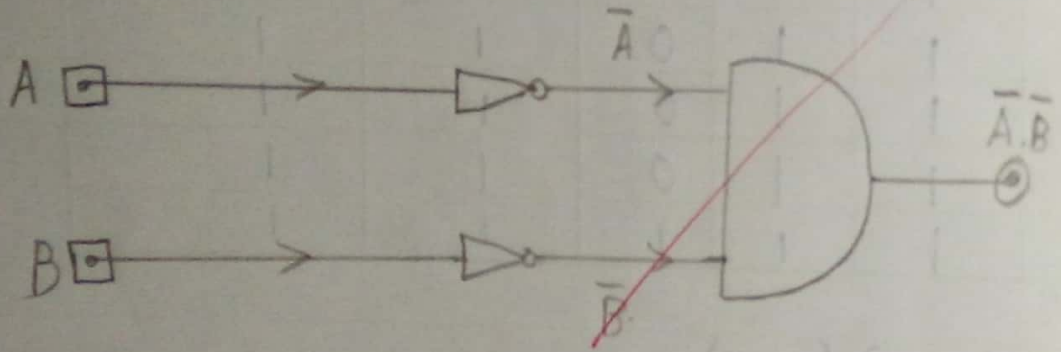
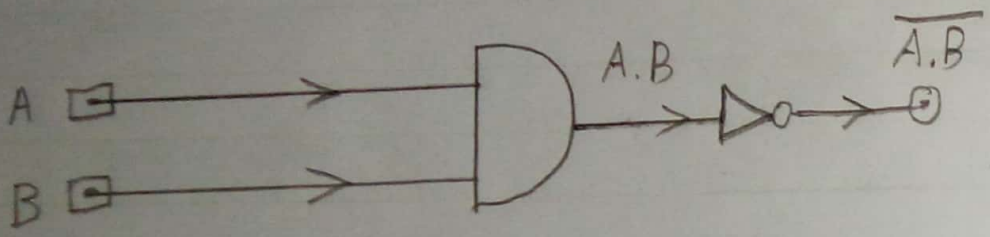


Diagram :-

$\overline{A.B}$



$\bar{A} + \bar{B}$

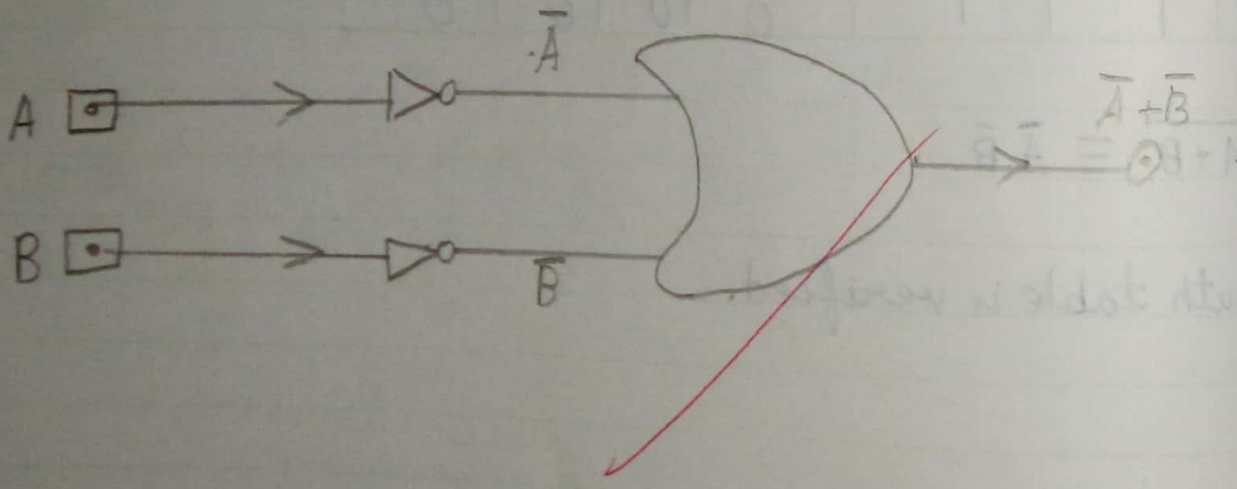
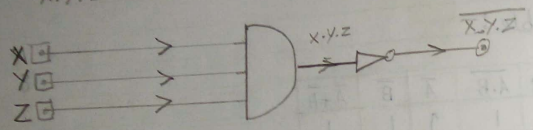
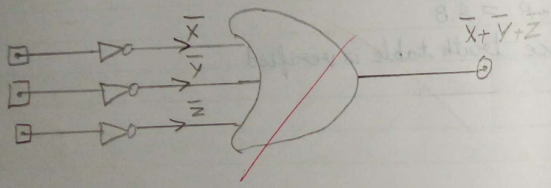


Diagram :-

$\overline{X.Y.Z}$



$\overline{X}+\overline{Y}+\overline{Z}$



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3) $\overline{X.Y.Z} = \overline{X}+\overline{Y}+\overline{Z}$

Truth table

X	Y	Z	X.Y.Z	$\overline{X.Y.Z}$	$\overline{X}$	$\overline{Y}$	$\overline{Z}$	$\overline{X}+\overline{Y}+\overline{Z}$
0	0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0	1
0	1	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0	1
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	0	1	1
1	1	1	1	0	0	0	0	0

$\therefore \overline{X.Y.Z} = \overline{X}+\overline{Y}+\overline{Z}$

$\therefore$ Truth table is verified

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Practical -03

Aim :- Draw block diagram, circuit diagram and verified truth table of half adder.

Half Adder :- The function of half adder is to add two binary digites producing sum and carry.

There are two inputs in to half adder denoted as 'A' and 'B' and output as 'S' and 'C'.

Truth table

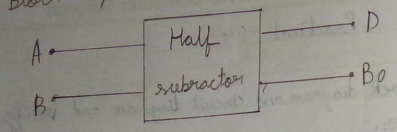
Practical -04

Aim :- Draw a block diagram and circuit diagram and verify truth table of full adder.

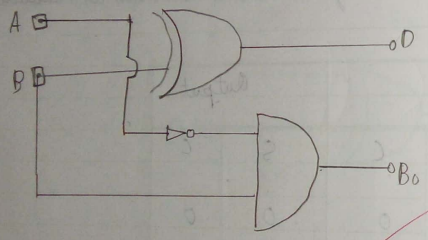
Full Adder :- Is a circuit diagram that can handle 3 bits at a time. Therefore full adder circuit is capable of adding the content of two registeration must pricuide provision for handling carriver as well as addend and augents bits. This is known as Fulladder.

Input	Output

Block Diagram



Circuit Diagram



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Practical -05

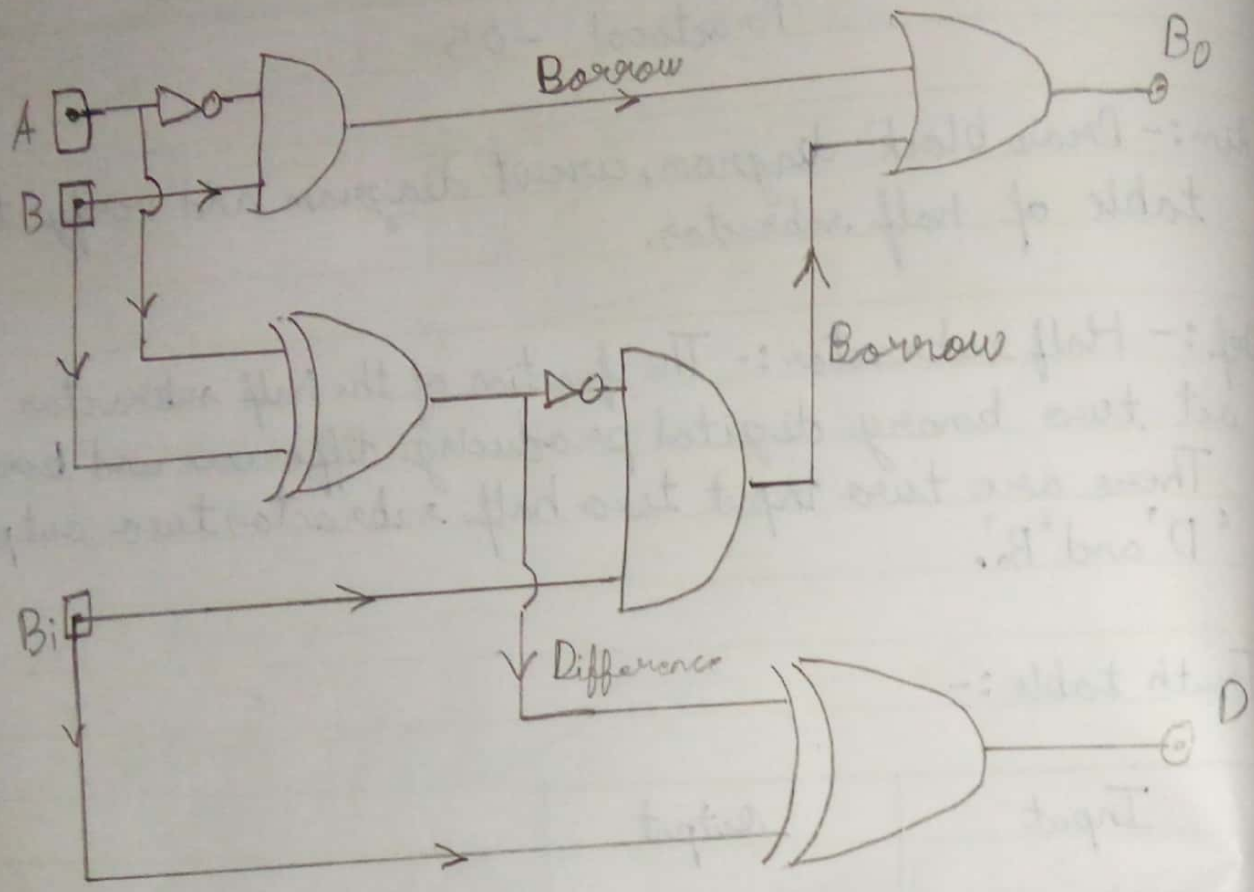
Aim :- Draw block diagram, circuit diagram and verify truth table of half subractor.

Def :- Half subractor :- The function of the half subractor to substract two binary digital producing difference and borrow and. There are two input two half subractor two outputs as 'D' and 'Bo'.

Truth table :-

Input		Output	
A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Hence truth table of Half S ~~of~~ is verified.



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Practical No 7

Aim :- Draw block, circuit Diagram of SP flip flop.

Discription :-

The storage element in clocked sequential circuit are called flip flop. ∴ O flip-flop is binary cell capable for storing one bit of information it has 2 outputs one normal value and 1 for compliment value of the bit storaged in it a flip flop maintains a binary state unit directed by clock pluse who switch the state.

Truth table

2] let $Q=0$ and $\bar{Q}=1$ are initial state $s=1, R=0$ output $\bar{Q}$ should be 0 Now input to the NOR Gate A are $R=0$, $Q=0$, Hence its output Q changed to 1.

3] let $Q=1$ and $Q=0$ are initial state with $S=0$, $R=1$, output of the NOR Gate A should be $Q=0$, Therefore input to the NOR Gate 5 are $S=0$ and $Q=0$.

Circuit diagram of D. flip flop

Defination:- The S=R flip flop has two data input S and R to store a beat. Therefore two singles are required to drive a flip flop which is disadvantages also there is forbiddent condition appearing in S-R flip flop. This S-R flip flop can be modified. To overcome this disadvantage called D-flip flop.

Working :- The D flip flop stored the output whatever logic level is applied to its data terminal so long as Clk input is high. once the Clk input goes low the set and reset input of the flip flop are both hold at logic level one. So it will not change state and stored whatever output was presented on its output before the clock transistion offered in other words is latched either zero (0) or one (1).

Truth table:-

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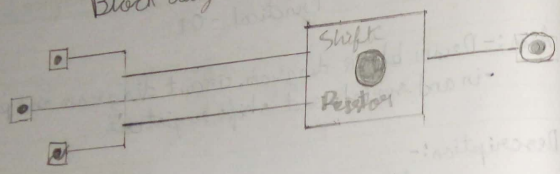
Practical - 09

Aim :- Draw block diagram, circuit diagram and perform serial -in and serial - out shift registers.

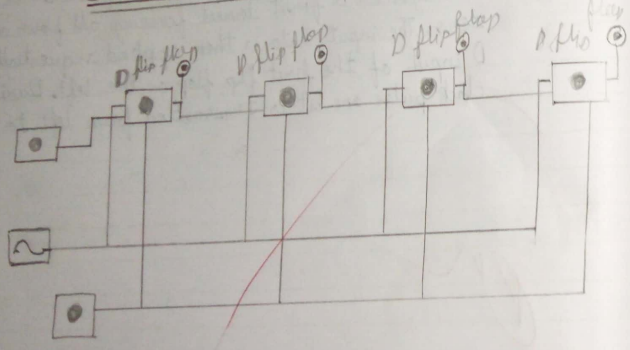
Description :-

A basic 4-bit shift register can be constructed using O-Flip flop as shown. The operation of circuit is as follows. The register is first element forcing all four output to zero. The input data is then applied sequentially to the

Block diagram:



Circuit diagram:



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Practical -10

Aim :- Draw block diagram, circuit diagram and perform serial-in and parallel-out shift registers.

Description :-

A basic 4-bit shift register can be constructed using four D-flip flop as shown. The operation of circuit is as follows. The register is first cleared, forcing all four output to zero. The data stored within the register is obtained as a parallel-output data at the individual output pins of the flip flops.