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SIR M.V. COLLEGE OF SCIENCE & COMMERCE**

Department of Computer Science

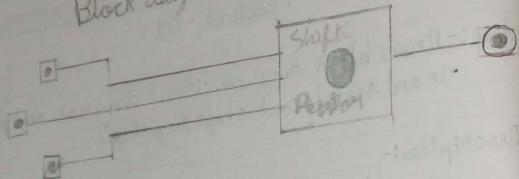
Practical -10

Aim :- Draw block diagram, circuit diagram and perform serial-in and parallel-out shift registers.

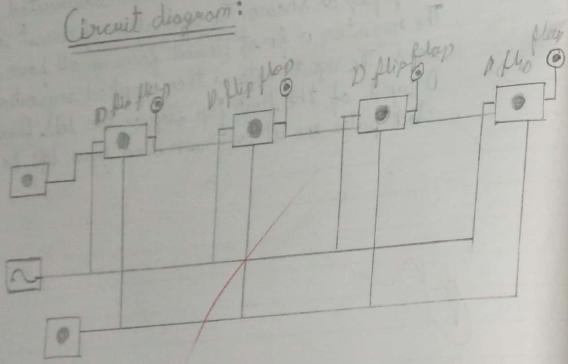
Description:-

A basic 4-bit shift register can be constructed using four D-flip flop as shown. The operation of circuit is as follows. The register is first cleared, forcing all four output to zero. The data stored within the register is obtained as a parallel-output data at the individual output pins of the flip flops.

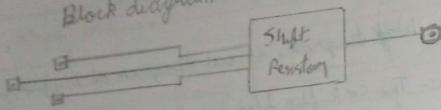
Block diagram:



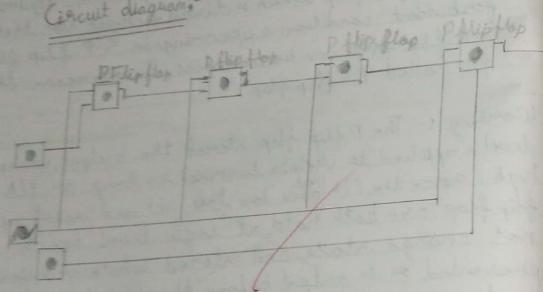
Circuit diagram:



Block diagram:-



Circuit diagram:-



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Practical - 09

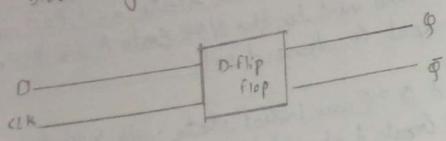
Aim:- Draw block diagram, circuit diagram and perform serial-in and serial-out shift registers.

Description:-

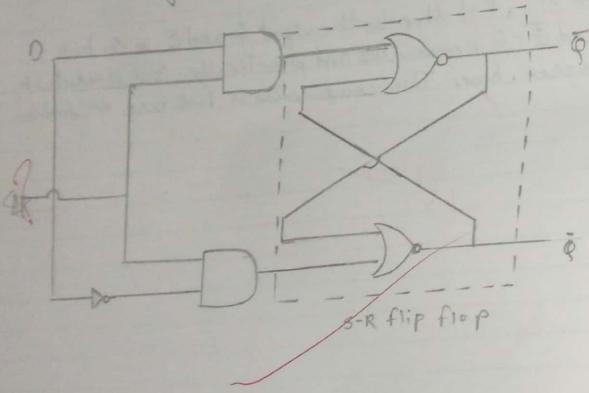
A basic 4-bit shift register can be constructed using D flip-flop as shown. The operation of circuit is as follows. The register is first element forcing all four output to zero. The input data is then applied sequentially to the D input of the first flip flop on the left. During each clock pulse one bit is transmitted from left to right.

OR

Block diagram:-



Circuit diagram:-



Practical 8

Aim:- Draw block diagram, circuit diagram of D. flip flop

Definition:- The S=R flip flop has two data inputs S and R to store a beat. Therefore two singles are required to drive a flip flop which is disadvantage also there is forbidden condition appearing in S-R flip flop. This S-R flip flop can be modified. To overcome this advantage called D-flip flop.

Working :- The D flip flop stored the output whatever logic level is applied to its data terminal so long as CLK input is high. Once the CLK goes low then set and reset input of the flip flop are both held at logic level one. So it will not change state and stored whatever output was presented on its output before the clock transition occurred in other words is latched either zero(0) or one(1).

Truth table:-

CLK	D	Q	\bar{Q}	Comment
0	X	0	1	Hold
1	0	0	1	Reset
1	1	1	0	Set

Qm



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- 2] let $Q=0$ and $\bar{Q}=1$ are initial state $s=1, R=0$ output \bar{Q} should be 0 Now input to the NOR Gate A are $R=0, Q=0$. Hence its output Q changed to 1.
- 3] let $Q=1$ and $\bar{Q}=0$ are initial state with $S=0, R=1$, output of the NOR Gate A should be $Q=0$. Therefore input to the NOR Gate S are $S=0$ and $Q=0$. Therefore output $\bar{Q}=1$
- 4] If both $S=1, R=1$ than both output Q and \bar{Q} is 0. but $Q=0$ and $\bar{Q}=0$ is meaningless and practically Not predictable by designer, hence This combination is Not use or forbidden.

JM

Aim:- Draw block diagram and Circuit Diagram of SR flip flop.

Description:-

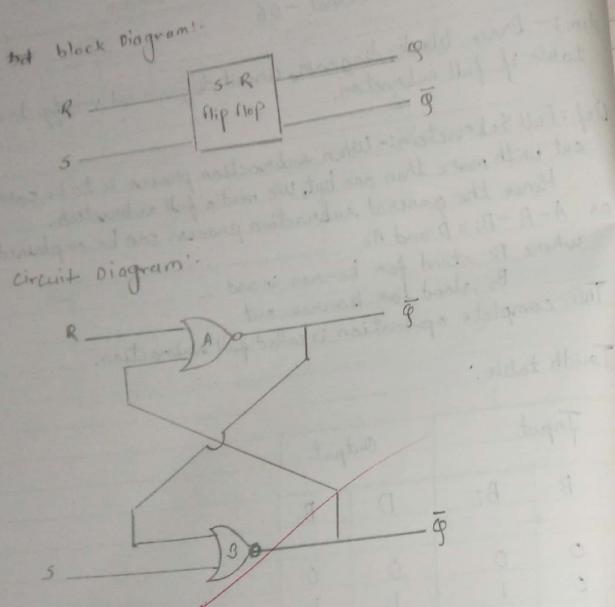
The storage element in clocked sequential circuit are called flip flop. A flip-flop is binary cell capable for storing one bit of information. It has 2 outputs one normal value and 1 for complement value of the bit stored in it. A flip flop maintains a binary state until directed by clock phase who switch the state.

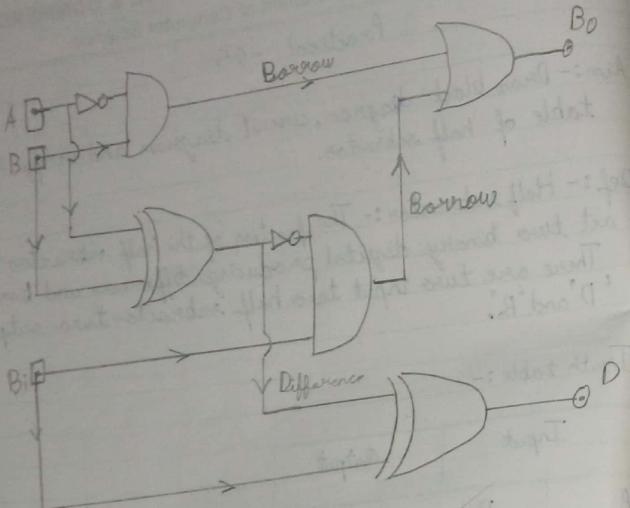
Truth table

S	R	Q	\bar{Q}	Comment
0	0	0	1	Hold condition
1	0	1	0	Set
0	1	0	1	Reset
1	1	0	0	Not-used

Working of SR flip flop:-

- 1] Let $Q=0$ and $\bar{Q}=1$ are initial state and $R=0$, $S=0$. Now the input to the NOR Gate A are $R=0$ and $Q=1$. Hence output Q should be 0 similarly input to the NOR Gate B are $S=0$ and $Q=0$. Thus output $\bar{Q}=1$ as initially $Q=0$ and $\bar{Q}=1$. Hence when $R=0$, $S=0$ there is no change in output.





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Practical - 06

Aim:- Draw block diagram, circuit diagram and verify truth table of full subtractor.

Def: Full Subtractor:- When subtraction process is to be carried out with more than one bit, we need a full subtractor.

Hence the general subtraction process can be explained as $A - B - B_i = D$ and B_o .

where B_i stand for borrow in and B_o stand for borrow out

This complete operation is called full subtraction.

Truth table:

Input			Output	
A	B	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Hence truth table of full subtraction is verified.



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Practical - 05

Aim:- Draw block diagram, circuit diagram and verify truth table of half subtractor.

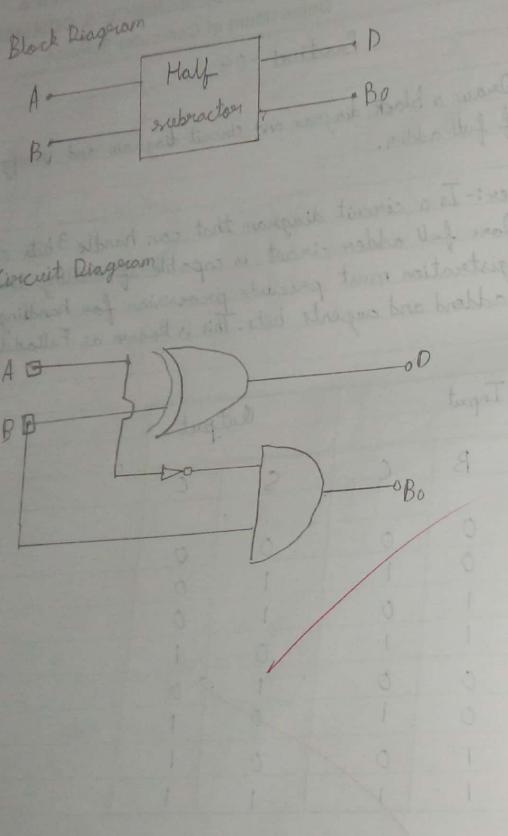
Def:- Half subtractor:- The function of the half subtractor to subtract two binary digits producing difference and borrow and. There are two input to half subtractor two outputs as 'D' and 'B_o'.

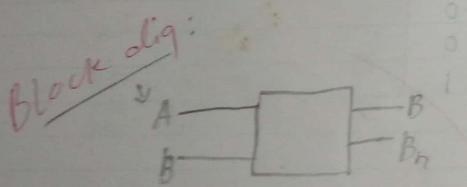
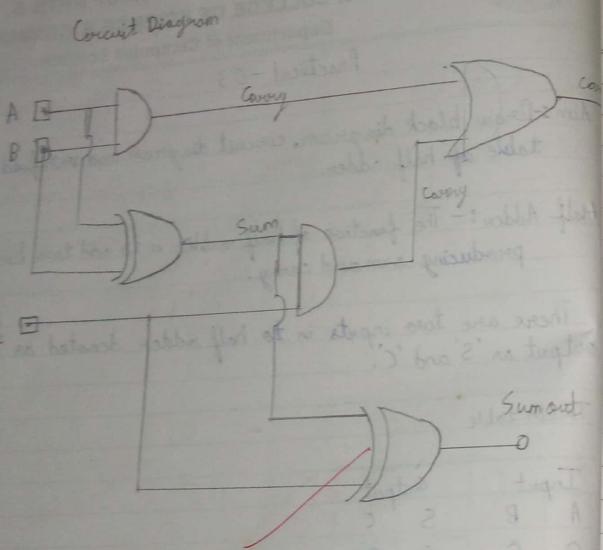
Truth table :-

Input		Output	
A	B	D	B _o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Hence truth table is verified. *✓ Half Sub*

R.M.





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Practical -04

Aim :- Draw a block diagram and circuit diagram and verify truth table of full adder.

Full Adder :- Is a circuit diagram that can handle 3 bits at a time. Therefore full adder circuit is capable of adding the content of two register must provide provision for handling carries as well as addend and augend bits. This is known as Full adder.

Input			Output	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Practical - 03

Aim :- Draw block diagram, circuit diagram and verified truth table of half adder.

Half Adder :- The function of half adder is to add two binary digits producing sum and carry.

There are two inputs in to half adder denoted as 'A' and 'B' and output as 'S' and 'C'.

Truth table

Input		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

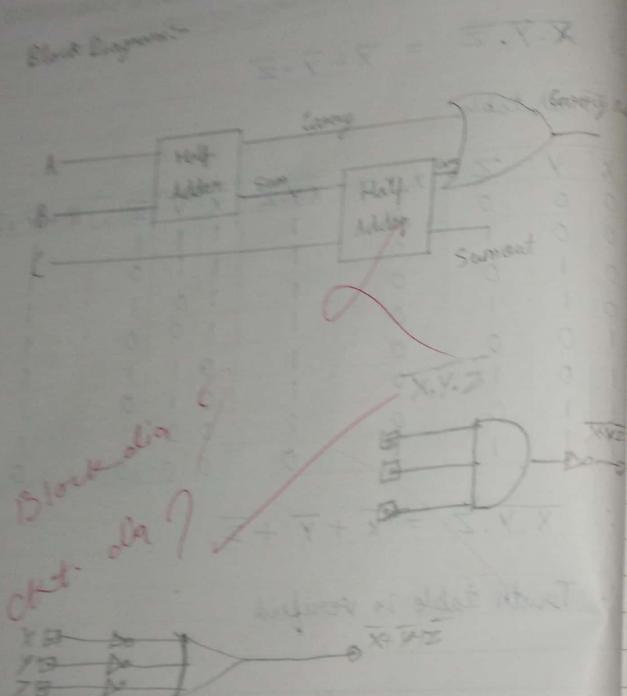
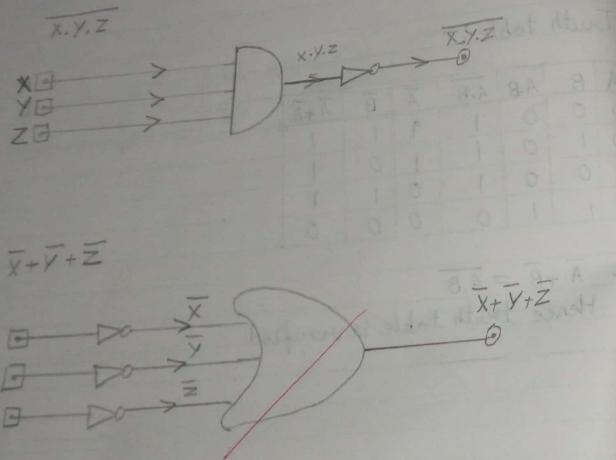


Diagram:-



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3) $\overline{X \cdot Y \cdot Z} = \overline{X} + \overline{Y} + \overline{Z}$

Truth table

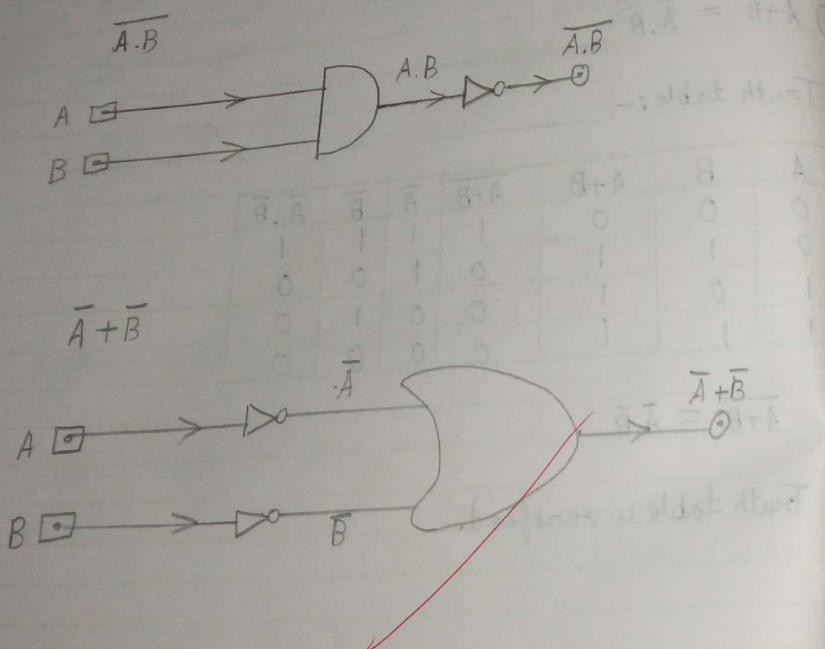
X	Y	Z	$X \cdot Y \cdot Z$	$\overline{X \cdot Y \cdot Z}$	\overline{X}	\overline{Y}	\overline{Z}	$\overline{X} + \overline{Y} + \overline{Z}$
0	0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0	1
0	1	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0	1
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	0	1	1
1	1	1	1	0	0	0	0	0

$\therefore \overline{X \cdot Y \cdot Z} = \overline{X} + \overline{Y} + \overline{Z}$

\therefore Truth table is verified

PM

Diagram :-



$$2) \overline{A \cdot B} = \overline{A} + \overline{B}$$

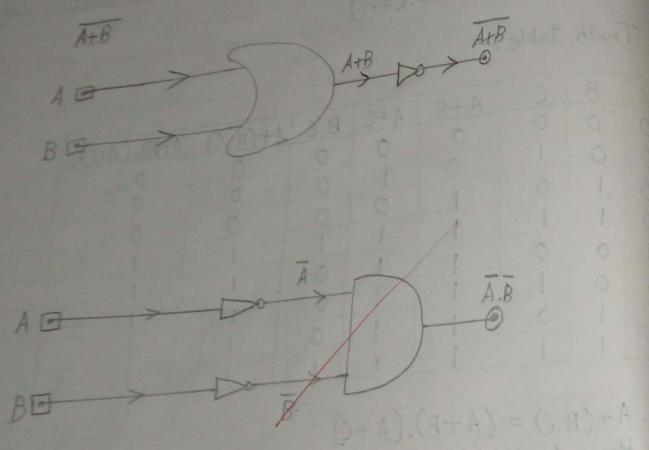
Truth table :-

A	B	$A \cdot B$	$\overline{A \cdot B}$	\overline{A}	\overline{B}	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

$$\therefore \overline{A} + \overline{B} = \overline{A \cdot B}$$

\therefore Hence truth table is verified

Diagram :-



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3) Demorgan's Law:-

$$D) \bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$$

Truth table :-

A	B	$A + B$	$\bar{A} + \bar{B}$	\bar{A}	\bar{B}	$\bar{A} \cdot \bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

$$\therefore \bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$$

∴ Truth table is verified.



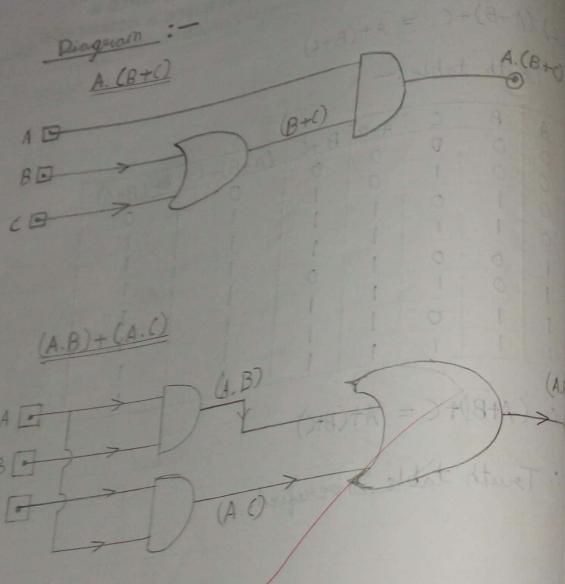
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$$2) A + (B \cdot C) = (A+B) \cdot (A+C)$$

Truth table:-

$$\therefore A + (B \cdot C) = (A + B) \cdot (A + C)$$

\therefore Hence truth table is verified.



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Distributive Law :-

$$i) A \cdot (B+C) = (A \cdot B) + (A \cdot C)$$

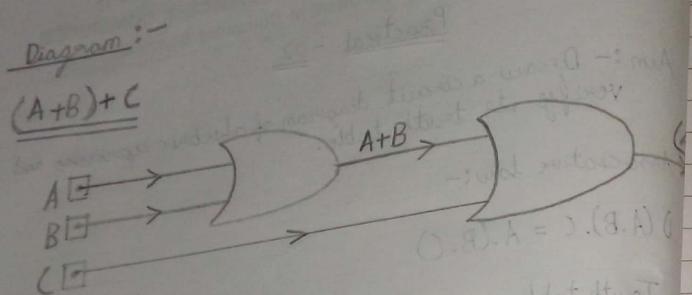
Truth table :-

A	B	C	$A \cdot B$	$A \cdot C$	$B+C$	$A \cdot (B+C)$	$(A \cdot B) + (A \cdot C)$
0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0
0	1	0	0	0	1	0	0
0	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0
1	0	1	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	1	1	1	1	1	1

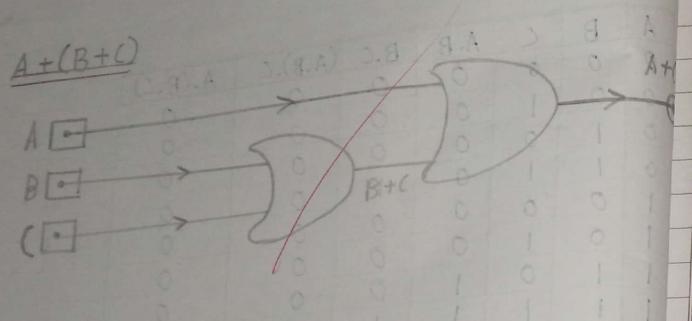
$$\therefore A \cdot (B+C) = (A \cdot B) + (A \cdot C)$$

\therefore The truth table is verified.

Diagram :-



$A+(B+C)$



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$$2) (A+B)+C = A+(B+C)$$

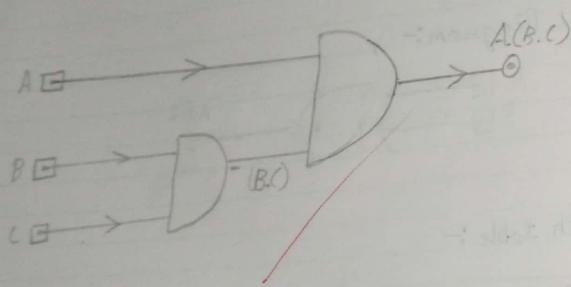
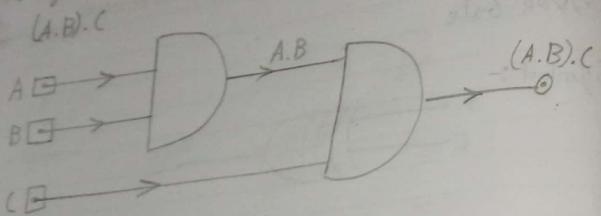
Truth table :-

A	B	C	$A+B$	$B+C$	$(A+B)+C$	$A+(B+C)$
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	0	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

$$\therefore (A+B)+C = A+(B+C)$$

$\therefore \text{Truth table is verified.}$

Diagram:-



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Practical -02

Aim :- Draw a circuit diagram of algebraic expression and verify its truth table.

1] Associative law:-

$$1) (A \cdot B) \cdot C = A \cdot (B \cdot C)$$

Truth table

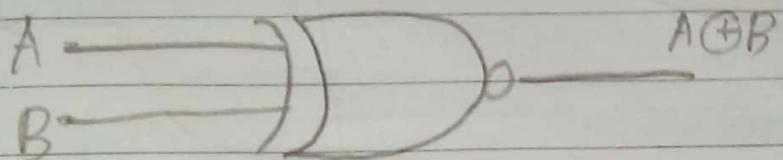
A	B	C	A · B	B · C	(A · B) · C	A · (B · C)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

$$\therefore (A \cdot B) \cdot C = A \cdot (B \cdot C)$$

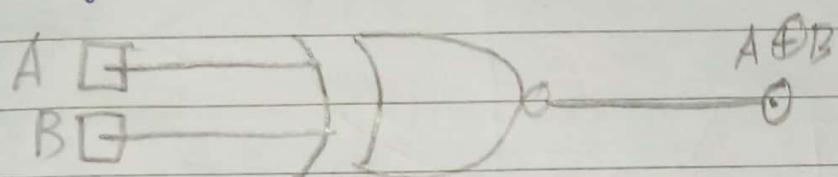
\therefore Truth table is verified.

7. ExNOR Gate

Symbol :-



Circuit Diagram :-



Truth table :-

Input		Output
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Hence the truth table of ExNOR Gate is verified.

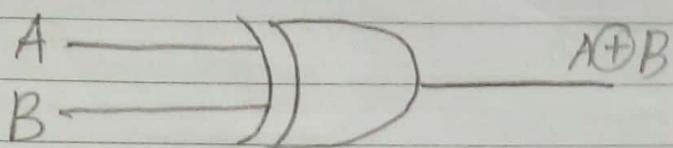
QM



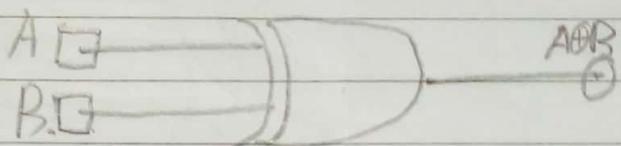
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6] EXOR Gate :-

Symbolic :-



CIRCUIT Diagram :-



Truth Table :-

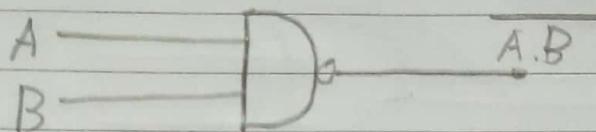
Input	Output	
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Hence :- The truth table of Exor gate is verified.

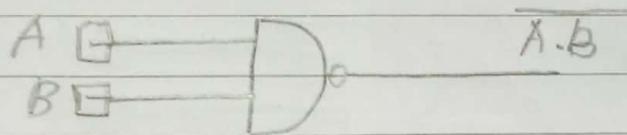


5) NAND Gate

Symbol :-



2) Circuit Diagram :-



Truth Table :-

Input Output

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

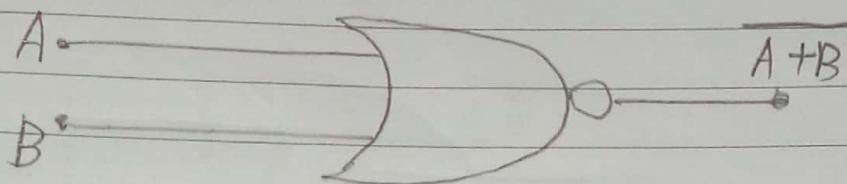
Hence The truth table of NAND Gate is verified.



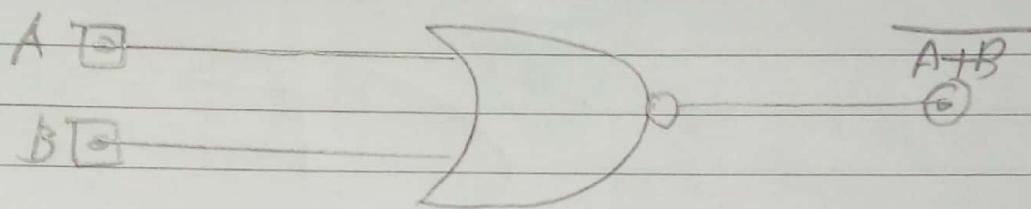
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4. NOR Gate

Symbol :-



Circuit Diagram :-



Truth Table :-

Input	Output	
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

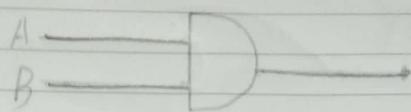
Hence :- The truth table of NOR Gate is verified.



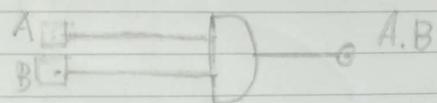
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③ AND Gate

Symbol :-



CIRCUIT Diagram :-



Truth Table :-

Input Output

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

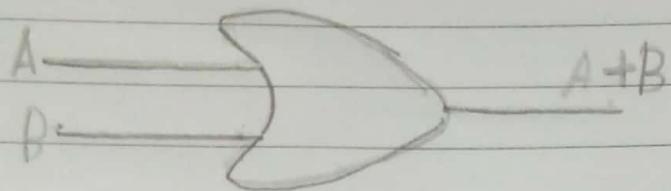
Hence :- The Truth table of AND Gate is verified.



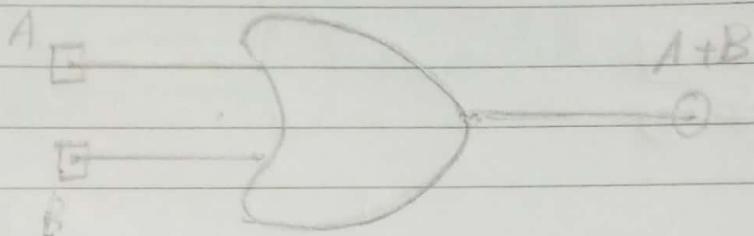
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OR Gate :-

Symbol :-



Circuit Diagram



Truth Table

Input Output

A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

Hence the truth table of OR gate is verified.



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Practical - 01

AIM: Draw symbol and circuit diagram of all logic gates and verify its truth table.

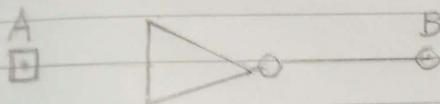
1. NOT GATE

Symbol :-



□ → input
○ → output

Circuit Diagram :-



Truth Table :-

Input	Output
0	1
1	0

Hence :- The Truth Table of NOT GATE is verified