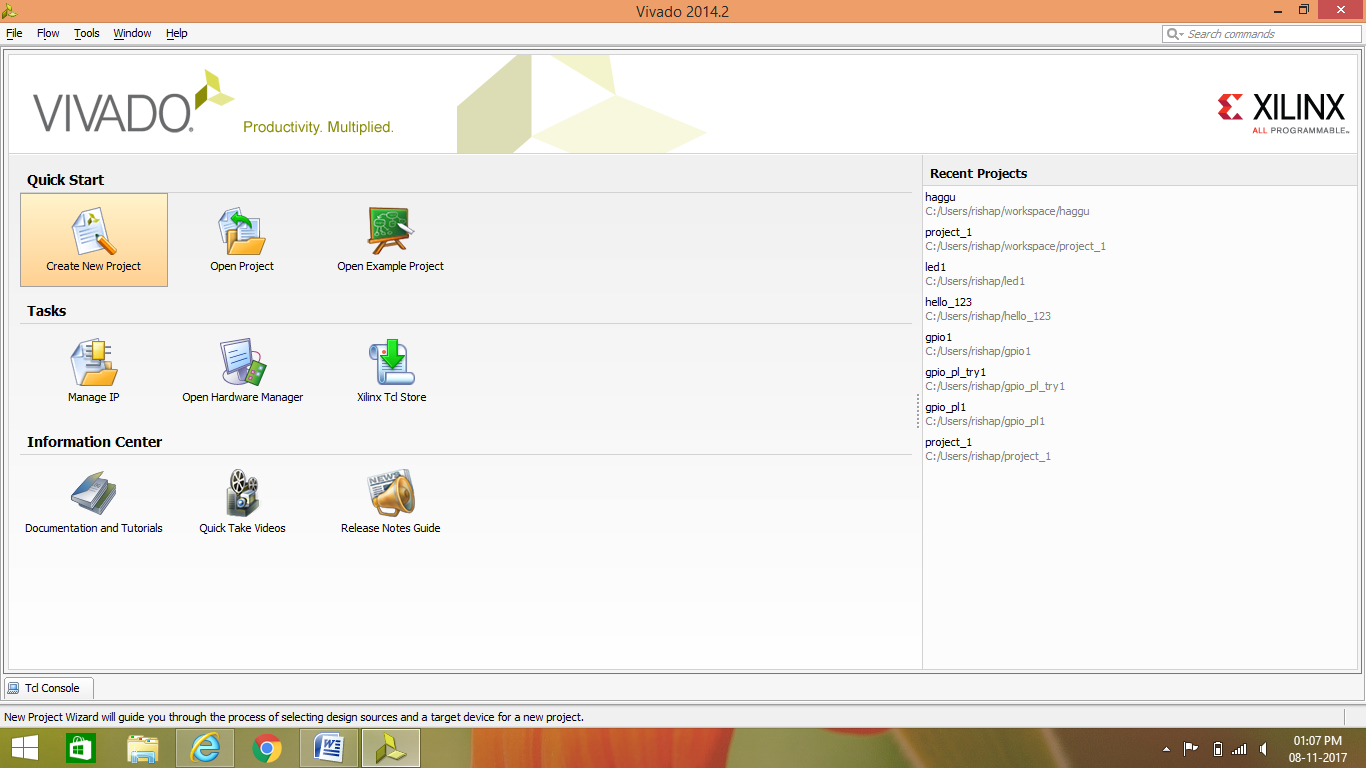
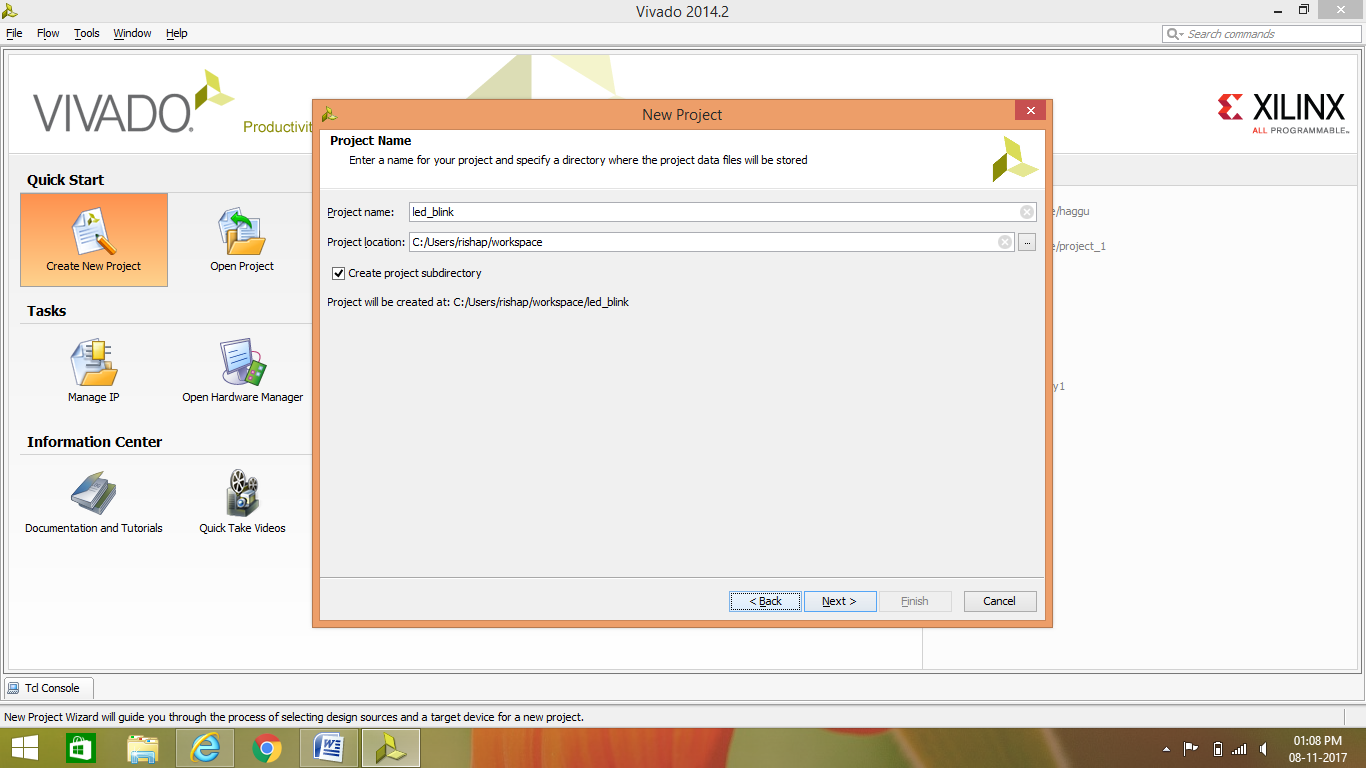
APPENDIX

A : STEPS FOR PROGRAMMING:

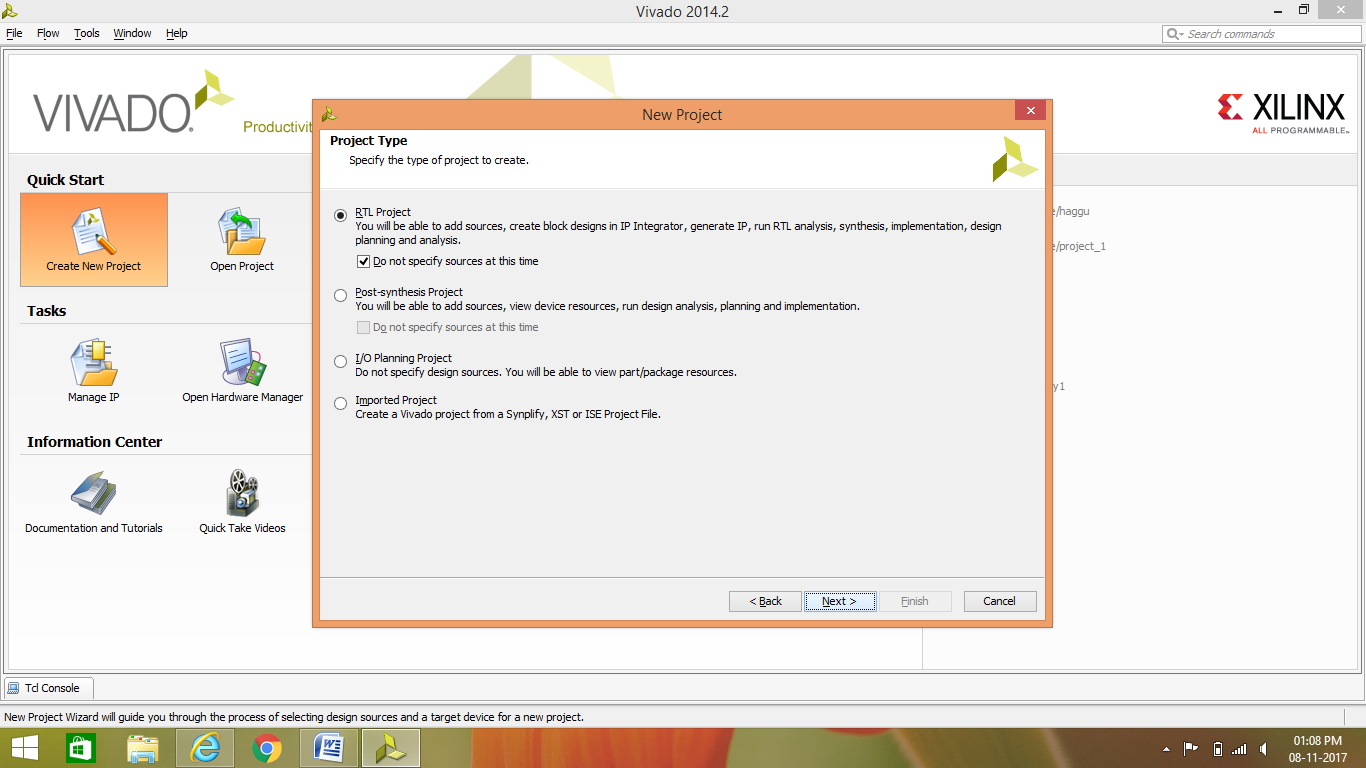
1 : Open vivado



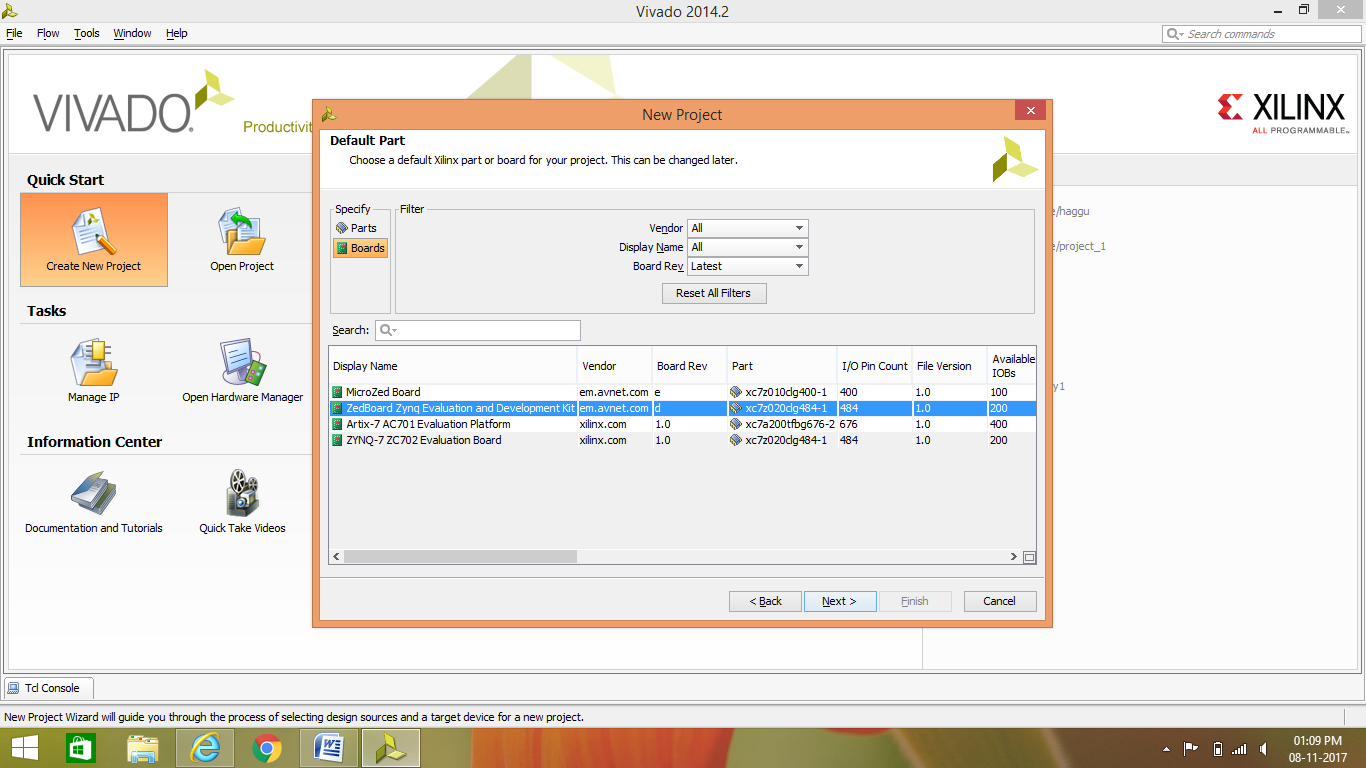
2 : Create new project:



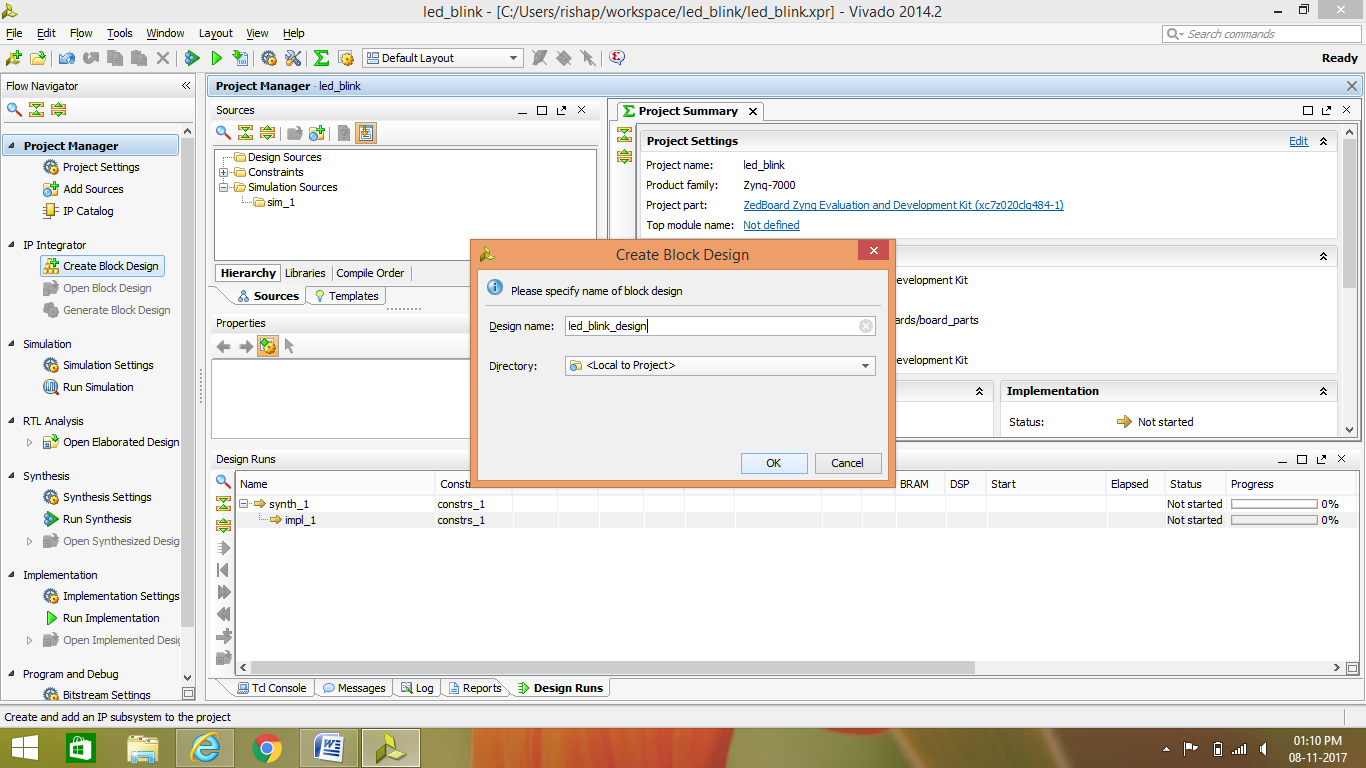
3 : Select RTL project



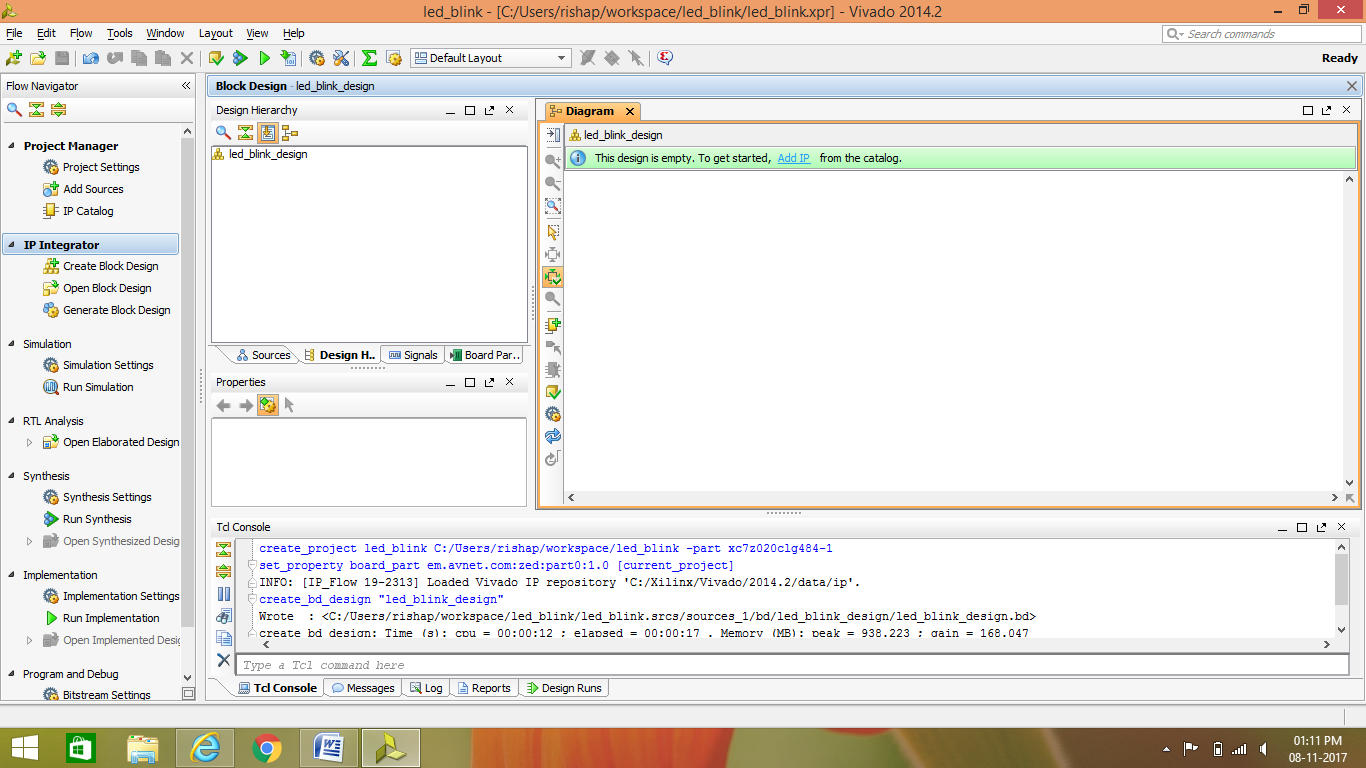
4 : Select which board/part is to be programmed:



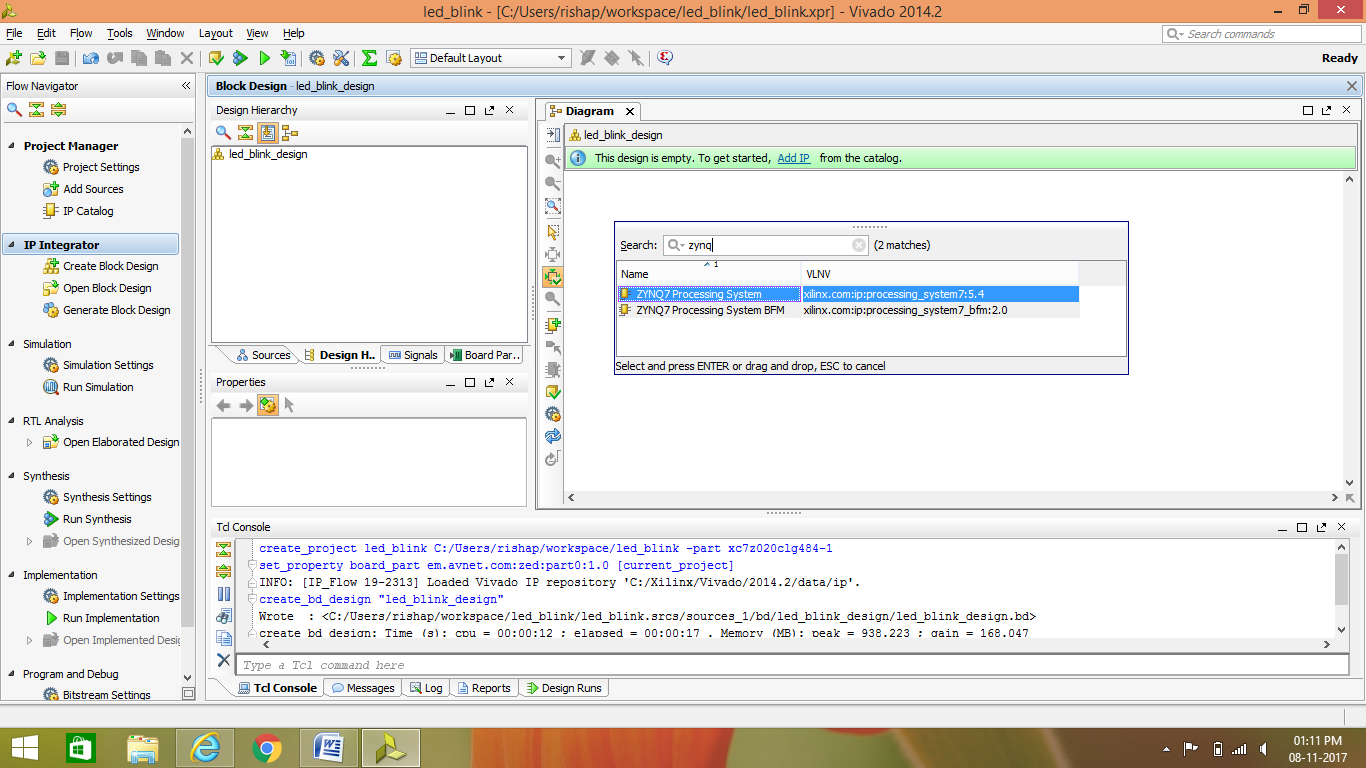
5 : Create a new block designed and name it.



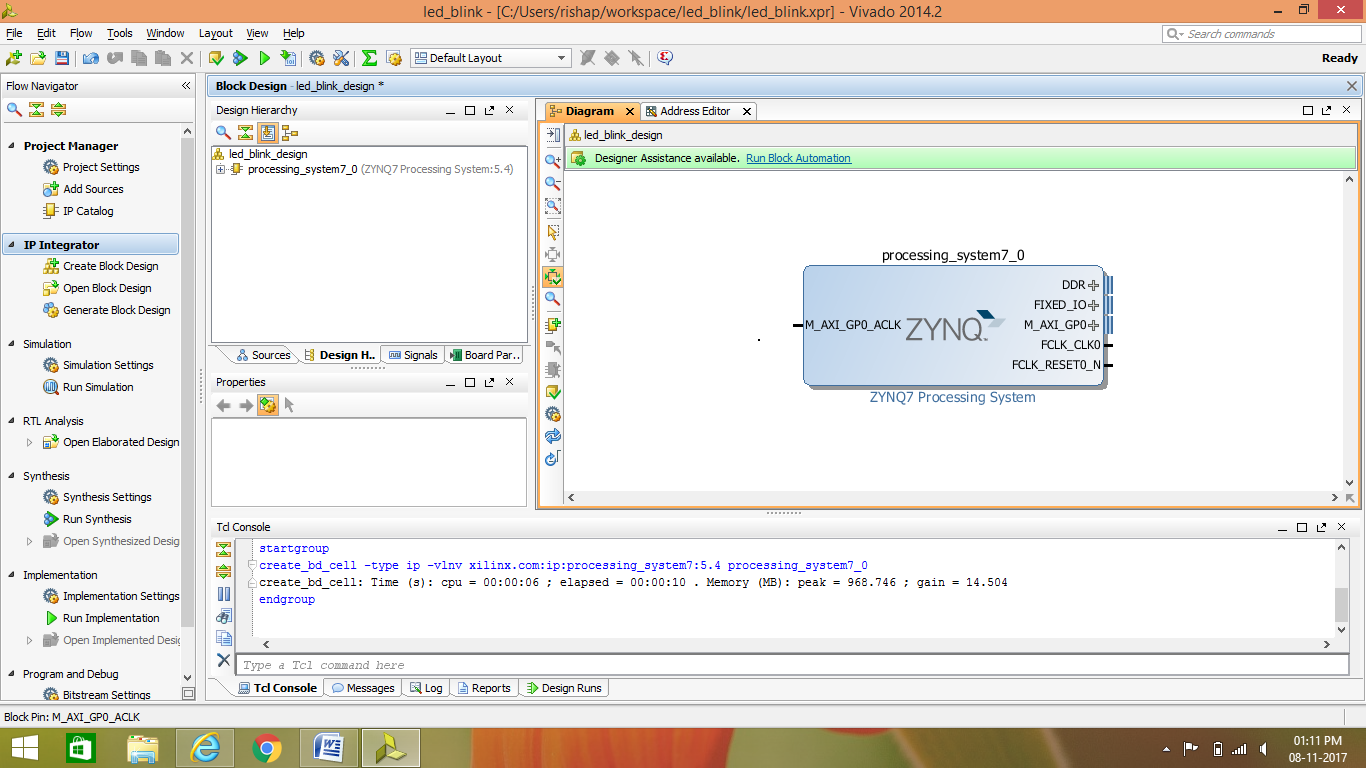
6 : Select add IP to Add ZYNQ processor



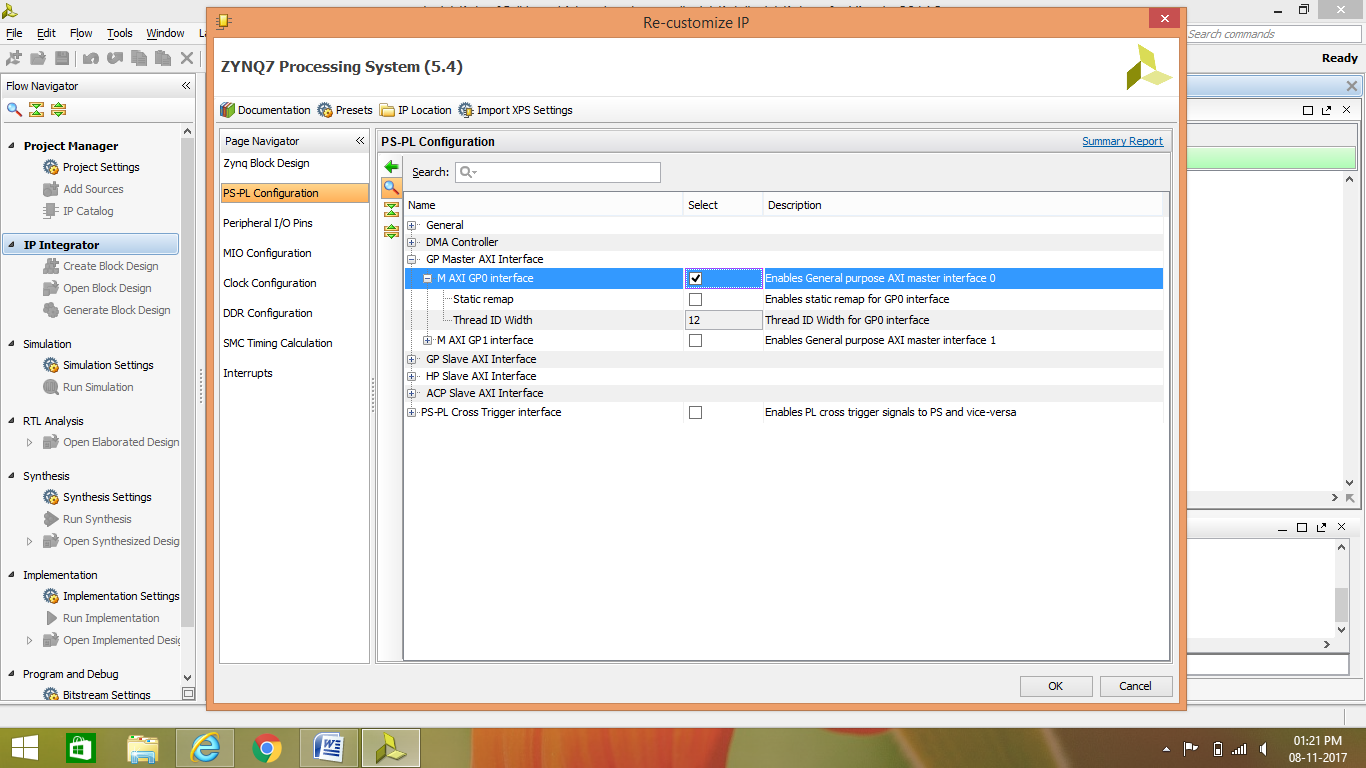
7 : Add ZYNQ processor



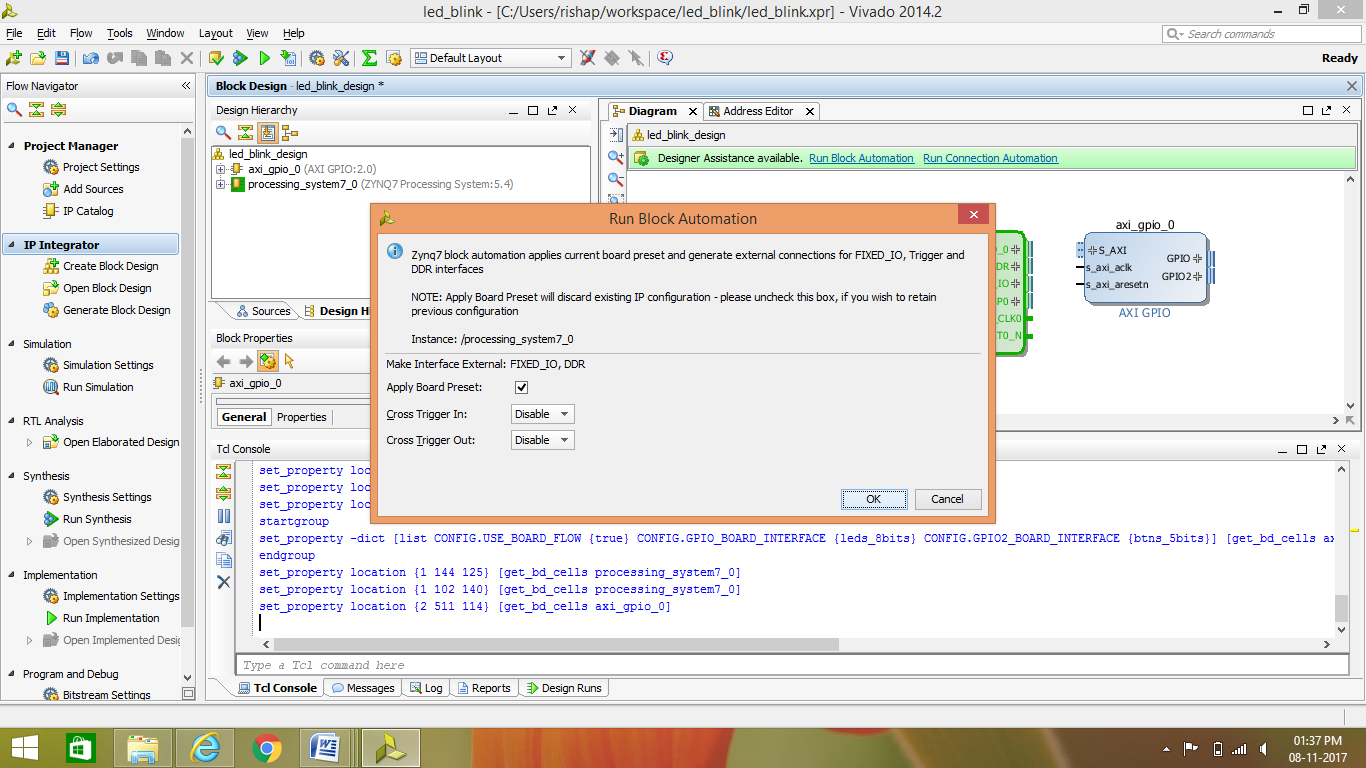
8 : double click on the ZYNQ block to open its properties:



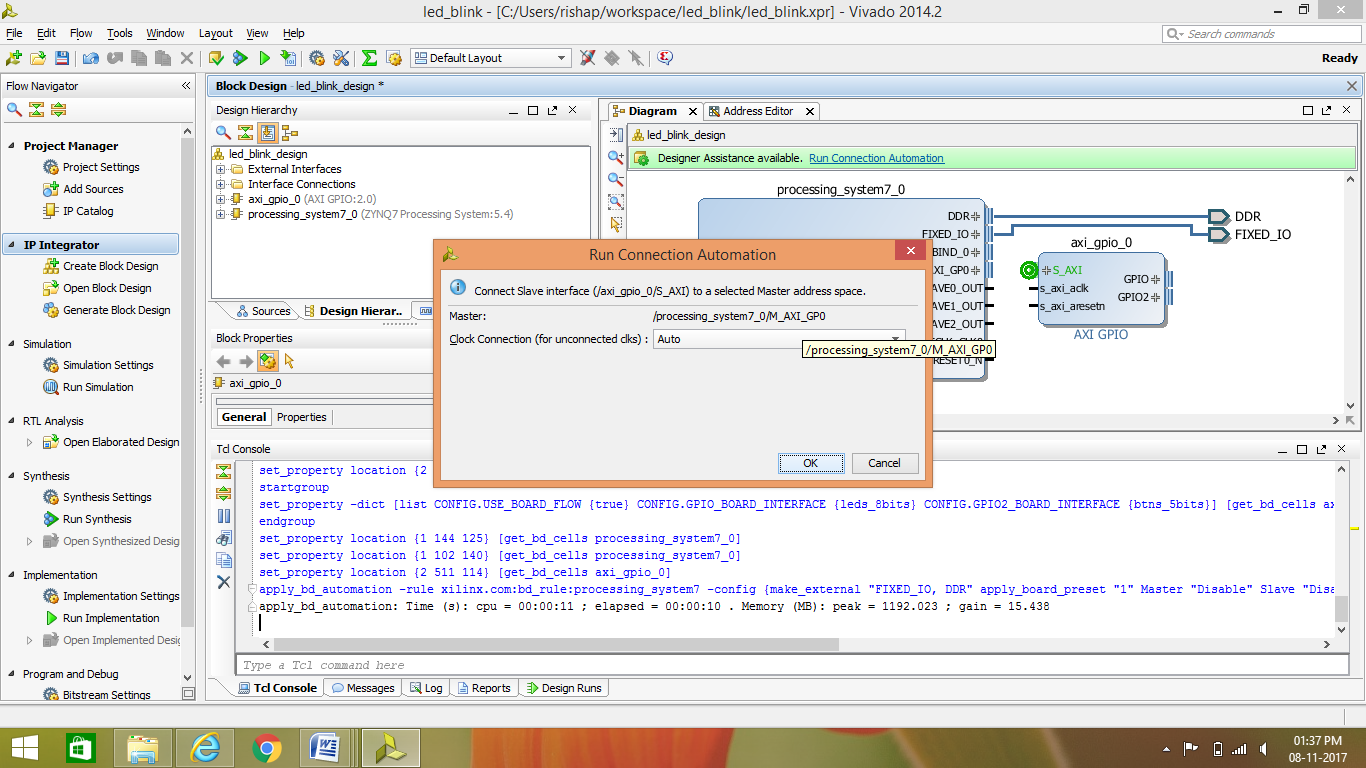
9 : configure the ZYNQ block according to need:



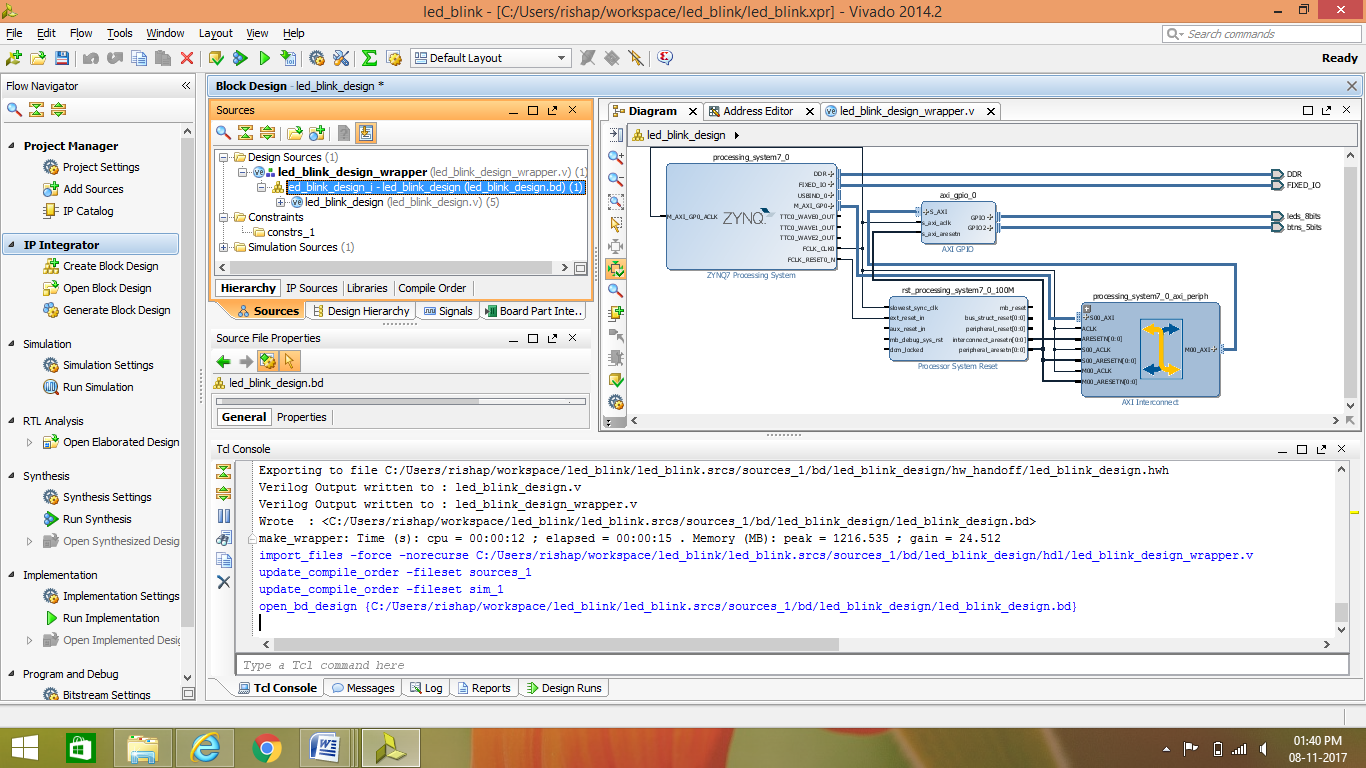
10 : Add other IP core as per need :



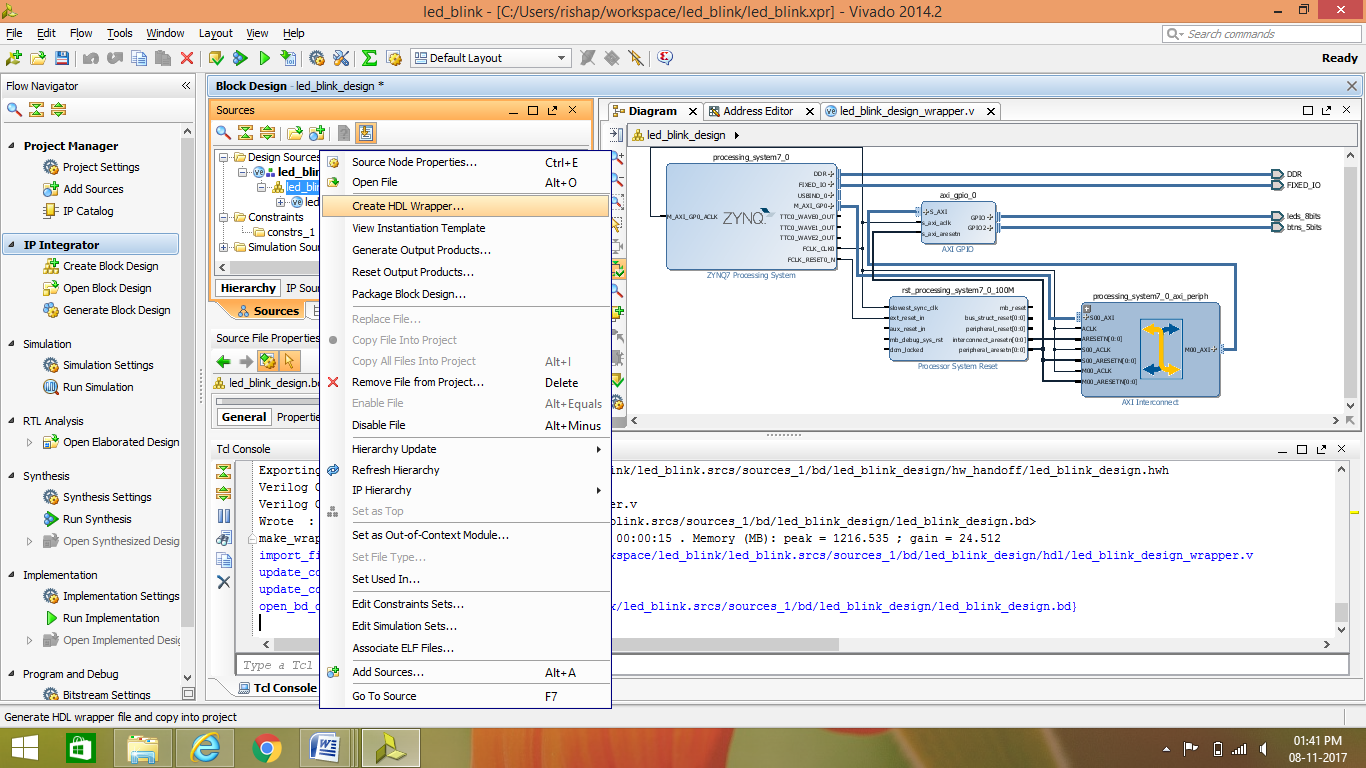
11 : use Run connection automation to connect your hardware:



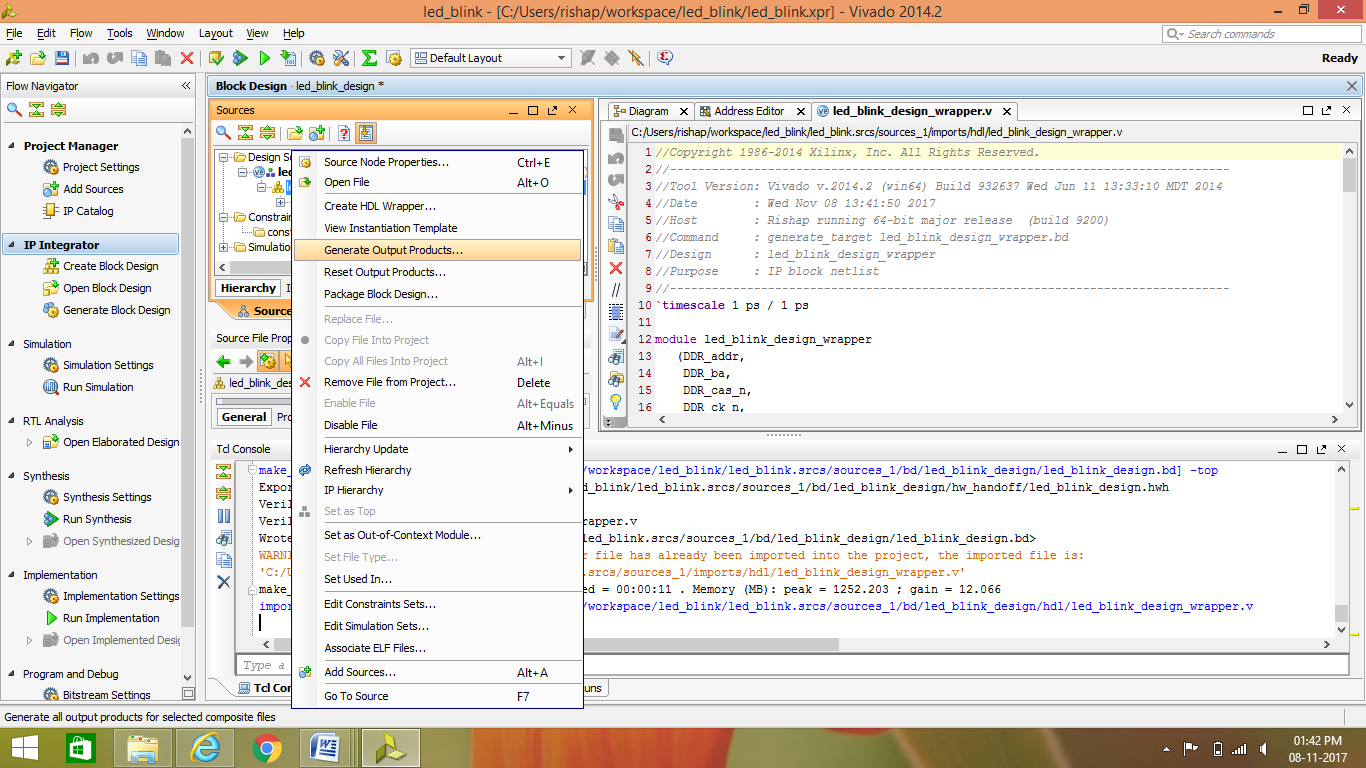
12 : finally your hardware block will be created then ,Right click on your design under Design sources

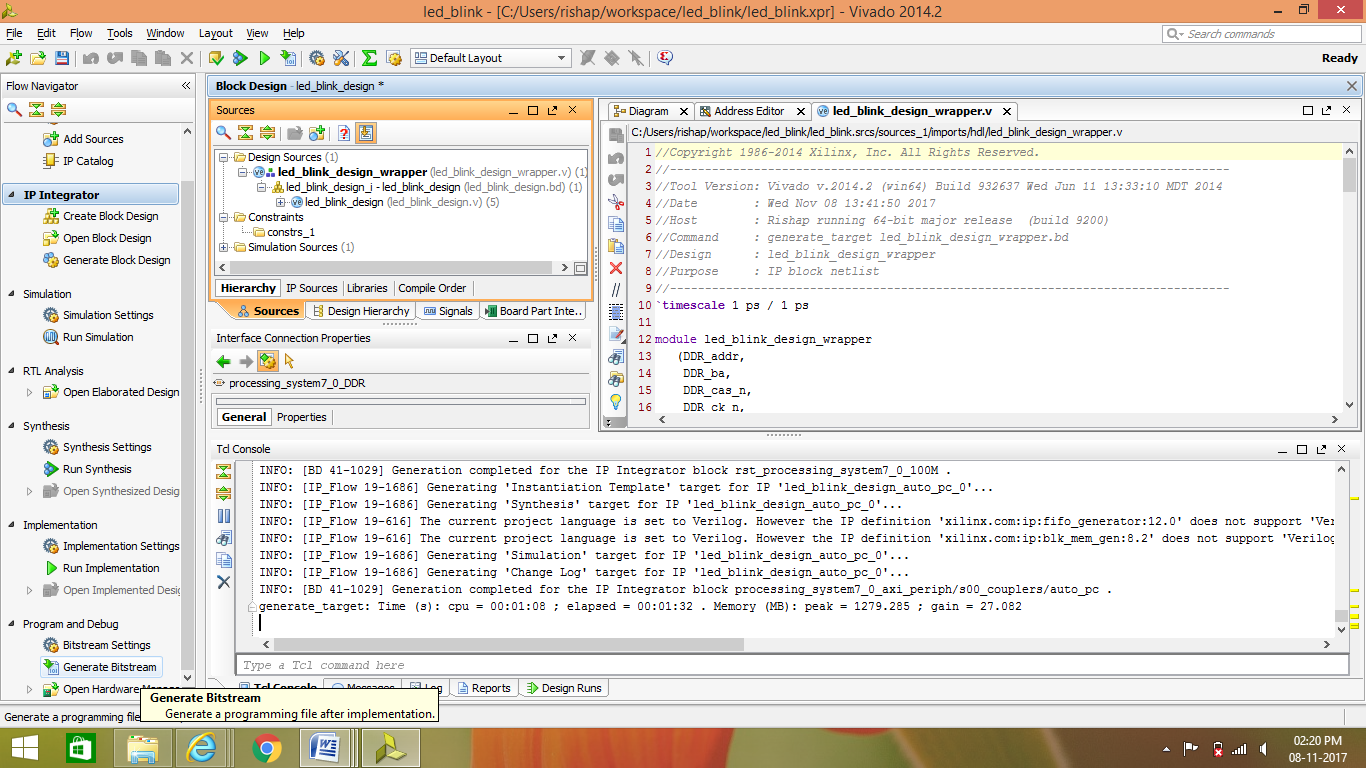


13 : select create HDL Wrapper to have a verilog file of the hardware

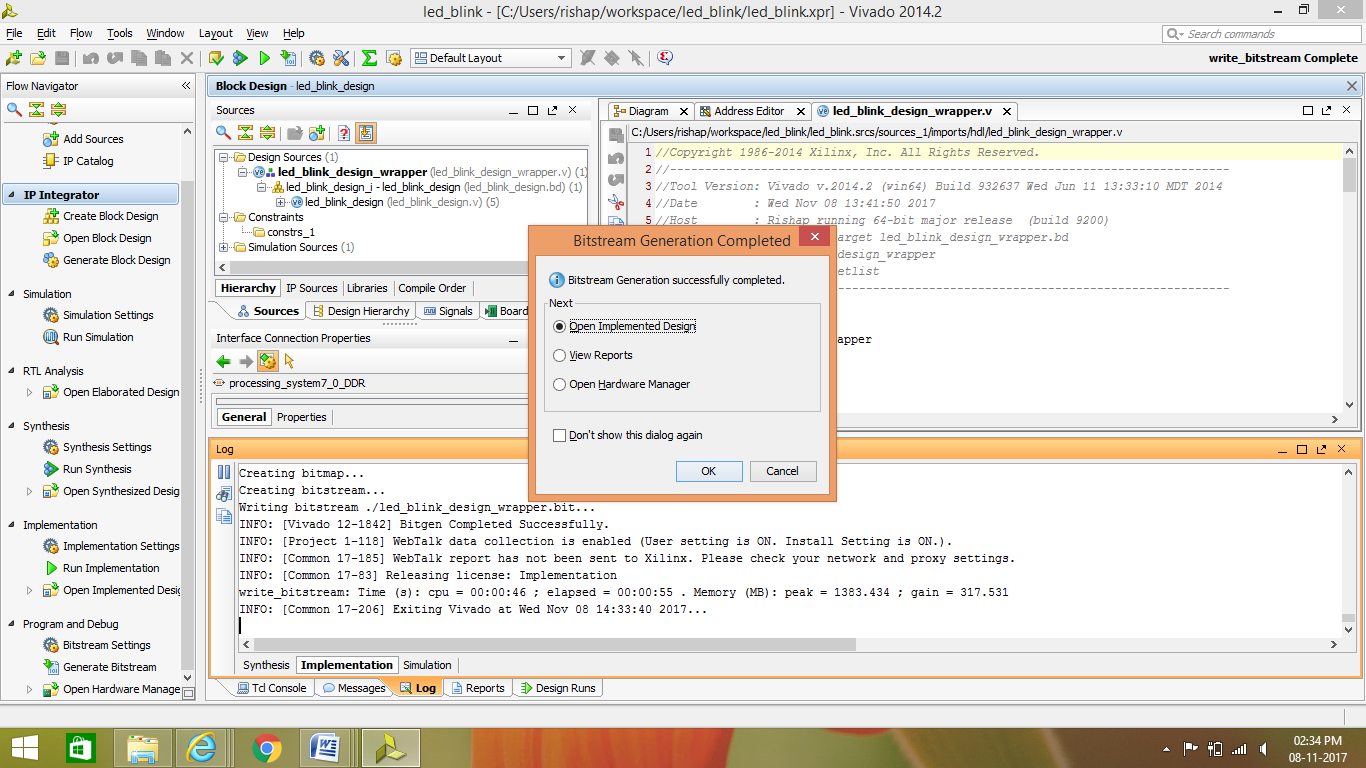


14 : Verilog code for configuring FPGA can be added if required, to the verilog code generated & then Select create ‘generate output products‘

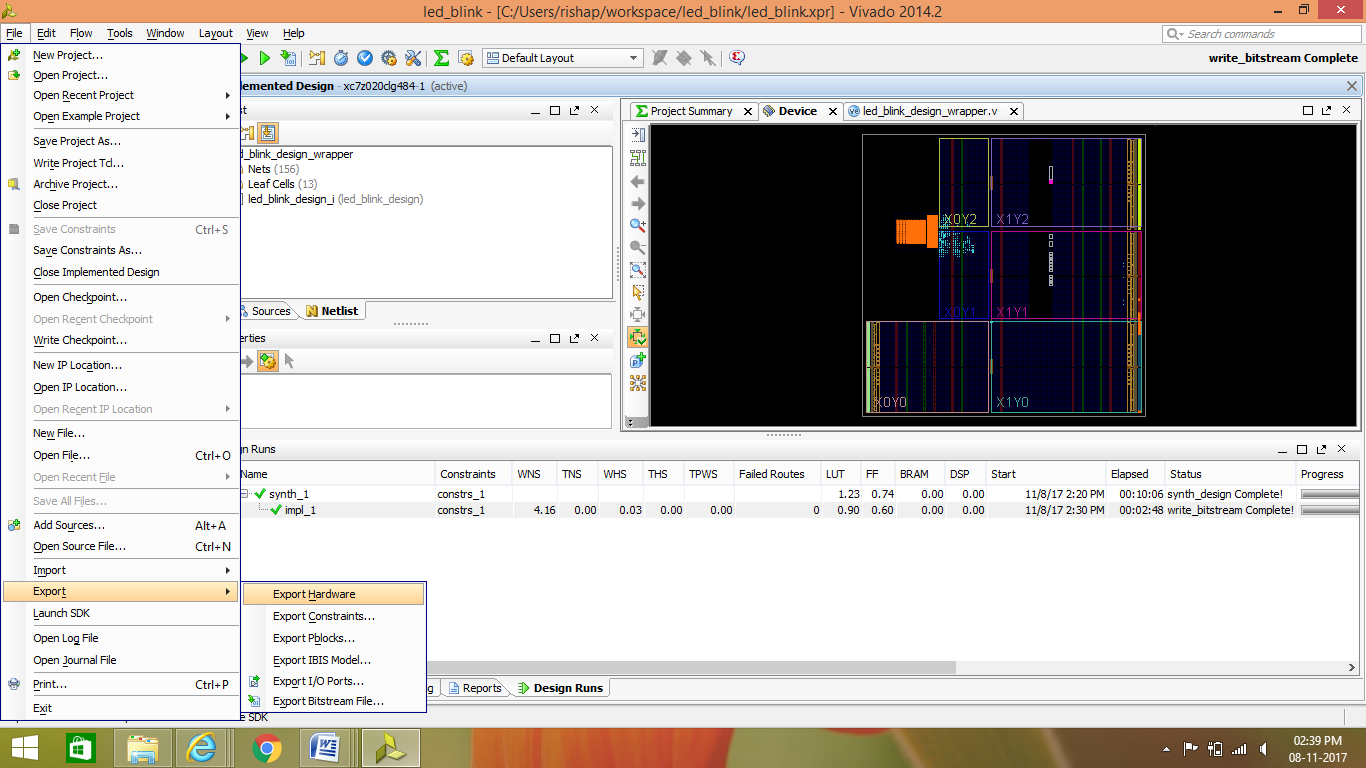


15 : click on’ generate bitstream’ to obtain bitstream file for programming FPGA 

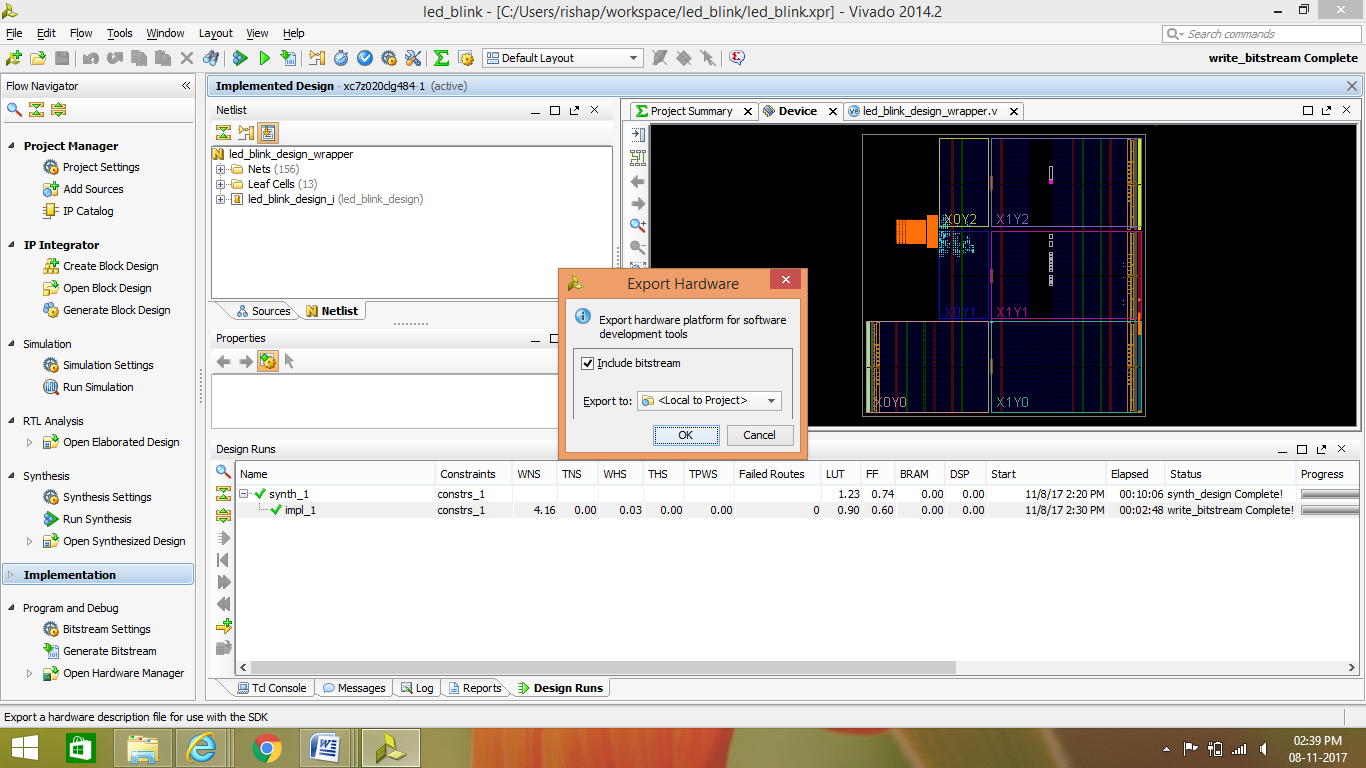
16 : After bitstream generation ,it should show a dialog box below and select “ Open Implement Design” to do floor planning,I/O planning,clock planning and timing Analysis.



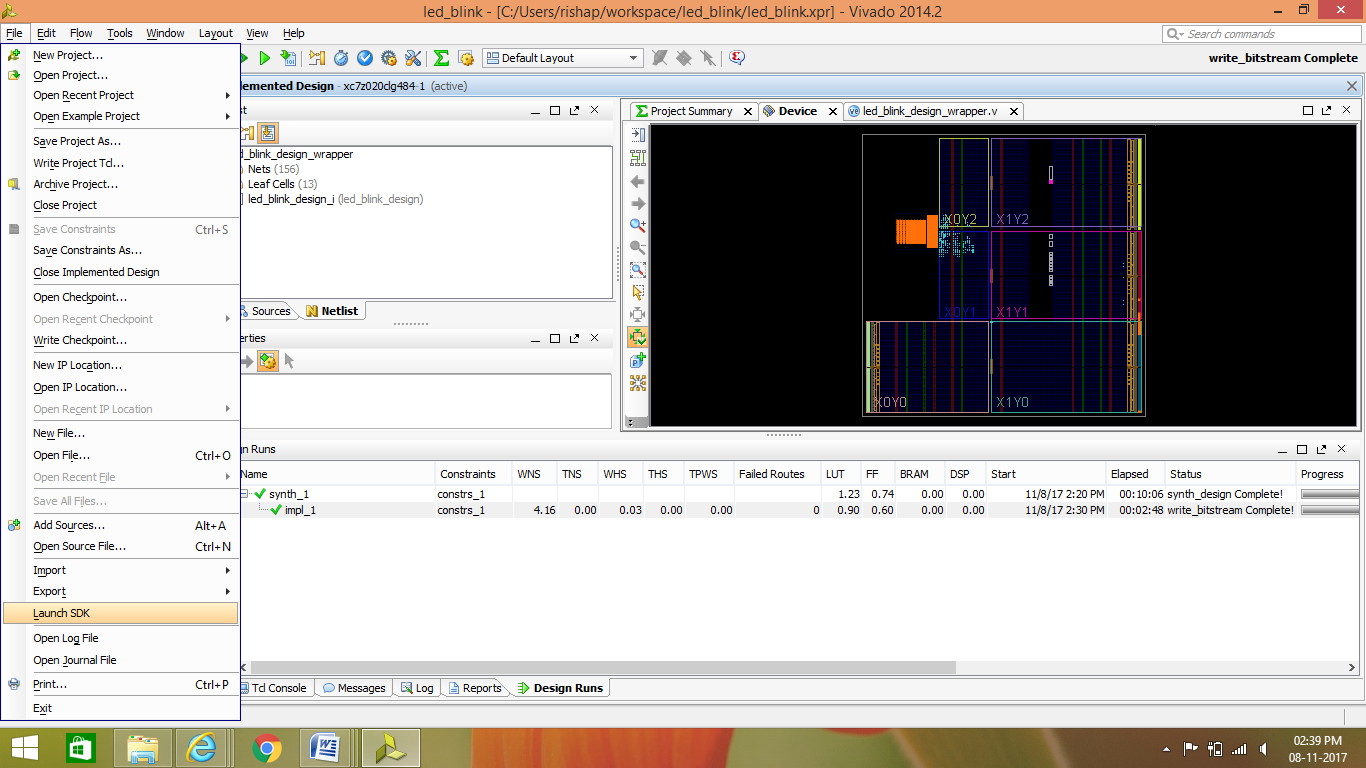
17 : click on file -> export -> export hardware



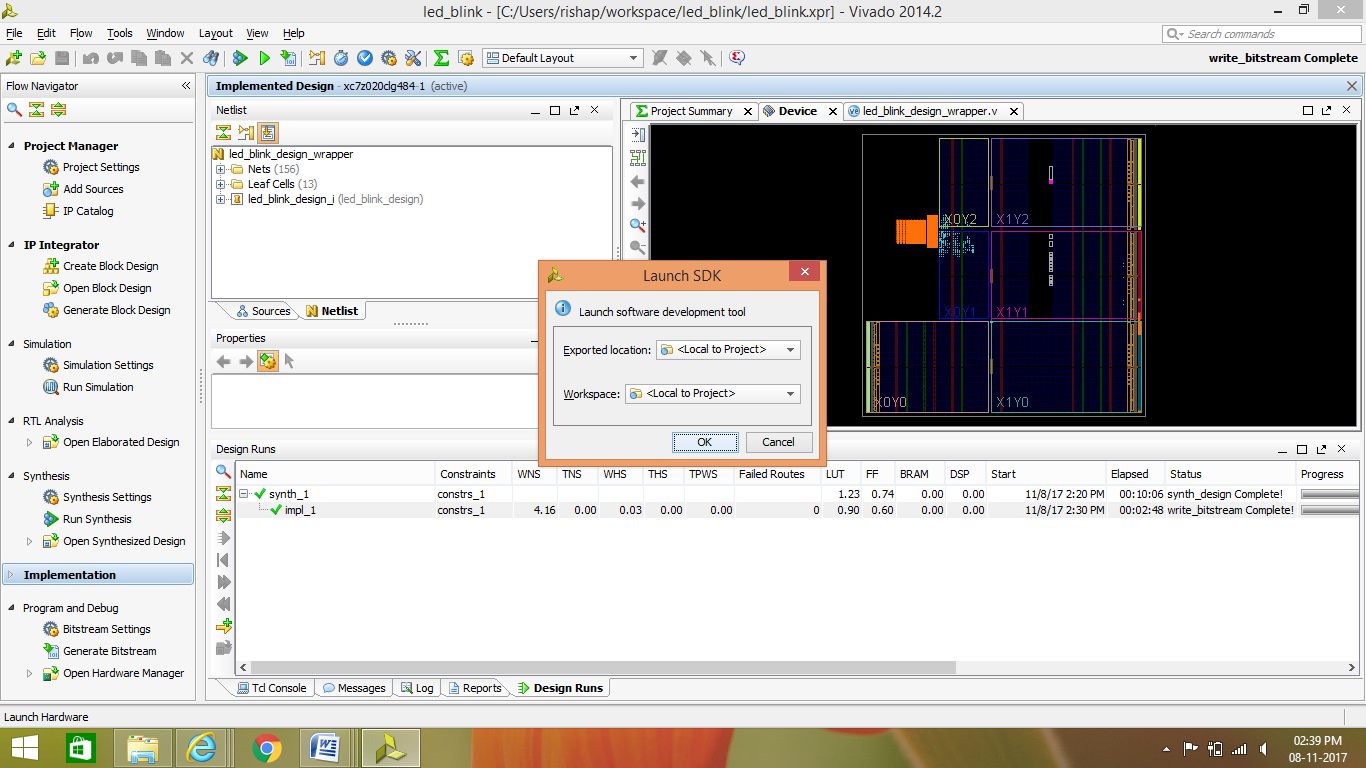
18 : Check the include bitstream



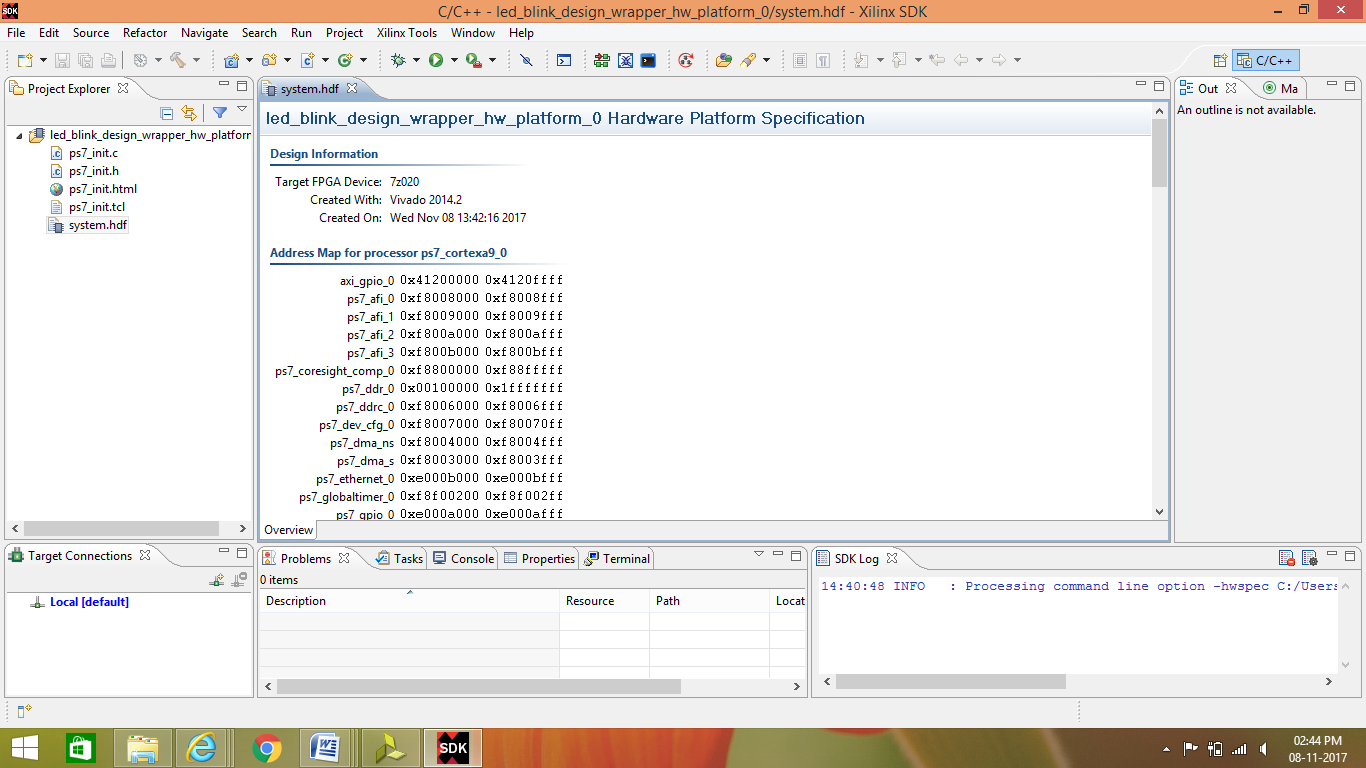
19 : click on file -> export -> export hardware



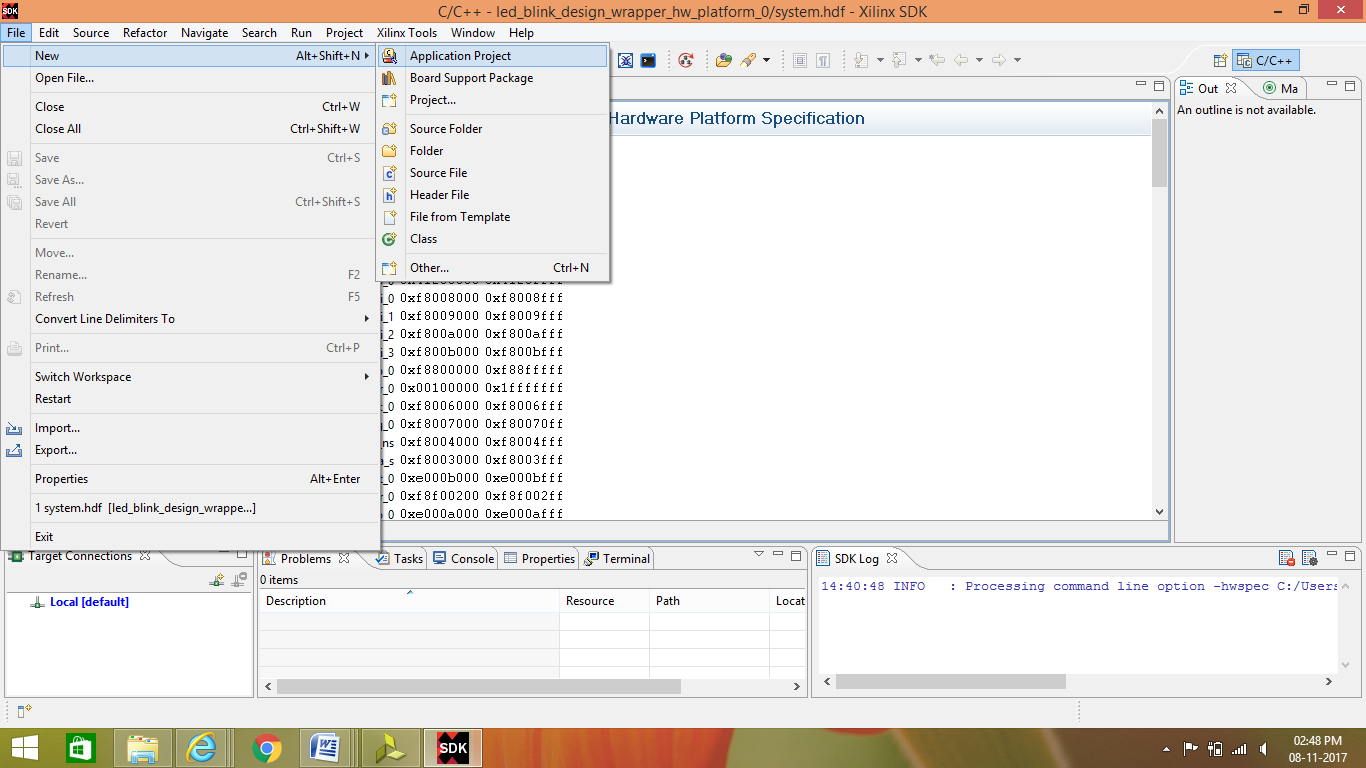
20 : Click OK to launch SDK



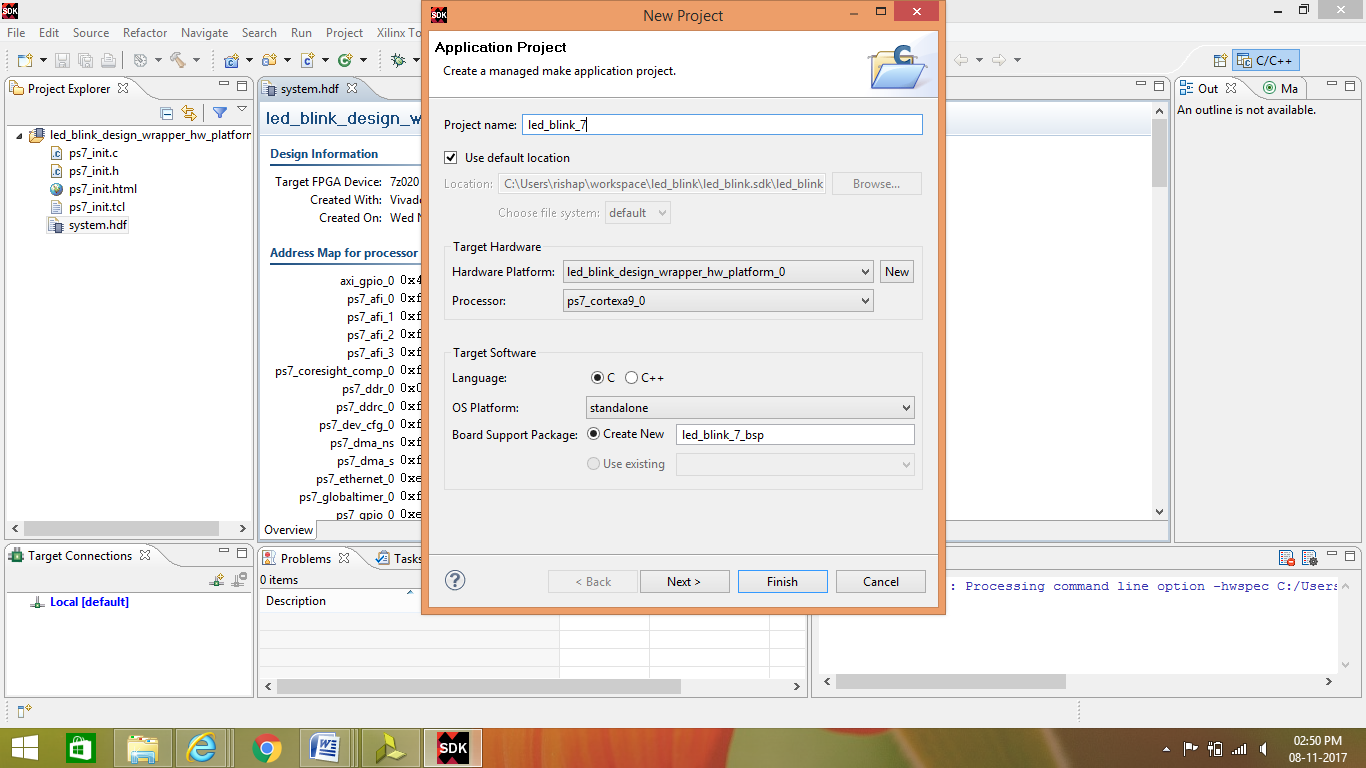
21 : After launching it will show the hardware platform specification which was exported from Vivado



22 : Click on file -> new -> select application project

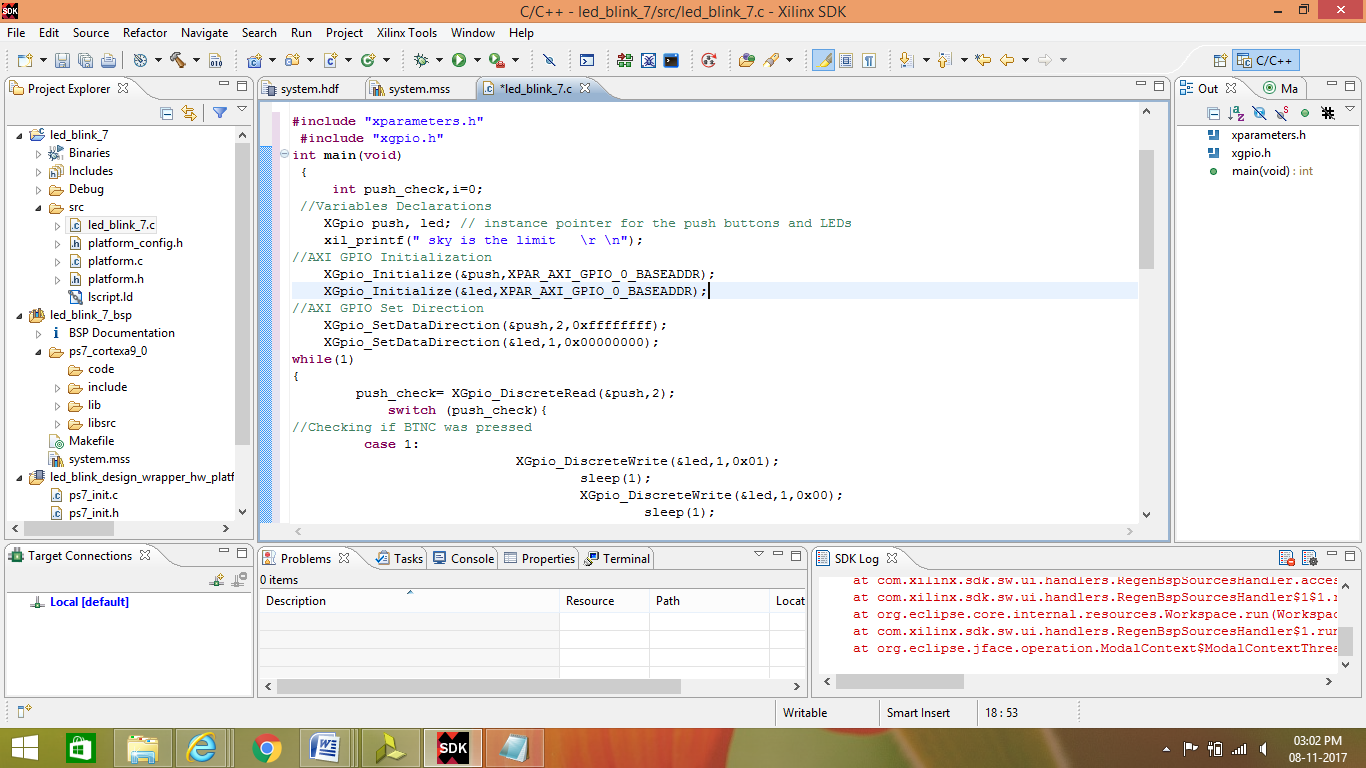


23 : type project name -> check create new bsp and select option shown below and click finish:



24 : Create ‘C’ source file from ->project dialog box at the left window in src folder

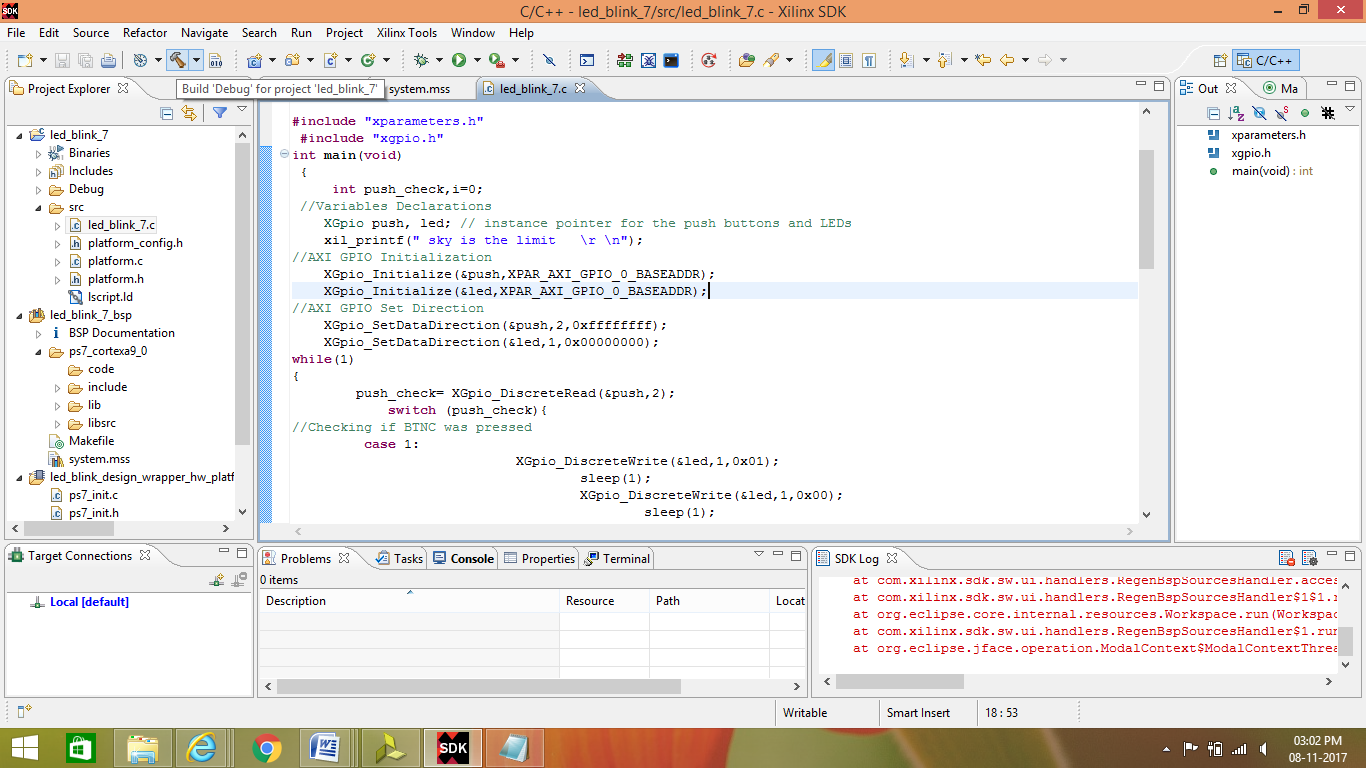
And type code in that file,



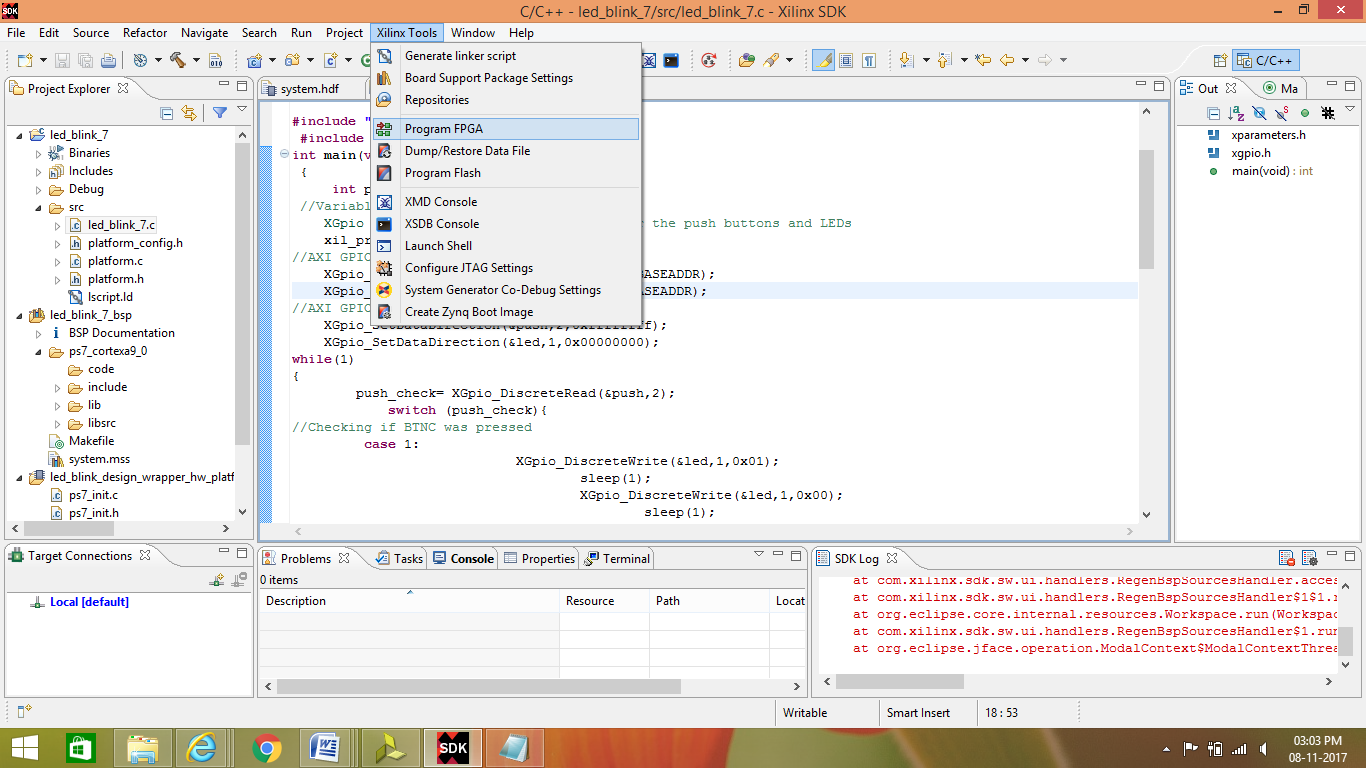
25 : click on -> file -> Save All



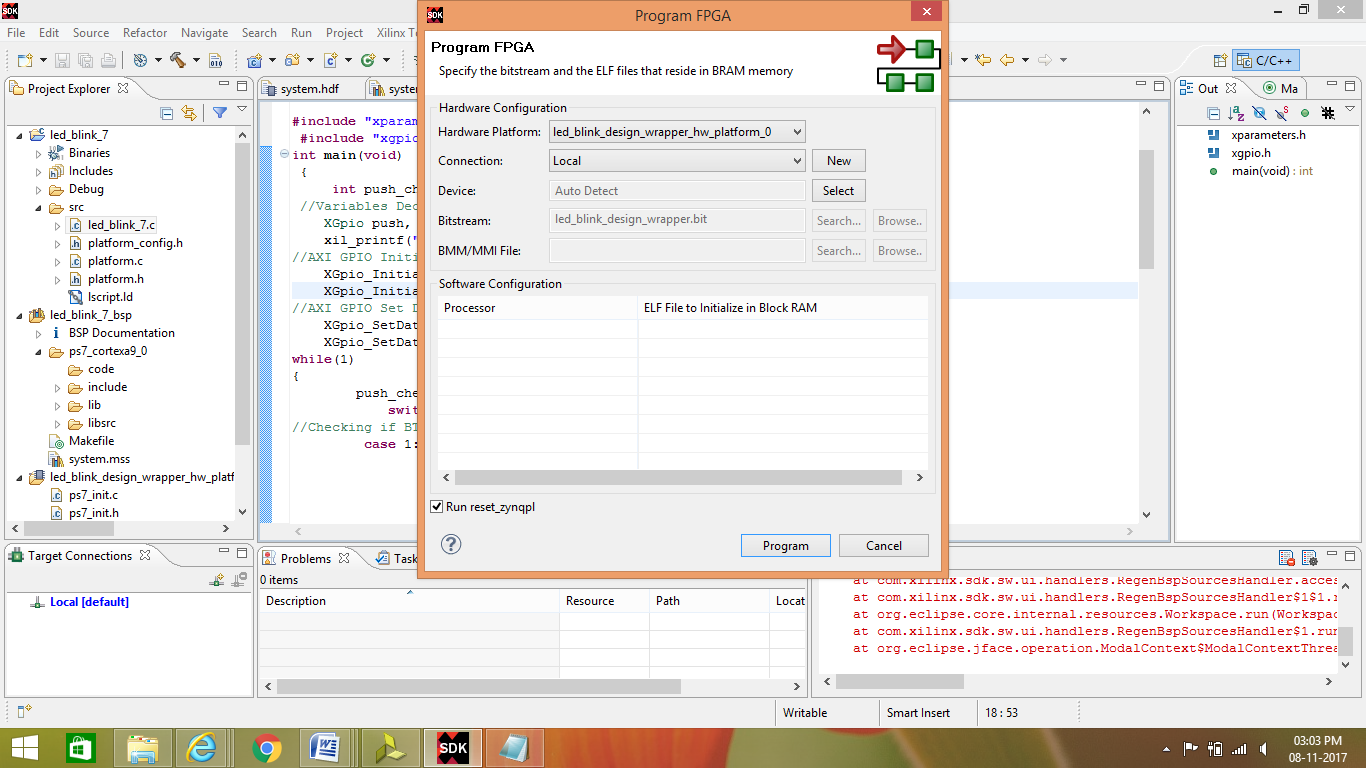
26 : Build the project by clicking on hammer sign



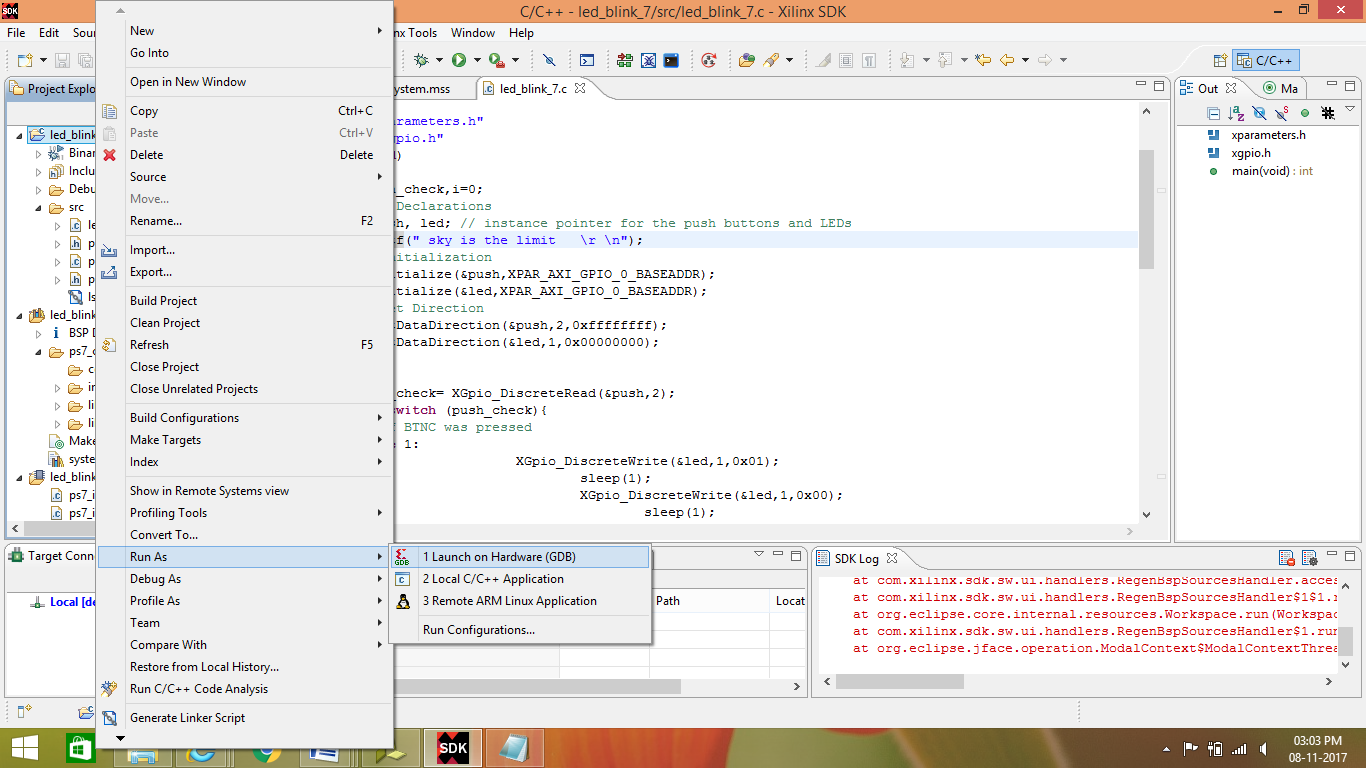
27 : click on -> Xilinx Tools -> select program FPGA



28 : select the bit file and then program:: it is use to program the FPGA part in the ZYNQ processor



29 : To program the ARM in ZYNQ :: Right click on -> project created name -> Run As -> Launch on Hardware(GDB) .



30 : Connect the Zedboard with the PC with the USB to JTAG cable to load the program .