Rishav Dokania

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Education

Texas A&M University — College Station, TX
Master of Science in Computer Engineering - ***GPA: 4/4*** — *Aug. 2022 – Dec 2023*

Delhi Technological University — New Delhi, India
Bachelor of Technology in Electrical and Electronics Engineering - GPA 3.6 — *Aug. 2015 – May 2019*

Technical Skills

Area of Expertise: Silicon Qualification, Simulation Tool, Package Development, Linux Kernel, Data Structures
Languages: System Verilog, Verilog AMS, C, C++ STL, Python, Linux Bash, Java
Developer Tools: Cadence Virtuoso, Linux, SPICE, Eagle ETS 364, MS Office

Experience

Cirrus Logic — May 2023 – Aug 2023
Software Engineer | DSP, Java, Test Panels — *Austin, TX*

- Designed complex Java reusable DSP test panels using functional, asynch programming saved 28+ hrs/month.
- Orchestrated scalable python infrastructure using Poetry, Pytest, CLI, Code Style, SVN and Jenkins CI/CD. Composed design patterns to reduce test panels development time by 3 weeks.
- Architectured 4 generators into 1 object oriented modular, extensible package for automated XML, YAML, JSON content generation over 30+ git commits to reduce turn around time by 25%.

Texas Instruments — July 2019 – July 2022
Design Verification Engineer | Analog IC Design, Python, Linux, Scripting — *Bangalore, India*

- Lead Aging Simulator development to estimate end-of-life performance of Integrated Circuit. Impact of 1 year, $100M+ business, avoid design induced fails by 100%. 3rd highest contributor of Patent Disclosure in 8.
- Verified System level behavior of power path protection circuits - eFuse. Debug design issues and implemented Design for Test (DFT), analysed CPK and Trim circuits to reduce post silicon testing cost by 30%.
- Created various project test plan, schedule, bug reports, 300+ test bench in Linux. Successfully delivered 100% projects on time with weekly peer review of bugs, project tracking on Jira and version control practices.
- Automated product specific test bench, report generation and single-click regression using Python to parse datasheet specification. Cut down 150+ manual setup, 2 weeks/project across various teams total 15+ projects.

Product Engineer | FMEA, Silicon Package Development, Qualification — *July 2019 - July 2022*

- Promoted to Senior Product Engineer, executed 7+ projects on time. Lead 5+ Automotive (with Q006) Qualification and Failure analysis - 8D, 5-Why of 3+ projects. Volunteered for DV role on business needs.
- Root Caused (FMEA) Electrical Over Stress (EOS) failures of e-Fuse controllers using PEM, OBIRCH, FIB and TEM. Collaborated with TI Fellow & process experts, improved Fabrication process of LBC9, 25M+ chips/year.
- Developed QFN package reduced cost by 59% using Cu wires instead of Gold for LM74700QDDF of TAM $60 Million. Debugged BHAST failures in Automotive Qualification and released to market in record 3.5 months.
- Devised navigation, image processing algorithm for robotic handler by object detection in OpenCV. Robot tested 5000+ devices supplied to critical customer and published paper.

Academic & Projects

Survivor Buddy Robot | *Python, ROS* — Jan 2023 – May 2023

- Architectured AI Rescue Robot class diagram, project structure over 2K+ lines of code for 65% more readability.
- Modularized 5 ML Human Interaction behaviors with Observer Design Pattern for 35% better extensibility.
- Designed multi-threading algorithm for parallel image & audio processing to reduce latency by 95%, below 0.1s.

Achievements

Patent Disclosure: Software to Simulate and Visualize all Datasheet Parameters Over the Lifetime of the Product.
Texas Instruments Global Recognition Award - 4 times : Diagnosed Fabrication Issue, 3 weeks early Project Delivery, Improved Qualification Hardware Design, Released LM74700DDF in record 3.5 months' time.
Publications - 3 Papers: Poster Presentation on EOS induced failure (April 2022); Qualification HW Design for contamination issue (Nov. 2022); Co-author, Robotic Handler for Qualification Test Automation (April 2020).