Experiment-9

Aim:

1.To write and simulate the Verilog codes for the following structural modelling.

- Full adder using two half adder and or gate
- 4 bit full adder using 1 bit full adder

Software required:

1.Quartus II

VHDL code:

Code a:

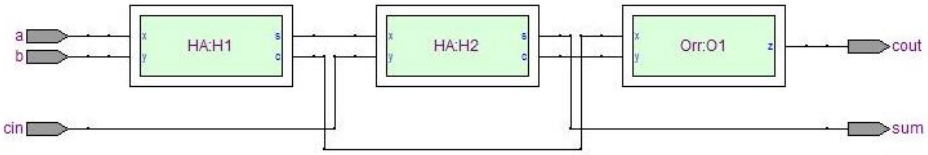
```
module full_adder(a,b,cin,cout,sum);
input a,b,cin;
output sum, cout;
wire s0,c0,c1;
HA H1 (a,b,s0,c0);
HA H2 (s0,cin,sum,c1);
Orr O1 (cout,c0,c1);
endmodule
module HA(x,y,s,c);
input x,y;
output s,c;
assign s = x^y;
assign c = x&y;
endmodule
module Orr(z,x,y);
input x,y;
output z;
assign z = x|y;
endmodule
```

Code b:

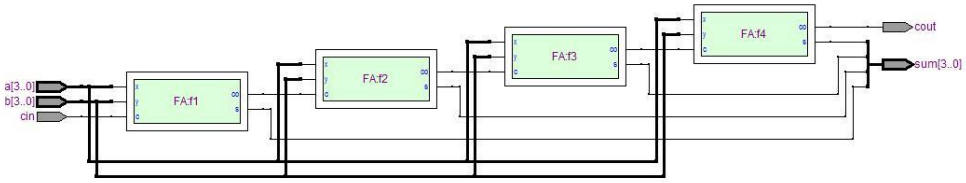
```
module FA_using_1bitFA(a, b, cin,sum, cout);
input [3:0] a,b;
input cin;
output [3:0] sum;
output cout;
wire c1,c2,c3;
FA f1 (a[0],b[0],cin,c1,sum[0]);
FA f2 (a[1],b[1],c1,c2,sum[1]);
FA f3 (a[2],b[2],c2,c3,sum[2]);
FA f4 (a[3],b[3],c3,cout,sum[3]);
endmodule
module FA(x,y,c,co,s);
input x,y,c;
output co,s;
assign s = x^y^c;
assign co = (x&y) | (c&(x^y));
endmodule
```

RTL schematic:

RTL a:

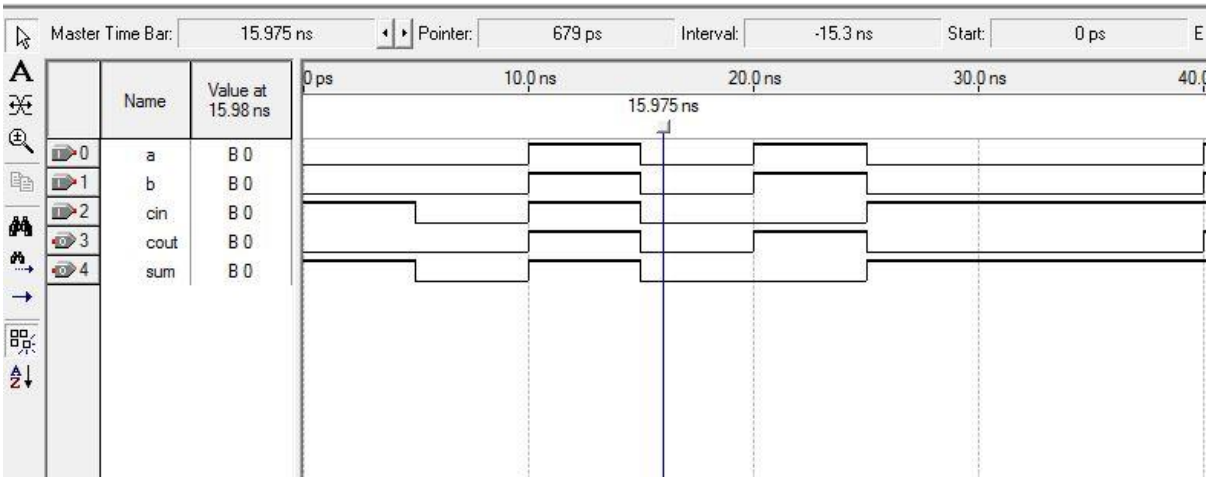


RTL b:

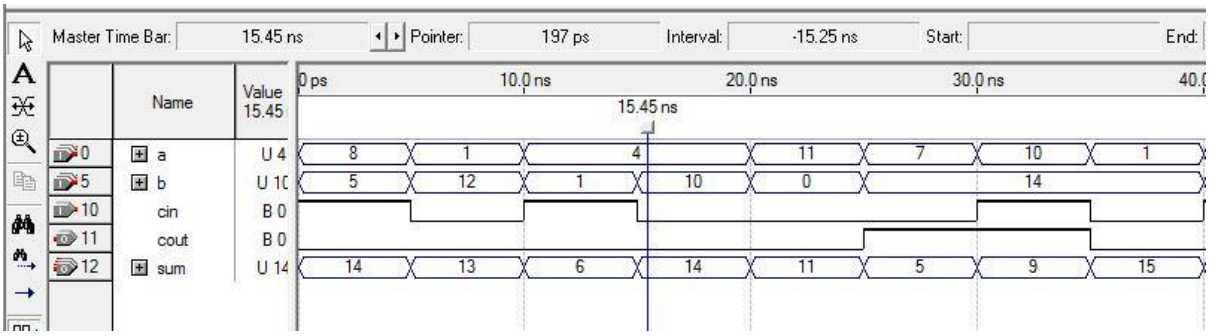


Waveforms:

Waveform a:



Waveform b:



Result:

Hence the Verilog codes were written and the simulation was successful for the given basic combinational logic.

Waveforms and RTL schematic were recorded and verified.