On Network-on-a-chip based Multiprocessors

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Abstract

The paper begins by providing a brief introduction to the concept of Network on a chip (NoC). Followed by an abstract overview of some of the popular NoC architectures, it presents a comparative analysis of the NoC architecture to its alternatives. Further, the paper discusses some of the efforts made towards the improvement in scalability and power efficiency of the multiprocessors implementing it. Briefing upon the latest key advancements in the NoC technology, the paper highlights the potential critical research questions catalytic to the proliferation of this technology. Finally, the paper concludes by expressing the opinions based on the current trends in multiprocessors and the ongoing development efforts in NoC.

1 Introduction

Network on a chip is a communication subsystem on an integrated circuit, typically between intellectual property (IP) cores on a System on a Chip (SoC), according to the Wikipedia[1]. This technology applies networking theory and methods to on-chip communication[1]. In one of the very early researches on on-chip interconnection networks[2], Dally et. al. study how the top level wires can be structured on a chip by using these networks in place of ad-hoc global wiring, facilitating modular design. They show that the processors, along with other system modules like memories, peripherals, etc. form the network clients that communicate by sending packets to one another over the network. Each client is placed in a rectangular tile on the chip; the network logic occupying a small amount of area (estimated 6.6%) in each of them[2].

Benini et. al. in their study of NoC as a new SoC paradigm[3], establish the premise that interconnect technology will pose itself as the limiting factor for achieving SoC's operational goals. They view an SoC as a micronetwork of components and propose that a layered design of reconfigurable micronetworks can best achieve efficient communication on SoCs by exploiting the methods and tools used for general networks. Moreover, the on-chip micronetwork architectures and protocols can be tailored to specific system configurations and application classes[3]. We reinforce this observation by briefing upon some of

the various architectural styles and implementations of this technology available till date.

We believe that the NoC technology exhibits strong potential for improvements in the processing systems on-chip and to base our argument firmly, we identify some of its inherent critical challenges like scalability and power efficiency among others. The unique characteristics of silicon chips define a new set of NoC specific problems like automatic network design process, power and area optimization and specialized system functionalities[4], the analyses of which is beyond the scope of our paper.

Research has been underway in this field for improving the efficiency[5], scalability[6, 7] and performance[7, 9], albeit mostly for particular NoC architectures. Furthermore, NoC, by virtue of its proven efficiency, has been used to improve the overall system performance and scalability of an existing FCUDA (CUDA-to-FPGA) architecture[10]. We will have a more detailed look at these efforts towards the end of this paper and discuss about the potential research areas and challenges.

2 Popular Architectures

Over the years, NoC technology has been molded by many to suit their own specific purposes. Therefore, one might like to assess the particular design that their application could be served the best by. We will broadly explore some of these architectures and attempt to provide the reader with a substantial idea about each of them.

2.1 Optical NoC

Optical NoCs use integratded optical interconnects[14], unlike traditional NoC whic hrelies on electrical signals to transfer information, hence called electrical network-on-chip (ENoC)[12]. But the performance and energy efficiency of ENoC are bound by the significantly unbalanced scaling of on-chip global metal wires comparing to transistors[12].

Optical NoCs are proposed to achieve low-power ultra-high-bandwidth data transmission in optical domain as states [13]. The most important components of optical NoCs are the optical on-chip routers that perform routing and flow control functions, it adds. Briere et. al., in [14] assess an ONoC for MPSoC (Multi-processor Systems on Chip) design. As per their study, ONoC guarantees low latency and a contention free interconnect and can also decrease processing time compared to traditional electrical interconnects. it os observed in [14] that ONoC may improve performances in MPSoC running intensive communication application.

With optical telecommunications proving to be successful in many networking domains in replacing electrical telecommunications[12], Optical NoC forms a promising style for improvements in the MPSoC designs as also suggested in [14].

2.2 Wireless NoC

With the increasing demand for faster and smaller technologies, in 2012, the engineers at Drexel University started their work on the idea of Wireless Network-on-Chip[15]. Back then, they earned an NSF grant for developing tiny Wireless radio frequency antennas intended for transmission between the parts of chip without using wired interconnections.

This approach is also interesting because unlike in Optical NoC, which requires clear line of sight between transmitters and receivers, the radio waves can travel through solids. It has been shown that the energy consumption and data rates in massively integrated multicore platforms can be significantly improved by small-world network architectures with long-range wireless shortcuts[16]. Recently, Kim et. al. incorporated the emerging mSWNoC (millimeter-wave small-world wireless NoC), comprising of two principal components- antennas and transceivers, as the communication backbone of a VFI-based multicore chip. They observed that it is possible to significant levels of energy efficiency without paying a large performance penalty[16].

In [17], the design of a small-world NoC architecture with mm-wave wireless interconnects used as long-range links is proposed and it has been observed that the mWNoC outperforms its more traditional wireline counterpart in terms of achievable bandwidth and energy dissipation in the presence of various synthetic and application specific traffic patterns.

2.3 3D NoC

3D NoC[18] is designed by Morris et. al. to leverage the advantages of both nanophotonic interconnects and 3D stacking[19] technologies with architectural innovations for achieving a high-bandwidth, low-latency, multi-layer, reconfigurable network.

3D stacking of multiple layers has been shown to be beneficial due to shorter inter-layer channel, reduced number of hops and increased bandwidth density[18]. Such an architecture consists of multiple cores in tile configuration on a 3D IC. In the particular architecture of [18], the tiles are divided into four groups based on their physical location with nanophotonic crossbars forming the inter-group connections. They conclude that using the integration of NIs and 3D interconnects, the optical power losses found in 2D planar NoCs can be reduced by decomposing a large 2D nanophotonic crossbar into multiple smaller nanophotonic crossbar layers.

Paper [20] advocates the performance improvements of the 3D NoC (without the NI integration) architecture. Combining the advantages of the two emerging technologies puts 3D NoC in the forefront of the trending NoC architectures.

3 Comparison with Alternatives

As the area of chip multiprocessors decreases, complicating the wire network on the chip cannot be afforded. Here, NoC architecture provides enhanced performance against the other alternatives like dedicated point-to-point signal wires, shared buses, or segmented buses with bridges[1].

According to [10], shared buses, although area efficient, do not scale in total bandwidth with the increase in the number of cores. Whereas, point-to-point interconnections, although scale the total bandwidth, the $O(n^2)$ scaling in connection area is infeasible for large designs. And this is where NoC interconnects balance bandwidth scaling and area consumption[10].

NoC enables integration of large number of IP cores in a single SoC[20]. The wires in the links of the NoC are shared by many signals thus yielding a high level of parallelism with all links simultaneously operating on different data packets[1]. The traditional bus architecture of SoC has several problems like the huge clock tree, the high power consumption and the limited scalability, that seriously restrict its average communication efficiency[21], all of which can be overcome using the different architectural styles like those in [13], [18] and [16]. Further, like popular system-level buses, NoC enhances modularity by providing a standard interface[2].

4 Improvement Efforts

In addition to the inherent advantages of NoCs, there have been many efforts made in improving the scalability and power efficiency, often targeted for specific applications.

4.1 Scalability

The Scalable, Programmable, Integrated, Network (SPIN) on-chip micronetwork from [3] defines packets as 32-bit words sequences with packet header fitting in the first word. Using a byte in the header to identify the destination allows it to scale up to 256 terminal nodes. The FCUDA-NoC[10] makes use of the Directory-Based Data Sharing mechanism in order to efficiently share on-chip data, a critical aspect of the performance scalability. In [], 3D integrated CLOS NoC is proposed, the major benefit of which has been claimed the easy scalability to accommodate any number of additional nodes in many-core chip multiprocessors. It is argued that the chip multiprocessors can be scaled to any

number of nodes keeping the radix and diameter of the network the same and that any limit to 3D stacking could only be due to limitations in 3D process technology.

4.2 Power Efficiency

[22] studied how the power consumption of hard and soft NoC components varies with design parameters and data injection rates. It was then used as a basis for designing energy-efficient NoCs to determine that the hard NoCs consisting of hard routers and hard links were more power efficient. Recently, Naik et. al. in [5] used heteregenous circuit switched routers in their NoC design to reduce power consumption by about 13%. They further claimed that the use of multistage CLOS switch network produced 26% reduction in power compared to the same sized Crossbar switches. In another latest work by Yadav et. al.[23], they proposed the Dual Link Mesh to be a power and cost efficient architecture compared to Single Link Mesh and other multiplane networks. They observed that the total router power benefit approached 58% for 32nm technology while it limited to 40% for 65nm.

5 Recent Advancements

Power and area have been observed to be two critical design aspects of CMPs (chip multiprocessors). With the ever rising number of integrated processing elements to chips, NoC can not only enable organized interconnections between IP cores but also create opportunities for improving in these vital areas. [9] evaluates the different NoC architectures based on these two criteria.

Recently[24], a Software Defined Network-on-Chip design has been proposed and compared against a 2D Mesh NoC topology which enables savings of 39.4% of the chip area and up to 72.4% of the consumed power. In another attempt[25] for improving the Wireless NoC efficiency, Catania et. al. have succeeded in reducing the total communication energy by up to 25% without impacting the performance metrics (although with a negligible impact on silicon area) while Munuswamy et. al. have not only provided energy-efficient on-chip data transfer but also a suitable liquid cooling technology[26].

A new approach of combining the advantages of optical and electronic technologies is proposed in [27] called the H2ONoC architecture. Through an experimental evaluation based on both synthetic benchmarks and real-world applications, H2ONoC has been shown to achieve 32% and 8% less energy consumption under synthetic traffic and 74% and 14% less energy consumption with real applications as compared to hybrid mesh- and torus-based NoC architectures.

6 Potential Research Areas

As we have seen, NoC technology has over time seen a lot of development in all possible areas like topologies, energy efficiency and even area consumption. Despite, some among the many areas remain less explored and therefore have a significant scope for research. One such area is the Network Main Memory as identified by Tang et. al. in [28]. As they presume, their memory architecture can provide a potential approach to solve the memory bottleneck problem of NoC-based chips. Besides, they argue that development of the appropriate OS model, application model and communication model is also important to achieve the most efficient use of parallelism of NoC and NMM.

On the other hand, due to the popularity of the 3D IC technology, effective design and usage of the interconnects in such architectures forms another potential domain for research as identified in [29]. Not only is delivering performance vital to their design but also checking the power consumption and mutual interference of the critically compact connections is a deal, which further requires efficient routing algorithms for better utilization of the network. It additionally touches the debate of circuit switching and packet switching within the on-chip networks. Since each technique has its own unique advantages, one could possibly think of a hybrid approach of using both the techniques as and when required dynamically.

7 Conclusion

NoC architectures have risen as a solution to the scalability problem of the conventional on-chip communication systems like buses which become a communication bottleneck as the systems grow large. The current trend has formed such that there are many different styles of NoC being developed for catering particular requirements. From among these different flavors available today, the 3D variation of NoCs appears to be the most popular owing to the fact that many more attempts to exploit or build on top of this style have been observed. Furthermore, some areas of the NoC technology remain very less explored while others require an even in-depth research.

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