Novel Signal Conditioning Circuits for Resistive Sensors

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Novel Signal Conditioning Circuits for Resistive Sensors

A Thesis

submitted by

Madhu Mohan N.

for the award of the degree of

Doctor of Philosophy

in

Electrical Engineering

Department of Electrical Engineering
Indian Institute of Technology Madras

October 2009

Thesis Certificate

This is to certify that this thesis titled "**Novel Signal Conditioning Circuits for Resistive Sensors**", submitted by **Madhu Mohan N.**, to the Indian Institute of Technology Madras, in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy in Electrical Engineering, is a bonafide record of research carried out by him, under my supervision. The contents of this thesis, in part or in full, have not been and will not be submitted to any other Institute or University for the award of any degree or diploma.

Place : Chennai – 600036.
Date : October 15, 2009.

Research Advisor

Prof. V. Jagadeesh Kumar
Department of Electrical Engineering,
Indian Institute of Technology Madras.

To Sreedharamama and Prem

Acknowledgement

How do you express your gratitude to a person who has been on the rock on which your work has been built, who has been unfailingly supportive, who has remained unflappable even when your initial work had to be abandoned, who has the foresight to direct you to work which would later develop into your thesis, who has the patience to listen to your wacky ideas and the wisdom and understanding to make you realise their wackiness, who has been a role model as a teacher and advisor, to whom you turn even for the smallest of help ? The answer is you can't. So, to my research supervisor, **Prof. Jagadeesh Kumar V.**, I will just content myself with saying, "Sir, thank you very much".

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List of Symbols and Abbreviations

A	*Area of cross-section of the resistor*
a,b,c,d	*Bridge terminals*
A_1, A_2	*Digital Control lines*
ADC	*Analog to Digital Converter*
A_v	*(i) Gain of the instrumentation amplifier* *(ii) Gain of the auxiliary amplifier (log amp)*
BA	*Buffer Amplifier*
BCD	*Binary Coded Decimal*
C_F	*Feedback capacitance of the integrator*
C_{AG}, C_{BG}, C_{CG}	*Stray capacitances between terminals P,S and COM respectively to ground*
CMOS	*Complementary Metal Oxide Semiconductor*
CMWB	*Current Mode Wheatstone Bridge*
D	*Input to the D Flip-flop*
DAQ	*Data Acquisition Device*
DSRDC	*Dual Slope Resistance to Digital Converter*
e[n]	*Discrete, noise signal*
f_B	*Frequency Bandwidth*
f_{in}	*Input frequency*
f_s	*Sampling frequency*
FSR	*Force Sensing Resistor*
G	*Gage factor of a typical resistive strain gage*
I/O	*Input / Output*
I_B	*Opamp bias current*

i_c	*Capacitor current*
IC	*Integrated Chip*
IEC	*International Electro-technical Commission*
IEEE	*Institute of Electrical and Electronics Engineers*
I_{LI}	*Leakage Current*
I_{ref}	*Current flowing through the reference resistor*
I_θ	*Current flowing through the thermistor*
k	*Transformation efficiency of the sensor*
k_1	*Transformation efficiency of the resistor* R_1
k_2	*Transformation efficiency of the resistor* R_2
K_1, K_2, K_3	*Material dependent constants defined by Bosson's Law*
K_4, K_5, K_6, K_7	*Constants*
l	*Length of the resistor*
LDC	*Linearising Digital Converter*
LPF	*Low-pass filter*
LSB	*Least Significant Bit*
MSa/s	*Mega* (10^6) *Samples per second*
MSB	*Most Significant Bit*
$N_{(0)}$	*Number of cycles when the output remains 'low'*
$N_{(1)}$	*Number of cycles when the output remains 'high'*
N_1	*Number of clock cycles during the period* T_1
N_2	*Number of clock cycles during the period* T_2
NASA	*National Aeronautical and Space Agency*

N_{fs}	*Full-scale count of the counter*
N_k	*Thermistor dependent constant count*
NTC	*Negative Temperature Coefficient*
OA	*Operational Amplifier*
OC	*Comparator*
OFCC	*Operational Floating Current Conveyor*
P, S,T,U,COM	*Terminals of the differential resistive sensor*
PCB	*Printed Circuit Board*
PCM	*Pulse Code Modulation*
P_{S1}, P_{S2}	*Output of the switches S_1 and S_2*
Pt100	*Platinum Resistance Temperature Detector with nominal resistance = 100 Ω*
Pt1000	*Platinum Resistance Temperature Detector with nominal resistance = 1000 Ω*
Pt10000	*Platinum Resistance Temperature Detector with nominal resistance = 10000 Ω*
PTC	*Positive Temperature Coefficient*
Q	*Output of the D Flip-flop*
r	*ON resistance of the switch*
r_1, r_2	*ON resistances of the switches S_1 and S_2*
R_1, R_2	*Resistances of the differential resistive sensor*
R_{B1}, R_{B2}, R_{B3}, R_{B4}	*Resistances of the different arms of the Wheatstone bridge*
R_5,R_6	*Resistors forming the feedback network for compensating the Wheatstone bridge*
R_G	*Galvanometer resistance*
R_I	*Resistance forming part of the integrator*
R_{o1}	*Nominal value of R_1*

R_{o2}	*Nominal value of R_2*
R_L	*Load resistance*
R_o	*Nominal Value of the resistance of the resistive sensor*
R_o'	*Actual value of the standard reference resistance*
R_s	*Resistance of a reference resistor*
RTD	*Resistance Temperature Detector*
R_x	*Resistance of the single element resistive sensor*
R_θ	*Resistance of the thermistor at temperature θ*
S_1, S_2	*Switches*
SDRDC	*Sigma Delta Resistance to Digital Converter*
SNR	*Signal to Noise Ratio*
SPDT	*Single-Pole, Double Throw switch*
T_1	*Fixed time period - for first integration*
T_2	*Time period to be measured*
T_A, T_B, T_C, T_D	*Periods of integration (Owen's method)*
T_c	*Time period of the clock input to the Timing and Control Unit*
TCU	*Timing and Control Unit*
T_s	*Sampling time interval*
TTL	*Transistor-Transistor Logic*
USB	*Universal Serial Bus*
V_B	*Excitation voltage of the Wheatstone bridge*
v_c	*Output of the comparator*
v_{log}	*Output of the logarithmic amplifier*

VLSI	*Very Large Scale Integration*
VMWB	*Voltage Mode Wheatstone Bridge*
$-V_R$	*Reference voltage of negative polarity*
$-V_u$	*Negative reference voltage*
$+V_d$	*Positive reference voltage*
$+V_R$	*Reference voltage of positive polarity*
v_o	*Output of the feedback compensated Wheatstone Bridge*
v_{oB}	*Output of the Wheatstone bridge*
v_{oc}	*Offset voltage of the comparator*
v_{oi}	*Output of the integrator*
v_{os}	*Offset voltage of the opamp*
x	*Measurand, physical quantity to be measured*
$x[n]$	*Sampled, continuous time signal*
$X_s[f]$	*Sampled signal in the frequency domain*
y	*Output of the D Flip-flop*
α	*Ratio of R_o to R_o'*
β	*Amount of feedback in the compensated Wheatstone bridge*
γ	*Ratio of the resistances of adjacent arms of the Wheatstone bridge*
ε	*Resistive strain*
ζ	*Variation from ideal for the compensated Wheatstone bridge($\zeta < 1$)*
η	*Ratio of the magnitudes of the reference voltages*
θ	*Temperature*
κ	*Ratio of ON resistances*

λ	*[(k_1/k_2) - 1] (Ratio of transformation efficiencies of the two elements of the differential sensor)*
ρ	*Resistivity of the material of the resistive sensor*
τ_b	*Time taken for the switch to break contact*
τ_c	*Time delay due to the comparator*
τ_m	*Time taken for the switch to make contact*
τ_s	*Delay caused by the switch*
χ	*[(R_A/R_B) - 1] (Ratio of nominal values of the two elements of the differential sensor)*

Abstract

Keywords – Resistive Sensors, Direct Digital Converter, Wheatstone bridge, thermistors, differential sensors, Sigma-Delta converters, dual slope integrators, ADC

Resistive sensors are widely used in the measurement of parameters like temperature, displacement, force and pressure. Development of appropriate signal conditioning circuits suitable for resistive sensors has been an active field of research for long. The work presented in this thesis augments the ongoing research in this area.

A novel solution is first presented for the long standing issue of linearising the output of a Wheatstone bridge based analog signal conditioning circuit, operating with a single element resistive sensor. It would be advantageous if the signal conditioning circuits provide a direct digital output proportional to the parameter being sensed. Such a transducer can be easily interfaced to the digital instrumentation systems used today, without the need for another analog to digital converter. The work presented in this thesis addresses this issue and proposes simple, highly effective and accurate direct digital converter topologies suitable for different kinds of resistive sensors. A direct digital converter scheme suitable for a single element resistive sensor (like the RTD) is first developed. A dual slope digital converter that accepts a nonlinear sensor like the thermistor and provides a digital output linear with the temperature being sensed is then presented. Two converter topologies, suitable for differential resistive sensors, based on the dual slope type and the sigma-delta principle are then proposed.

A common advantage of all the converter topologies is that the digital output is dependent only on the transformation efficiency of the sensors, a pre-determined fixed time period and a constant reference voltage or voltages. A high degree of accuracy is therefore easily established. All the techniques presented in this thesis are rigorously analysed and the constraints in selecting appropriate components clearly brought out. The practicality of all the methods is validated through simulation studies as well as test results obtained on prototype units.

1.Introduction

1.1 Transducers

The easy availability, excellent user interface and the ability to process and archive measured data have resulted in the prolific use of electrical / electronic instrumentation systems for the measurement of not only electrical but also non-electrical quantities. The task of converting non-electrical quantities into a form that can be measured by electrical means is normally entrusted to a transducer. The transducer is variously described as a device that “changes power from one system into another form for another system” [1] or even more specifically, “converts variations in a physical quantity into an electrical signal or vice versa” [2].

Linear and angular displacement, force, torque, fluid flow, temperature and strain are some of the parameters that are converted into a proportional electrical quantity (voltage or current) using a transducer. In some transducers the change in the physical quantity being measured is directly obtained as a voltage or current. A typical example is the thermocouple, which produces an output voltage / current proportional to its junction temperature. Such devices, called *active* transducers, do not require an external source of energy and are usually very compact and reliable. The disadvantage of such transducers is that they derive the energy for their operation from the system on which the measurement is being made. The output is usually low and requires amplification.

In a majority of the transducers, which can be labelled as *passive*, the change in the physical quantity (measurand) being measured alters some passive parameter like the capacitance, inductance or resistance of a sensing element. To obtain a measurable output from the variations of the passive parameter, a signal conditioning circuit powered by an external power source is required. Even for active transducers a signal

conditioning circuit becomes necessary to either amplify or filter the output from the sensor element. Thus a typical transducer is made of *sensor* elements whose output parameter changes as a function of the measurand and a signal conditioning circuit that provides a conveniently measurable voltage or current output. A large portion of the energy required for transduction is supplied by an auxiliary power supply with the sensor demanding an insignificant part of the energy budget from the measurand. Passive transducers enjoy an advantage over active ones in that, we can get an increased output by choosing a higher level of excitation. Typical examples of passive transducers are strain gages, platinum resistance thermometers, variable reluctance type sensors, capacitive and semi-conductor sensors.

1.2 Resistive transducers

One of the most common forms of passive transduction is the resistive transducer, in which the change in the measurand alters the resistance of a resistive sensing element. Resistive transducers are commonly employed to measure physical quantities like linear and angular displacements, force, temperature, pressure and strain [3]. The resistance R_x, of a resistive sensor element is given by the expression

$$R_x = \rho l / A, \tag{1.1}$$

where ρ represents the resistivity of the material of the resistor, l is the effective length of the resistance and A is the area of cross-section of the sensing element. As can be seen from equation (1.1), resistive sensors can be used to measure any quantity which changes the resistivity or effective length or area of cross-section of the element.

The resistance R_x, of a typical single element resistive sensor like the strain gage can be expressed as

$$R_x = R_o(1 \pm G\varepsilon), \tag{1.2}$$

where G is the gage factor and R_o is the nominal value of the resistance of the strain

gage when the input strain ε (μm/m) is zero. In general, the resistance of a single element resistive type sensor can be written as

$$R_x = R_o(1 \pm kx), \tag{1.3}$$

where k is the transformation efficiency of the sensor and R_o is the nominal value of the resistance of the sensor when the input quantity being measured x is zero. It can be seen here that the fractional change in resistance $\left(\Delta R_x / R_o\right)$ has a linear relationship with the quantity being sensed. But occasionally $\Delta R_x / R_o$ can have an inverse relationship with the quantity being sensed [4] as

$$R_x = \frac{R_o}{\left(1 \pm kx\right)}. \tag{1.4}$$

Typical examples are the force sensing devices manufactured by M/s Tekscan [5] and the Force Sensing Resistors (FSR) from M/s Interlink Electronics [6]. The inverse characteristic of these sensors is primarily because the force applied on the resistive sensor element changes the dimensions of the area of the sensor resistor, which as

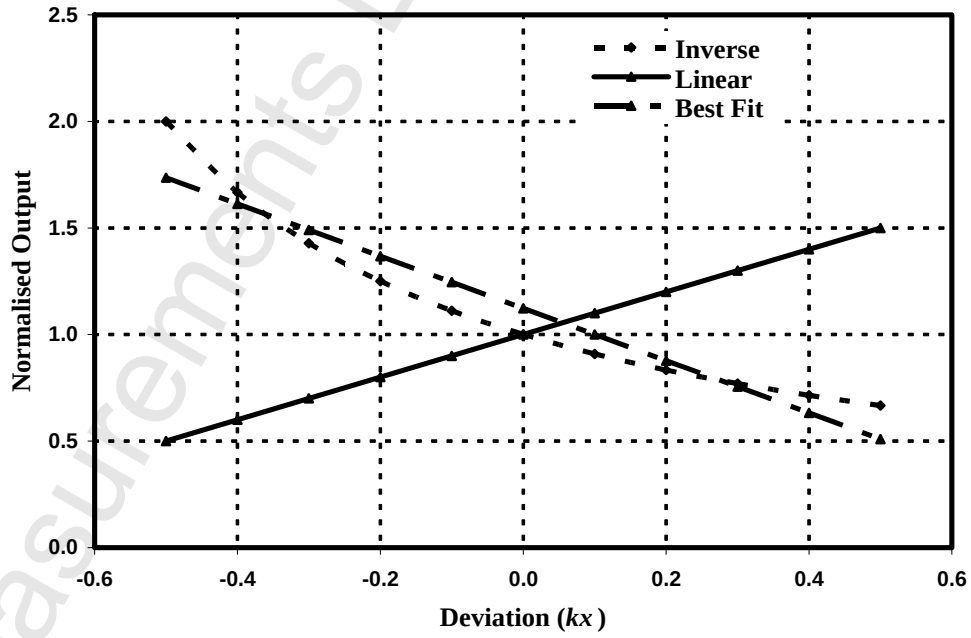


Fig. 1.1 Normalised output characteristics for a typical differential transducer – with linear or inverse relationship

shown by equation (1.1), alters the effective resistance in an inverse manner. The typical, normalised output characteristics of both these sensors are shown in Fig. 1.1. As can be seen, the output of the sensor having an inverse relationship with the measurand is nonlinear, with both offset and gain variation, posing particular challenges when designing a suitable signal conditioning interface.

Even for resistive sensors where the resistance is expected to be proportional to *kx*, the output may be linear over only a portion of the operable range, called the dynamic range of the sensor. This could be due to a number of reasons like the non-uniformity of the material of the resistance or due to localised temperature variations. The linearity of a device is specified as the maximum deviation of the output function from an ideal straight line. A typical characteristic of a displacement-measuring transducer possessing nonlinearity is shown in Fig. 1.2 [7]. In the figure, v_o represents the output of the transducer when the displacement is x, with V_R being the maximum output corresponding to a displacement of x_p.

The linearity of sensors is generally in the range of 0.1 % to 1 % of full scale and could be much better in precision devices. While the nonlinearity arising out of the inverse characteristics can be compensated, the inherent minor nonlinearity of a sensor is quite difficult to correct. A resistive sensor could also have other types of output characteristics other than the linear and inverse ones discussed above. For example, the

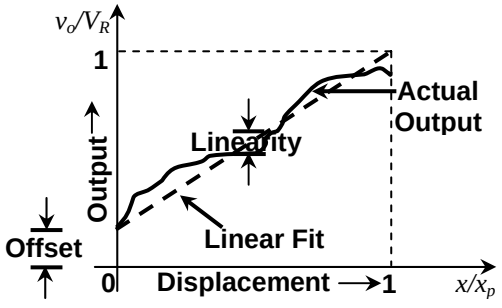


Fig. 1.2 Performance of an actual potentiometer

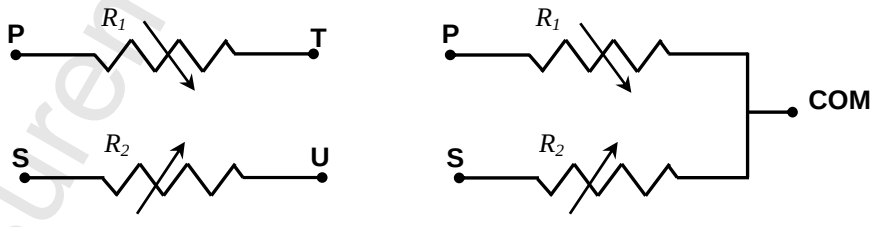
"thermistor", a resistive type temperature sensor exhibits *inverse exponential* relationship between its resistance and the temperature it is trying to measure.

For increased sensitivity and to decrease the nonlinearity to some extent, resistive sensors are also employed in a differential configuration. In the differential mode, two sensing elements are utilised to sense the given physical quantity in such a fashion that when the resistance of one of the element increases corresponding to a change in the measurand, the value of the other element decreases by an equal amount [3]. The differential resistive sensors are available in either three-terminal (with one each of the terminals of the two resistors combined to obtain a common terminal) or four-terminal (with all the four terminals of the two resistors brought out) configurations, as illustrated in Fig. 1.3. If the differential resistive sensor has a linear characteristic (sensing parameter is either the resistivity ρ or the length l) then the resistances R_1 and R_2 can be represented as

$$R_1 = R_o\left(1 \mp kx\right) \text{ and } R_2 = R_o\left(1 \pm kx\right). \tag{1.5}$$

The resistances of a differential resistive sensor possessing an inverse characteristic (sensing parameter is area A) are given by

$$R_1 = \frac{R_o}{\left(1 \pm kx\right)} \text{ and } R_2 = \frac{R_o}{\left(1 \mp kx\right)}. \tag{1.6}$$



(a) 4-terminal Configuration **(b) 3-terminal Configuration**

Fig. 1.3 Differential resistive sensor configurations

1.3 Signal conditioning circuits

As discussed earlier, signal conditioning electronics is essential to obtain a voltage or current output from a passive sensor, or to enhance the output from an active sensor. It may often be necessary that a signal conditioning circuit is called upon to perform, apart from providing a measurable voltage or current output, tasks such as isolation, amplification, filtering, linearization, impedance matching, level translation, gain correction and offset compensation [8]. In short, signal conditioning systems have to suitably modify and shape the output of the sensor, so that the final output from the transducer is compatible with the rest of the system.

A modern measurement / instrumentation / control system would typically consist of a sensor, a signal conditioning circuit (for sensing), an analog to digital converter (for interfacing the output of the signal conditioning units to the digital system) and a digital system for data acquisition (measurement), processing, control and display. A schematic representation of such a system is shown in Fig. 1.4.

The less the number of building blocks in a system, the more robust and less complex it would be. Moreover, with fewer number of intermediate stages, the output of

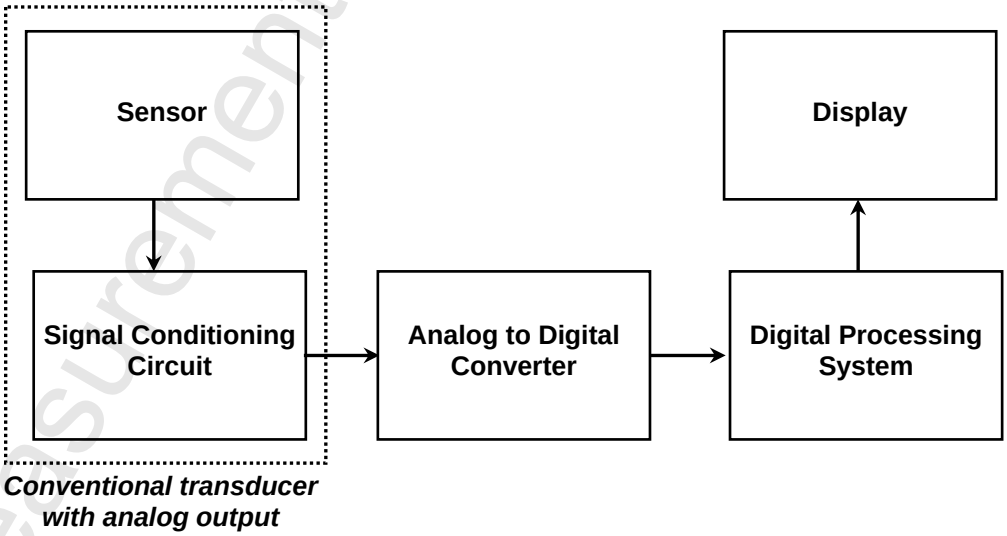


Fig. 1.4 Schematic representation of a typical measurement system

the system would be less prone to errors and therefore, more reliable. One way of reducing the number of building blocks required would be to design a transducer where the signal conditioning circuit produces a digital output which can be directly interfaced to the digital processing system without the need for an intermediate analog to digital converter, as illustrated in Fig. 1.5. Thus, while designing an appropriate signal conditioning circuit, one must keep in mind that not only must the output of the circuit be compatible with modern, digital instrumentation systems; the circuit should also process the signal from the sensor elements in such a fashion as to produce the optimum results. Besides, it has to be ensured that no additional errors are introduced by the signal conditioning circuit or if unavoidable, are kept to a minimum and the necessary circuits incorporated to compensate for or nullify such errors

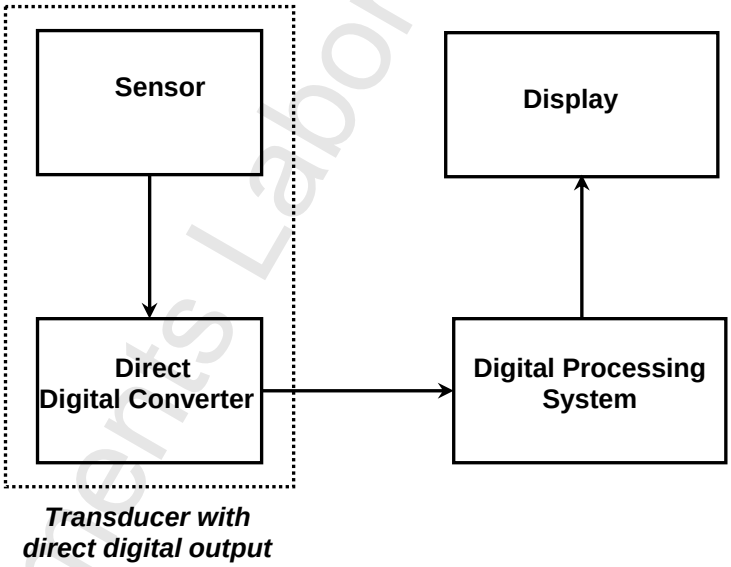


Fig. 1.5 Schematic of a measurement system using a transducer with a direct digital converter

1.4 Motivation for the present work

Quite often, the choice of a signal conditioning circuit is decided not by its technical quality, but more due to reasons of its economic viability and its backward

compatibility with circuits and systems already in place. Multiple sensors and connected systems, in a typical process control plant which have been in place for a long time, would need to be upgraded or changed to make them compatible with modern instrumentation systems. It would be very difficult, if not impossible, to economically justify the costs of such an exercise, including fully or partially shutting down the plant. More so, when one considers the fact that the sensors and systems are still fully functional. A classic example of such a system would be the conventional Wheatstone bridge, which was the work horse of the early measurement industry. Though problems like decreased sensitivity and increased nonlinearity (when used with a single element sensor) are associated with the bridge, they are still not enough to justify the cost of replacing entire systems with the technology of today, like the Anderson current loop or the current-mode Wheatstone bridge . There is no alternative but to design a signal conditioning circuit that would interface the Wheatstone bridge with modern digital systems, with a high degree of linearity over a wide dynamic range.

As has been pointed out in section 1.3, it would be highly advantageous to have the signal conditioning circuit as compact as possible. It would be even better if an analog to digital converter could be modified such that the analog part of the converter takes on the additional task of signal conditioning the output from the sensor elements. Such an arrangement will not require the use of a separate analog signal conditioning circuit and the digital converter itself could be designed to provide a direct digital output proportional to the physical quantity being measured. Attempts have been made to modify one of the most popular and effective methods of analog to digital conversion, particularly of slowly-varying signals, namely, the dual slope integrating type analog to digital converter (ADC) to accommodate the sensor elements of a capacitive [9] and a resistive sensor [10].

1.5 Objective and Scope of the work

The work reported in this thesis is concerned with the signal conditioning aspects of resistive sensors. Initially, the classical problem of nonlinearity in the output of a Wheatstone bridge when applied to a single resistive sensor is addressed. A major portion of the work reported is focused on developing new digital converter topologies that provide a direct digital output proportional to the parameter being sensed by resistive sensors, both of the single element and differential types. The challenging problem of obtaining a digital output linear with the temperature being sensed by a thermistor that possesses an inherently inverse exponential characteristic is also taken up and a novel solution is arrived at.

1.6 Organisation of the thesis

Chapter 1 introduces different kinds of resistive transducers and the need for signal conditioning as well as digitisation. It discusses the motivation as well as the objective and scope of the work reported herein.

Chapter 2 takes up the problem of the nonlinear output characteristic associated with a conventional Wheatstone bridge signal conditioning circuit used with a single element resistive sensor. In this chapter, a novel solution is proposed, based on a feedback compensation scheme, for linearising the output of a Wheatstone bridge operated with a single element resistive sensor.

In Chapter 3, the problem of directly digitising, the output of a single element type resistive sensor like the Pt1000 RTD, without additional analog signal conditioning circuitry is taken up. An appropriate dual-slope digital converter topology that provides an elegant solution to this problem is provided in this chapter.

Chapter 4 deals with the task of developing a digital converter which would linearise as well as digitise the output of a thermistor. It also details the work that has

been done so far in the area of linearising the resistance-temperature characteristic of a thermistor.

Chapters 5 and 6 elaborate on direct resistance to digital converters suitable for differential resistive sensors. In Chapter 5, the technique developed in chapter 3 for a single element resistive sensor is appropriately modified so that it can be used with a differential resistive sensor.

Chapter 6 presents a Sigma-Delta Resistance to Digital Converter which provides a digital output proportional to the measurand being sensed by a differential resistive sensor. This method provides higher conversion rate when compared to the methods presented in chapters 3 to 5.

The practical feasibility of all the techniques developed (chapters 2 to 6) are established through simulation studies and demonstrated with experimental results obtained from prototype units. The thesis concludes with a brief summary of the work done as well as the inferences drawn from the results obtained. The final chapter also lists the possible directions in which the reported research work can be extended.

1.7 Soft copy of the thesis

A fully indexed and hyperlinked version of this thesis is available at http://tinyurl.com/ycx5ab9. The resource locator will have to be typed exactly as given as no links have been provided to the thesis from anywhere else. Adobe Acrobat Reader (v6.0 and above) would be required to view the file. All the figures, tables and chapters have been bookmarked and linked so that they can be easily accessed – clicking on any of the links will lead one to the referred figure, table or section. The ALT + Left arrow keys will lead back to the source.

2. Linearising a Wheatstone bridge based Signal Conditioning Circuit

2.1 Wheatstone bridge for the measurement of resistance

Bridge circuits are quite popular for the measurement of the component values of resistors, inductors and capacitors. The Wheatstone bridge is the simplest of all bridge circuits and is widely used for the measurement of resistances. A typical Wheatstone bridge is shown in Fig. 2.1 for the measurement of an unknown resistance R_x, which is introduced as one of the arms of the bridge. The value of R_{B2} is adjusted such that the bridge is balanced with the galvanometer showing null deflection for $R_G = 0$. Under such conditions, it is easily seen that

$$R_x = \frac{R_{B3}}{R_{B1}} R_{B2}. \tag{2.1}$$

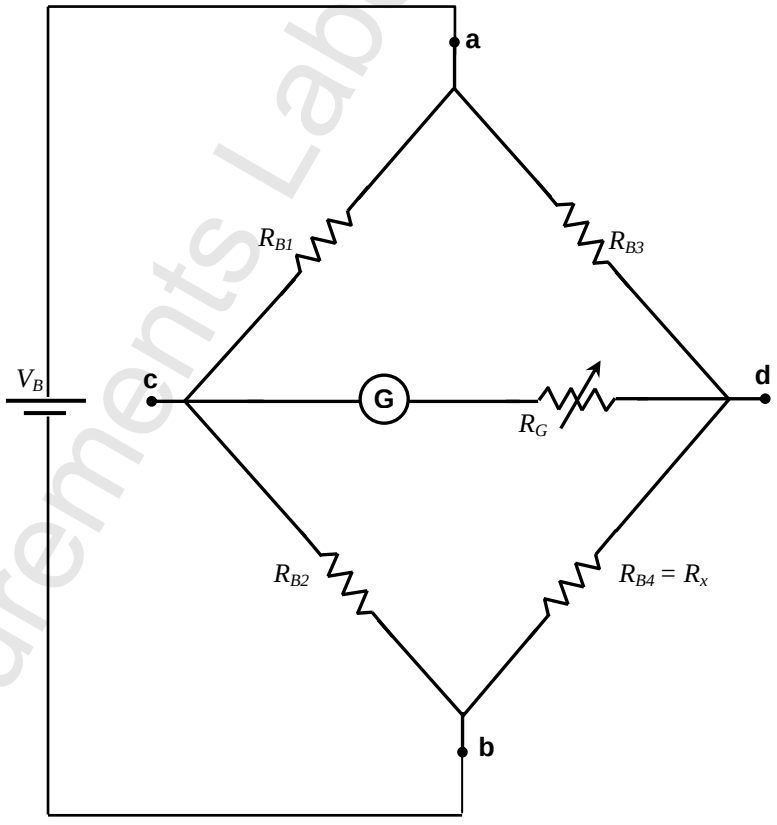


Fig. 2.1 Traditional Wheatstone bridge circuit

R_x is thus computed from the known values of R_{B1}, R_{B2} and R_{B3}. When a Wheatstone bridge is employed for signal conditioning of resistive sensors, balancing cannot be an option as it is tedious and time-consuming. For signal conditioning, the sensor becomes an integral part of a Wheatstone bridge, the output of which is taken as the signal conditioned output representing the physical quantity being sensed. It is well known that the Wheatstone bridge method of signal conditioning provides a linear output for differential resistive sensors, but introduces nonlinearity in its output if used with a single element resistive sensor [3], as is brought out in the next section.

2.2 Wheatstone bridge for a single element resistive sensor

For signal conditioning a single resistive sensor, the sensor is introduced as one of the elements in a Wheatstone bridge, say R_{B4}, as indicated in Fig. 2.2. Here, $R_{B4} = R_o\,(1 \pm kx)$, where k is the sensitivity factor of the sensor and R_o is the nominal value of the sensor resistance when the physical quantity being sensed, namely x, is

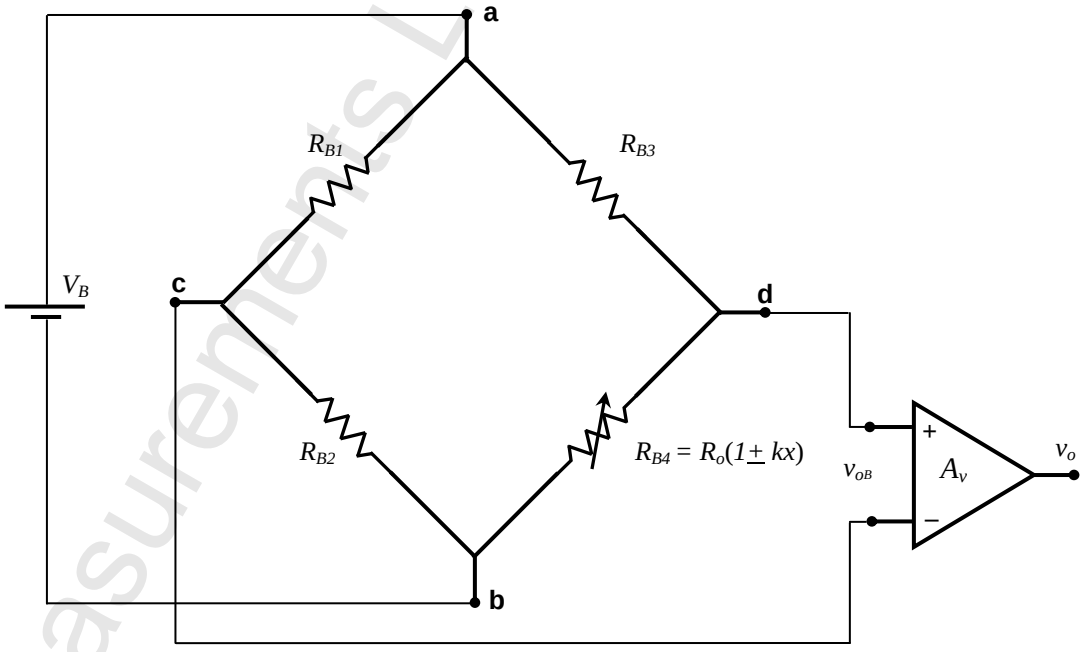


Fig. 2.2 Wheatstone bridge circuit for signal conditioning a single element resistive sensor

zero. For example, if the sensor is a strain gage, then $R_{B4} = R_o(1 \pm G\varepsilon)$, where R_o is the nominal value of the resistance of the strain gage, G is the gage factor and ε is the strain sensed by the gage. The other three elements R_{B1}, R_{B2}, and R_{B3} are chosen so that the bridge output is zero when the physical quantity being sensed is zero. The output of the bridge is then amplified suitably as shown in Fig. 2.2 and the output of the amplifier taken to represent the change in the sensor resistance and thereby, the physical quantity being sensed. In the figure, the excitation used is shown as dc but in some situations, the excitation can be chosen to be a single frequency sinusoid. In such a case, the bridge output needs to be amplified and demodulated to obtain the final output [11]. Such an ac excitation scheme is popularly known as "*carrier frequency amplifier*" scheme.

On analysis, the Wheatstone bridge circuit of Fig. 2.2 yields

$$v_{oB} = V_B \frac{\frac{R_{B4}}{R_{B3}} - \frac{R_{B2}}{R_{B1}}}{\left(1+\frac{R_{B2}}{R_{B1}}\right)\left(1+\frac{R_{B4}}{R_{B3}}\right)}. \tag{2.2}$$

If we choose $R_{B2} = R_o$ and $R_{B1} = R_{B3} = \gamma R_o$, where $\gamma > 0$, the output of the bridge can be expressed in terms of the bridge excitation voltage V_B as

$$v_{oB} = V_B \left[\frac{\gamma}{(1+\gamma)^2}\right] \frac{kx}{\left(1+\frac{kx}{1+\gamma}\right)}. \tag{2.3}$$

It is easily seen from expression (2.3), that the output of the bridge is a nonlinear function of the physical quantity x that is being measured [12]. Since kx is usually small (for example, in most metallic strain gages k is the gage factor, $G \approx 2.5$ and x is the strain ε, normally in the range of micro strains, μm/m), the output of the bridge will be low and hence needs to be amplified with the help of an instrumentation amplifier for any meaningful measurement to be made.

The output of the bridge shown in Fig. 2.2, as expressed by equation (2.3), is

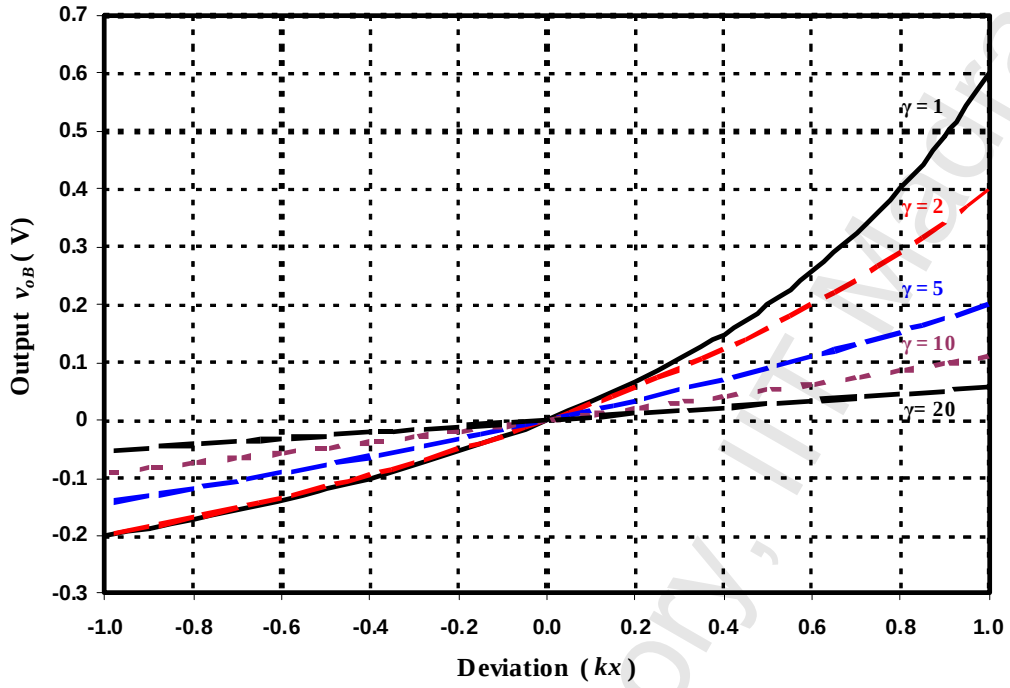


Fig. 2.3 Output of the Wheatstone bridge for different values of γ, without compensation

given in Fig. 2.3 as a function of *kx*, for various values of γ. It can be observed from Fig. 2.3 that the output of the bridge remains linear only for small changes in *kx*. When the deviation from the nominal value is large, the nonlinearity increases considerably. Large values of γ improve linearity but at the cost of the sensitivity of the bridge, resulting in low bridge output and hence low resolution and poor signal to noise ratio (SNR). The nonlinearity can be reduced to a large extent by a judicious choice of γ depending on the maximum value of *kx*.

However, for resistive sensors like the Pt100, the platinum resistance temperature detector (RTD), the value of *kx* can be as large as 3 [13] and hence even with a γ of 10, the nonlinearity will be much more than depicted in Fig. 2.3, where the maximum value of *kx* is shown to be 1. Thus the Wheatstone bridge, though simple, cannot provide a perfectly linear output for a single element sensor, especially if the sensor possesses a large variation in *kx*. The classic wide-deviation bridge amplifier [14] can provide a

linear output whenever the deviation in the measurand is so large that linear approximations are no longer valid. Not only does it require the modification of an existing Wheatstone bridge but its calibration is also difficult as it requires the trimming of two resistors if its' sensitivity is to be maintained. Moreover, its gain is also low necessitating the use of another amplifier. Further, its output is sensitive to the input offset voltages of the operational amplifiers used as well as to their thermal drift. A high gain, drift insensitive, wide deviation bridge amplifier has been patented [15] while a similar one has been specifically devised for platinum resistance temperature devices [16].

Attempts have also been made to linearise the bridge specifically for an RTD sensor, using positive feedback compensation [17],[18], but they involve specific application designed chips and are expensive. Moreover, they are limited to a narrow dynamic range of the RTD. Even ICs which have been specifically designed for Strain Gage / RTD type of sensors require external components as well as iterative procedures for linearising the transducer output in addition to manual operation to determine the sense of the feedback [19]. A unique idea which has come up recently, for compensating and improving the performance of a Wheatstone bridge is the use of continuous valued, adjustable resistors or *rejustors* as they are called [20].

Some of the drawbacks of the traditional bridge, also called the voltage mode Wheatstone bridge (VMWB), were sought to be overcome by making use of a current source for bridge excitation. One of the earliest attempts in this direction makes use of a square wave generator which is converted into a bilateral current source for the Wheatstone bridge so as to overcome some of the disadvantages associated with a dc excitation, like thermoelectric emf [21]. The problems of lead-wire resistance as well as the number of leads required for multiple sensing elements in the bridge led to the

invention of the Anderson loop [22]-[24], which makes use of a constant current source to excite the traditional Wheatstone bridge. The Anderson loop suffers from the disadvantage that it requires a dual-differential *subtractor* circuit to achieve the same result that the Wheatstone bridge delivers by means of a suitable and elegant layout of passive components. A new circuit topology has also been developed based on the duality of the voltage-mode Wheatstone bridge [25], which can implement ratiometric current measurement. A precise, dc floating-current source has been designed [26] for use as a constant current drive for resistive sensors with a generalised impedance converter [27]. A current-mode Wheatstone bridge (CMWB) using an operational floating current conveyor (OFCC) has also been proposed [28]. A CMOS-based circuit suitable for low voltage IC implementation has also been designed around a current source, using current mirrors and just two resistive sensors [29]. Recently, a simple circuit incorporating current mirrors, accomplishing essentially the same task as a traditional voltage-mode Wheatstone bridge, has also been suggested [30].

One of the major drawbacks of all the alternatives suggested above has been that they involve a total change of an existing setup, from a voltage-mode Wheatstone bridge to a current-mode one. None of them are capable of working with voltage-mode Wheatstone bridge based systems which are already in place, except the one suggested by Anderson [22]. Even this method involves the total replacement of Wheatstone bridge based systems with current-loop based ones but in a manner which is transparent to the end-user. This shortcoming has been sought to be overcome by Sheingold [8] (pages 99 – 101), by making use of a novel, feedback scheme that operates on the output of an existing Wheatstone bridge with minimal alterations. The disadvantage with this scheme is that it is applicable only for bridges with $\gamma = 1$. This drawback is rectified by means of the circuit presented in the following section. The proposed

method not only provides a final output that is linear with the measurand x and reduces the nonlinearity that would otherwise be present in the bridge output but also accepts bridges with different values of γ.

2.3 Proposed feedback compensation scheme

The proposed scheme [31] is illustrated in Fig. 2.4. The output of the Wheatstone bridge v_{oB} is amplified by an instrumentation amplifier of gain A_v to obtain the final output v_o as in a conventional circuit (shown in Fig. 2.2). A part of the output, say βv_o ($\beta < 1$) is added to a reference voltage V_R, with the help of a unity gain adder. The output of the adder provides the bridge excitation, V_B. Using expression (2.3), we get

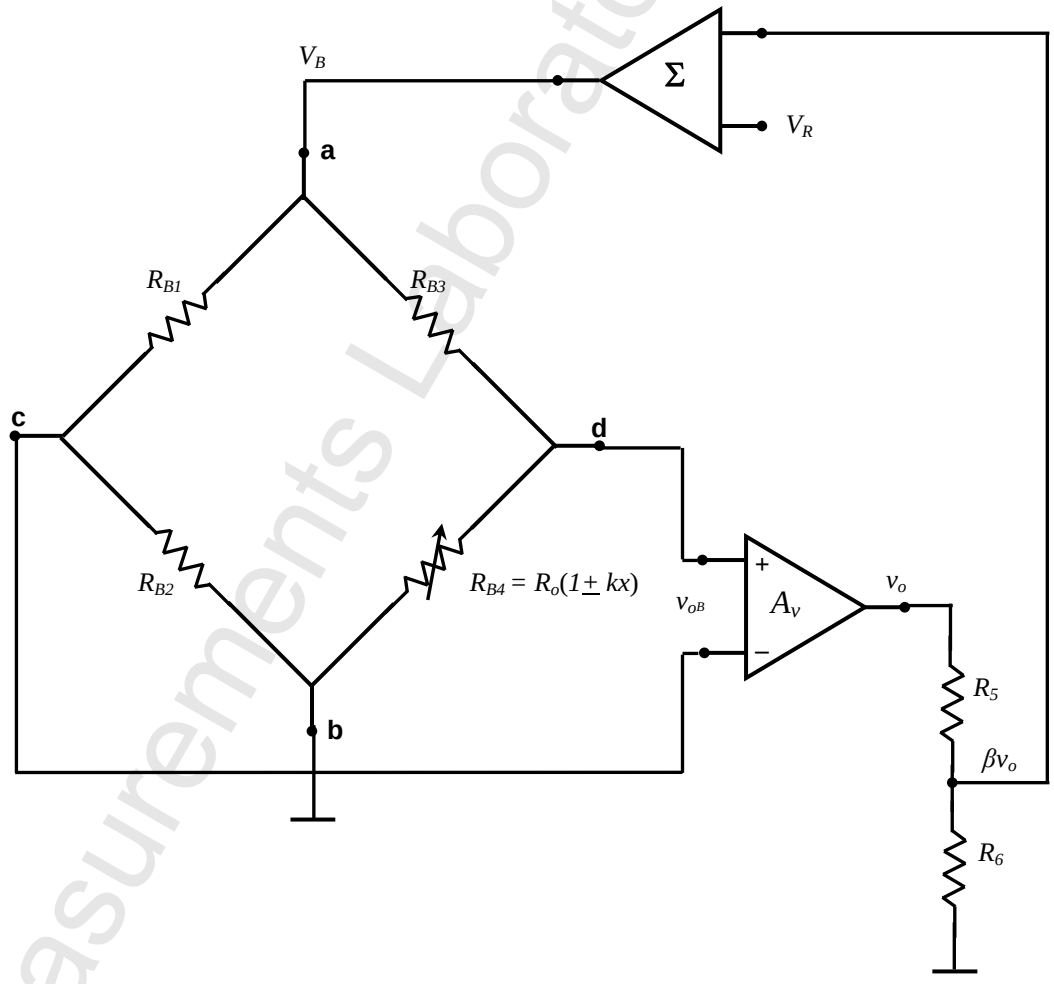


Fig. 2.4 Feedback compensated Wheatstone bridge circuit

$$v_o = A_v v_{oB} = AV_B \left[\frac{\gamma}{(1+\gamma)^2} \right] \frac{kx}{\left(1 + \frac{kx}{1+\gamma} \right)} \tag{2.4}$$

and
$$V_B = V_R + \beta v_o, \tag{2.5}$$

resulting in

$$v_o = A_v v_{oB} = \left(V_R + \beta v_o \right) A_v \left[\frac{\gamma}{(1+\gamma)^2} \right] \frac{kx}{\left(1 + \frac{kx}{1+\gamma} \right)} \tag{2.6}$$

Rearranging equation (2.6), we get:

$$v_o - \beta v_o \left[\frac{\gamma}{(1+\gamma)^2} \right] \frac{A_v}{\left(1 + \frac{kx}{1+\gamma} \right)} kx = V_R \left[\frac{\gamma}{(1+\gamma)^2} \right] \frac{A_v}{\left(1 + \frac{kx}{1+\gamma} \right)} kx \tag{2.7}$$

The above expression simplifies to

$$v_o = V_R \left[\frac{\gamma}{(1+\gamma)^2} \right] \frac{A_v}{\left(1 + \frac{kx}{(1+\gamma)^2} (1 + \gamma - A_v \beta \gamma) \right)} kx \tag{2.8}$$

If the feedback factor β is chosen such that

$$A_v \beta = \frac{1+\gamma}{\gamma} \tag{2.9}$$

then, it follows from equation (2.8) that

$$v_o = A_v V_R \left[\frac{\gamma}{(1+\gamma)^2} \right] kx \tag{2.10}$$

Equation (2.10) demonstrates that the feedback scheme of Fig. 2.4 would deliver an amplified output, linear with the parameter x that is being sensed by the resistive sensor, provided the feedback is adjusted such that equation (2.9) is satisfied. To determine the efficacy of the proposed method, simulation and experimental studies were carried out as detailed in the following sections. The sensitivity of the output to variations in the degree of adjustment of the feedback was also analysed.

2.4 Simulation studies

The entire circuit outlined in Fig. 2.4 was simulated using the circuit layout and

simulation software, PSpice, forming part of the OrCAD (v16.2) software suite. Resistor R_{B4} of the Wheatstone bridge was replaced with a resistor having a nominal value R_o of 100 Ω and kx varying from -1 to +1. The INA101 was chosen for use as the instrumentation amplifier not only because its PSpice model was easily available but also because of its low offset voltage, low noise and low nonlinearity as well as its high input impedance, making it ideal for use with devices like strain gages and RTDs [32]. The commonly used OP07 [33] was employed for realizing the summer. The reference voltage of 1.2 V was obtained with the help of a precision voltage reference diode LM385-1.2 [34].

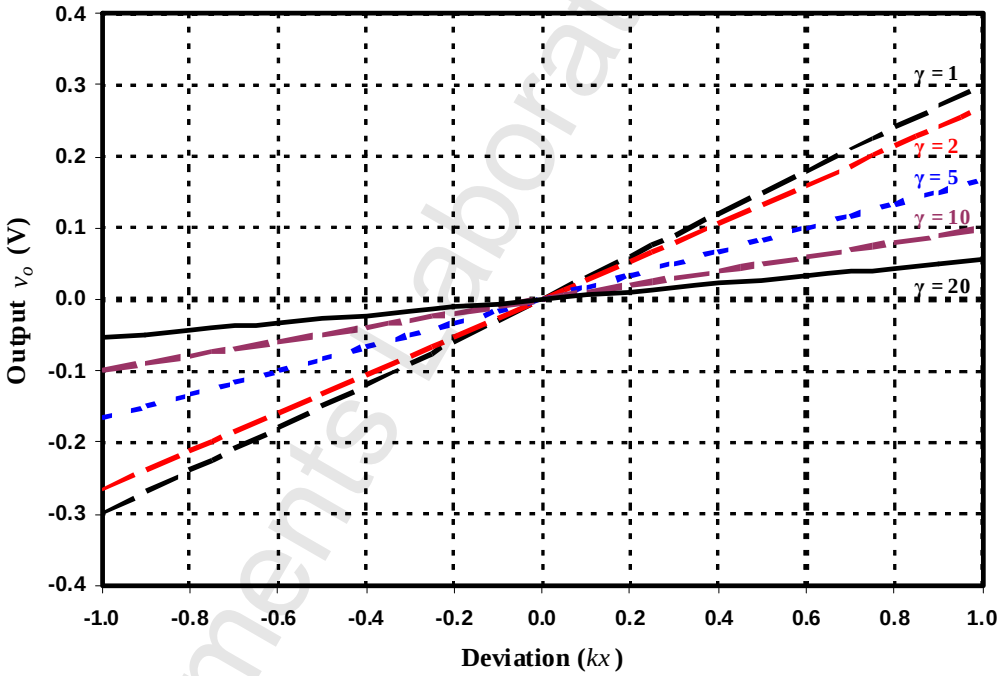


Fig. 2.5 Output of the feedback compensated Wheatstone bridge, for different values of γ (Simulation study)

The results of the simulation are portrayed in Fig. 2.5. A comparison of Fig. 2.3 and Fig. 2.5 clearly shows that the proposed feedback compensation scheme provides a linear output and considerably reduces the nonlinearity that would otherwise be present in the output. Table 2.1 presents the improvement in performance of the bridge brought

about by the proposed scheme.

Table 2.1 Comparison of simulation results for the Wheatstone bridge, with and without feedback

γ	Maximum Nonlinearity (%FS)	
	Without Feedback	With Feedback
1	23.79	0.000
2	13.33	0.009
5	5.84	0.011
10	3.03	0.036
20	1.55	0.028

2.5 Sources of errors

The output of the feedback compensated Wheatstone bridge depends on the following factors : (i) the stability of the feedback amplifier gain (A_v), (ii) the stability of the reference voltage V_R, (iii) the tolerance of the resistors forming the bridge, (iv) the self-heating of the bridge and (v) the extent to which the compensation as suggested by equation (2.9) is achieved.

2.5.1 Stability of the amplifier gain (A_v) and reference voltage (V_R)

As is made clear by equation (2.10), the output of the circuit is directly proportional to the gain of the instrumentation amplifier (A_v) as well as the reference voltage V_R. Any changes to these parameters are likely to directly affect the output of the circuit. Hence, it is necessary to ensure the stability of the amplifier gain as well as of the magnitude of the reference voltage. The components chosen have to possess high stability and very low drift due to temperature. The LM385-1.2 selected for providing the reference voltage as well as the INA101 instrumentation amplifier have very low temperature coefficients, of the order of parts per million, ensuring excellent stability to the circuit.

2.5.2 Tolerance of the resistors

Another factor which influences the output of the circuit is γ, the ratio of R_{B1} to

R_{B2}. A larger value of γ drastically reduces the nonlinearity in the circuit caused by any non-idealities but at the same time, significantly brings down the dynamic range of the bridge output. This can be easily rectified by introducing another amplifier, to sufficiently boost the signal. The drawback of working with high values of γ is that the circuit will now have to contend with different values of resistances, with the resultant chances of mismatch. But this is a small price to pay for the benefits derived from such an arrangement, especially if resistors of better tolerances are used.

2.5.3 Self-heating of the bridge

Since a certain amount of current always flows through the resistors of the bridge, they tend to heat up due to the Joule effect. As the increase in temperature leads to a change in resistance of the resistors, the output of the bridge will be in error unless steps are taken to minimise or nullify these errors. This is one of the reasons that the Wheatstone bridge is normally used with a dummy sensor, similar to the one that is actually used, in order to provide temperature compensation. When very high temperature sensitivities or very low amounts of infra-red radiation are to be measured, complex compensation techniques will have to be used [35]. Fortunately, the use of a single element sensor like the Pt100 RTD does not require such methods. The use of the reference voltage (V_R) ensures that the bridge excitation current stays well within the limits prescribed for the RTD [36]. A higher value of γ also reduces the excitation current and further minimises the effect of self-heating of the sensor and the bridge.

2.5.4 Extent of bridge compensation

As is evident from equation (2.8), the degree to which expression (2.9) is satisfied, is crucial to the success of the compensation scheme to reduce the nonlinearity of the bridge output. The performance of the circuit of Fig. 2.4 was analysed for different degrees of variation of the compensation from that stipulated by equation (2.9).

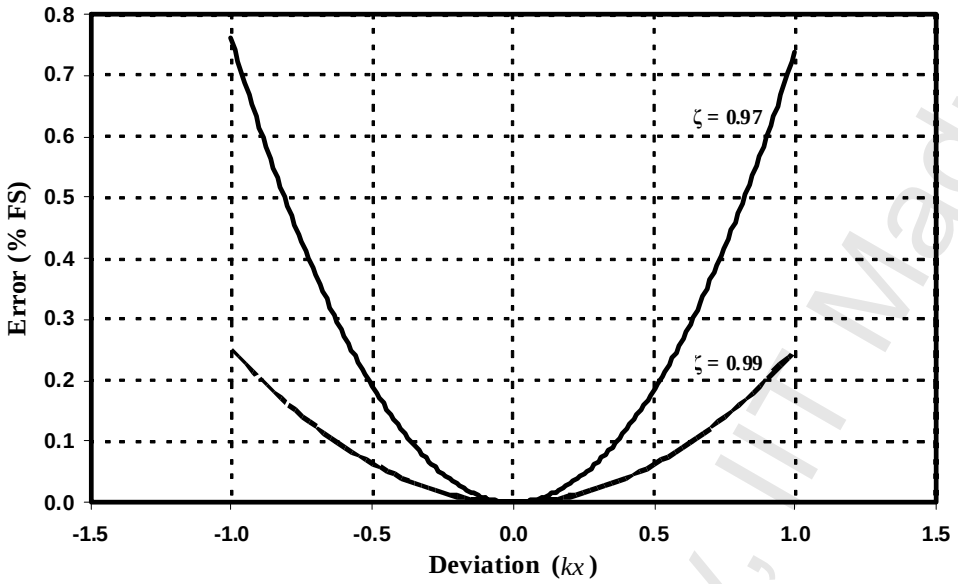


Fig. 2.6 Output of the bridge, when the feedback is not fully compensated

The results of the analysis are shown in Fig. 2.6, where

$$A_v\beta = \zeta\frac{1+\gamma}{\gamma} \tag{2.11}$$

with ζ (ζ < 1) representing the variation from ideal (ζ = 1). As the curves indicate, the nonlinearities assume serious proportions when ζ decreases. To maintain the nonlinearity within reasonable limit, it has to be ensured that the attenuation of the feedback network (β) and the amplifier gain (A_v) remain stable. Use of precision resistors to determine β as well as A_v, ensures that ζ is kept to values better than 0.99.

2.6 Experimental verification

The circuit of Fig. 2.4 was set up using off-the-shelf components and bread-boarded. The INA101 from Burr-Brown (now Texas Instruments) was used for the instrumentation amplifier while the OP07 was the opamp of choice for the adder as well as the voltage followers, mainly due to its low input offset voltage (~25 μV), easy availability and affordability. The LM385-1.2 reference voltage diode from National Semiconductor Corp. was employed for generating the reference voltage. The sensor

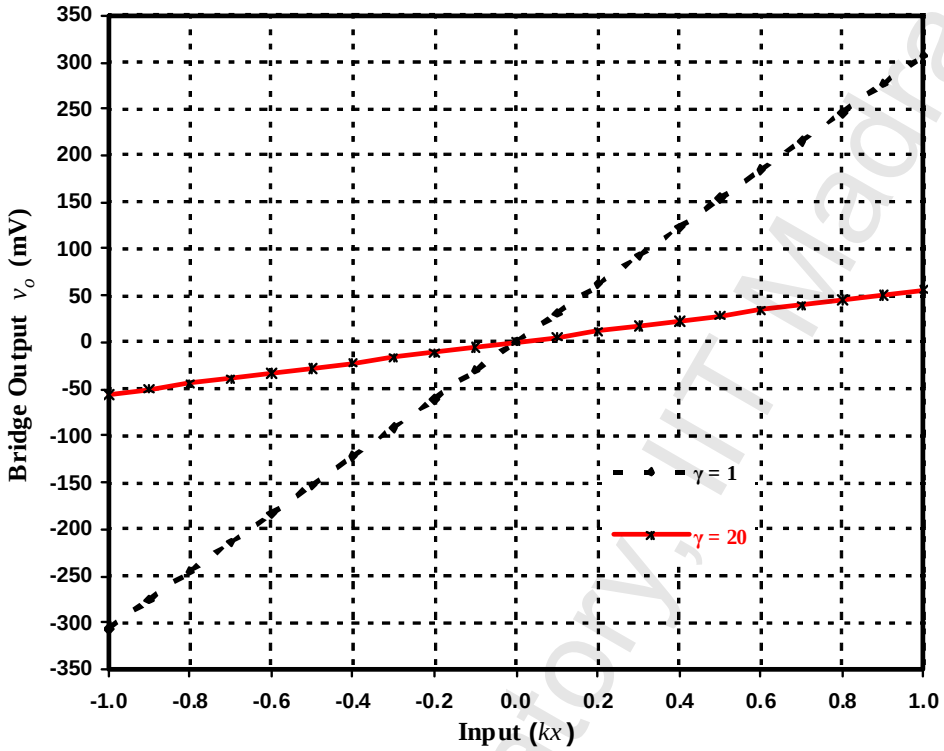


Fig. 2.7 Performance of the Wheatstone bridge with feedback compensation

resistance values were set up using a precision resistance box ranging from 0.1-1221 Ω (Model V441 from Otto Wolff Berlin, Germany), having an accuracy of ± 0.001 %. The bridge was set up for various values of γ from 1 to 20. The precision resistance was varied from 0 to 200 Ω, in steps of 10 Ω, corresponding to a change in kx of 10 %. The output across the bridge was measured using a 6½-digit multimeter (HP34401A). The ambient temperature was maintained at 25 ^{o}C, to nullify any change in the resistances due to temperature variations.

The results obtained are plotted in Fig. 2.7 for the two extreme values of γ. The nonlinearity was calculated in each case as a fraction of the full scale reading. As can be seen, the dynamic range of the bridge decreases dramatically with increase of γ, when feedback compensation is employed. But this disadvantage is more than made up for, when the nonlinearity present in the output after compensation is compared with the earlier situation when compensation was absent. Table 2.2 clearly shows that feedback

Table 2.2 Performance of the Wheatstone bridge – with and without feedback compensation

γ	Maximum Nonlinearity (%FS)	
	Without Feedback	With Feedback
1	23.77	0.05
2	13.11	0.07
5	5.73	0.09
10	3.01	0.02
20	1.58	0.05

compensation improves the performance of the conventional Wheatstone bridge by more than an order of magnitude.

2.7 Merits of the proposed scheme

The simplicity of the feedback network as well as the marked improvement in the performance of the Wheatstone bridge makes this scheme particularly attractive. Moreover, existing Wheatstone bridge based networks do not have to be extensively modified as the present circuit can be incorporated at the sensing end of the network. A separate floating bridge excitation source can be dispensed with as the dc excitation is provided by the compensation circuit itself. Results indicate that the compensation circuit significantly reduces the nonlinearity in the output of the bridge, using easily available, off-the-shelf, inexpensive components. It is to be emphasised that the reduction in nonlinearity is due to the nature of the compensation employed and that further improvement in performance can be achieved if components with better specifications and tolerances are used. The performance would be even better if the entire circuit consisting of the instrumentation amplifier, the feedback network, the voltage reference diode, voltage divider network, the summer amplifier and any buffers, along with the three fixed arms of the Wheatstone bridge can all be implemented together as a system-on-chip for specific resistive sensors.

Due to inherent advantages such as signal processing capability, high noise

immunity and better user interface, present day instrumentation systems are of the digital kind. An analog to digital converter (ADC) would be required to convert the analog output of a transducer so that it can be interfaced with a digital instrumentation system. It would be advantageous to have ADCs that accept the sensor elements directly and provide a digital output without the need for intervening analog signal conditioning circuitry. A novel solution in this direction, suitable for a single element resistive sensor is developed in the next chapter.

3. Dual Slope Resistance to Digital Converter for Single Element Resistive Sensor

3.1 Introduction

In the last chapter, a feedback compensation technique has been proposed for obtaining a linear output from a single element resistive sensor employed with a Wheatstone bridge circuit. But the feedback-compensated bridge circuit provides an analog output. Most of the instrumentation systems in use today are digital in nature, being very popular amongst end users as they provide excellent processing power and user-friendly interfaces when compared to their analog counterparts. To interface a sensor having an analog voltage or current output to a digital instrumentation system, a suitable analog to digital converter (ADC) is required. A digital converter that incorporates the element(s) of a sensor and provides a digital output directly proportional to the physical quantity (measurand) being sensed, is known as a *direct digital converter*. Such a converter would be more compact and robust as the number of components and hence the complexity decreases, resulting in reduced errors and increased reliability. Some of the earlier attempts in this direction resulted in digital converters suitable for capacitance type sensors, where the measurand was converted to a proportional change in frequency or pulse width [37], [38]. A direct resistance to digital converter (RDC) suitable for a differential type resistive sensor that requires four integration periods, T_A, T_B, T_C and T_D has been presented earlier [39]. In this method, T_A and T_C are set, while T_B and T_D are measured. The final output is computed as $\frac{(T_B - T_D)}{(T_B + T_D)}$. Since the output is obtained by subtracting one measured time period from another, large systematic errors may result, especially when the difference between the two measured periods is very small. This is normally the case when the measurand is

very nearly zero. Improved RDCs that avoid subtraction and obtain the final output with three [40] and two integrations [10] have also been proposed earlier. The topology coupled with the conversion logic of these converters is such that they are suitable only for differential resistive sensors. Moreover, the implementation of offset compensation with these circuits would require more integrations, reducing the conversion speed even further. A dual slope method suitable for a single element resistive sensor has been presented recently [41]. Though this method employs only one measured time period, it still requires the subtraction of that measured time period from a preset value.

A novel technique of resistance to digital conversion, incorporating the popular dual slope method of analog to digital conversion is presented in the next section. It converts the change in the resistance of a single element resistive sensor directly to a proportional digital output. The proposed method uses only two periods of integration, one set and the other measured. More importantly, it completely avoids the subtraction of one measured quantity from another to obtain the result.

3.2 Proposed Dual Slope Resistance to Digital Converter (DSRDC)

The schematic of the proposed DSRDC is shown in Fig. 3.1. As in a conventional dual slope ADC, the DSRDC consists of an integrator, a comparator and a timing and control unit (TCU) comprising an n-bit (for a binary output DSRDC) or N-digit (for a BCD output DSRDC) timer-counter and control logic. In the proposed DSRDC, the single resistance of the integrator in a conventional dual slope ADC is replaced with two resistances as shown in Fig. 3.1. The sensor resistance R_x becomes one of the resistances of the integrator which is realized with an opamp OA and a feedback capacitance C_F. Thus, the sensor becomes a part of the integrator in the DSRDC. The second resistor of the integrator is chosen to be of fixed value, having a resistance equal to the nominal value R_o of the resistance of the sensor R_x. One terminal each of R_x and

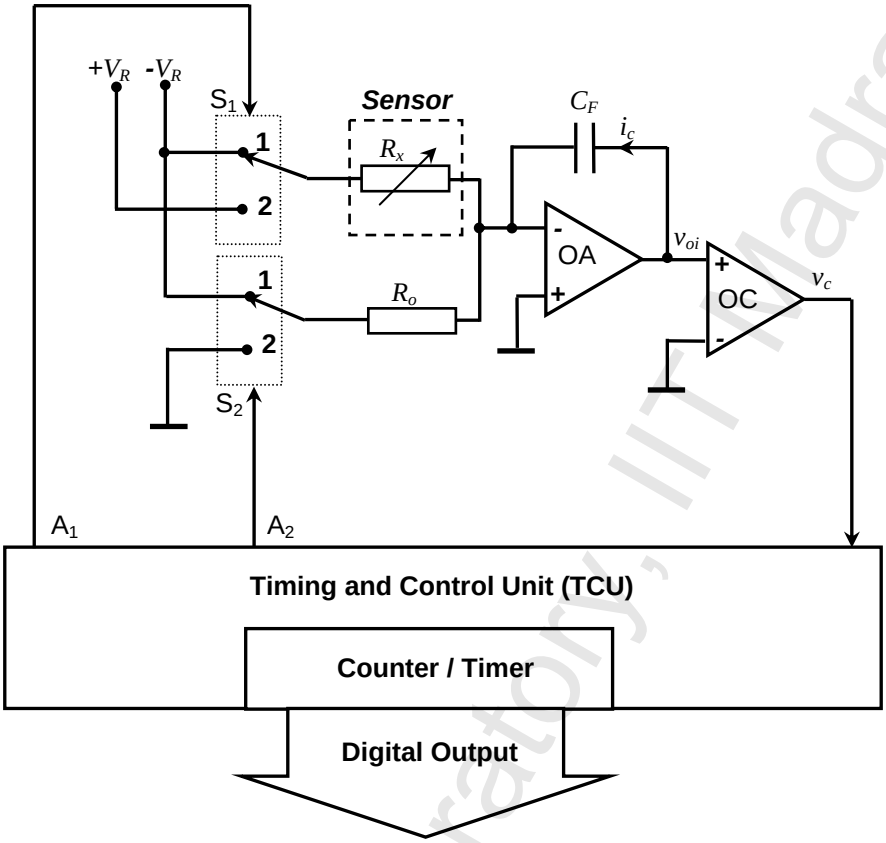


Fig. 3.1 Block schematic of the proposed DSRDC for single element resistive sensor

R_o are tied together to the inverting input of the opamp OA. The free end of R_x is connected to the output of a single-pole, double throw (SPDT) switch S_1. The free end of R_o is tied to the output of another SPDT switch S_2. Digital control lines A_1 and A_2 control switches S_1 and S_2, respectively. If A_1 is "1" (digital high), position 1 is selected on switch S_1 and $-V_R$ is applied to R_x, while position 2 is selected and $+V_R$ is applied to R_x if A_1 is "0" (digital low). Position 1 is selected on S_2 and $-V_R$ is applied to R_o if A_2 is "1" and R_o is grounded if A_2 is "0". The voltages $+V_R$ and $-V_R$ are stable dc reference voltages, equal in magnitude (V_R) but of opposite polarity.

The output of the integrator, v_{oi}, is fed to the non-inverting input of a comparator (OC) which functions as a zero-crossing detector. If the output of the integrator is positive ($v_{oi} \geq 0$), then the comparator output (v_c) would be "1" (high); else v_c will be "0" (low). The output of the comparator v_c serves as the input to the Timing and Control

Unit (TCU). The TCU logic senses v_c and sequences the integrations by suitably controlling switches S_1 and S_2 through control lines A_1 and A_2. Prior to a conversion, the circuit of Fig. 3.1 must be appropriately initialised. For the present scheme, the necessary initial condition is that the output of the integrator be made zero. The process of ensuring this initial condition is popularly known as "auto-zero" in a dual slope technique. The auto-zero phase for the proposed DSRDC is detailed next.

3.2.1 Auto-zero phase

In the auto-zero phase, the TCU senses the comparator output v_c. If v_c is high, then the feedback capacitor C_F possesses a charge with a positive polarity on its terminal connected to the output of OA. For this condition, the TCU sets both S_1 and S_2 in position 2 (A_1 = A_2 = "0") connecting $+V_R$ to R_x and grounding R_o. The resulting capacitor current $i_C = -V_R / R_x$, discharges the feedback capacitor and the integrator output ramps down to zero (or de-integrates as it is sometimes called) as shown by the dotted line in Fig. 3.2 (and Fig. 3.3). On the other hand, if v_c is initially low, feedback capacitor is so charged that its terminal connected to the output of OA has a negative polarity. For this condition, the TCU sets both S_1 and S_2 to position 1, connecting $-V_R$ to both R_x and R_o. The resulting capacitor current $i_C = \left(\frac{V_R}{R_o} + \frac{V_R}{R_x} \right)$ discharges C_F and the integrator output, v_{oi}, ramps up towards zero (indicated by the dashed lines in Fig. 3.2 and Fig. 3.3). In either case, the integrator becoming zero is indicated to the TCU by a transition (high to low in the former case and low to high in the latter) of the comparator output v_c, which marks the end of the auto-zero phase. The flowchart of the logic of the auto-zero phase is depicted in Fig. 3.4. A conversion phase is initiated at the end of the auto-zero process.

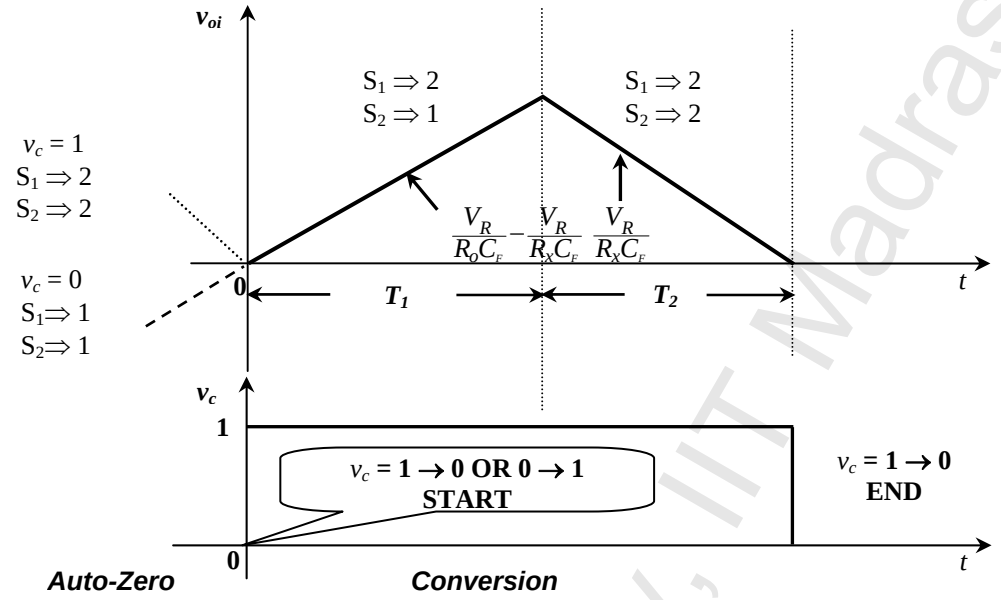


Fig. 3.2 Waveforms of the integrator output v_{oi} and comparator output v_c for a complete conversion (kx is positive)

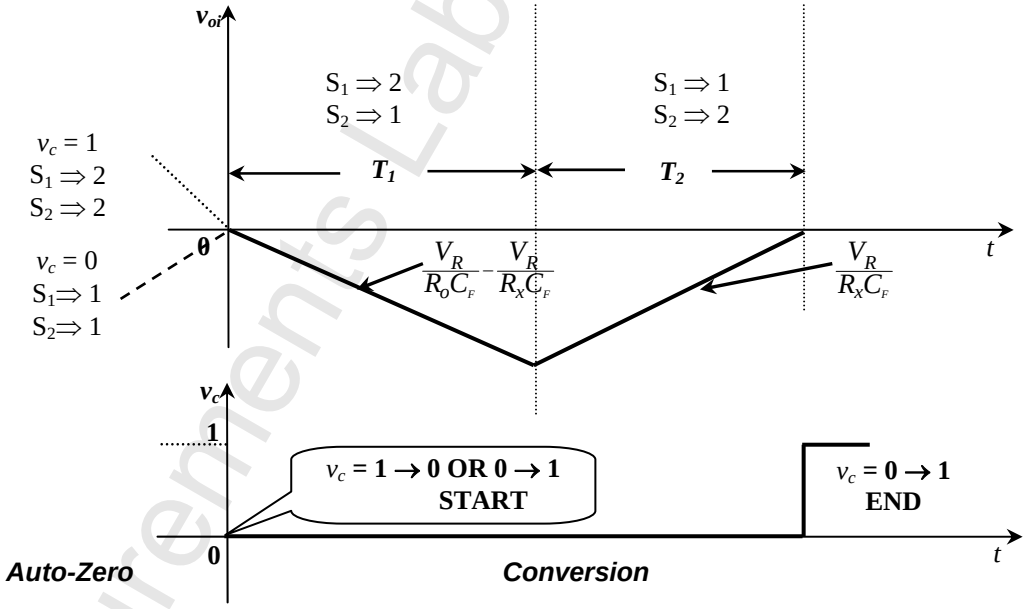


Fig. 3.3 Waveforms of the integrator output v_{oi} and comparator output v_c for a complete conversion (kx is negative)

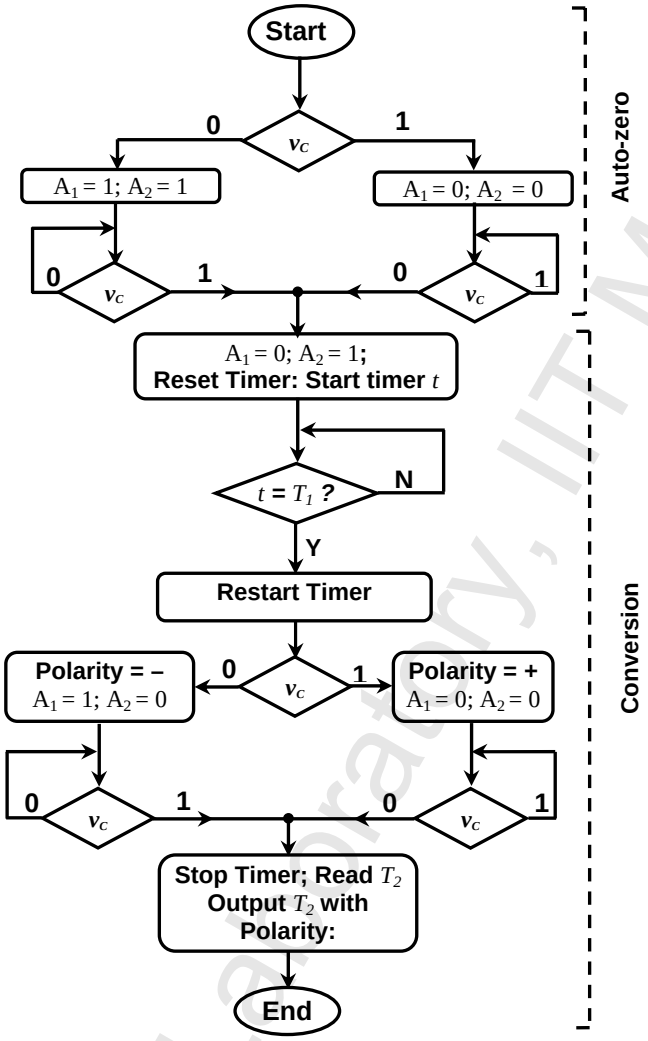


Fig. 3.4 Flowchart showing the auto-zero and conversion logic of the DSRDC for a single element resistive type sensor

3.2.2 Conversion phase

The conversion phase consists of two integration periods. The first integration period T_1 is a pre-selected, set value and the second integration period T_2 is measured and taken as the output. The conversion phase (measurement cycle) is started, immediately following the end of an auto-zero phase (start-stop conversion mode) or the end of a previous conversion phase (continuous conversion mode), by setting switches S_1 and S_2 to positions 2 and 1 respectively, thus connecting $+V_R$ to R_x and $-V_R$

to R_o. Simultaneously, he TCU starts an internal timer for a pre-set time period of T_1. The resulting current $i_C = \left(\frac{V_R}{R_o} - \frac{V_R}{R_x} \right)$ is injected into the feedback capacitor C_F by the opamp OA.

If *kx* is positive, then i_c will be positive and C_F would be charged in a manner such that the terminal connected to the output of the opamp OA acquires a positive polarity. The opamp output will therefore ramp up with a positive slope $\left(\frac{V_R}{R_o C_F} - \frac{V_R}{R_x C_F} \right)$ as shown in Fig. 3.2. At the end of T_1, the integrator output will be positive and the output of the comparator v_c will be high. At t = T_1, the TCU resets and restarts the internal timer to measure the elapsed time interval T_2 during the second integration. Since v_c is high at the end of T_1, the polarity of *kx* is taken as positive and the TCU sets both S_1 and S_2 to position 2, connecting $+V_R$ to R_x and grounding R_o. As a result, the charging current $i_c = -V_R / R_x$ flows into C_F and causes the integrator output to ramp down with a slope $V_R/(R_x C_F)$, reaching zero in time T_2, as illustrated in Fig. 3.2.

On the other hand, if *kx* were negative, then $i_c = \left(\frac{V_R}{R_o} - \frac{V_R}{R_x} \right)$ will be in a direction opposite to that indicated in Fig. 3.1 and the output of the integrator would ramp down during T_1 as shown in Fig. 3.3. At the end of T_1, the TCU senses v_c to be "0" and hence (i) marks the polarity as negative and (ii) sets switches S_1 and S_2 to positions 1 and 2 respectively and restarts the internal timer to measure T_2. In this condition, the capacitor current $i_c = V_R / R_x$ forces the output of the integrator to ramp up and reach zero, as shown in Fig. 3.3.

In either case, the output of the integrator v_{oi} reaching zero is indicated to the TCU by a transition in v_c. Sensing the transition, the TCU stops the counter-timer and reads

the time taken for the output of the integrator to reach zero (T_2) and outputs T_2 along with the polarity. The logic for both the conversion and auto-zero phases is shown in Fig. 3.4. Since the total charge acquired by the capacitor C_F over the conversion cycle ($T_1 + T_2$) is zero, we get:

$$\left(\frac{V_R}{R_o C_F} - \frac{V_R}{R_x C_F}\right) T_1 = \left(\frac{V_R}{R_x C_F}\right) T_2 \tag{3.1}$$

Rearrangement of equation (3.1) results in

$$\frac{R_x - R_o}{R_o} = \frac{T_2}{T_1} \tag{3.2}$$

Substituting for R_x as given by expression (1.3) in equation (3.2), we obtain:

$$kx = \frac{1}{T_1} T_2 \tag{3.3}$$

Since T_1 is a pre-set constant and k, the transformation efficiency of the sensor is also time-invariant, the measured time period T_2 directly indicates x, the measurand being sensed by the single element resistive sensor. Thus, in principle, the output of the DSRDC is influenced only by a fixed time period T_1, which can be set with great accuracy.

3.3 Analysis of the DSRDC

The derivation of equation (3.3) assumes ideal conditions and components. Deviations from such ideal conditions and the non-idealities of the components in a practical implementation of the proposed scheme will introduce errors in the output. These sources of errors are analyzed and the circuit is simulated before experiments are conducted on a prototype to validate its practicality. The following sections analyse the effects of various sources of errors on the performance of the circuit as well as discuss the results of the simulations and experiments carried out.

3.3.1 Effect of the 'ON' resistances of the switches

In deriving equation (3.3), it was assumed that the switches employed in the DSRDC were ideal, possessing zero 'ON' resistances. In reality, practical switches possess finite, 'ON' resistances which would appear in series with the resistances R_x and R_o. Hence, for a practical case, equation (3.2) gets modified as $\frac{(R_x + r_1) - (R_o + r_2)}{(R_o + r_2)} = \frac{T_2}{T_1}$, where r_1 and r_2 are the ON resistances of the switches S_1 and S_2. Simplifying the above expression, we obtain

$$kx = \frac{1}{T_1}\left(1 + \frac{r_2}{R_o}\right) T_2 + \frac{(r_2 - r_1)}{R_o} \tag{3.4}$$

A comparison of equation (3.4) with (3.3) shows that the 'ON' resistances of the switches introduce a gain error as well as an offset in the output. The former will be insignificant if the ratio r_2 / R_o is chosen to be very small, a condition easily met with most modern-day switches, possessing 'ON' resistances as low as 1.25 Ω [42] or even lower [43],[44]. As can be seen, the offset can be eliminated by employing two identical switches ($r_1 = r_2$). The effect of the 'ON' resistances of the switches can also be eliminated by using low offset, unity gain buffers at the outputs of the switches S_1 and S_2, as indicated in Fig. 3.5.

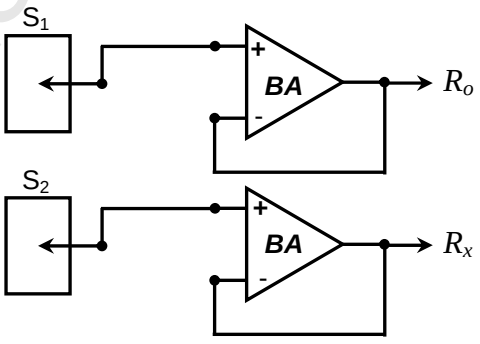


Fig. 3.5 Use of buffers to remove the effect of switch 'ON' resistance

3.3.2 Effect of the deviation of the fixed resistance from its expected value of R_o

Equation (3.2) is based on the assumption that the fixed resistance has a value exactly equal to the nominal value R_o of the sensor. In practice, the value of the fixed resistance may deviate from the expected value, in which case, equation (3.2) becomes

$$\frac{R_x - R_o^{'}}{R_o^{'}} = \frac{T_2}{T_1}, \tag{3.5}$$

where $R_o^{'}$ is the value of the fixed resistance ($R_o^{'} \neq R_o$). If the ratio $R_o / R_o^{'}$ is taken as α, then equation (3.5) simplifies to

$$kx = \frac{1}{T_1} T_2 \left(\frac{1}{\alpha} \right) + \left(\frac{1}{\alpha} - 1 \right) \tag{3.6}$$

A comparison of equations (3.6) and (3.3) indicates that the deviation in the value of the fixed resistance from the expected nominal value of the sensor resistance also introduces a gain error and an offset. The greater the deviation from the nominal value, larger is the error produced in the output. Use of precision resistors for the fixed resistance will go a long way towards minimising the errors caused by such deviation. Remaining errors, if any, can be easily nullified by proper gain correction and offset compensation.

3.3.3 Effect of reference voltage mismatch and opamp offset voltage

Equation (3.1) assumes that the reference voltages $-V_R$ and $+V_R$ are of equal magnitude. In practise, $-V_R$ is obtained by inverting a positive reference voltage. Hence, the degree of match of the magnitudes of the two voltages depends on the precision with which the inversion is performed. Any offset voltage in the integrator opamp, if present, also manifests as a mismatch between reference voltages. Whatever be the reason for the mismatch, equation (3.1) will have to be suitably modified. If the ratio ($\left|-V_R\right| / \left|+V_R\right|$

is taken as η, then for positive *kx*, equation (3.1) becomes,

$$\left(\frac{\eta V_R}{R_o C_F} - \frac{V_R}{R_x C_F}\right) T_1 = \left(\frac{V_R}{R_x C_F}\right) T_2 \tag{3.7}$$

On simplification, we get,

$$kx = \frac{1}{T_1} T_2 \left(\frac{1}{\eta}\right) + \left(\frac{1}{\eta} - 1\right). \tag{3.8}$$

On the other hand, for negative *kx*, we have

$$\left(\frac{\eta V_R}{R_o C_F} - \frac{V_R}{R_x C_F}\right) T_1 = \left(\frac{\eta V_R}{R_x C_F}\right) T_2, \tag{3.9}$$

resulting in,

$$kx = \frac{1}{T_1} T_2 + \left(\frac{1}{\eta} - 1\right). \tag{3.10}$$

A comparison of equations (3.8) and (3.3) shows that if the measurand *kx* is positive, the mismatch in the two reference voltages introduces a gain error and an offset. On the other hand, as indicated by expression (3.10) it produces only an offset if the measurand has a negative polarity.

It is seen that all the non-idealities, namely, ON resistances of the switches, mismatch between the fixed resistance and the nominal resistance values, mismatch in the reference voltage magnitudes and the opamp offset voltage not only cause an error in the designed gain of the circuit but also an offset. The gain error as well as the offset can be easily compensated by gain correction and offset nulling.

3.3.4 Errors due to the delays caused by the comparator, control circuit and the switches

While discussing the operation of the proposed DSRDC, it was assumed that the circuit was ideal in that the comparator detected the zero crossing of the output of the integrator perfectly and that it also indicated the zero crossing instantaneously to the TCU. In practice, the comparator will possess an offset as well as a delay. The offset will result in the comparator detecting the “zero” at the offset voltage instead of at

actual zero. It is easily seen that the presence of offset in the comparator shifts the base line of comparison shown in Fig. 3.2 (and Fig. 3.3) up or down depending on the polarity and by an amount equal to the magnitude of the offset voltage. This shift in the baseline does not alter T_1 or T_2 as long as the offset is constant during one conversion cycle (which implies that the offset drift is zero). Hence the offset of the comparator does not affect the functioning of the DSRDC.

If the delay due to the comparator is denoted by τ_c, then the resultant error in the output is given by τ_c/T_1. The comparator delay is normally small (200 ns for the LM311 used in the prototype) when compared to the period T_1. Hence, the delay of the comparator has negligible effect on the performance of the DSRDC. Though the delay introduced by the switches is a few hundred ns, this is again very small when compared to T_1 and T_2 (which are normally in the range of ms) and hence does not significantly affect the performance of the DSRDC.

3.4 Simulation studies

To test the efficacy of the proposed method, the DSRDC was simulated using OrCAD-PSpice (v16.2) from M/s Cadence Corp. Since the PSpice model of the HCF4052 proposed to be used for the switches was not available, it was decided to simulate the DSRDC using the ADG508 octal switch from Analog Devices. The OP07 was used as the opamp and the LM311 as the comparator. The timing and control unit was implemented using simple logic gates and the LM555 timer IC.

Simulations were carried out for RTD types of sensors. A typical RTD sensor with a nominal value of 10000 Ω (Pt10000) was chosen as the sensor and the circuit operation was simulated. The time taken for the integrator output voltage to return to zero (T_2) was measured for each run of the simulation. A screenshot of one of the simulation runs is shown in Fig. 3.6. The waveform shown as V(COMP_1) represents

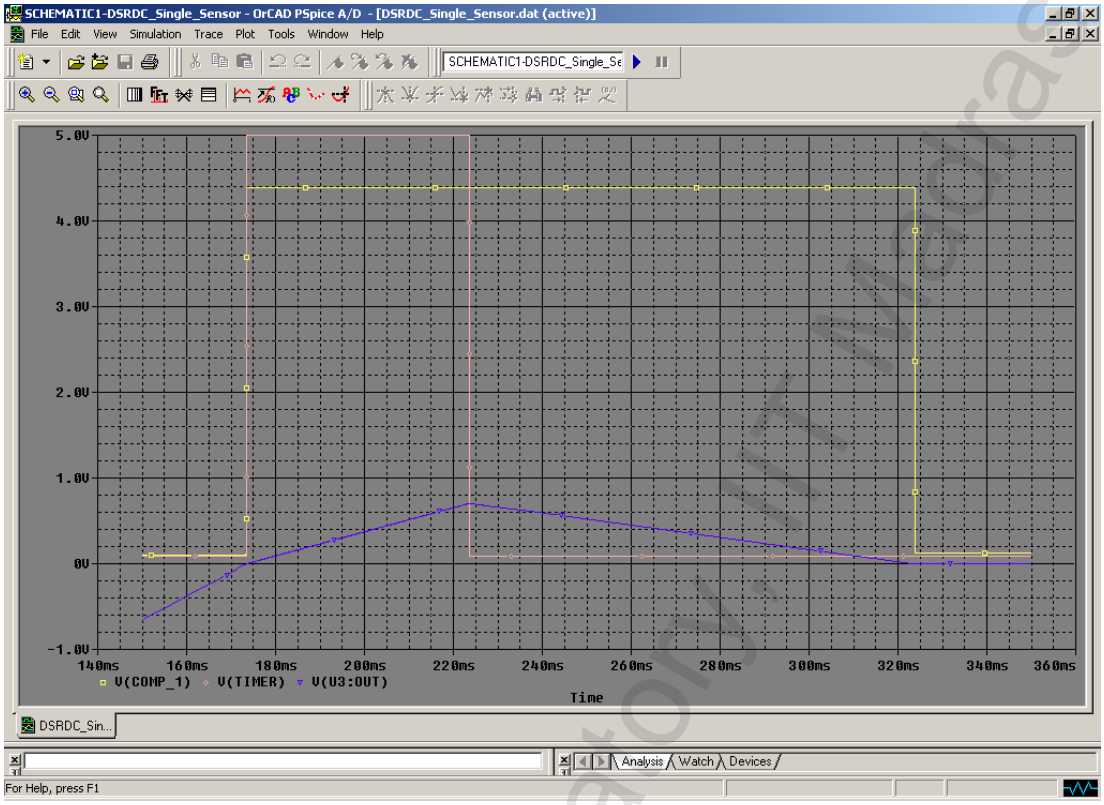


Fig. 3.6 Snapshot of a single run of the simulated DSRDC

the output of the comparator while V(TIMER) indicates the output of the LM555 timer used to generate the fixed duration pulse of T_1. As can be seen, in the interval between the falling edges of the two signals, V(COMP_1) and V(TIMER), the integrator output (shown as V(U3:OUT)) discharges to zero. This duration was measured as T_2. T_2 was used to calculate the temperature using the coefficients provided by M/s Heraeus Sensor-Technology, Germany, manufacturer of the sensor used in prototyping the circuit. Various likely sources of error like comparator and switch delay, opamp and comparator offset voltage, 'ON' resistance of the switches and change in the nominal value of the fixed resistance, were incorporated into the circuit, to determine the worst-case performance. The simulation was run for a temperature range from -50 ºC to 150 ºC, in steps of 10 ºC. The results of the simulation are presented in Fig. 3.7. As can be seen, the output was highly linear as expected and the errors in the output were well within acceptable limits (± 0.02 %).

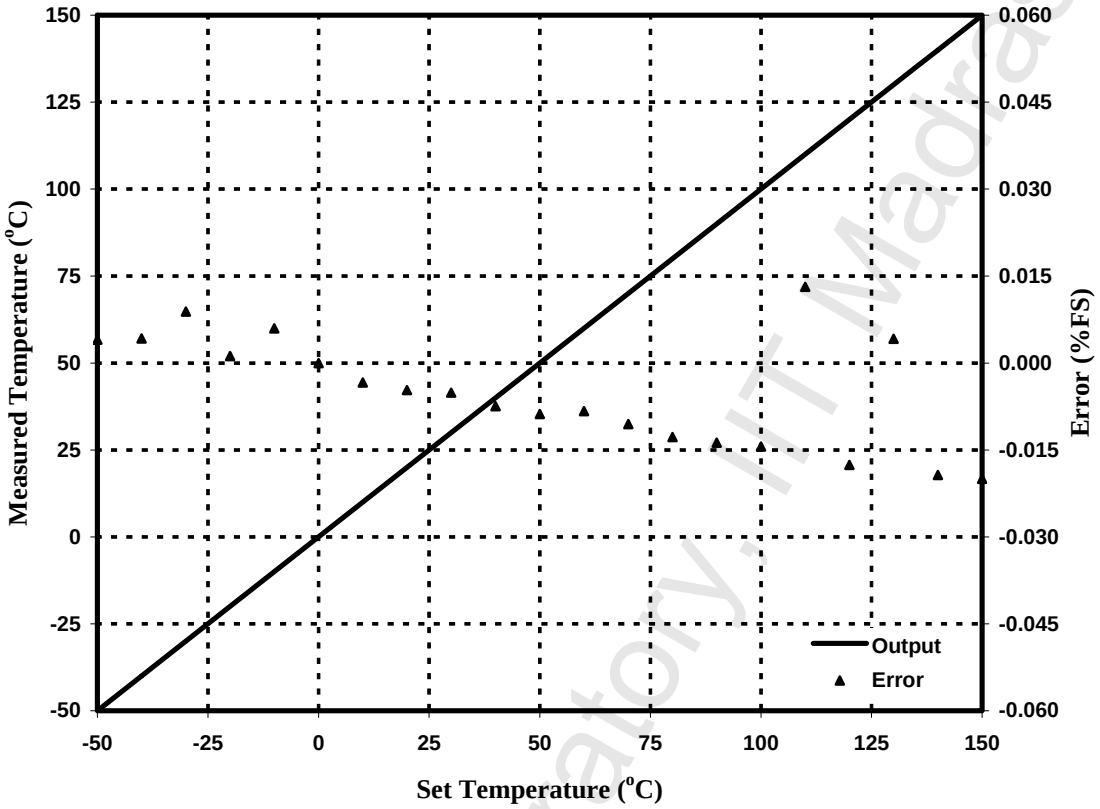


Fig. 3.7 Performance of the circuit in the temperature range from -50 °C to 150 °C (Simulation Study)

The magnitude of the positive reference voltage was then shifted by 1 % and the simulation was run again. As predicted by expression (3.10), there was a degradation in the circuit performance, with the full scale error going up to ± 0.35 %. In fact, the mismatch in reference voltage magnitude is the major and only significant source of error in the circuit.

3.5 Experimental studies

The circuit depicted in Fig. 3.1 as well as the control logic illustrated by the flowchart of Fig. 3.4 was implemented using easily available, off-the-shelf components and tested. The OP97 [45] was the opamp of choice for the integrator while the LM311 was employed for use as the comparator. The comparatively high input offset voltage of the LM311 (30 mV maximum) was moderated by making use of the fact that it is the

transition of the integrator output which is of significance rather than the magnitude of the voltages themselves. Therefore, the output of the integrator was amplified by a factor of 100, before being used with the comparator, due to which the comparator could detect the zero crossing of the integrator output voltage within ± 300 μV. The positive reference voltage $+V_R$ was obtained using an LM385-1.2 Voltage Reference Diode. The negative reference voltage $-V_R$ was derived from $+V_R$ using an opamp inverter realized with another OP97. The magnitudes of the reference voltages were continuously monitored using two 6½-digit multimeters from M/s Keithley (Model 2100) and were matched to ± 10 μV by making use of precision, variable resistances from Otto Wolff, Berlin. The HCF4052 [46] containing Dual, Quad-channel switches was used for switching the appropriate reference voltages to the sensor R_x and the fixed value resistor R_o. The entire circuit was powered by a ± 5 V/1.5 A, DC/DC Converter (AEE01AA18-L) from M/s Astec Power, USA [47]. The sensor (R_x) used was a Pt10000 RTD Sensor (M622) [48] from M/s Heraeus Sensor-Technology, Germany. It was first calibrated using the MP40R and MTC650 temperature calibrators from M/s Nagman Instruments, India, for the range from 0 ^oC to 600 ^oC, in steps of 10 ^oC. The resistance of the RTD at the various temperatures was carefully measured using the 34401A, 6½-digit multimeter from Hewlett-Packard. The DL-750P Scopecorder from M/s Yokogawa, Japan was employed to continuously monitor the waveforms at the cardinal points of the circuit.

The control and timing logic was implemented on a Virtual Instrument platform so as to bring in flexibility, modularity and easy scalability. The NI USB-6251 universal series bus (USB) based hardware from M/s National Instruments [49] formed the core of the control and logic unit with the control logic being implemented in LabVIEW. The digital input and output lines and the two 32-bit, general purpose counter-timers of the

USB-6251 formed the heart of the control and logic system. The NI USB-6251 was interfaced to the switches and the comparator through the BNC-2120 termination board. Two of the digital output lines of the USB-6251 served as the control lines, A_1 and A_2, for the HCF4052. The comparator output was made TTL compatible and tied to a digital input line of the NI USB-6251. A snapshot of the entire experimental setup is shown in Fig. 3.8.

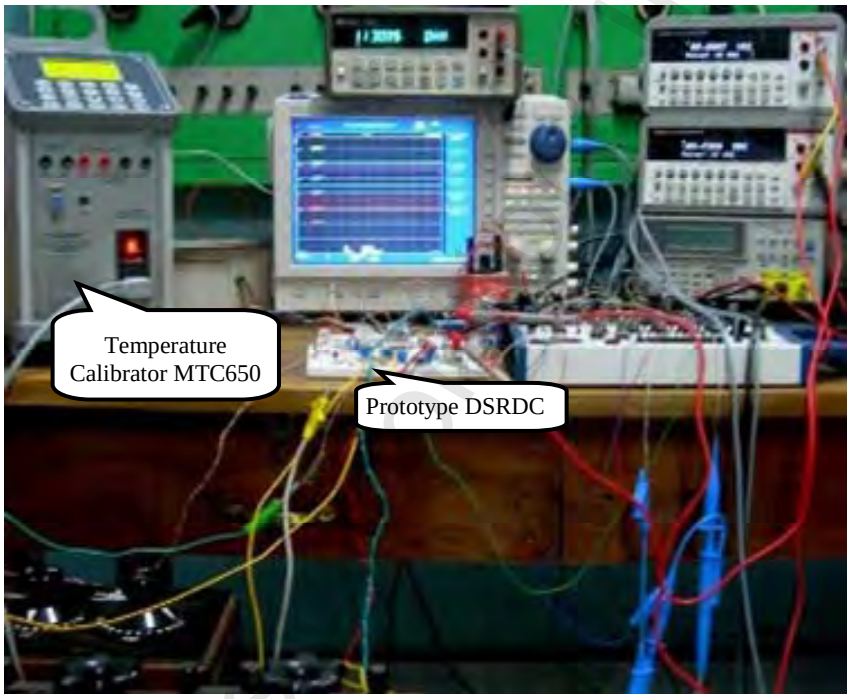


Fig. 3.8 Snapshot of the experimental setup for the Dual Slope Resistance to Digital Converter

The auto-zero and conversion logic was realized by a suitable program written in LabVIEW. A screenshot of the front panel of the Virtual Instrument developed for this purpose is shown in Fig. 3.9. The program makes use of one of the counters in the USB-6251 to generate a precise pulse train of the required frequency ($1/T_1$). This frequency can be controlled by software from the front panel and hence T_1 can be modified to accommodate different combinations of R_o and C_F. At the beginning of T_1, the digital lines controlling the switch cause the resistive sensor (R_x) and the standard,

fixed resistance (R_o) to be switched to the respective reference voltages. The rising edge of the counter output of the USB-6251 at the end of T_1 switches the sensor resistance R_x to the positive reference voltage while the fixed resistance R_o is grounded. The instant the integrator output voltage reaches zero, the output of the comparator toggles indicating the end of T_2 and thereby the end of the measurement cycle. The start of T_2 (end of T_1) and the change in the comparator output at the end of T_2 serve as markers for another USB-6251 counter and hence are used to measure the time period T_2 accurately.

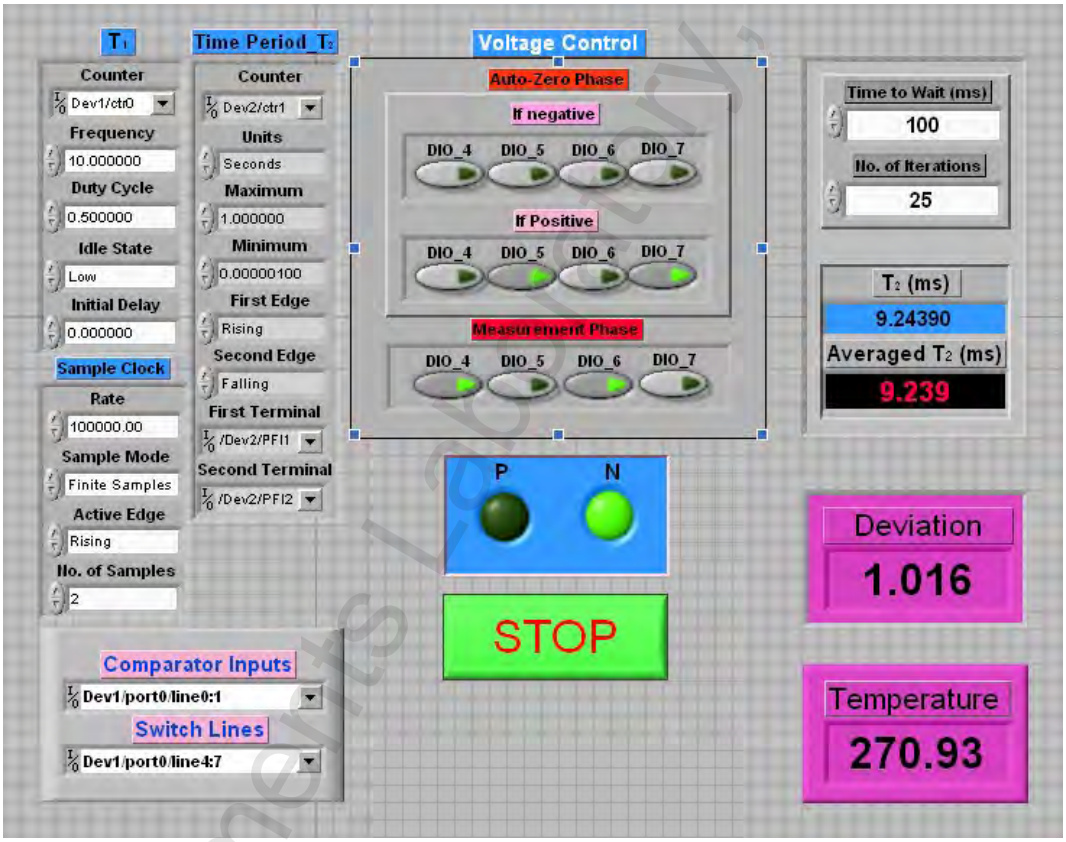


Fig. 3.9 Screenshot of the front panel of the Virtual Instrument developed for the Dual Slope Resistance to Digital Converter

A snapshot of the waveforms at different points of the circuit is shown in Fig. 3.10. In the figure, channels 1 and 2 indicate the voltage applied to the sensor and fixed resistances respectively, while channel 3 records the output of the comparator. Channel 4 indicates the status of the switch line A_1, which changes state at the end of

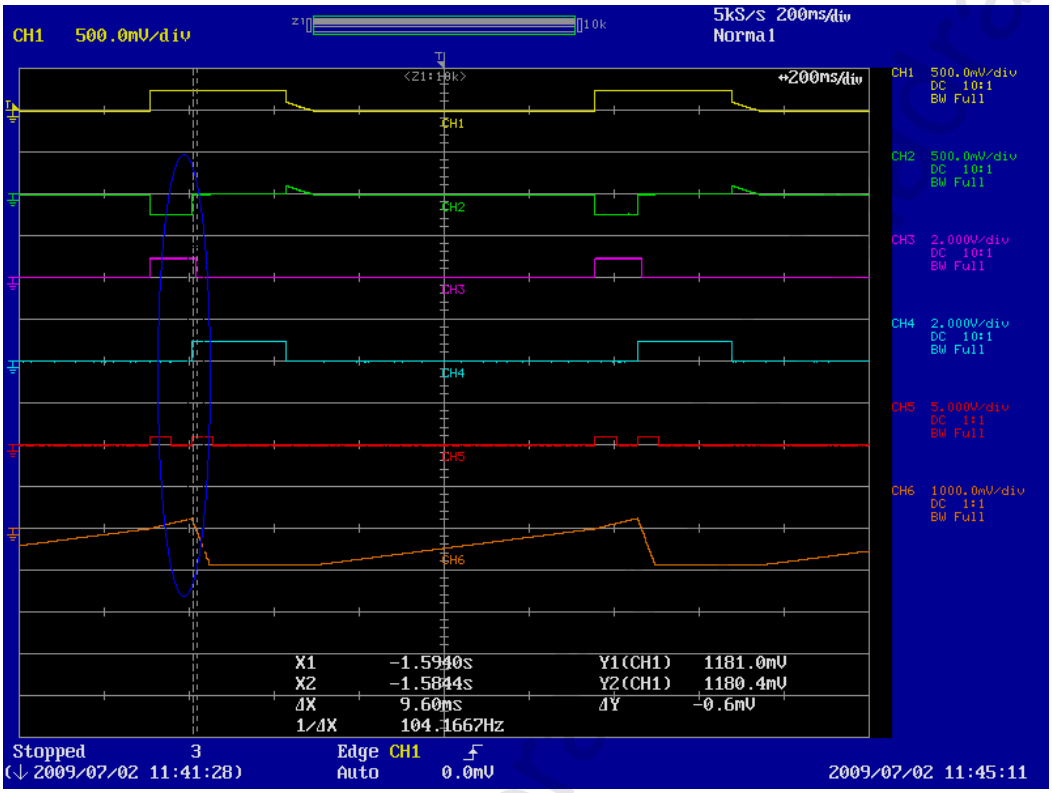


Fig. 3.10 Snapshot of the voltage waveforms at the cardinal points of the DSRDC, with the area of interest clearly marked

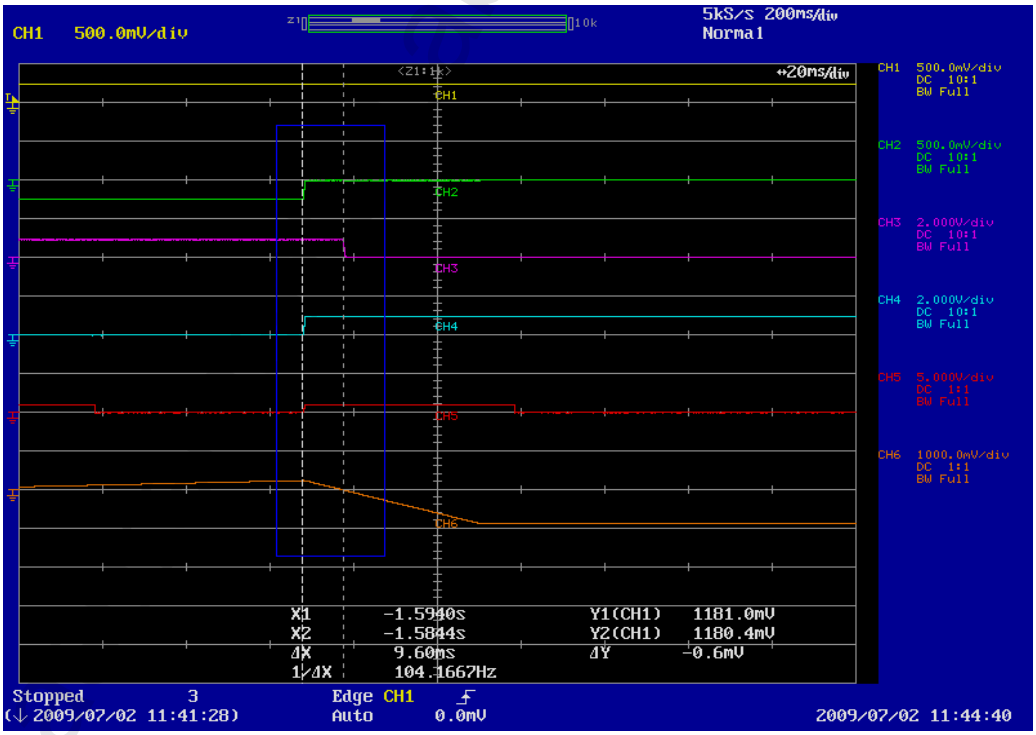


Fig. 3.11 A magnified view of the area highlighted in the previous figure

T_1. Channel 5 of the scopecorder shows the pulse train generated by the counter of the USB-6251 Data acquisition device while the integrator output is displayed in Channel 6. The interval of interest, during which the integrator discharges to zero, is clearly marked in the figure. A magnified view of the marked area, indicating the time duration between the change of state of the comparator and A_1 lines, which serve as markers for the period T_2, is presented in Fig. 3.11.

Each measurement was repeated 25 times to average out any random errors and the resulting value of T_2 was used to calculate the deviation *kx*, using equation (3.3). This calculated value of *kx* was utilised to determine the temperature in accordance with the IEC60751 Standard [50] and the associated coefficients for a Platinum RTD (Pt 10000). The measured temperature is plotted in Fig. 3.12 against the temperature set on the calibrator for the range from 0 ^{o}C to 600 ^{o}C, in increments of 10 ^{o}C, along with the corresponding errors for the different measurements. As can be seen, the prototype exhibits excellent linearity over the entire range of measurement, with a maximum error of less than ± 0.2 %. The experiment was conducted again in the temperature range from 330 ^{o}C to 350 ^{o}C, in steps of 1 ^{o}C, to determine the sensitivity of the circuit to small changes in the input. The performance of the circuit over this truncated range is indicated in Fig. 3.13 and as can be seen, the circuit affords very good resolution, with very low errors.

3.6 Summary

The resistance to digital converter presented here has all the advantages of the conventional dual slope technique such as good resolution, accuracy and tolerance to component variations as well as the attendant limitation of the technique, namely, low conversion speed. A conversion speed of a few conversions to a few hundred samples

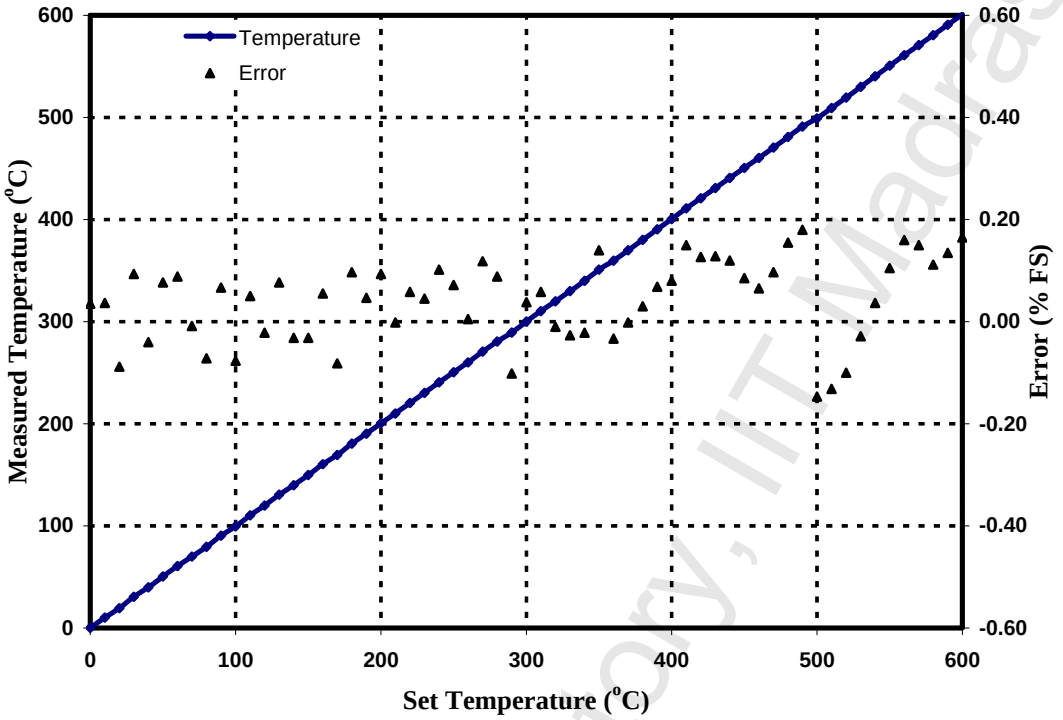


Fig. 3.12 Performance of the prototype for a temperature range from 0 °C to 600 °C, in steps of 10 °C

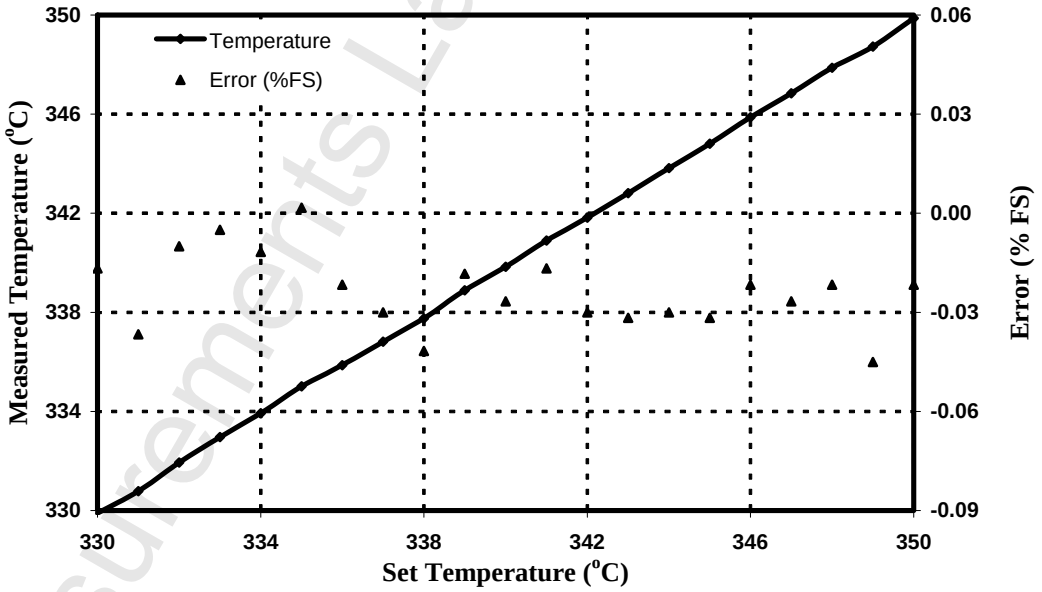


Fig. 3.13 Performance of the prototype in the temperature range of 330 °C to 350 °C, in steps of 1 °C

per second is achievable. This speed is quite adequate for most applications involving resistive sensors. Analysis of the proposed method for possible sources of errors, indicates that most of the non-idealities introduce a gain error and an offset, which can be easily nullified by employing suitable gain correction and offset compensation Results obtained on a prototype, presented here, establish the efficacy of the proposed method and justify the inferences drawn through analysis.

Though the dual slope resistance to digital converter described in this chapter provides excellent results when used with an intrinsically linear, single element resistive sensor like the RTD, it cannot accept sensors like the thermistor, which exhibits a typical inverse exponential resistance-temperature relationship. The DSRDC for a single element sensor is not capable of linearising such a relationship. In the next chapter, a circuit which not only linearises the exponential resistance-temperature characteristic of a thermistor but also produces a digital output which is directly proportional to the temperature being sensed by the thermistor is discussed in detail.

4.Linearising Digital Converter for a Thermistor

4.1 Introduction

Temperature is one of the primary physical parameters to be measured in a typical control or instrumentation process. Depending on the nature of the process as well as the kind of output and the degree of accuracy required, various devices are used to measure temperature. Due to its compactness, high sensitivity, accuracy, ruggedness, bio-compatibility as well as its relatively low price and time constant, the thermistor has been a popular choice of device for the measurement of temperature. Thermistors are also used for measuring fluid flow, as temperature compensating devices in electronic circuits and as inrush current and voltage limiters, to mention a few other applications [51]-[53].

Thermistors may posses either a positive (PTC Thermistor) or a negative temperature coefficient (NTC Thermistor) of resistance. However, the latter are generally preferred when one needs to measure temperature precisely and hence the term “thermistor” usually refers to an NTC thermistor.

Unfortunately, due to the highly nonlinear relationship between the resistance of the thermistor and the temperature it is subjected to, it is very difficult to readily exploit the various advantages that the thermistor offers. The precise nature of this relationship as well as the means to linearise it has been a matter of study for a long time. Though the exponential nature of the resistance-temperature relationship of a thermistor was known as far back as 1946 [54], with Bosson *et al*. formulating the three-constant fit for the *log R-1/T* curve of the thermistor in 1950 [55], the problem of linearising this relationship for it to be of accurate use in the determination of temperatures, remained.

4.1.1 Linearisation using hardware

Different methods have been tried in linearising the temperature-resistance relationship of a thermistor, with varying degrees of success. One of the simplest means to achieve this has been to include a resistor in series or parallel with the thermistor, so that the response is almost linear with the change in temperature over a small range [56]. But with this technique, achievement of sufficiently good linearity is at the expense of drastically reduced dynamic range. This drawback was sought to be overcome by the use of a reciprocal time generator to obtain a digital output proportional to the temperature [57]. The linearity was further improved by employing a four-constant fit for the relationship governing the temperature and the resistance of the thermistor [58], though at the cost of increased complexity as four simultaneous, nonlinear equations had to be solved to obtain the constants. Bosson's three-constant law was also employed to develop a linear temperature-to-time period converter, incorporating a thermistor [59]. The circuit provided excellent linearity (~ 0.02 %) but over a very narrow range of 10 K, the reason being that such a small variation was one of the essential assumptions on which the approximation of the thermistor characteristic was based.

Another of the earlier techniques was to incorporate the thermistor as one of the arms of a Wheatstone bridge, with the output being linearised by a three-point method [60]. Another established technique for the linearisation of the output of a thermistor involved the use of different kinds of multivibrators [61]-[67], where differing degrees of linearity were obtained over limited ranges of temperatures. An improvement on this method using an astable multivibrator has also been reported [68], due to which acceptable levels of linearisation have been achieved over a greatly increased temperature range of 0 to 85 ^{o}C.

Another way in which the output of the thermistors has been sought to be linearised is by including them as part of logarithmic amplifier networks [69]-[71]. The same purpose has been achieved by means of a relaxation oscillator based circuit, where the output of a voltage divider of which the thermistor forms a part, is compared with that of a RC network. The output of the comparator triggers a timing circuit, which in turn controls the RC network in a closed loop feedback configuration. A modified form of such a temperature to frequency converter has been implemented using a delay network [72], with promising results. An innovative approach to solving the thermistor linearisation problem has been by using the inverse-exponential nature of the voltage-time relationship of a charging RC-network, which is based on a modified square wave generator [73]. One of the major drawbacks of these early attempts has been the necessary compromise between linearity and dynamic range. Desirable levels of linearity have been achieved only over limited temperature ranges. When the temperature range was extended, the linearity dropped considerably.

4.1.2 Linearisation employing software

With the advent of digital technology and the easy availability of faster and economically viable processing power, software has come to be increasingly used in the linearisation of transducer outputs [74]-[77], making use of ‘look-up tables’ and ‘maps’. New techniques like artificial neural networks and evolutionary algorithms have been proposed to iteratively linearise the output of thermistor based circuits [78]-[80]. An application specific chip has also been designed for the purpose [81]. The downside of such methods has been the increasing reliance on brute computing power to find the ‘best’ polynomial fit for the temperature-resistance relationship of a thermistor.

Except for the software based techniques, the outputs of most of these linearising circuits are analog in nature and need to be converted to a digital form before being

interfaced to the digital instruments which are widely used today. It would evidently make for a simpler and more robust system if the analog to digital converter were to be made an integral part of the linearising circuit, so that the final output is digitally compatible. The circuit described in the following sections of this chapter, incorporates the thermistor as part of a logarithmic amplifier, the output of which is interfaced to a conventional dual slope, analog to digital converter to accomplish temperature-to-time conversion by providing a digital output, directly proportional to the temperature being sensed. Simulations as well as results on a prototype developed in the laboratory validate the exercise, by providing a linear temperature-time curve over the temperature range from 0 ^{o}C to 120 ^{o}C.

4.2 A Linearising Digital Converter (LDC) for thermistors

The proposed linearising digital converter for the thermistor can be considered to be of three parts : (i) the thermistor, (ii) a logarithmic amplifier and (iii) a voltage to time converter. The three parts can be described respectively by the following individual expressions:

$$log\, R_\theta = K_1 + \frac{K_2}{\theta + K_3}, \tag{4.1}$$

$$v_{log} = K_4 + K_5\, log\, R_\theta \tag{4.2}$$

and

$$T_2 = K_6 + \frac{K_7}{v_{log}}, \tag{4.3}$$

where $K_i (i = 1,2....7)$ are constants, R_θ is the resistance of the thermistor, θ is temperature of the thermistor which is to be measured, v_{log} is the output of the logarithmic amplifier and T_2 is the time period measured at the output of the voltage to time converter. The three-constant law proposed by Bosson *et al*. [55] was adopted to describe the thermistor in equation (4.1). Using the expression (4.1) for $log\, R_\theta$ in equation (4.2), we get

$$v_{log} = K_4 + K_1K_5 + \frac{K_2K_5}{\theta + K_3} = \frac{(K_4 + K_1K_5)\theta + K_2K_5 + K_3(K_4 + K_1K_5)}{\theta + K_3}. \quad (4.4)$$

Replacing v_{log} in equation (4.3), with the expression obtained above, we have

$$T_2 = K_6 + \frac{K_7\theta + K_3K_7}{(K_4 + K_1K_5)\theta + K_2K_5 + K_3(K_4 + K_1K_5)} \quad (4.5)$$

Equation (4.5) indicates that the system as a whole has a nonlinear response. The degree of nonlinearity of the system is dictated by the relative magnitudes of the co-efficients K_7 and $(K_4 + K_1K_5)$. The system represented by expression (4.5) will be linear if and only if $K_4 + K_1K_5 = 0$, in which case the system reduces to

$$T_2 = \left(K_6 + \frac{K_3K_7}{K_2K_5}\right) + \left(\frac{K_7}{K_2K_5}\right)\theta. \quad (4.6)$$

It can be seen that the constant K_3 has no effect on the gain of the circuit, contributing only to an offset. Moreover, if K_6 were to be made zero as would be the case if the voltage to time converter were to be compensated for offset, equation (4.6) would reduce to

$$T_2 = \frac{K_7}{K_2K_5}(\theta + K_3). \quad (4.7)$$

The remainder of this section will be devoted to describing how the proposed circuit implements equation (4.7).

The front end of the circuit, shown in Fig. 4.1, is built around a logarithmic amplifier of which the thermistor forms a part. The output of the logarithmic amplifier serves as the input to an integrator, which in turn feeds a comparator, providing a quasi-digital output. The comparator output acts as the control signal for a timing and control unit (TCU), which forms the final part of the proposed converter. The TCU controls the sequence and duration of the signal to which the integrator input is connected. Fig. 4.1 shows the schematic representation of the circuit used for the purpose.

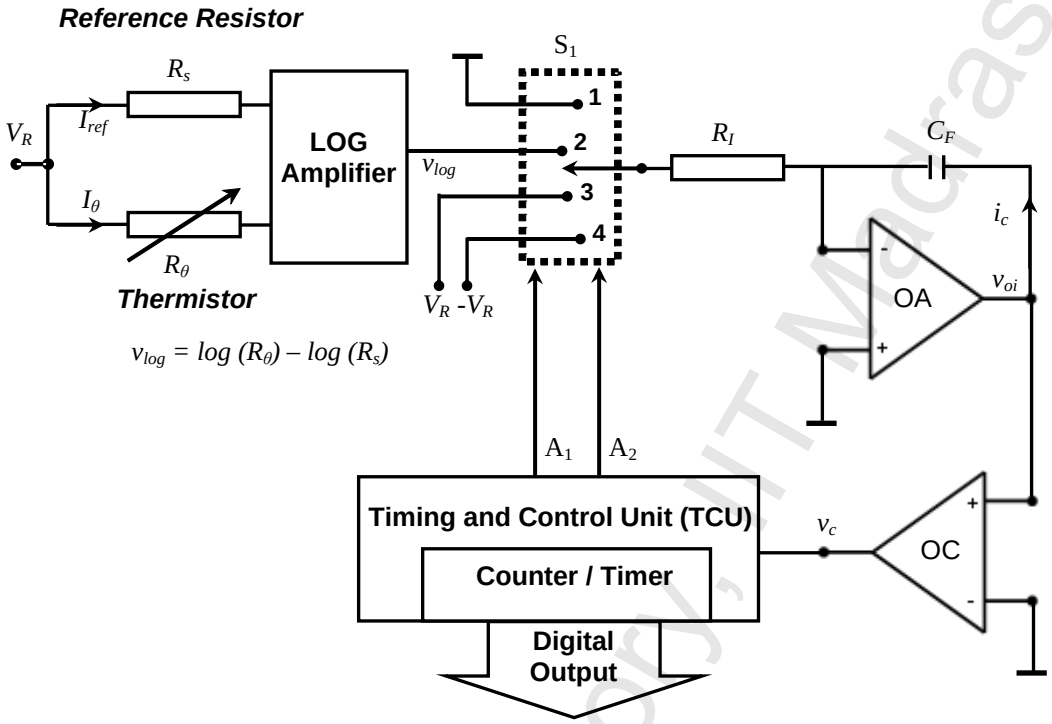


Fig. 4.1 Block schematic of the proposed LDC for a thermistor

The primary task of linearising the output of the thermistor falls on the logarithmic amplifier. The block schematic of the logarithmic amplifier used is shown in Fig. 4.2. A_v represents the closed-loop gain of the auxiliary amplifier stage and is determined by external components connected to terminals marked 1 and 2 [82].The output v' of the logarithmic amplifier used in the circuit is given by

$$v' = 0.5 log\left(\frac{I_{ref}}{I_\theta}\right) = 0.5 log\left(\frac{R_\theta}{R_s}\right), \tag{4.8}$$

where I_{ref} refers to the current flowing through a reference resistor shown as R_s in

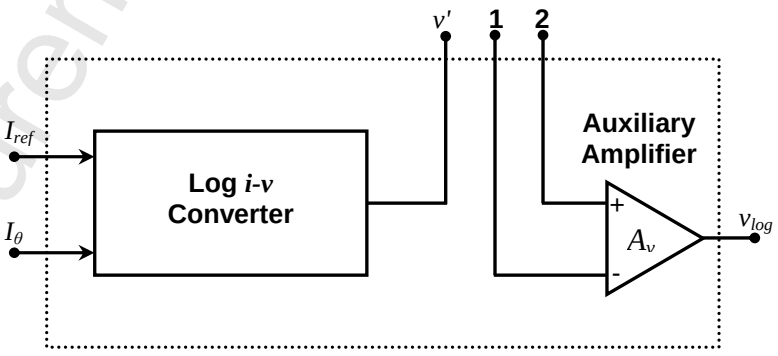


Fig. 4.2 Block schematic of the logarithmic amplifier used

Fig. 4.1 and I_θ indicates the current flowing through another resistor R_θ, which in this case, happens to be the thermistor. It is assumed that both resistors are connected to the same reference voltage. Simplifying equation (4.8) further, we get,

$$v' = 0.5\left(\log R_\theta - \log R_s\right) \tag{4.9}$$

Making use of equation (4.1), the above expression changes to

$$v' = 0.5K_1 - 0.5\log R_s + \frac{0.5K_2}{\theta + K_3},$$

leading to

$$\frac{1}{\theta + K_3} = \frac{1}{0.5K_2}\left(v' - 0.5K_1 + 0.5\log R_s\right). \tag{4.10}$$

If R_s is chosen such that $\log R_s = K_1$ and the gain of the auxiliary opamp of the logarithmic amplifier block shown in Fig. 4.2 adjusted so that $v_{log} = \frac{v'}{0.5}$, expression (4.10) simplifies to

$$v_{log} = \frac{K_2}{\theta + K_3}, \tag{4.11}$$

which is the defining expression for this circuit.

The integrator consisting of the opamp OA, the feedback capacitance C_F and the fixed resistance R_I, is connected to the appropriate voltage by the switch S_1, which is a 4:1 multiplexer. The switch in turn is controlled by the status of the control lines A_1 and A_2 from the timing and control circuit (TCU). Table 4.1 indicates the voltage connected to the resistance R_I for the different states of the control lines A_1 and A_2.

Table 4.1 Voltages switched to the fixed resistance R_I

A_1	A_2	**Voltage connected to R_I**
0	0	*Ground*
0	1	v_{log}
1	0	$+V_R$
1	1	$-V_R$

The values of '0' and '1' shown for the control lines A_1 and A_2 stand for digital

low and high respectively. The voltages $+V_R$ and $-V_R$ are two stable, dc reference voltages of equal magnitude but of opposite polarity. The output of the integrator v_{oi}, is input to a comparator (OC) which acts as a zero-crossing detector. The comparator output v_c, is fed to the TCU, which causes the correct sequence of voltages to be switched to the integrator for the appropriate duration.

Before the process of converting v_{log} can begin, it needs to be ensured that the output of the integrator is at zero. Therefore, as in any typical analog to digital converter, every conversion sequence is preceded by an auto-zero phase, where the output of the integrator is made to be zero before the conversion process takes place.

4.2.1 Auto-zero phase

Assume that the initial state of the circuit in Fig. 4.1 is such that the output of the integrator v_{oi}, is negative. v_{oi} being negative implies that the output of the comparator v_c will be low. This is sensed by the timing and control unit and the TCU logic ensures that the control lines to the switch, (A_1, A_2) are set at '11', so that the negative reference voltage $-V_R$ is connected to the fixed resistance R_I. As a result, a constant current, $i_c = V_R/R_I$, starts flowing through the capacitor and the output of the integrator ramps up towards zero. v_{oi} reaching zero is indicated to the TCU by v_c changing state from low to high. The output of the integrator reaching zero marks the end of the auto-zero phase.

On the other hand, if the circuit were to come up in a state where the integrator is in positive saturation, this would be indicated to the TCU by the comparator output v_c being high. Such a state would cause the TCU logic to set the control lines to '10', so that the resistance R_I is connected to the positive reference voltage, $+V_R$, causing a current $-V_R/R_I$ to flow through the capacitor, discharging it. As a result, the output of the integrator would now ramp down towards zero. When v_{oi} reaches zero, v_c changes state from high to low. This signals the end of the auto-zero phase to the TCU, which then

initiates the appropriate sequence for the conversion phase. Thus, a transition of the comparator state, either from low to high or from high to low, indicates the end of the auto-zero phase. The broken lines in the waveform diagram of Fig. 4.3 indicate the integrator output during the auto-zero phase.

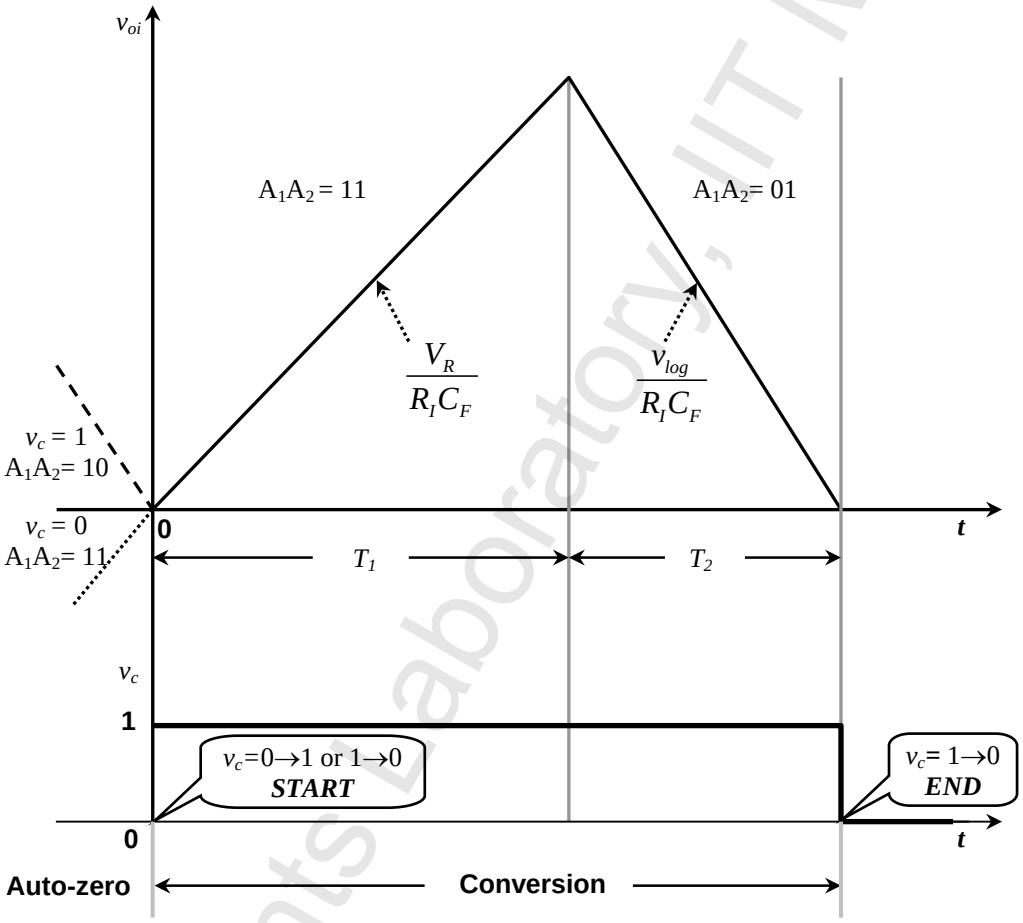


Fig. 4.3 Waveforms at the output of the integrator (v_{oi}) and the comparator (v_c)

4.2.2 Conversion phase

The LDC can be operated either in a controlled (start-stop) or a continuous conversion mode. In the former, an auto-zero phase precedes every conversion cycle while in the latter, the auto-zero phase is invoked only once at the start of the measurement cycle. A new conversion is initiated at the end of a previous conversion and hence the name continuous conversion mode.

The preceding auto-zero phase ensures that in every measurement cycle, the output of the integrator v_{oi} at the beginning of the conversion phase is zero. The TCU logic recognises the transition of the comparator output at the beginning of the conversion phase and sets the control lines A_1 and A_2 to '11', which causes S_1 to connect the negative reference voltage $-V_R$ to the resistance R_I. As a result, v_o charges towards V_R with a slope given by $V_R/(R_I C_F)$. This state is maintained for a pre-set, fixed period of time T_1, which is measured in terms of clock cycles as $T_1 = N_1 T_c$, where T_c indicates one clock period. This is accomplished by pre-loading the counter / timer of the TCU with N_1 and setting the counter to 'count down'.

At the end of T_1, which is accurately set by the timing and control unit, the counter rolls over and the TCU logic sets (A_1A_2) to '01', switching the output of the logarithmic amplifier v_{log}, to R_I. Simultaneously, the counter is loaded with a value of $(N_{fs}-N_k)$ and is set to 'count up'. N_{fs} is the full scale count of the counter and N_k is a constant, dependent on the thermistor characteristic. Since the logarithmic amplifier has been so designed that its output is positive, v_{oi} starts to ramp down with a slope $v_{log}/(R_I C_F)$, until it reaches zero after a time period denoted by T_2. The output of the integrator reaching zero is marked by a change of state of the comparator, from high to low, which indicates the end of the conversion phase and thereby, the measurement cycle. This is sensed by the TCU which outputs the contents of the counter at that instant, N_2, such that $T_2 = (N_2 + N_k - N_{fs})\, T_c$. The relevant waveforms along with the status of the control lines are shown in Fig. 4.3.

Since the total charge acquired by the capacitor over the entire measurement cycle is zero, we have

$$\frac{V_R}{R_I C_F} T_1 - \frac{v_{log}}{R_I C_F} T_2 = 0\,, \tag{4.12}$$

which simplifies to

$$v_{log} = V_R \frac{N_1}{N_2 + N_k - N_{fs}}. \tag{4.13}$$

If expression (4.11) were to be used for v_{log}, equation (4.13) will be modified to

$$\theta + K_3 = \frac{K_2}{V_R N_1}\left(N_2 + N_k - N_{fs}\right). \tag{4.14}$$

If N_k is chosen such that

$$N_k - N_{fs} = \frac{V_R K_3}{K_2} N_1, \tag{4.15}$$

we find that equation (4.14) simplifies to

$$\theta = \frac{K_2}{V_R N_1} N_2. \tag{4.16}$$

Since V_R and N_1 are pre-determined, time-invariant quantities and k_2 is dependent only on the material of the thermistor, equation (4.16) shows that the measured count N_2 is linearly related to the temperature θ, which the thermistor is subjected to. Thus, theoretically the measurement of temperature is influenced only by the constants, V_R and N_1, which can be accurately set and taken into account in the final display of the result. For example, if $\frac{K_2}{V_R N_1}$ were to be made equal to 1, then N_2 directly indicates θ in ^{o}C or K, as the case may be. N_2 would indicate the temperature in steps of 0.1 ^{o}C or 0.1 K, if $\frac{K_2}{V_R N_1}$ were to be made equal to 10. It can also be seen that equation (4.16) has succeeded in realising what was sought to be achieved by expression (4.7).

While deriving equation (4.16), it was tacitly assumed that the circuit conditions and components were ideal. Any deviations from such idealities would imply corresponding errors in the result indicated by the above expression. The remainder of the chapter is devoted to analysing the sources of such errors and determining their effect on the performance of the circuit. The circuit is simulated for various error conditions, for the entire temperature range of interest from 0 ^{o}C to 120 ^{o}C and the

results are analysed and presented. It is then prototyped in the laboratory to test its practicality.

4.3 Error analysis of the LDC

A glance at equation (4.16) might seem to indicate that the stability of the measured temperature θ, depends only on the fixed quantities V_R and N_1. But, a deeper analysis of the process which led to the formulation of the above expression would show that the success of equation (4.16) depends on a few assumptions that can deviate from the ideal in a practical implementation of the scheme. Some of these assumptions are that the reference voltage V_R and the time period T_1 ($=N_1T_c$) are constant and stable, that the change in resistance of the thermistor is due only to the temperature that it seeks to measure and that none of the opamps or other active devices used in the circuit introduce any offset voltage of their own. Moreover it is also assumed that the comparators and switches used in the circuit are ideal in that they change states instantaneously without affecting the circuit in any other way. In this section, we investigate whether these assumptions are justified and if not, to determine the extent to which equation (4.16) and thereby, the circuit performance is affected.

4.3.1 Stability of the reference voltage V_R

The linearising digital converter for the thermistor is essentially a voltage-to-time converter, where the unknown voltage v_{log} is compared with a standard, reference voltage V_R. Therefore, any uncertainty or instability in V_R is bound to affect the measurement of v_{log} and thereby, the determination of temperature θ. If the reference voltage changes to $V_R+\Delta V_R$, then using this value for V_R in equation (4.12), we find that expression (4.16) is now modified to

$$\theta + K_3 = \frac{K_2}{\left(V_R + \Delta V_R\right) N_1} N_2 . \qquad (4.17)$$

As can be seen, the effect of the change in the reference voltage has only been to introduce a gain error in the above expression for the measured temperature and can be easily compensated for.

Equations (4.16) and (4.17) have been based on the assumption that the reference voltage is time-invariant and remains stable during the measurement interval. Any variation in the magnitude of the reference voltage during measurement will seriously affect the accuracy of the result. This is particularly so in this case for two reasons:

(i) All reference voltages used in the circuit are likely to be derived from the same source and hence, any drift in the magnitude of V_R is bound to effect not only the voltage to which the resistance R_I is connected during the period T_1, but also v_{log} as the currents I_θ and I_{ref} to the logarithmic amplifier are also derived from the same reference voltage. Therefore, any fluctuation in the reference voltage is not only likely to affect θ directly as shown in expression (4.17) but also indirectly by its effect on v_{log}.

(ii) By making use of a logarithmic amplifier, a very large variation in the resistance of the thermistor over the entire range of temperature measured, is compressed to a very small change in v_{log}. For example, a change of more than 65 kΩ over 120 ^{o}C, causes the output of the logarithmic amplifier to vary only by 1 V. As a result, even small errors in v_{log} seriously affect the calculation of temperature, as shown in Table 4.2. This is true especially at higher temperatures when the slope of the R-θ curve of the thermistor ($\Delta R/\Delta\theta$) is much smaller, leading to greater error in the result.

Table 4.2 Variation in temperature with v_{log}

Nominal θ (^{o}C)	**Measured θ (^{o}C)**	
	v_{log}+ 5 mV	**v_{log} - 5 mV**
0	-0.3	+0.3
60	59.6	60.4
120	119.5	120.5

One of the major reasons for the fluctuations in reference voltage is improper grounding. Even minor variations in ground potential which would otherwise not have serious consequences can destroy the efficacy of this circuit. It has to be ensured that ground potential remains within a few tens of microvolts through standard grounding practises, like connecting all ground points to the same potential and having a ground plane on a PCB. Use of separate standard reference voltage diodes, with stabilities of parts per million and resistances with tight tolerances, for deriving the reference voltages $\pm V_R$ and reference currents for the logarithmic amplifier ensures that errors due to fluctuations in the reference voltage remain well within limits.

4.3.2 Stability of the fixed time interval T_1

As in a conventional dual slope analog to digital converter, the integrator in the proposed circuit is connected to the reference voltage $-V_R$ for a fixed duration T_1. At the end of the period, the output voltage of the integrator v_{oi}, would be $\frac{V_R}{RC_F}T_1$. If the time period T_1 is in error by an amount ΔT, then the integrator output would read $v_{oi} = \frac{V_R}{RC_F}\left(T_1 + \Delta T\right)$, which indicates that the measurement of T_2 would now be in error by an amount equal to $\frac{V_R}{v_{log}}\Delta T$. Since V_R and v_{log} are of the same order of magnitude, the error in T_1 has a direct impact on the measurement of T_2 and thereby, on the temperature θ. This error can be minimised by ensuring that ΔT is very small when compared to T_1 and can be nullified by proper calibration.

On the other hand, it is essential that, once the circuit is calibrated for a particular value of the time period, T_1 remains invariant, at least over the duration of the measurement cycle. Therefore, it is the stability of the time period which is of concern, rather than the accuracy of T_1. Use of accurate timing circuits and phase locked loops in

the derivation of the time period as well as the use of components that have very good stability will ensure that the value of T_1 remains fixed.

4.3.3 Error due to self-heating of the thermistor

When discussing the operation of the circuit, it was assumed that the change in resistance of the thermistor was solely due to the temperature that the device was seeking to measure. This assumption is not entirely valid, because the measurement of thermistor resistance is accomplished by electrically exciting it. As a result, there is a small amount of local heating due to the i^2R effect, which could degrade the performance of the circuit, unless carefully designed for. Self-heating is normally specified by the dissipation constant, which indicates the amount of power in milliwatts, required to raise the temperature of the thermistor by 1 K. A thermistor excited by a constant voltage source could introduce significant errors due to self-heating, when its resistance decreases at higher temperatures. For example, the NTCS0603E3223FMT thermistor from Vishay Electronics, which has a dissipation constant of 3 mW/K [83], when excited by a 1.5 V source, would introduce an error as large as 1 ^{o}C, when measuring a temperature of 120 ^{o}C. The error due to self-heating can be minimized by limiting current through the thermistor or by choosing a thermistor with a large dissipation constant, if the former choice cannot be availed of for reasons of sensitivity.

4.3.4 Delays caused by the comparator and switch

During the discussion on the operation of the circuit, it has been assumed that the comparator would change states instantaneously when the integrator output changes polarity. Similarly, it was assumed that the switch would respond immediately to the change of status of its control lines, A_1 and A_2. In actual practice, both the comparator as well as the switch would take a finite amount of time to respond to changes in their inputs. If the delay due to the comparator is denoted by τ_c and that caused by the switch

as τ_s, then the effect of such delay would be that the voltage v_{log}, instead of being switched to the fixed resistance at time T_1, would now be connected only at $(T_1 + \tau_c + \tau_s)$. Therefore, the capacitance would charge from the reference voltage $-V_R$ for a duration $(\tau_c + \tau_s)$ longer than necessary. This acquired charge would also have to be discharged during the measured time period T_2. Therefore, equation (4.12) would stand changed to

$$\frac{V_R}{R_I C_F}\left(T_1 + \tau_c + \tau_s\right) - \frac{v_{log}}{R_I C_F} T_2 = 0 . \tag{4.18}$$

This expression would reduce to equation (4.12) if $\frac{\tau_c + \tau_s}{T_1} \ll 1$. In other words, if the total delay caused by the comparator and switch is very small when compared to the fixed time period T_1, the errors caused by such delays can be considered to be negligible. For comparators like the LM311 which was used in the prototype or the switch HCF4052, the maximum delay would be 200 ns and 60 ns respectively, which are very small in comparison to the normal value of 100 ms used for T_1.

4.3.5 Error caused by offset voltage of the opamp and log amplifier

The offset voltage of the opamp used in the integrator has the effect of adding to or subtracting from the total charge gained by the feedback capacitor during T_1, depending on the polarity of the offset voltage. Its action is therefore similar to that of the change in the reference voltage V_R, described in Section 4.3.1. For high accuracy measurements, it is therefore necessary that opamps with low input offset voltages be used or appropriate steps taken to trim the offset voltages using external circuitry. The offset voltage of the log amplifier also has a similar effect. If the error produced by the input offset voltage of the amplifier is not acceptable, then its' effect should be minimized by the use of a low-offset opamp like the OPA335 [84].

Since the magnitude and polarity of the offset voltages are not known *a priori*, it

is not possible to account for their effects in measuring the temperature and hence, the results could be in considerable error, if high accuracy is required. The effects would be more noticeable at higher temperatures and with lower values of the reference voltage. We will then have to compensate the entire circuit for the offset voltages by a proper calibration at the beginning of the measurement process. Table 4.3 shows the effect of such compensation for a range of temperature from $0\ ^{o}C$ to$120\ ^{o}C$ and for

Table 4.3 Effect of compensation on the output

θ		V_R = 1 V				V_R = 0.1 V			
Set (K)		273.15	298.15	333.15	393.15	273.15	298.15	333.15	393.15
Measured (K)	W/o comp.	273.86	298.95	333.91	394.01	274.25	299.27	334.31	394.40
	With comp.	273.62	298.60	333.57	393.54	273.89	298.59	333.48	393.29
Error (K)	W/o comp.	0.71	0.80	0.76	0.86	1.10	1.12	1.16	1.25
	With comp.	0.47	0.45	0.42	0.39	0.74	0.44	0.33	0.14

two values of the reference voltage V_R. The unshaded parts of the table indicate the temperature measured as well as the deviation from the set temperature, when the circuit was not compensated for the offset voltage of the log amplifier and the opamp. As can be seen, the value of the measured temperature tends to drift more from the true value at higher temperatures and for a lower value of V_R in the case of the uncompensated circuit.

4.3.6 Effect of the switch performance

In the discussion so far, it has been assumed that the switch used for connecting the resistance R_I to the different reference voltages and v_{log}, has no effect on the circuit operation other than to introduce a delay τ_s, as discussed in Section 4.3.4. It was assumed that the switch does not introduce any additional resistance into the circuit. This assumption is not quite valid in practice. Quite a few of the commercially available analog SPDT switches and multiplexers like the MAX333 [85] and the HCF4052 have typical switch ON resistances, designated as $R_{ON,}$ in excess of 100 Ω and a few of them

in excess of 250 Ω [86]. This would cause a significant deterioration in the circuit performance, as the input to the voltage to time converter is now less than the exact value required for the accurate measurement of the temperature. As has been explained in the previous sections, a discrepancy of even a few millivolts is sufficient to cause significant error in the output. This is illustrated quite clearly by Table 4.4, which shows the voltages recorded at some of the cardinal points of a partially compensated version of the proposed circuit. In the table, v_1 represents the reference voltage that is actually switched to the fixed resistance R_I. As can be seen, v_1 is in error from the true value of –1 V by ~ 10 mV, sufficient to cause the error seen in the final value.

Table 4.4 Output at salient points of the circuit for different temperatures

	V_R = 1 V			
Set θ (K)	273.15	298.15	333.15	393.15
v_{log} (V)	4.826	4.343	3.776	3.019
v_1 (V)	-0.989	-0.989	-0.989	-0.989
v_2 (V)	2.408	2.168	1.885	1.508
T_1 (ms)	99.84	99.84	99.85	99.84
T_2 (ms)	41.02	45.58	52.42	65.52
Estimated v_2 (V)	2.408	2.167	1.885	1.508
Estimated R (Ω)	65416.8	21594.2	5878.6	1035.7
Estimated θ (K)	273.62	298.60	333.57	393.54

This error can be overcome by making use of low offset voltage buffers at the output of the switch or by making use of switches with low ON resistance like the MAX4680, with an R_{ON} of 1.25 Ω or the MAX4734 and the MAX4735 with values of R_{ON} less than 1.0 Ω.

As shown in Table 4.4, the maximum error in the output of the circuit, even with partial compensation is about 0.4 % of the full scale. When all the modifications and improvements as suggested above are implemented, it is expected that the circuit performance will improve further. The results obtained when the circuit was simulated as well as those from the experiments conducted on the prototype are now presented.

4.4 Simulation studies on the proposed LDC

The design of a prototype from a circuit is made much simpler if it is possible to study it under a variety of simulated conditions. Appropriate measures can then be taken to trim various parameters of the circuit to obtain optimum performance without having to prototype the circuit each time a change is made. Therefore, the proposed linearising digital converter for thermistors was simulated and its performance studied under various conditions before it was set up in the laboratory. The simulation package chosen was PSpice from the OrCAD suite of software (v 16.2) from M/s Cadence Corp. OrCAD-PSpice was chosen not only for the highly user-friendly graphical interface that it provides to the familiar PSpice program but also for the extensive range of device models available in the PSpice libraries and for its relatively economical use of system resources.

The circuit chosen for simulation was essentially the one displayed in Fig. 4.4, with a few modifications to accommodate the fact that some of the parts displayed in the figure do not lend themselves to simulation with PSpice. The OP97 was chosen for the integrator while the LM311 was used as the comparator. Since the PSpice model of the HCF4052 switch was not available, the ADG508 from M/s Analog Devices was made use of. The LOG112 from M/s Texas Instruments was used for the logarithmic amplifier. The timing and control unit consisting of the BNC2120, USB-6251 and the PC was replaced by simple digital gates, generating the logic necessary for initiating and controlling the switching of the various voltages to the fixed resistance R_I. The clock was modelled as a simple digital stimulus running at 1 MHz, while the fixed time period T_1 was chosen as 100 ms and generated using the popular timer IC, NE555. The resistance of the thermistor R_θ, was replaced by a variable resistance, modelled using the expression and coefficients provided by M/s Vishay Electronics for their SMD0603

– Glass encapsulated series of negative temperature coefficient thermistors.

The simulation was run with G_{min} stepping to improve the speed of convergence, on a notebook computer with an Intel Pentium (M) processor running at 1.7 GHz and having 2 GB of RAM. To facilitate the early convergence of the simulation, the best accuracies of the calculated voltages and currents were chosen to be 10 μV and 100 pA respectively. The simulation was run for two values of the reference voltage, namely, 1 V and 100 mV. The circuit was simulated so as to reflect all the errors discussed in Section 4.3 above. A deviation of 1 % in the magnitude of the reference voltage from its design value was intentionally introduced. The offset of the logarithmic amplifier was also not properly compensated. The temperature was varied from 0 ^{o}C to 120 ^{o}C, in steps of 5 ^{o}C.

The outputs at three significant points were studied – (i) the timer, (ii) the comparator and (iii) the integrator. A screenshot of the simulation output during one of the runs is shown in Fig. 4.5, where v(timer) and V(COMP_1) are the outputs of the timer and the comparator respectively. As is clear from Fig. 4.5, the time period to be measured T_2 is the interval between the falling edges of the signals v(timer) and V(COMP_1). T_2 was automatically measured and plotted against temperature. The temperature was then calculated and compared with the set value, to determine the deviation of the circuit from the ideal, under less than ideal conditions. The results are plotted in Fig. 4.6 and as can be seen, the measured temperature is in error from the actual value by not more than ± 0.12 %, over the entire range of 120 ^{o}C, thereby validating the theoretical analysis of the previous sections as well as justifying the prototyping of the circuit.

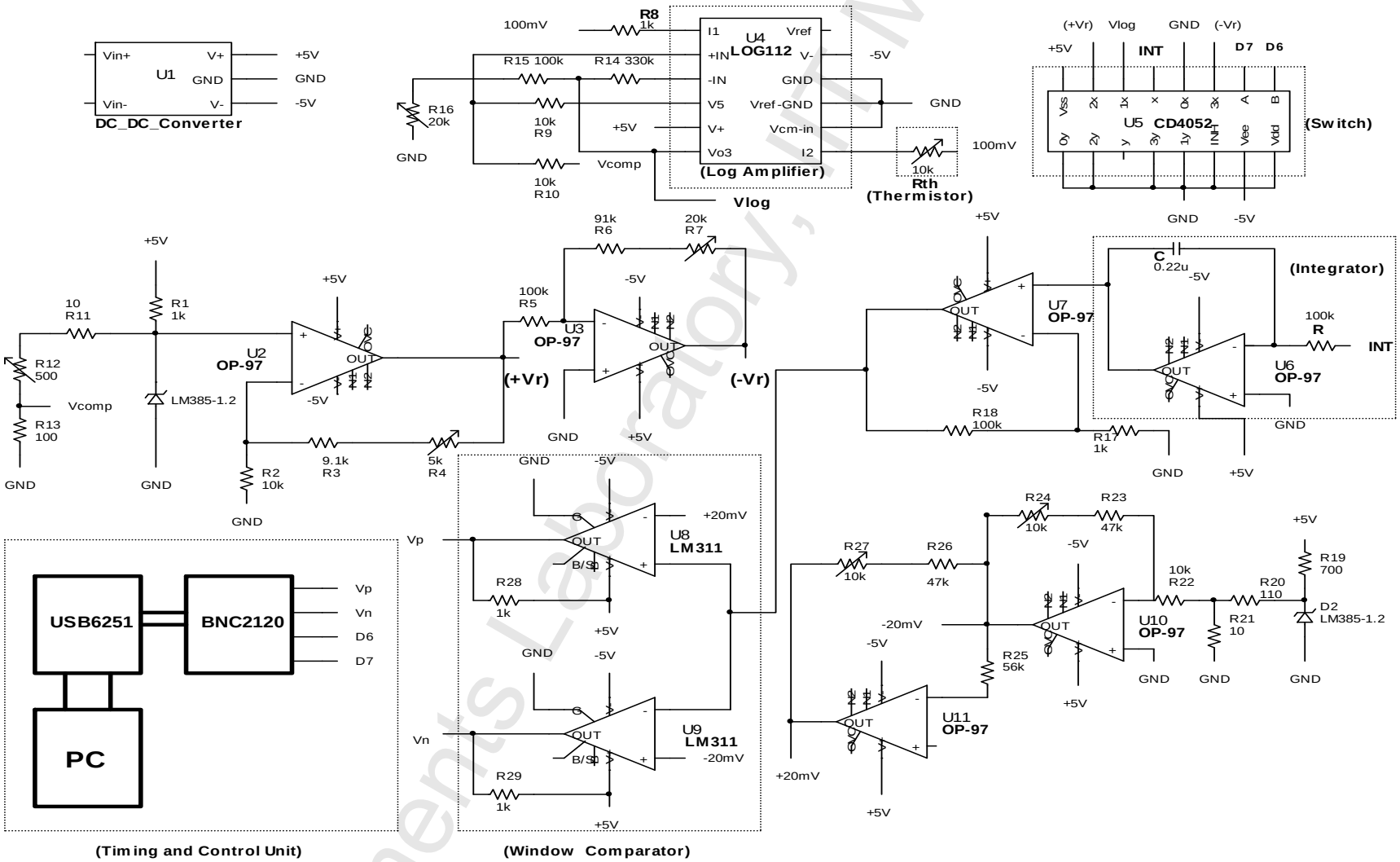


Fig. 4.4 Circuit schematic of the proposed linearising digital converter for the thermistor

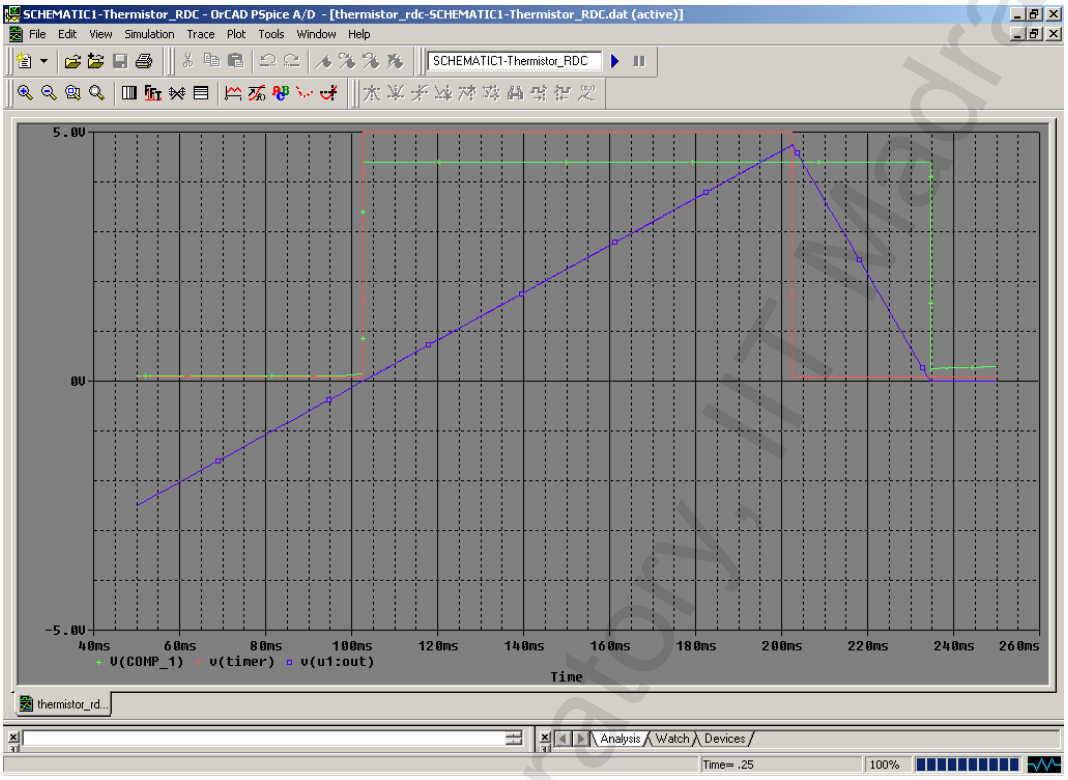


Fig. 4.5 Screenshot of a simulation run of the proposed circuit

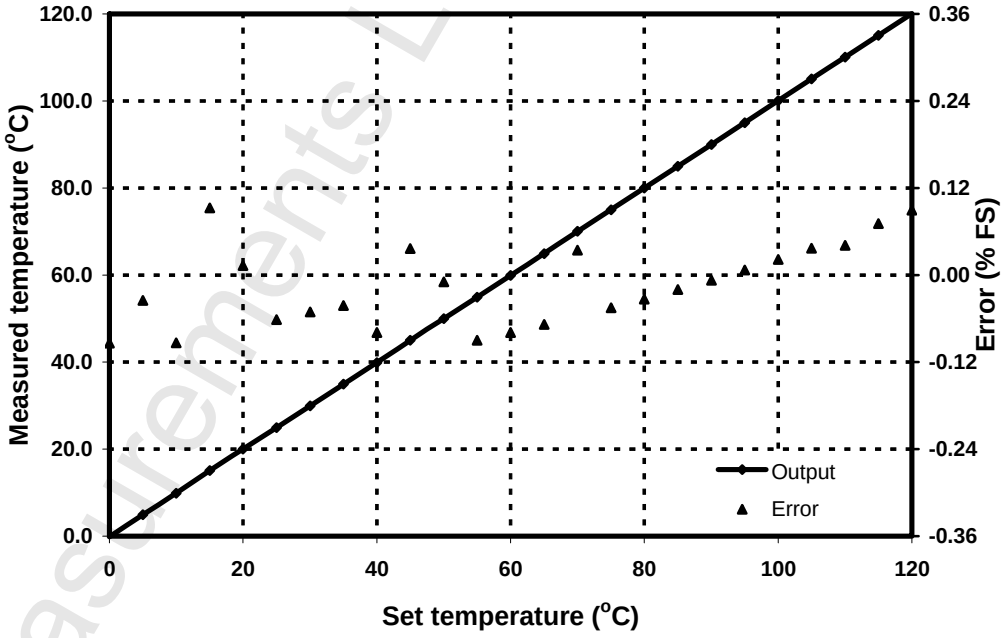


Fig. 4.6 Results of the PSpice simulation of the proposed circuit

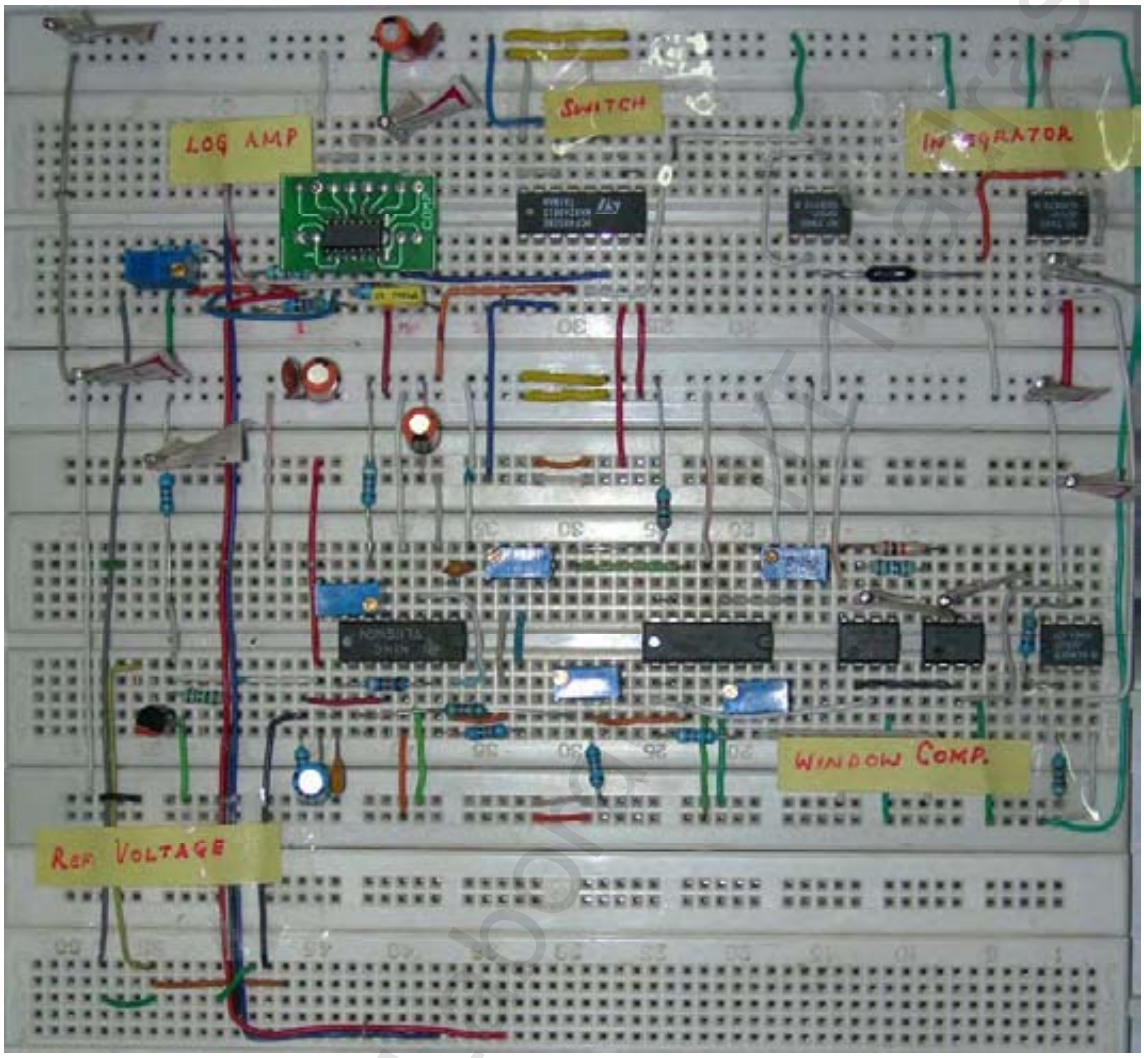


Fig. 4.7 Photograph of the prototype linearising digital converter for thermistors

The next section explains the experimental verification of the proposed LDC and discusses the results which are presented.

4.5 Experimental results

The circuit schematic of the proposed LDC for a thermistor, shown in Fig. 4.4, was set up on a prototyping board in the laboratory, as shown in the photograph of Fig. 4.7. The power supply, thermistor, the feedback capacitor of the integrator and the timing and control unit were housed separately from the breadboard.

The entire circuit was powered by the AEE01AA36, a 5 V DC/DC converter from M/s Astec Power. The reference voltages of ± 1 V and ± 100 mV were derived using the

LM385-1.2 voltage reference diodes and precision resistances. The LOG112 from M/s Texas Instruments was chosen for use as the logarithmic amplifier not only for the high accuracy and precision it provides over a wide dynamic range but also for its low offset voltage and temperature drift. More importantly, the LOG112 provides an output scaling amplifier, which simplifies the task of compensating the logarithmic amplifier. With its low offset voltage and bias currents, the OP97 was an easy choice for use in the integrator. The comparator was built using the LM311 while the HCF4052 was used as the switch to connect the resistance R_I to the various voltages. Power supplies including the derived ones were bypassed to ground with 10 μF and 0.01 μF capacitances. All ground lines were connected to one single point, whose potential was continuously monitored to ensure that it was within ± 50 μV of power supply ground.

The thermistor used in the prototype was the NTCS0603E3223FMT from the SMD0603 series of glass encapsulated NTC thermistors manufactured by M/s Vishay Electronics. It was carefully calibrated in the range of 0 ^{o}C to 120 ^{o}C using the MP40R [87] and MTC650 [88] temperature calibrators from M/s Nagman Instruments, India, which are certified to be within ± 0.6 ^{o}C of the set temperature. The resistance of the thermistor was noted for increasing as well as decreasing values of temperature using the 34401A, a 6½ -digit multimeter from Hewlett-Packard. These measured values of the thermistor resistance were then plugged into the prototype circuit using precision decade resistance boxes, with an accuracy of ± 0.01 %, from M/s Otto-Wolff, Germany.

The timing and control unit (TCU) was built on a Virtual Instrument platform, around the hardware and software products from M/s National Instruments. The outputs of the window comparator were made TTL-compatible and connected to two of the digital I/O lines of the USB-6251, which were configured as input lines. The USB-6251 Data Acquisition Device (DAQ) from National Instruments was interfaced to the circuit

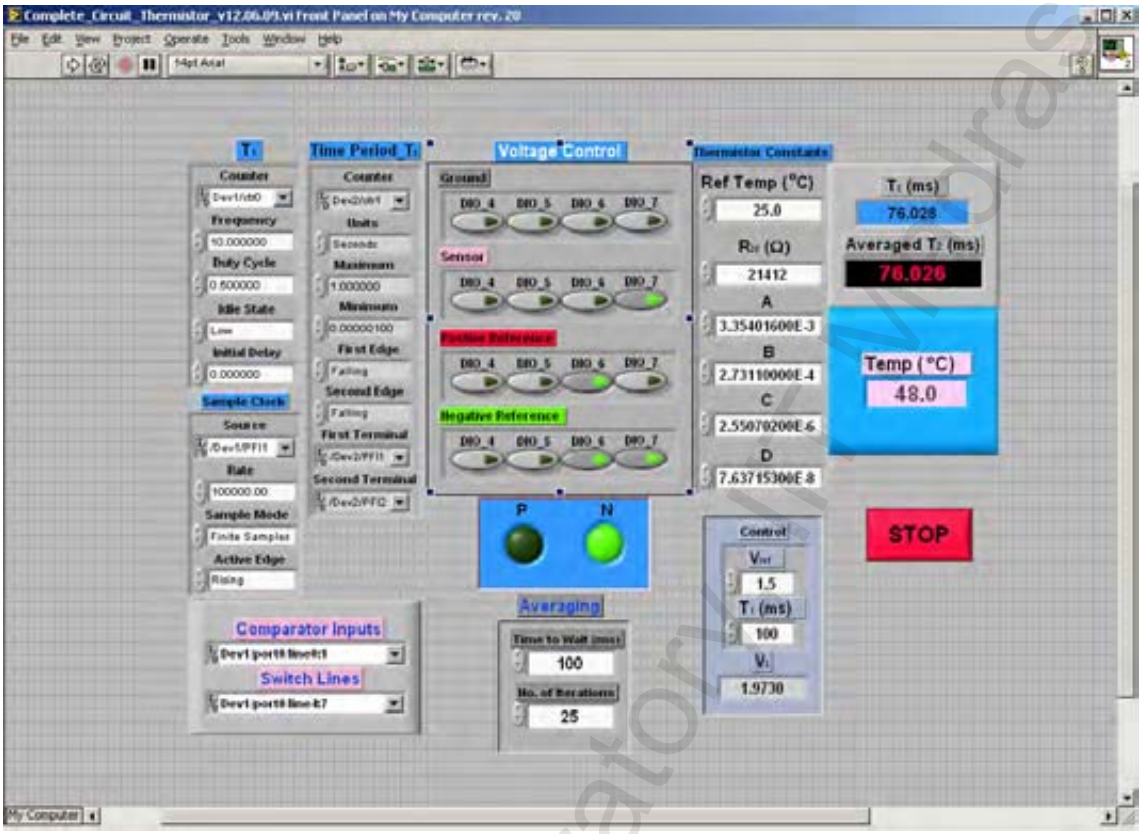


Fig. 4.8 Screenshot of the front panel of the Virtual Instrument developed for the Timing and Control Unit

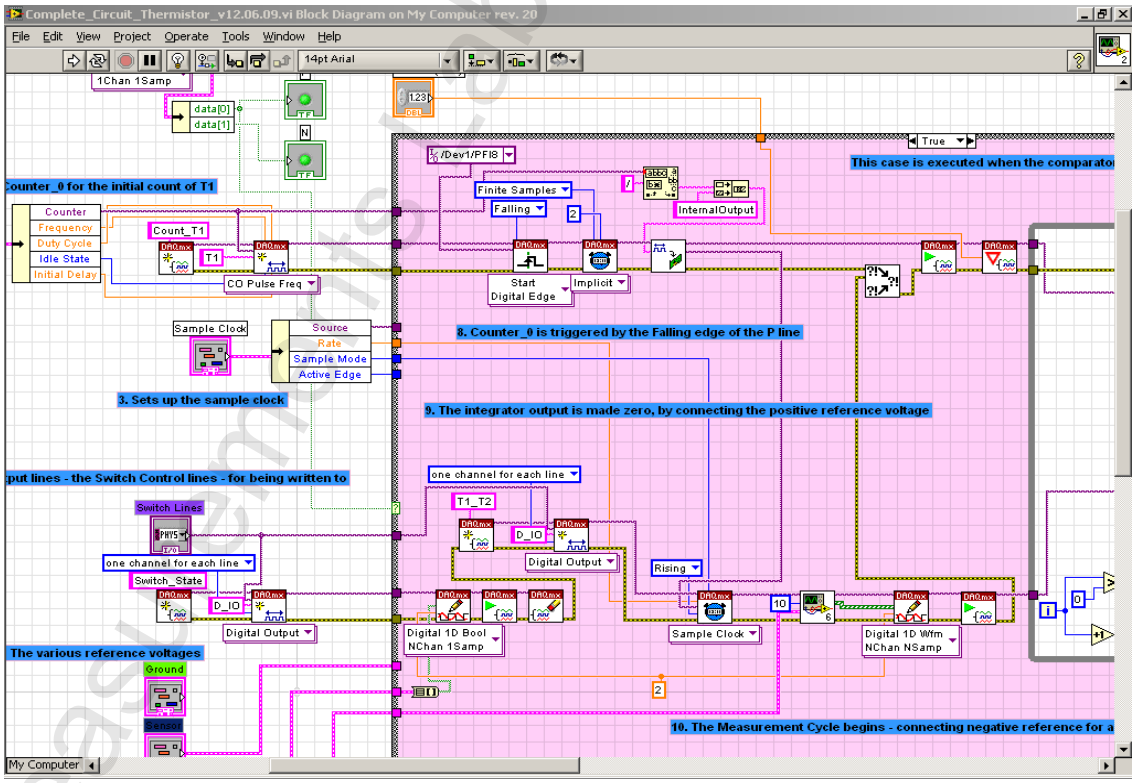


Fig. 4.9 Screenshot of part of the block diagram of the Virtual Instrument developed for the Timing and Control Unit

through the BNC2120 accessory. Another pair of the digital I/O lines of the DAQ were used as the control lines A_1 and A_2 for the switch, S_1. The logic for the auto-zero and conversion phases of the measurement cycle was implemented using a program written in LabVIEW. The front panel of the virtual instrument (VI) developed for this purpose is shown in Fig. 4.8 while a part of its block diagram is displayed in Fig. 4.9. One of the 32-bit, general purpose counter-timers of the DAQ was used to generate a highly stable and precise pulse train for the fixed time duration T_1. This is configurable from the front panel of the VI and hence can accommodate different values of the fixed resistance R_I and the feedback capacitance C_F. At the beginning of the measurement cycle, the polarity of the comparator lines is checked based on which the required reference voltage is switched to the resistance R_I, to ensure that the output of the integrator (v_{oi}) goes to zero.

The positive line of the comparator is used to check the status of the integrator output. Any transition in the status of this line indicates the end of the auto-zero phase. This transition triggers the counter to generate T_1 as well as to output '11' on the control lines A_1, A_2 so as to switch $-V_R$ to the resistance R_I. The rising edge of the pulse train at the end of T_1 serves as the trigger for another counter of the DAQ to start the measurement of T_2. The program logic also recognises this rising edge to change the status of the A_1 and A_2 lines to '01', which causes the switch to connect v_{log} to R_I, making the integrator output go to zero. The change in polarity of v_{oi} is marked by a transition of the comparator from high to low, indicating the end of the measurement phase. The falling edge of A_1 at the end of T_1 and the falling edge of the comparator at the end of T_2 serve as markers for the counter measuring T_2. The 32-bit counters of the USB-6251 have a resolution of 50 ns and hence, can measure the time period very accurately.

During the entire process, the reference voltages as well as the output of the logarithmic amplifier were continuously monitored using highly accurate multimeters from M/s Keithley (Model 2100) and Hewlett-Packard (34401A). The voltages at critical points of the circuit were also monitored using the DL750P Scopecorder from M/s Yokogawa. A snapshot of the waveforms during one of the runs is given in Fig. 4.10. Channels 1 and 2 display the voltage connected to R_I and v_{oi} respectively, while the digital I/O line A_1 is shown on Channel 3. The output of the positive line of the window comparator is recorded on channel 4 and the negative line is captured on channel 5. Channel 6 indicates the pulse train generated by the counter of the USB-6251.

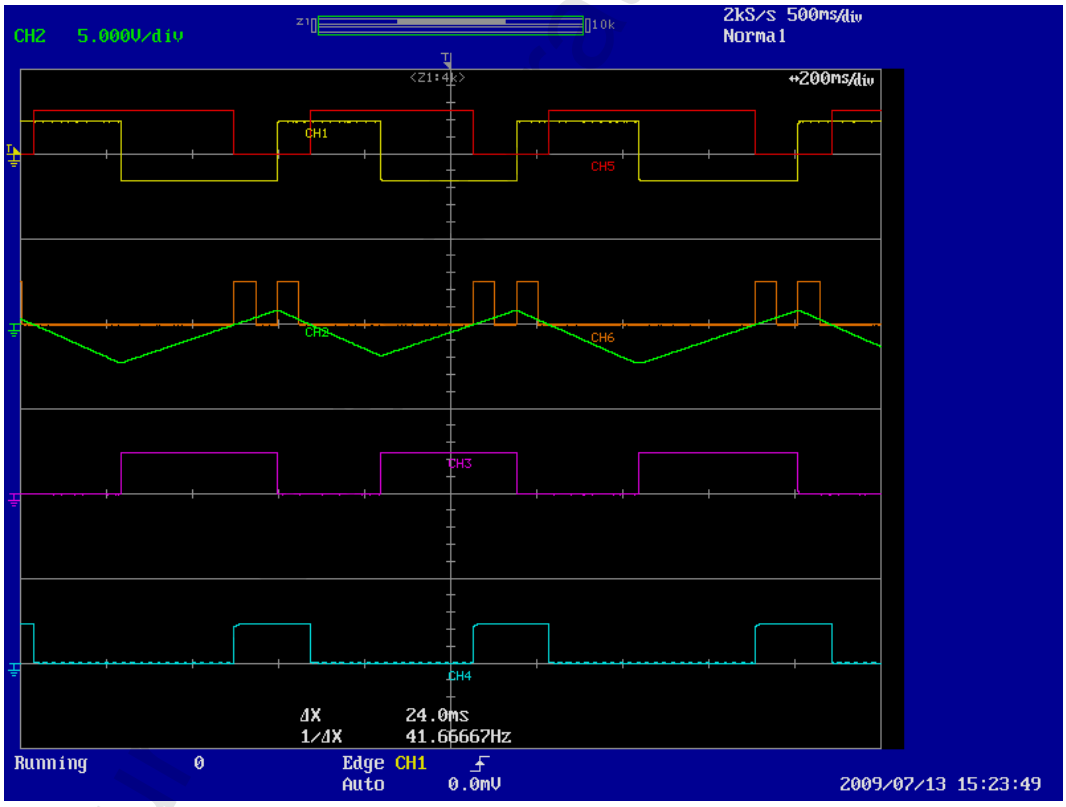


Fig. 4.10 Voltage waveforms at the cardinal points of the circuit

The resistance of the thermistor at a temperature of 25 ^{o}C as determined by the calibration done earlier, was set using the precision resistance boxes and the circuit was

carefully compensated. The virtual instrument was then executed to determine the value of T_2. Each measurement was repeated ten times to take care of any random errors. Based on this value of T_2, v_{log} was calculated using equation (4.13), from which the temperature was determined by making use of the coefficients provided by the manufacturers. The measured temperature along with the associated errors is plotted against the actual temperature of the thermistor, in Fig. 4.11. The figure shows the

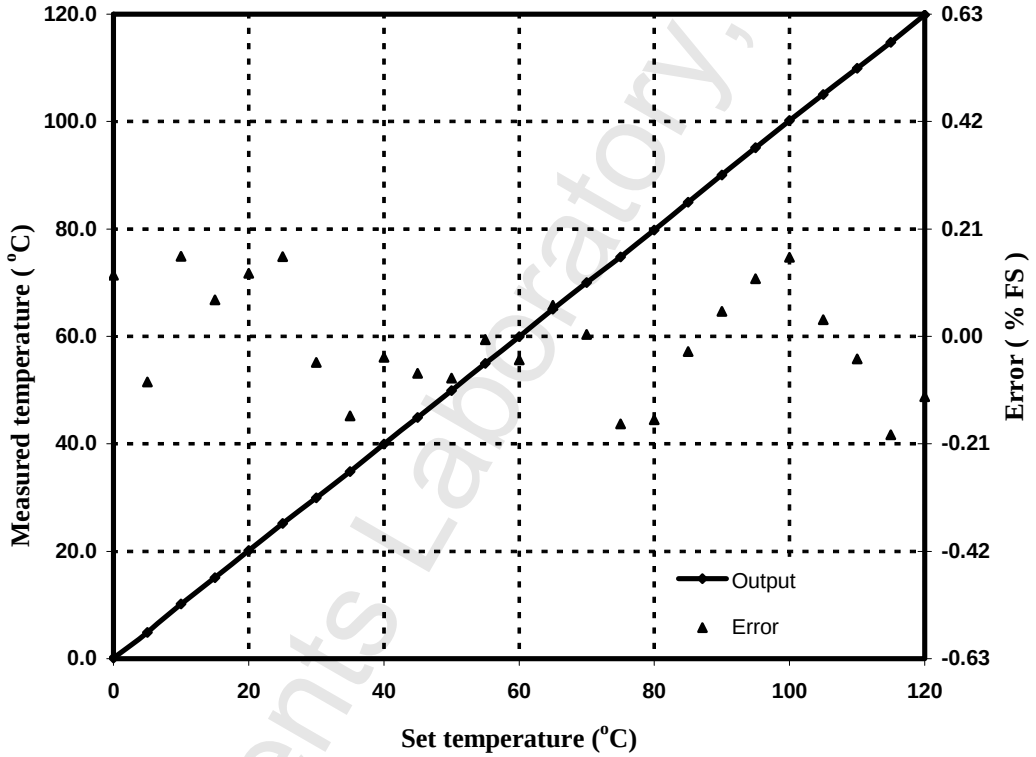


Fig. 4.11 Performance of the prototype in the temperature range 0 °C to 120 °C

performance of the proposed LDC for a temperature range from 0 °C to 120 °C, in increments of 10 °C. The maximum error over the entire range was found to be less than ± 0.2 %. The experiment was repeated for temperatures in the range from 30 °C to 50 °C, with smaller increments of 1 °C to check the resolution of the system. The results which are displayed in Fig. 4.12 indicate an even better performance, with a maximum

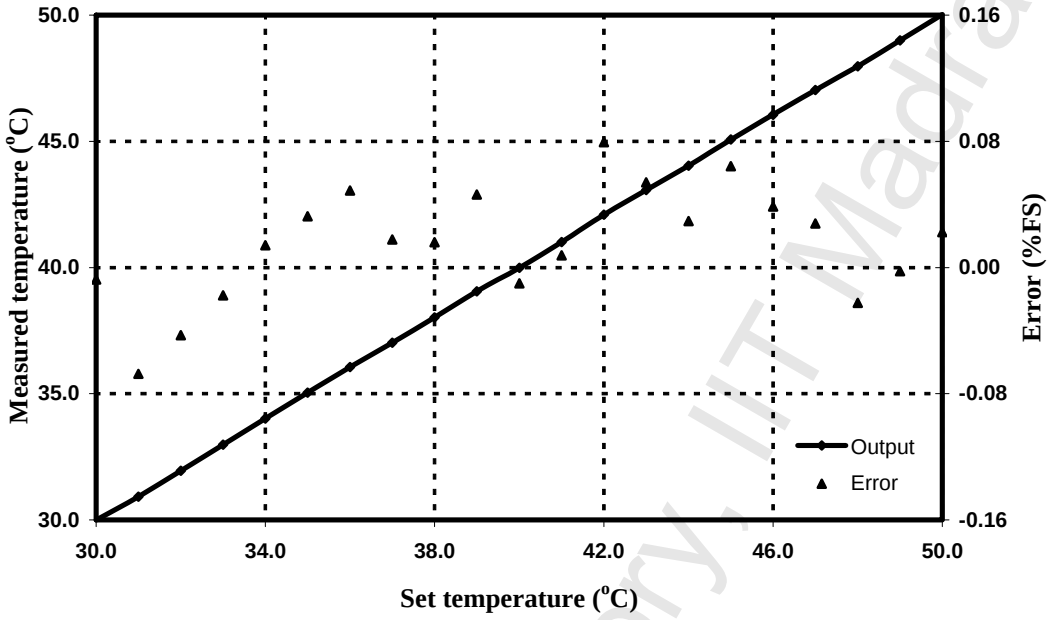


Fig. 4.12 Performance of the prototype in the temperature range 30 °C to 50 °C

full scale error of less than ± 0.1 %. As the figures illustrate, the performance of the proposed circuit closely matches the results predicted by simulation.

4.6 Summary

A circuit which not only linearises the typical, inverse-exponential, *R-θ* characteristic of the thermistor but also provides a digital output proportional to the temperature has been presented in this chapter. The circuit has been analysed for various possible sources of errors and their effects on the performance of the circuit. The proposed LDC was also simulated to study its performance under controlled conditions with various non-idealities incorporated. It was then prototyped and its response studied. It was found that the circuit functioned as expected and produced results which justify its use with thermistors for the accurate and reliable measurement of temperature, with a maximum error of ± 0.3 °C, over the range from 0 °C to 120 °C.

The linearisation and digitisation procedures discussed so far in this work, dealt with single-element resistive sensors. Resistive sensors like strain gages are normally

operated in the differential mode, where the resistance of one element increases due to the variation in the measurand, while the resistance of the other element decreases by the same amount. In the next chapter, a circuit for digitizing the output of such a differential resistive sensor is presented and analysed.

5. Dual Slope Resistance to Digital Converter for a Differential Resistive Sensor

5.1 Signal conditioning for differential resistive sensors

As discussed in chapter 1, a differential type resistive sensor is often preferred over the single element type for reasons like increased sensitivity and reduced nonlinearity. It consists of two separate resistive elements, one of which increases with the change in the measurand while the other decreases by the same amount. The expressions governing the output characteristics of such a sensor are given in equation (1.5) for a sensor possessing a linear characteristic and in equation (1.6) for one with an inverse characteristic. The dual slope resistance to digital converter described in Chapter 3, which provides a linear digital output for a single element resistive sensor, cannot be directly employed with a differential resistive sensor.

Some of the earlier attempts to obtain direct digital converters for differential sensors resulted in capacitance or resistance to frequency / time period converters [89]-[92]. To interface such transducers possessing a quasi-digital output to a digital instrumentation system, a counter-timer block is necessary. Owen has proposed a direct resistance to digital converter (RDC) suitable for a differential type resistive sensor [39]. Owen's method has the advantage of having built-in offset compensation but requires four integration periods, achieved with a double dual-slope structure. Moreover, as his method involves the subtraction of a measured time interval from another similar measured quantity, large systematic errors may result when the difference between the two intervals is very small. An improved direct resistance to digital converter for differential type sensors that avoids subtraction and employs only three integrations instead of the four required in Owen's method has also been

proposed [40] but does not incorporate offset compensation. In this method, two additional integration periods are necessary for offset compensation, thereby slowing down the process.

An improved dual slope, direct resistance to digital converter (DSRDC) suitable for use with differential resistive sensors is discussed in this chapter. It requires only two integrations and hence is faster than either Owen's technique or the triple slope method. Moreover, since the proposed method employs the dual slope principle, it possesses all the attendant advantages [93].

5.2 The proposed DSRDC for a differential resistive sensor

As mentioned earlier, a typical differential resistive sensor will contain two resistive elements, say, R_1 and R_2. In the proposed dual slope RDC, R_1 and R_2 become a part of the integrator in a suitably modified dual slope integrating type digital converter as shown in Fig. 5.1. The integrator is realized using an opamp (OA) with a capacitor C_F inserted in its feedback path. S_1 and S_2 in Fig. 5.1 are single-pole, double-throw (SPDT) analog switches operated by a timing and control unit (TCU). The TCU consists of a logic unit that determines the sequence of operations to be carried out and a counter-timer to obtain a pre-set time period as well as measure an elapsed time interval. If the differential resistive sensor is a four terminal one as in Fig. 1.3a, then one terminal each of R_1 and R_2 are tied together. The common terminal thus formed or the common terminal in a three-terminal differential resistive sensor (Fig. 1.3b), is connected to the inverting input of the opamp OA. The free end of R_1 is connected to either of two reference voltages $-V_u$ (position 1) or $+V_d$ (position 2) depending on the status of A_1, which acts as the control signal to S_1. The switch S_1 is at position 1 when A_1 is '0' (digital low) and at position 2 when A_1 is '1' (digital high). Similarly, S_2 connects either $-V_u$ or $+V_d$ to the free end of R_2 depending on its control signal A_2.

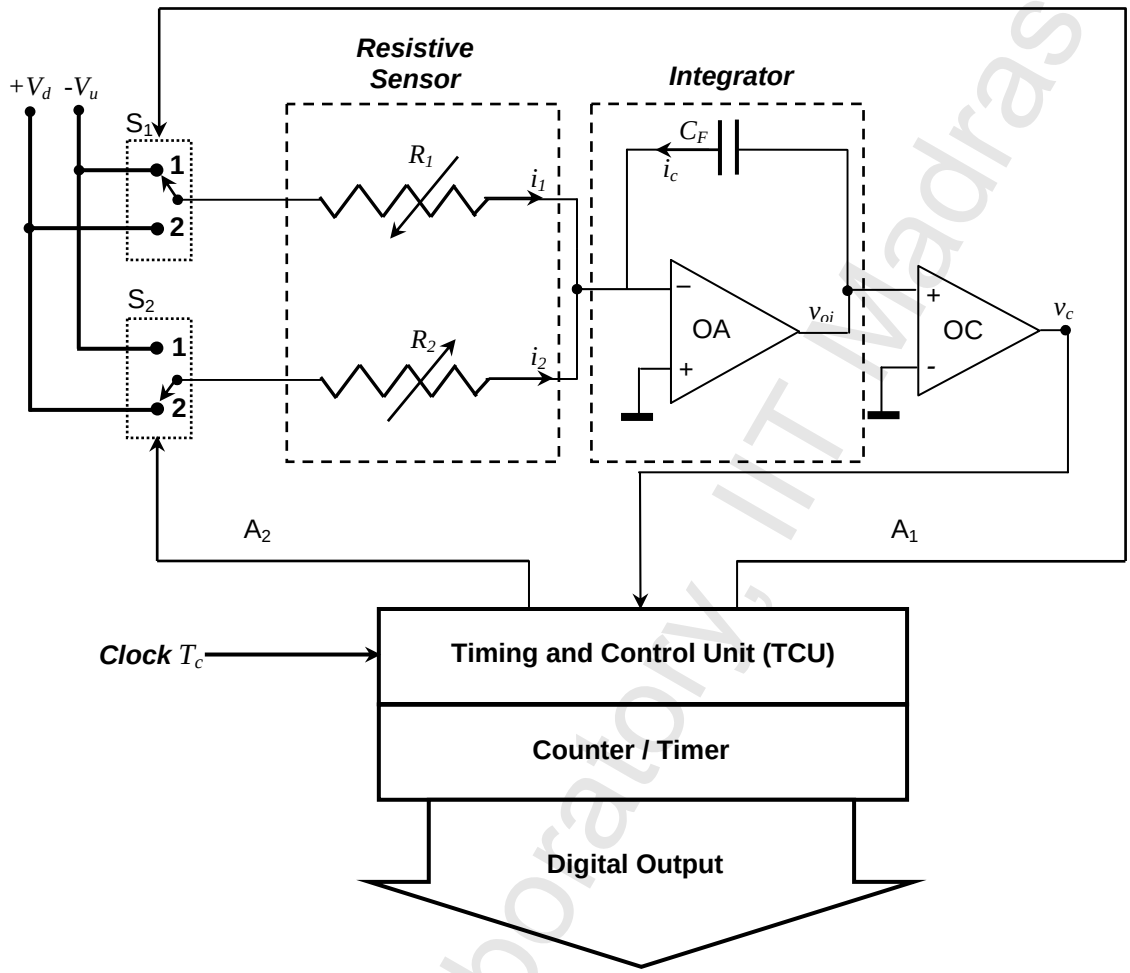


Fig. 5.1 Schematic representation of the proposed Dual Slope Resistance to Digital Converter for a differential resistive sensor

$+V_d$ and $-V_u$ are two stable reference dc voltages, equal in magnitude but of opposite polarity.

The output of the integrator (v_{oi}) - is fed to a comparator which functions as a zero-crossing detector. The comparator output (v_c) serves as an input signal to the TCU. If the output of the integrator is zero or positive ($v_{oi} \geq 0$) then v_c would be high; else, it will remain low. The control unit is designed to sense v_c and sequence two integration periods by providing the necessary control signals A_1 and A_2 to the switches S_1 and S_2, based on the status of v_c, thus obtaining a digital output directly proportional to the measurand. Here too, as in the conventional dual slope technique, the sequence is an initial auto-zero phase followed by the conversion phase which consists of two

integrations. The first is carried out for a fixed interval of time while the time duration of the second integration is measured as the output.

5.2.1 Auto-zero phase

A typical conversion (first integration) starts after ensuring that the output of the integrator (and thereby the charge on the capacitor C_F) is zero. This is achieved in the auto-zero phase. The flow chart for the implementation of this phase is shown in Fig. 5.2.

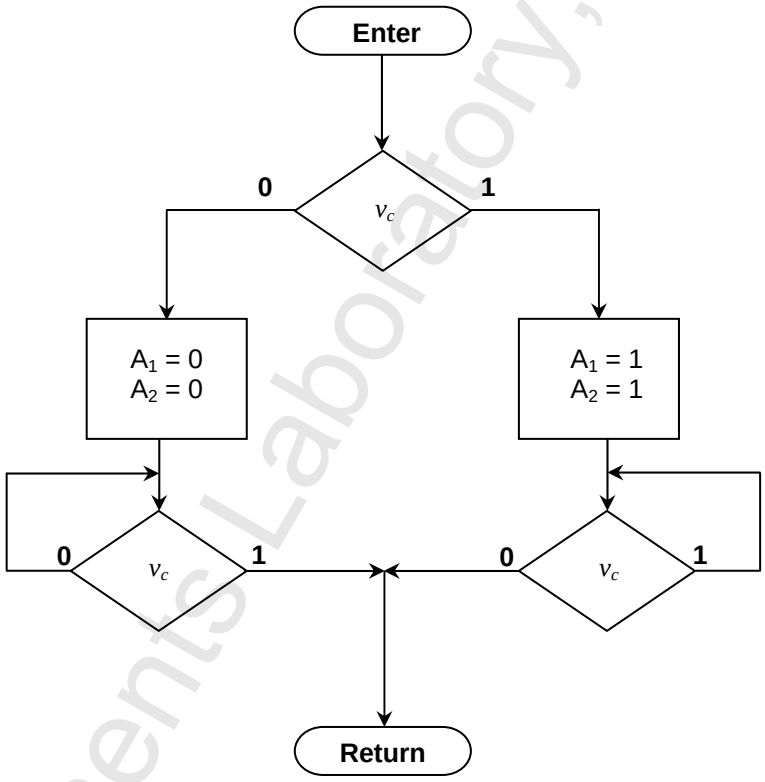


Fig. 5.2 Flowchart for the auto-zero phase

During this period, the TCU senses the comparator output v_c. If v_c is high, both S_1 and S_2 are set to position 2, by making A_1 and A_2 go high. R_1 and R_2 are connected to $+V_d$, making the integrator output ramp down to zero. If, on the other hand, v_c is low, indicating that the polarity of the output of the integrator is negative, control lines A_1 and A_2 go low, setting both S_1 and S_2 to position 1. The integrator output is then forced

to ramp up towards zero, as R_1 and R_2 are connected to $-V_u$.

In either case, the integrator output becoming zero would be indicated by a transition of the comparator output (high to low in the former case and low to high in the latter). This marks the end of the auto-zero phase and the start of a conversion phase. The waveforms at the output of the integrator during this phase are clearly shown in Fig. 5.3 and Fig. 5.4 by dotted lines, to the left of $t = 0$.

5.2.2 Conversion phase

A typical conversion phase, as indicated in Fig. 5.3 and Fig. 5.4, consisting of two integration periods, starts when the integrator output is sensed to be zero. First, A_1 goes low, setting S_1 to position 1 which connects R_1 to the reference voltage $-V_u$. Simultaneously, A_2 goes high, switching S_2 to position 2 and connecting voltage $+V_d$ to R_2. This condition is maintained for a pre-set period of T_1, where T_1 is an integral multiple of the time period of the clock (T_c) given to the timing and control circuit (TCU). i.e.

$$T_1 = N_1 T_c \tag{5.1}$$

During T_1, the current $i_c \left[= \left(\frac{V_u}{R_1} - \frac{V_d}{R_2} \right) \right]$ is injected into the feedback capacitor C_F by the opamp OA. If the measurand (kx) is positive, then $R_1 < R_2$ and hence, i_c would be positive. Capacitor C_F would be charged with the terminal connected to the output of the opamp OA acquiring a positive polarity. The opamp output will ramp up at a rate, $\frac{1}{C_F}\left(\frac{V_u}{R_1} - \frac{V_d}{R_2} \right)$. Hence, at the end of T_1, the integrator output will be positive and the output of the comparator (v_c) will be high as shown in Fig. 5.3.

On the other hand, if kx is negative, it is easily seen that during T_1, the opamp output will ramp down as $\frac{V_u}{R_1} < \frac{V_d}{R_2}$. Therefore, at the end of T_1, the integrator output

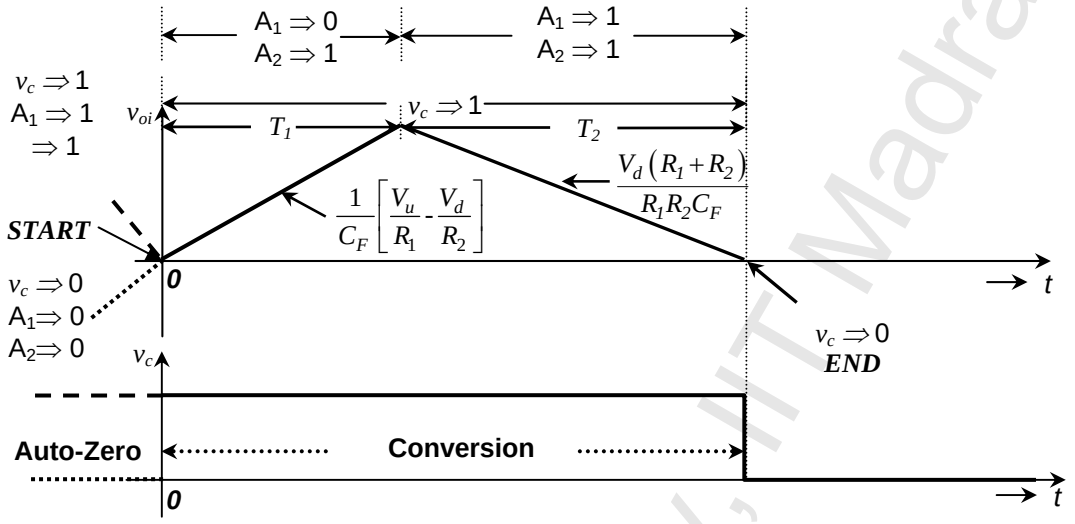


Fig. 5.3 Waveforms at the output of the comparator (v_c) and the integrator (v_{oi}) – for positive kx

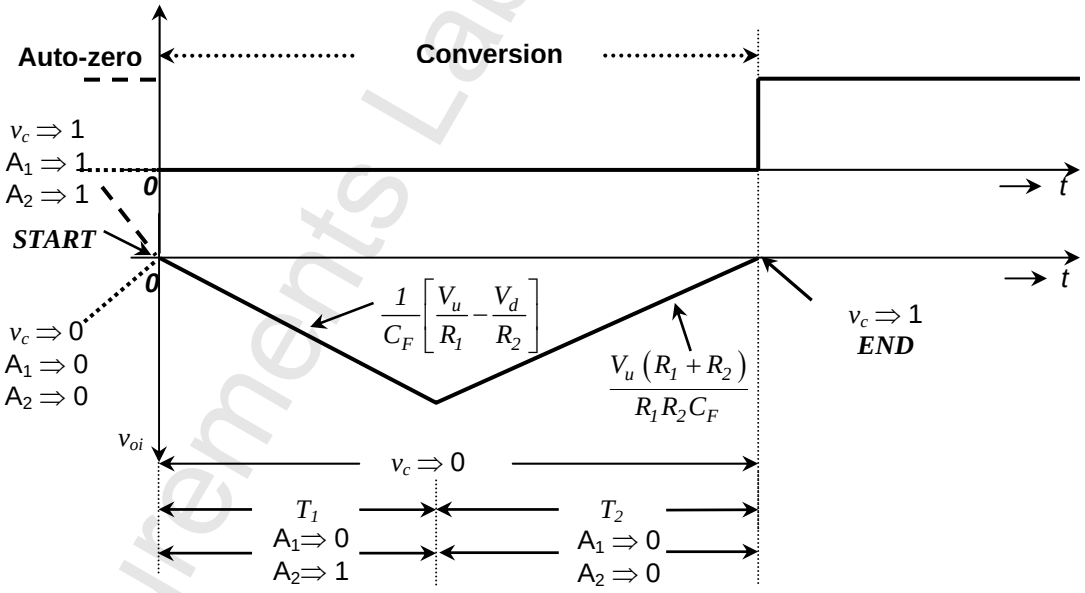


Fig. 5.4 Waveforms at the output of the comparator (v_c) and the integrator (v_{oi}) – for negative kx

will be negative, as is made clear in Fig. 5.4. For this condition, the output of the comparator (v_c) will be low. If measurand x is zero, then $R_1 = R_2$ and the integrator output will be zero at the end of T_1. At $t = T_1$, the TCU senses the comparator output. If v_c is high, the control unit causes A_1 to go high, switching S_1 to position 2, while S_2 remains in its earlier position. As a result, the charging current i_c is now $-\left(\frac{V_d}{R_1}+\frac{V_d}{R_2}\right)$ and hence the integrator would ramp down as illustrated by Fig. 5.3.

The control unit activates a timer at the end of T_1, and measures the time taken (say, $T_2 = N_2T_c$) for the output of the integrator to become zero. The output of the integrator reaching zero is signalled to the control unit by a high to low transition on the output of the comparator, v_c. The polarity of the output is taken as positive. On the other hand, if kx is negative, the situation at the end of T_1 would be as indicated in Fig. 5.4. The comparator output being low, indicates that the polarity of the output is to be taken as negative. Sensing this condition, the control unit connects both R_1 and R_2 to $-V_u$, by causing A_2 to go low, which makes S_2 to switch to position 1. The signal level of A_1 and thereby, the position of S_1 are maintained. The integrator output will then ramp up with a slope equal to $\frac{V_u}{C_F}\left(\frac{R_1+R_2}{R_1R_2}\right)$. The time taken for the output of the integrator to reach zero, signalled by a low to high transition on v_c, is measured as T_2 (= N_2T_c). The integrator output starting from zero, becoming a maximum either in the positive or negative direction and then returning to zero, constitutes one conversion cycle.

At the end of T_2, we have

$$\frac{1}{C_F}\left[\frac{V_u}{R_1}-\frac{V_d}{R_2}\right]T_1 = \frac{V_d\left(R_1+R_2\right)}{R_1R_2C_F}T_2$$
$$\text{or} \quad \frac{1}{C_F}\left[\frac{V_u}{R_1}-\frac{V_d}{R_2}\right]T_1 = \frac{V_u\left(R_1+R_2\right)}{R_1R_2C_F}T_2. \tag{5.2}$$

Substituting the values of R_1 and R_2 as given by expression (1.5), as well as assuming that the reference voltages are of equal magnitude, i.e. $V_u = V_d = V_R$, we get ,

$$kx = \frac{T_2}{T_1} = \frac{N_2}{N_1}. \tag{5.3}$$

Since the time period T_1 is chosen to be an integral multiple of T_c (say $N_1 = 10000$), the fractional change in the transducer resistance and hence the change in the physical quantity being measured (x), is indicated by T_2 (N_2). The polarity of kx is indicated by the condition of v_c at the end of T_1. As mentioned earlier, if v_c is high at the end of T_1, the output is taken as positive and is treated as negative otherwise.

Occasionally, a differential resistive sensor may possess inverse characteristics, as described by expression (1.6). Using these values of R_1 and R_2 in equation (5.2), we obtain, $kx = (T_2/T_1)$. It can be seen that even under such circumstances, equation (5.3) remains valid. Thus, the present scheme provides a linear digital output irrespective of whether the differential resistive sensor has a linear or inverse characteristic. The flowchart indicating the conversion logic is shown in Fig. 5.5.

The circuit to implement the proposed method is first analysed for various possible sources of errors and their effects on its performance. It is then simulated to check its operation. The circuit is fine-tuned to conform to specifications and then prototyped using off-the-shelf components. The remaining sections of this chapter detail the analysis of the circuit as well as present the results obtained from the simulation and the experiments conducted on the prototype.

5.3 Error analysis

In the preceding discussion, it was assumed that the components used in the dual slope RDC were ideal. This section analyses possible errors that can occur in the dual slope RDC due to the non-ideal characteristics of practical components.

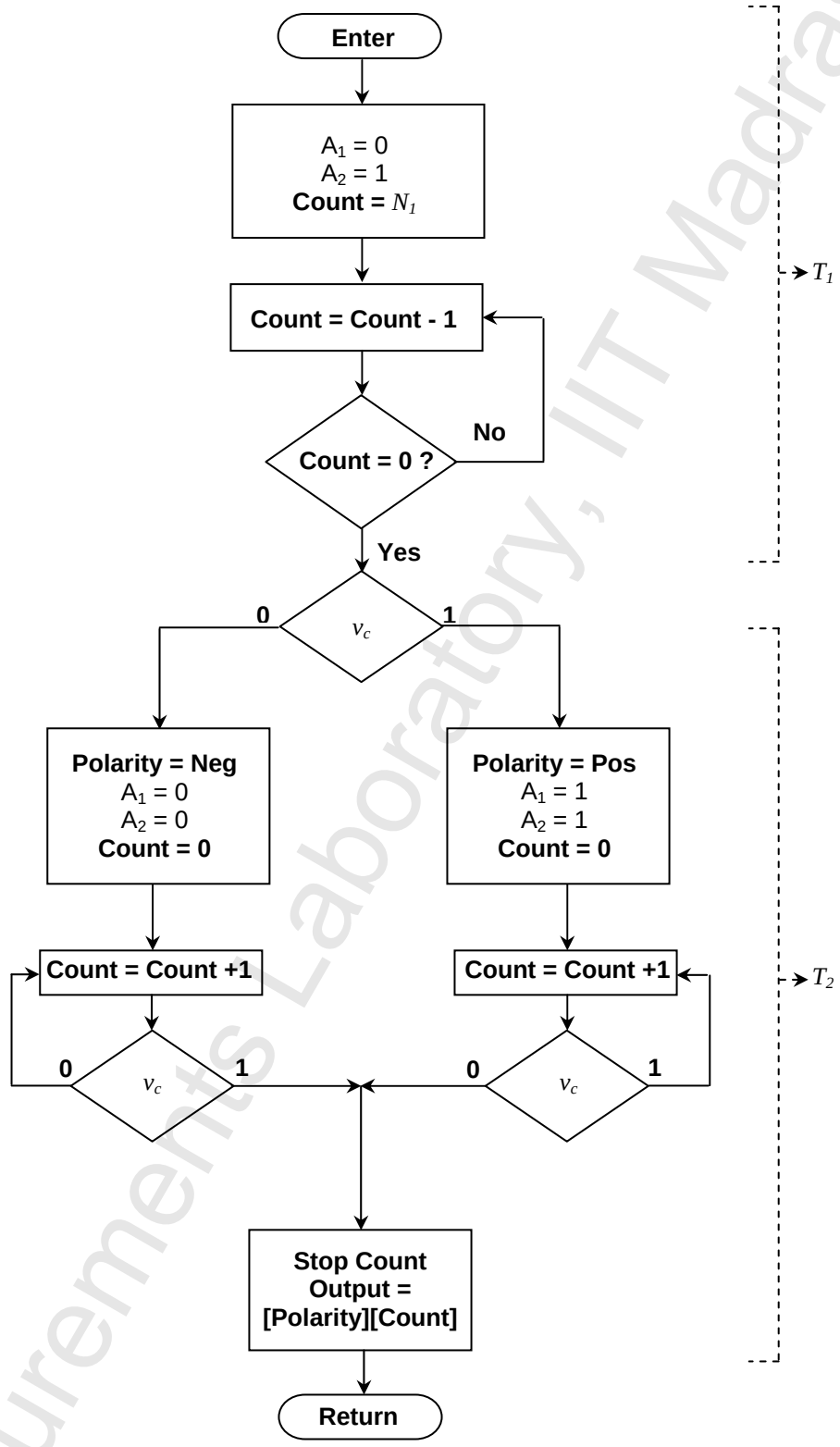


Fig. 5.5 Flowchart for the conversion phase of one measurement cycle

5.3.1 Error due to the 'ON' resistance of the switches

It was assumed that the switches employed in the digital converter circuit described above were ideal, possessing zero 'ON' resistances. In reality, the switches used will have finite 'ON' resistances which would appear in series with the transducer elements and affect the performance of the circuit. If the ON resistances of the switches S_1 and S_2 are denoted by r_1 and r_2 respectively, equation (5.2) would be modified as

$$\frac{1}{C_F}\left[\frac{V_u}{R_1+r_1}-\frac{V_d}{R_2+r_2}\right]T_1=\frac{V_d\left(R_1+R_2+r_1+r_2\right)}{\left(R_1+r_1\right)\left(R_2+r_2\right)C_F}T_2 \tag{5.4}$$

The above expression would simplify to

$$k\,x=\frac{T_2}{T_1}\left(1+\frac{r_1+r_2}{2R_o}\right)+\frac{r_1-r_2}{2R_o} \tag{5.5}$$

A comparison of equations (5.3) and (5.5) indicates that the 'ON' resistances of the switches contribute to gain as well as offset errors, both of which can be easily removed by suitable calibration. If the two switches are identical, then $r_1 \approx r_2$ and the circuit is free from offset. As is illustrated by Fig. 5.6, which depicts the error in the measured value of kx as obtained from expression (5.5) for different values of κ, where $\kappa=\frac{r_2}{r_1}$, the maximum error is 0.011 %. A typical value of 0.8 Ω for surface mounted switches has been used for the switch resistance, in deriving the above curves. The effect is more pronounced when the ratio $\frac{r}{R_o}$ increases. For values of R_o of the order of 100 Ω, the error is about 0.56 %. But it has to be emphasised that even these errors can be easily compensated as they introduce only an offset and a change in the gain. The effects of the switch 'ON' resistance can be minimized by keeping the ratio as small as possible. This can be easily ensured with most modern-day switches, possessing 'ON' resistances as low as 0.8 Ω for those of the surface mounted type [49].

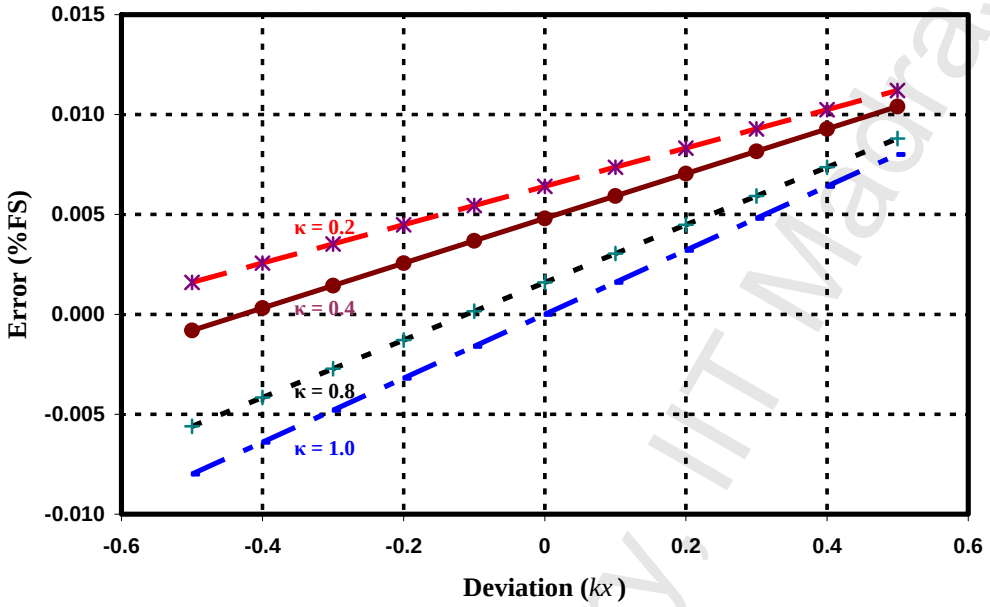


Fig. 5.6 Error in the output for variation in the switch resistances (κ)

The effect of the ON resistances of the switches can also be minimized by buffering the outputs of S_1 and S_2, as demonstrated earlier for the DSRDC for a single element sensor in Fig. 3.5. The complete circuit with the buffers included is shown in Fig. 5.7. The figure indicates the integrator and comparator part of the Dual Slope RDC, where the integrator is interfaced to the switch ADG508F by means of the unity gain amplifiers built around the OP07 opamps.

5.3.2 Effect of mismatch in the magnitudes of the reference voltages ($-V_u$ and $+V_d$) and the offset voltage of the opamp

In deriving equation (5.3), it was assumed that the reference voltages $-V_u$ and $+V_d$ are of equal magnitude. In practice, it is found that the ratio V_d / V_u, denoted by η, is not equal to unity. An offset voltage in the integrator, if present, results in a mismatch between the voltages to which the integrator ramps up or down. Whatever be the reason for the mismatch, for positive kx, equation (5.2) will be modified as

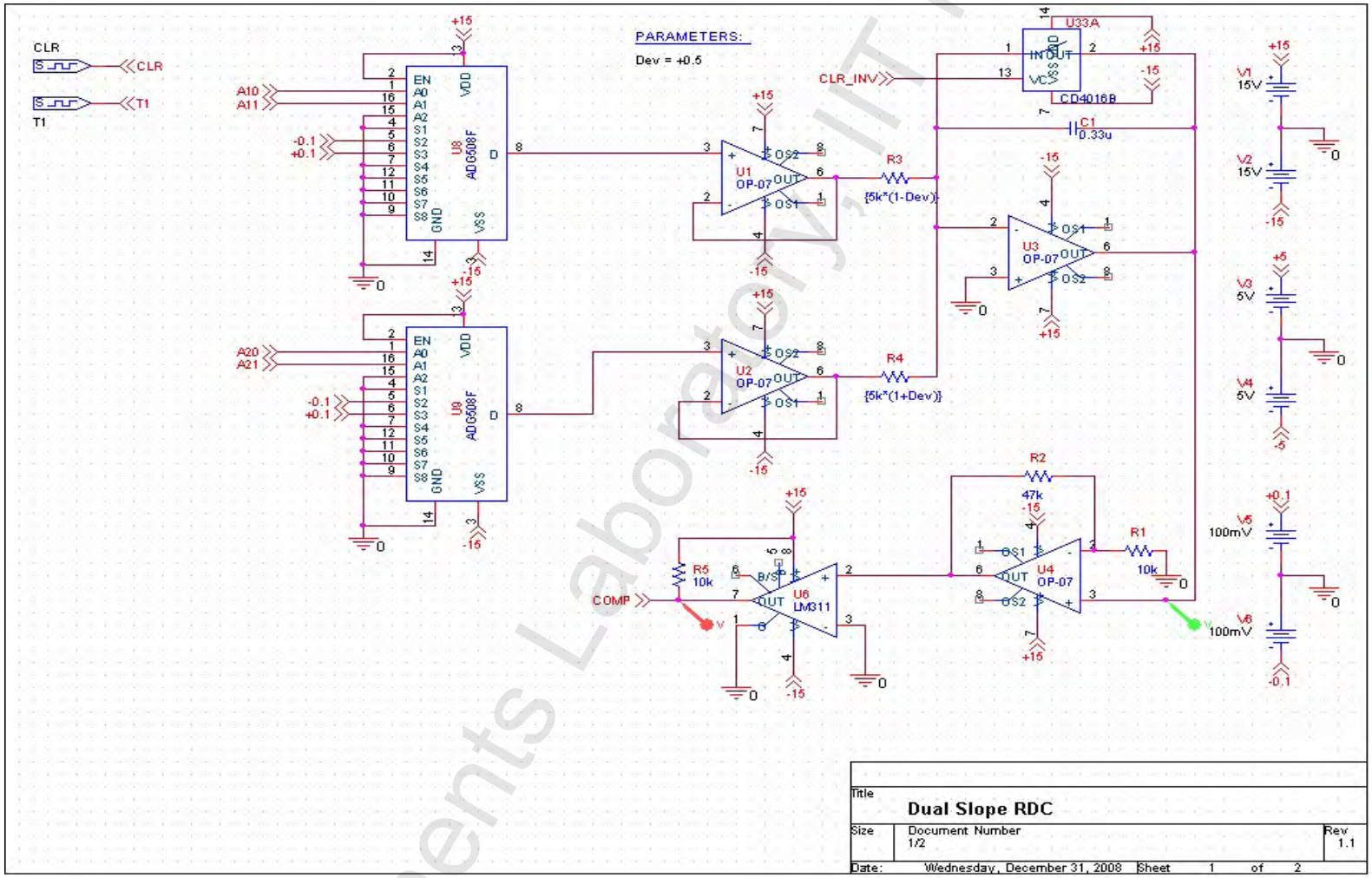


Fig. 5.7 Circuit layout of the proposed DSRDC showing the integrator and comparator as well as the switches and the buffers

$$\frac{V_u T_1}{C_F R_o (1-kx)} - \frac{\eta V_u T_1}{C_F R_o (1+kx)} = \frac{2V_u T_2}{C_F R_o \left(1-(kx)^2\right)} \tag{5.6}$$

leading to the expression,

$$kx = \frac{2}{1+\eta}\frac{T_2}{T_1} - (1-\eta). \tag{5.7}$$

As can be seen from a comparison of expressions (5.3) and (5.7), the mismatch in the magnitudes of the reference voltages modifies the gain of the circuit as well as introduces an offset. Fortunately, with modern technology, voltage levels can be stabilised to accuracies of parts per million, with very low temperature drift by using reference diodes like the LM385, thus ensuring that errors due to mismatch of reference voltage levels are kept negligible by appropriate choice of the devices.

5.3.3 Errors due to the delays caused by the comparator, control circuit and the switches

In the discussions so far, it was assumed that the switching between the two different reference voltages takes place instantaneously. However, in practice, the finite switching times of the comparator as well as the analog switches cause delays. The delay of the comparator, τ_c causes an offset in the final expression [equation (5.3)] which will be modified as $kx = \frac{T_2}{T_1} + \frac{\tau_c}{T_1}$.

The delay in switching affects the circuit operation in a slightly different manner. Fig. 5.8 illustrates, in an exaggerated fashion, how the switching delay affects the output of the integrator. In the figure, τ_b is the time taken for the switch to break the contact while τ_m is the time taken to make one. The control circuit is so constructed that the timer is set to operate only at the end of time period τ_m. Hence, the time taken for the switch to break the contact causes the integrator to ramp up for an additional period of time τ_b. The initial expression given by equation (5.2) will then be modified to

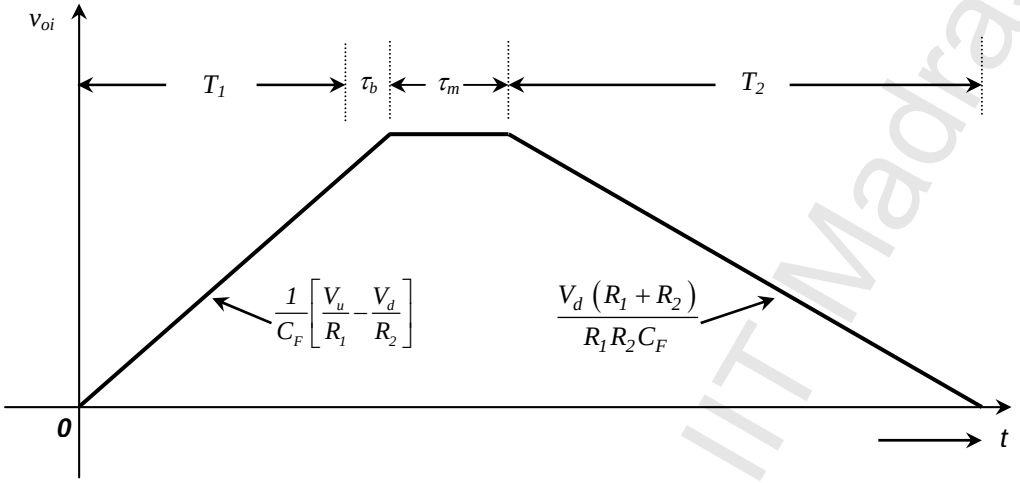


Fig. 5.8 Effect of comparator and switch delay on the output (exaggerated for clarity)

$$\frac{1}{C_F}\left[\frac{V_u}{R_1}-\frac{V_d}{R_2}\right]\left(T_1+\tau_b\right)=\frac{V_d\left(R_1+R_2\right)}{R_1R_2C_F}T_2 \tag{5.8}$$

The measured value of the physical quantity *kx* is now given by

$$kx=\frac{T_2}{T_1}\frac{1}{\left(1+\frac{\tau_b}{T_1}\right)} \tag{5.9}$$

Expression (5.9) makes it clear that the switching delay causes a change in the designed gain of the circuit. But, as is evident, this can be easily corrected by suitable calibration. Moreover, by choosing T_1 to be much larger than τ_b as is normally the case, this error can be made insignificant.

5.3.4 Effect of mismatch in the sensor resistances and their sensitivity factors

We assumed that the sensor was perfectly symmetrical and that when *x* was zero, $R_1 = R_2 = R_o$. But in practice, there would be a small mismatch, both in the nominal values as well as the sensitivities (transformation efficiency) of the resistors, R_1 and R_2. In such a situation, we would have $R_1 = R_{o1}(1 - k_1x)$ and $R_2 = R_{o2}(1 + k_2x)$, where R_{o1} and R_{o2} are the nominal values of the resistances R_1 and R_2 while k_1 and k_2 are their

transformation efficiencies, respectively. Equation (5.2) is now modified as

$$\frac{V_R}{C_F R_{o1}\left(1-k_1 x\right)} T_1 - \frac{V_R}{C_F R_{o2}\left(1+k_2 x\right)} T_1 = \frac{V_R\left(R_{o1}\left(1-k_1 x\right)+R_{o2}\left(1+k_2 x\right)\right)}{C_F\, R_{o1} R_{o2}\left(1+k_1 x\right)\left(1-k_2 x\right)} T_2 \quad (5.10)$$

In general, if $R_{o1} = R_{o2}\,(1 + \chi)$ and $k_1 = k_2\,(1 + \lambda)$, then Equation (5.10) simplifies to

$$\frac{T_2}{T_1} = \frac{\chi + \left(2 + \chi + \lambda + \chi\lambda\right) k_2 x}{2 + \chi + \left(\chi + \lambda + \chi\lambda\right) k_2 x} \quad (5.11)$$

Case 1 : When $R_{o1}\, k_1 = R_{o2}\, k_2$

This is the case when the absolute change in the sensor resistances due to the measurand is the same, despite the fact that the nominal values and transformation efficiencies of R_1 and R_2 are different. The condition implies that $\chi + \lambda + \chi\lambda = 0$. Equation (5.11) transforms to

$$\frac{T_2}{T_1} = \frac{\chi}{\chi + 2} + \frac{2 k_2}{\chi + 2} x \quad (5.12)$$

Equation (5.12) shows that such a mismatch in the sensor resistances causes an offset as well as a gain error. The degree of this type of mismatch is normally very low, as differential resistive sensors are generally not manufactured as individual units. They are available as matched pairs, with very similar properties. Besides, they are usually placed close to each other so that variations due to any local conditions also track each other. Moreover, as can be seen, the errors due to such mismatch, if any, can be easily eliminated by employing appropriate offset compensation and calibration.

Case 2 : When $R_{o1} \neq R_{o2}$ **but** $k_1 = k_2$

This is normally the case for strain gauges which are made out of the same material and are subject to the same conditions. Under the circumstances, equation (5.11) modifies to

$$\frac{T_2}{T_1} = \frac{\chi + \left(2 + \chi\right) k_2 x}{2 + \chi\left(1 + k_2 x\right)} \quad (5.13)$$

Fig. 5.9 plots the variation in error with the measured deviation for various values

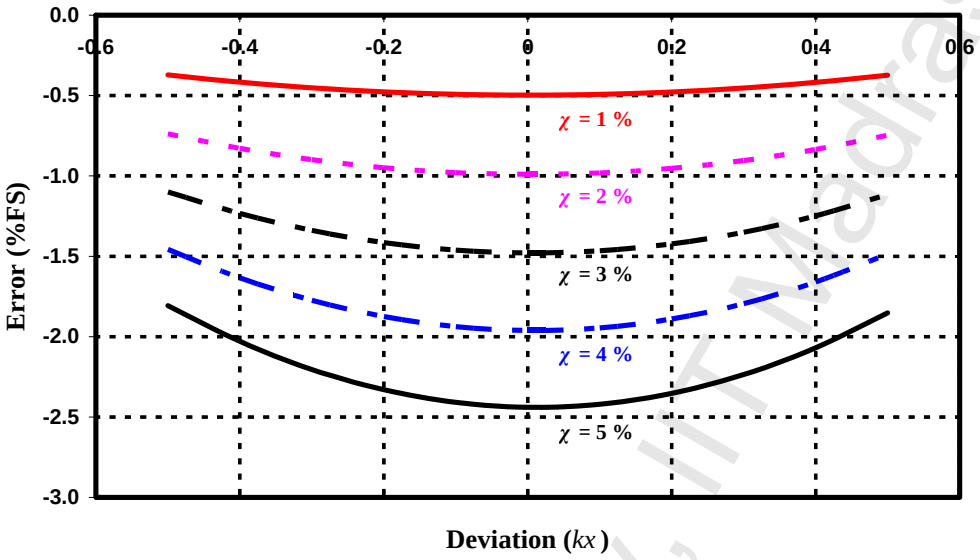


Fig. 5.9 Effect of mismatch of nominal value of the resistance

of χ, ranging from 1 % to 5 %. As the mismatch increases, so does the error. When the mismatch is 5 %, the error in the output is almost 2.5 %. It should be noted that the error caused by the difference in the transformation efficiencies of the two resistors constituting the differential resistive transducer, is nonlinear.

Case 3 : When $\chi \neq 0$ and $\lambda \neq 0$

This is the general case, when the nominal values of the resistances as well as the transformation efficiencies of the two resistors are independent of each other. If the maximum mismatch of both transducer sensitivities as well as the nominal values of the resistances are taken to be ± 5 % ($\chi = \lambda = \pm 0.05$), evaluating equation (5.11) shows that the maximum gain error in the measurement of T_2/T_1 is well within limits.

5.4 Simulation studies

The circuit schematic shown in Fig. 5.1 was simulated using OrCAD PSpice (v16.2) from M/s Cadence Corporation. This is a program which enables one to not only design and layout an electrical circuit but also allows one to simulate, fairly realistically, the operation and performance of the developed circuit. Besides having a

library of models for most of the commonly used analog and digital components, it uses a graphical, interactive user-interface to set the parameters and specifications of the circuit schematic as well as of the simulation to be run. A separate window displays the voltage and currents at the desired nodes on the schematic.

A few changes were made in the circuit to accommodate the fact that the PSpice models of some of the components were not available. Accordingly, the CD4053 used in the prototype was replaced by the ADG508F from M/s Analog Devices. Switch resistances of 1.25 Ω and 2.5 Ω were employed in series with R_1 and R_2 respectively, over and above those included in the models, to explicitly demonstrate the effect of the mismatch in switch resistances. Similarly, reference voltages of + 100 mV and - 100 mV were used, with the latter varied by 1 % to study the effect of the mismatch in the magnitudes of the reference voltages.

The nominal value of the resistance of the differential resistive sensor was set at 5 kΩ - typical of a high resistance strain gage, used with 4 – 20 mA transmitters and battery powered transducers [94] - and accordingly, the feedback capacitor was fixed at 0.33 μF, to accommodate the variation in sensor resistance as well as the need for a sufficiently large value of T_1, so that N_1 may remain large. T_1 was initially taken to be 100 ms, with a clock frequency of 20 kHz (in order to represent the operation of the prototype as far as possible). T_1 was provided by means of a digital stimulus which remained high for a period of 100 ms, before going low. The output T_2 was measured automatically as the period from when T_1 goes low to the instant when the output of the comparator (v_c) changes state.

The parameter, *kx*, was chosen to vary between + 0.5 and - 0.5, in steps of 0.1. The program suitably adjusts the values of R_1 and R_2 to accommodate the corresponding value of *kx* for each run of the simulation. It was found that with the values chosen,

each run of the simulation was taking quite a long time, around 15 minutes each, and therefore, T_1 was scaled down to 50 ms and the clock suitably scaled up to 40 kHz. The simulation was allowed to run uninterruptedly on a dedicated machine, with a 2.4 GHz, Pentium IV processor, having 1 GB of RAM and 80 GB of hard disk space. Using the 'Parameter Sweep' and 'Performance Analysis' options of the software, the value of T_2 was measured. The deviation was calculated and plotted as a function of the change in input (kx), as illustrated by Fig. 5.10. As can be seen, the errors in the simulated circuit are within ± 0.15 %.

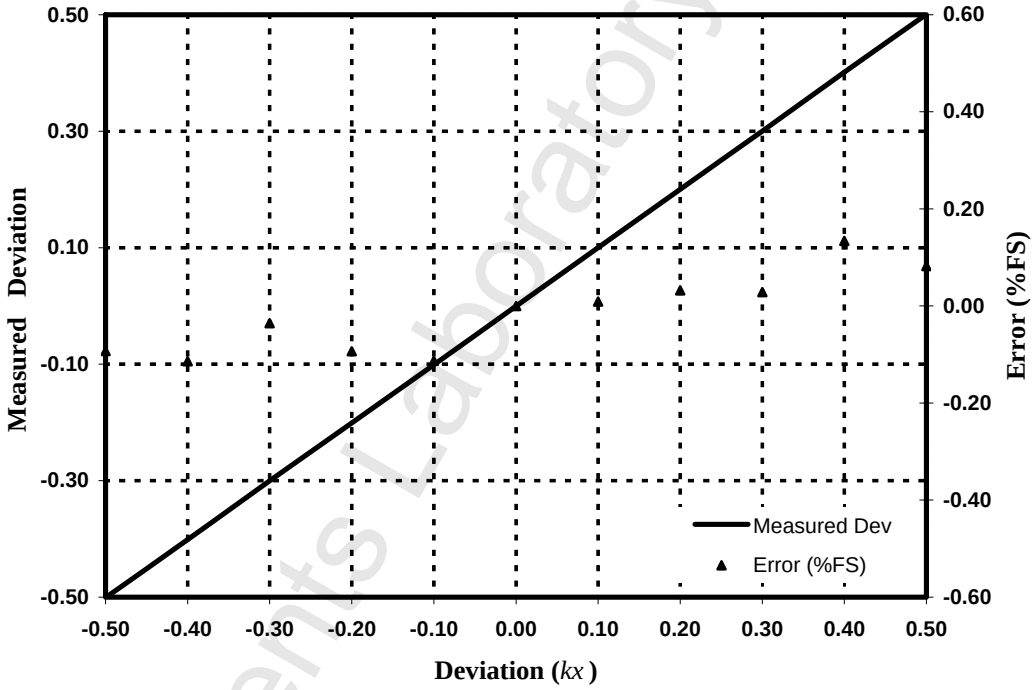


Fig. 5.10 Performance of the proposed DSRDC for a differential resistive sensor (Simulation Study)

The magnitudes of the reference voltages were then changed to reflect a mismatch of 1 % and the simulation was run again, for a smaller step size of 0.01. As is clearly indicated in Fig. 5.11, the errors increase when the voltage mismatch increases, bearing out the conclusions of the discussion in Section 0.

5.5 Experimental verification

After checking the efficacy of the proposed circuit by simulation studies, a

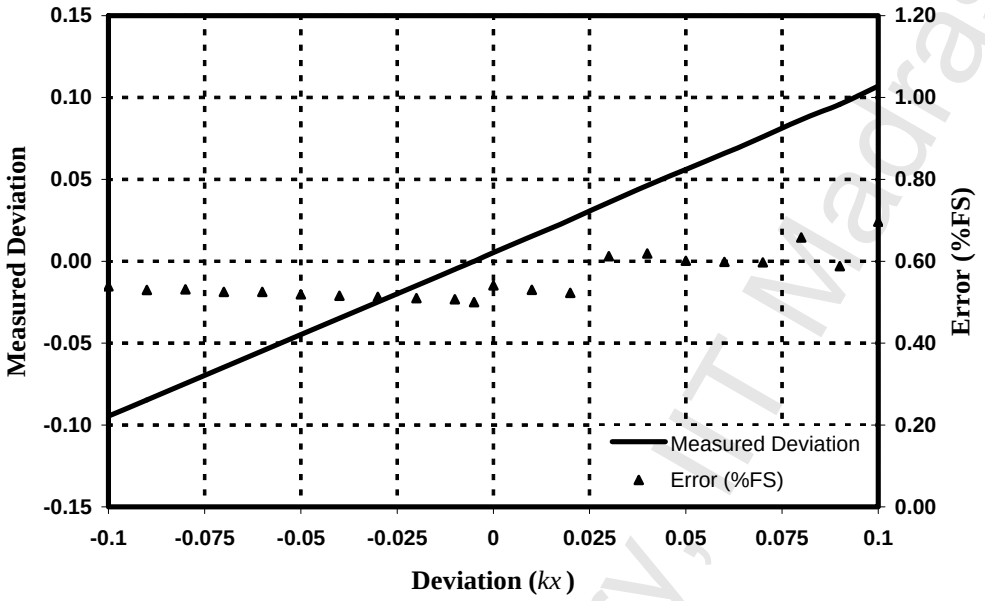


Fig. 5.11 Effect of voltage mismatch on the output (Simulation Study)

prototype was built and tested to confirm the results on an experimental model. The reference voltage of $+V_d$ was derived from the LM385-1.2, which was then inverted using the OP07 to obtain $-V_u$. The reference voltages were separately and independently measured using a 6½-digit multimeter (34401A) from Hewlett-Packard. The gain of the inverter was appropriately trimmed to obtain a η of 1.0004. The OP07, with its low offset voltage was used for building the integrator. The CD4053 [95] served as the switches S_1 and S_2 with buffers made of OP07 to eliminate the effect of the 'ON' resistance of the switches. The LM311, with its fast rise and fall times as well as large bandwidth, was used for the comparator.

The control and timing circuit was implemented using the PIC16F877A micro-controller [96]. The internal counters of the microcontroller were used to set the fixed time period T_1 and also measure T_2. The program to implement the necessary control logic was developed and burnt into the micro-controller. Instead of using a commercially available, differential resistive sensor, whose characteristics would not be under our control, the sensor resistances R_1 and R_2 set up using two precision, decade

resistance boxes from Otto Wolff, Germany, varying from 0 to 12,221 Ω having a resolution of 1 Ω and an accuracy of ± 0.01 %.The nominal values of the resistances were set at 5 kΩ and the two resistances were varied in steps of 100 Ω to simulate a *kx* variation in the range of ± 0.2, in steps of 0.02. At the two extremes of the range, the resolution of the circuit was sought to be checked by varying the resistances in steps of 0.002. The results obtained as well as the measurement errors are shown in Fig. 5.12.

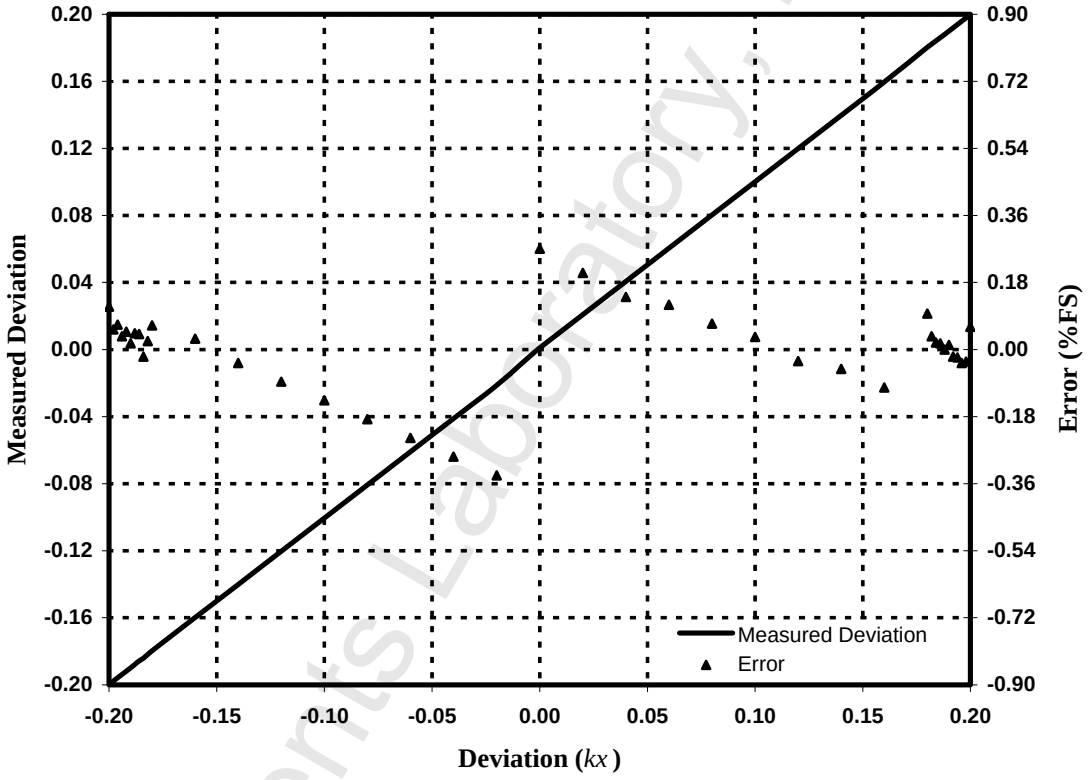


Fig. 5.12 Output and error characteristics of the prototype DSRDC

As can be seen, the performance of the circuit matches the analysis and predictions of the previous sections. It is found that the worst case error is less than ± 0.35 %. It is to be emphasised that the characteristics depicted were obtained by bread-boarding easily available, off-the-shelf components.

5.6 Summary

An innovative concept for obtaining a digital output directly from a differential

type resistive sensor has been presented. The scheme accepts sensors with both linear as well as inverse characteristics and provides a linear digital output. The Resistance to Digital Converter presented here has all the advantages of the integrating, dual slope ADC. The circuit has been analysed for all possible sources of errors and results obtained with a prototype are presented to justify the inferences drawn.

One of the major disadvantages of the dual slope analog to digital converter principle is its low conversion speed, with an upper limit of a few hundred samples per second. This would be inadequate when sampling quickly varying quantities or when required to oversample a signal for higher time resolution. The Sigma Delta resistance to digital converter described in the next chapter has been designed with such a need in mind.

6. Sigma-Delta Resistance to Digital Converter for Differential Resistive Sensors

6.1 Need for an alternative method of resistance to digital conversion

Resistance to digital converters suitable for different types of resistive sensors based on the dual slope principle (DSRDC) were discussed in the previous three chapters. While the DSRDC has several advantages as brought out earlier, its low conversion rate, typically a few samples to a few hundred samples per second, is a serious drawback, especially when dealing with quickly varying data. Hence, there exists a need for developing a resistance to digital converter that is suitable for applications which require the output of a resistive sensor to be sampled at rates of upto a few tens of kilo samples per second. A novel resistance to digital converter based on the popular sigma-delta ADC technique which addresses this need is presented in this chapter.

6.2 Sigma-Delta modulated analog to digital conversion

The Sigma Delta Modulated ADC (SDADC) represents an optimal compromise between the twin considerations of high resolution and bandwidth in an analog to digital converter. It would be ideal for applications where ADCs having high resolution coupled with moderate sampling rate are required. Though the process of sigma-delta modulation was expounded way back in 1963 [97], the technique has become more popular only in the last two decades due to the rapid advances in mixed signal integrated circuit technology. The block schematic representation of a typical “first order” sigma delta type ADC is shown in Fig. 6.1. It can be shown that the integrator helps in shaping the noise power out of the signal band and amplifying it elsewhere [98], thus pushing noise out of the signal band to higher frequencies. The

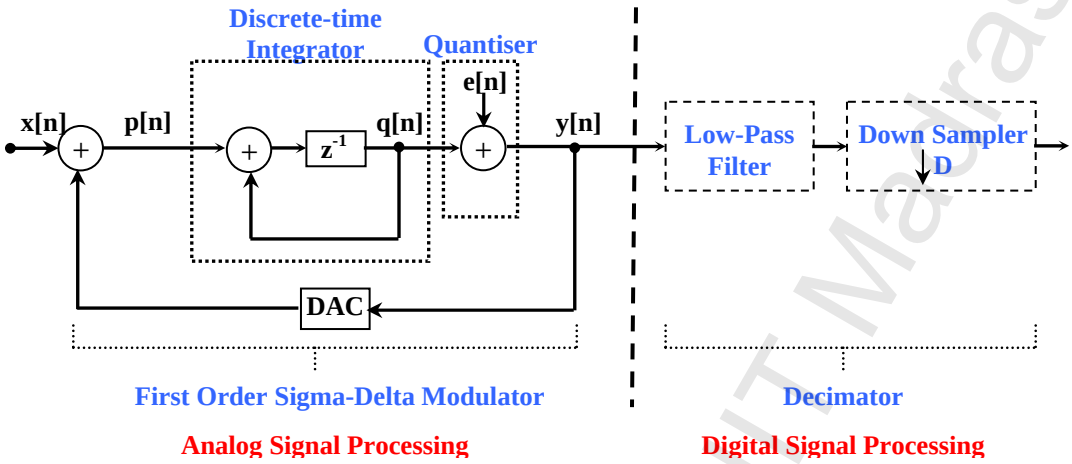


Fig. 6.1 Block schematic of a first order Sigma-Delta modulator based ADC

high frequency noise can then be removed by filtering.

6.3 Sigma-Delta Resistance to Digital Converter (SDRDC)

To obtain a sigma-delta type resistance to digital converter (SDRDC), suitable for a differential resistive sensor, the conventional sigma delta type ADC of Fig. 6.1 is suitably modified as shown in Fig. 6.2 [99]. As in a sigma delta type SDC, the SDRDC presented here also makes use of a Δ-modulator followed by an over-sampler and a digital filter. The analog input voltage is removed from a classical SDADC. The integrator which is realised using an opamp OA with a capacitor C_F in its feedback loop, includes the resistors R_1 and R_2 of a differential resistive sensor. A terminal each of the sensor resistors R_1 and R_2 are tied together (or the common point of a three terminal resistive sensor) and connected to the inverting input of the opamp OA. The free end of R_1 is tied to the output of a single-pole, double-throw (SPDT) analog switch S_1 while the free end of R_2 is similarly connected to a second SPDT switch S_2. Switch S_1 connects either $-V_u$ (S_1 in position 1) or ground (S_1 in position 2) to R_1 depending on the control signal applied to it. Similarly S_2 connects the free end of R_2 to ground (S_2 in position 1) or to $+V_d$ (S_2 in position 2) depending on its control signal. $-V_u$ and $+V_d$ are dc reference voltages of equal magnitude but of opposite polarity.

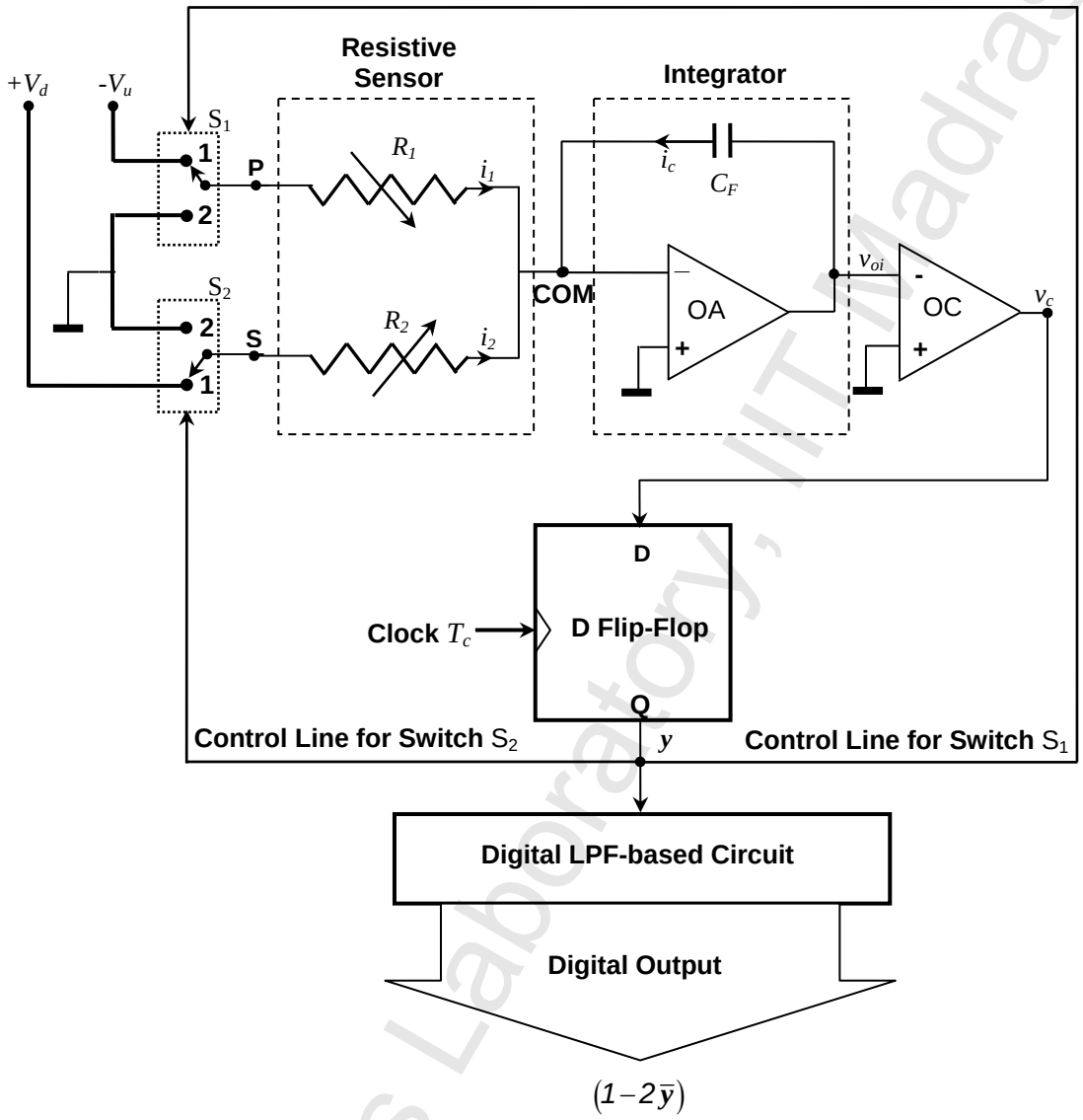


Fig. 6.2 Schematic representation of the Σ-Δ resistance to digital converter

The output v_{oi} of the integrator is fed to the inverting terminal of a comparator OC. The output of the comparator (v_c) is "low" if $v_{oi} \geq 0$ and "high" otherwise. v_c in turn, serves as the input of a D-flip-flop. The binary output of the flip-flop ***y***, controls switches S_1 and S_2. Switches S_1 and S_2 are set at position 1 if $\boldsymbol{y} = 1$ and at position 2 whenever $\boldsymbol{y} = 0$. ***y***, updated (say, at the leading edge) by a high frequency clock of time period T_c, also acts as the input to a digital low-pass filter (LPF) based circuit, which extracts and provides as the final output $(1-2\bar{y})$, where $\bar{y}$ is the average value of the LPF input bit stream ***y***.

Initially, assume $v_{oi} < 0$ and $\boldsymbol{y} = 1$. Hence, switches S_1 and S_2 are set to position 1, where R_1 is connected to $-V_u$ and R_2 is tied to ground. Under this condition, v_{oi} ramps up with a slope of $\frac{V_u}{R_1 C_F}$ till it becomes positive. Once v_{oi} is positive ($v_{oi} > 0$), the comparator output becomes low. The D-flip-flop output gets updated at the very next (leading edge of the) clock and the output $\boldsymbol{y}$ toggles ($\boldsymbol{y} = 0$). Switches S_1 and S_2 are set to position 2, grounding resistance R_1 and connecting R_2 to $+V_d$. The current $\frac{V_d}{R_2}$ charges C_F. Consequently, v_{oi} ramps down with a slope $\frac{V_d}{R_2 C_F}$ till v_{oi} turns negative, forcing the v_c to go high. The D-type flip-flop output gets updated on the next clock, making $\boldsymbol{y} = 1$, bringing the status of the circuit back to its assumed initial condition and thereby, making the entire cycle repeat continuously. When $\boldsymbol{y} = 1$, the change in the integrator voltage for each clock period, is given by $\Delta v_{oi(1)} = \frac{V_u T_c}{R_1 C_F}$. Similarly, for $\boldsymbol{y} = 0$, the change in the integrator voltage for each clock period is $\Delta v_{oi(0)} = \frac{-V_d T_c}{R_2 C_F}$. After a finite number of clock cycles, say N (period $T = N T_c$) the integrator output is

$$v_{oi(N)} = \frac{V_u T_c}{R_1 C_F} N_{(1)} - \frac{V_d T_c}{R_2 C_F} N_{(0)}, \tag{6.1}$$

where $N_{(1)}$ and $N_{(0)}$ are the number of clock cycles for which the output of the D-flip-flop is 1 and 0 respectively within the period T and $N = N_{(1)} + N_{(0)}$. If N is sufficiently large, then the value of $v_{oi(N)}$ has to be less than or equal to the maximum possible change in integrator voltage per clock cycle $v_{oi(m)}$,

$$v_{oi(m)} = \frac{(V_u, V_d)_{max} T_c}{(R_1, R_2)_{min} C_F}, \tag{6.2}$$

where $(V_u,V_d)_{max}$ is the larger of the two reference voltages and $(R_1, R_2)_{\min}$ is the minimum among R_1 and R_2. Then,

$$\frac{T_c}{C_F}\left(\frac{V_u N_{(1)}}{R_1} - \frac{V_d N_{(0)}}{R_2}\right) \le \frac{T_c}{C_F}\frac{(V_u, V_d)_{max}}{(R_1, R_2)_{min}}. \tag{6.3}$$

If we assume that the dc reference voltages have equal magnitude, i.e. $V_u = V_d = V_R$, then the above expression simplifies to

$$\left(N_{(1)}R_2 - N_{(0)}R_1\right) \le (R_1, R_2)_{max}. \tag{6.4}$$

In the above expression, $(R_1, R_2)_{\max}$ is the maximum of R_1 and R_2. Using the values of R_1 and R_2 for a differential resistive sensor possessing linear characteristics as given by equation (1.5), equation (6.4) is modified to

$$\left(R_o(1 \pm kx)N_{(1)} - R_o(1 \mp kx)N_{(0)}\right) \le (R_1, R_2)_{max},$$

leading to

$$\frac{R_o}{N}\left[(N_{(1)} - N_{(0)}) \pm kx\,N\right] \le \frac{1}{N}(R_1, R_2)_{max}. \tag{6.5}$$

For a very large value of N, the value of $\frac{1}{N}(R_1, R_2)_{max}$ becomes small and therefore,

$$kx = \pm\left[\frac{N_{(0)} - N_{(1)}}{N}\right] = \pm\left(1 - 2\left(\frac{N_{(1)}}{N}\right)\right) = \pm(1 - 2\bar{y}). \tag{6.6}$$

$\frac{N_{(1)}}{N}$ is the average value $\bar{y}$, of the bit-stream $\boldsymbol{y}$ over the period NT_c. As the digital low-pass filter based circuit is designed to extract $(1 - 2\bar{y})$, its output is kx. Hence, for differential resistive sensors possessing linear characteristics as given in expression (1.5), the proposed technique provides a linear digital output proportional to the quantity being sensed.

Occasionally, differential resistive sensors may possess inverse characteristics as given by equation (1.6). It turns out that substituting the values of R_1 and R_2 as defined by expression (1.6) in equation (6.4) results in

$$\left(\frac{R_o}{(1 \mp kx)}N_{(1)} - \frac{R_o}{(1 \pm kx)}N_{(0)}\right) \le (R_1, R_2)_{max},$$

leading to $$\frac{R_o}{N}\left[\left(N_{(1)}-N_{(0)}\right)\pm kxN\right]\le\frac{1}{N}\left(1+k^2x^2\right)\left(R_1,R_2\right)_{max}. \quad (6.7)$$

For a very large value of N, the value of $\frac{1}{N}\left(1+k^2x^2\right)\left(R_1,R_2\right)_{max}$ becomes small, modifying equation (6.7) as

$$kx=\pm\left[\frac{N_{(0)}-N_{(1)}}{N}\right]=\pm\left(1-2\left(\frac{N_{(1)}}{N}\right)\right)=\pm\left(1-2\bar{y}\right). \quad (6.8)$$

As can be seen from expressions (6.6) and (6.8), the output of the digital filter based circuit is identical. Hence, the proposed method provides a digital output linear with the measurand, for sensors with either linear or inverse characteristics.

The above discussion assumes a circuit with ideal components. Such a situation is rarely obtained in practice, with various parts of the circuit contributing to the overall error of the circuit. The errors introduced due to various circuit parameter variations and non-idealities are studied and the results presented in the next section. The simulation studies and details of a prototype RDC built along the lines of the schematic outlined above and tested using off-the-shelf components are detailed in the subsequent sections.

6.4 Error analysis

It should be noted here that the proposed converter is obtained by suitably modifying the 1-bit quantiser (Δ-modulator) of a conventional Sigma-Delta ADC. Therefore, the SDRDC will necessarily possess uncertainties as detailed in IEEE Std. 1241-2005 [100], and elsewhere [101]-[105]. Over and above these uncertainties, the RDC will be prone to additional errors due to the modification of a conventional Sigma-Delta ADC like the introduction of an additional switch and the use of two reference voltages, instead of one.

Hence, errors will be introduced in the output due to the:

(i) Difference in the magnitudes of the positive and negative dc reference voltages,

(ii) Offset voltages of the integrator and the comparator,

(iii) ON resistances of the switches,

(iv) Switch leakage currents,

(v) Opamp bias current and

(vi) Stray capacitances.

The following sub-sections discuss in detail the effect of each parameter on the output.

6.4.1 Effect of mismatch in the magnitudes of the dc reference voltages

In the discussion so far, the magnitudes of the dc reference voltages $+V_d$ and $-V_u$ were assumed to be equal. However, in practice, as the negative reference voltage is derived from $+V_d$, the degree of match between the magnitudes of the two reference voltages will depend on the precision with which the inversion is performed. In general, if we represent V_d as $V_d = \eta V_u$, where η is the factor indicating the extent of mismatch, then equation (6.3) gets modified as $\left(N_{(1)} R_2 - \eta N_{(0)} R_1\right) \le \left(R_1, R_2\right)_{max}$. Hence, $kx = \left[\dfrac{N_{(1)} - \eta N_{(0)}}{N_{(1)} + \eta N_{(0)}}\right]$, resulting in the error ε_{V_R} due to mismatch in the magnitude of the dc reference voltages as,

$$\varepsilon_{V_R} = \frac{\left[\dfrac{N_{(1)} - \eta N_{(0)}}{N_{(1)} + \eta N_{(0)}}\right] - \left[\dfrac{N_{(1)} - N_{(0)}}{N}\right]}{\left[\dfrac{N_{(1)} - N_{(0)}}{N}\right]} 100\,\% = \left(2\eta + \eta^2\right) * 100\,. \qquad (6.9)$$

Fortunately, with modern technology, the reference voltages can be obtained with very high precision. For the prototype developed, η was found to be $4*10^{-5}$ and the corresponding error in the output of the SDRDC, due to mismatch in dc reference voltages alone, works out to be only 0.008 %.

6.4.2 Effects of offset voltages of opamp OA and comparator OC

If the opamp OA has an offset voltage $\pm v_{os}$, then the voltages across the sensor

resistances R_1 and R_2 become $\left(+V_d \mp v_{os}\right)$ and $\left(-V_u \pm v_{os}\right)$ respectively. This condition is equivalent to a mismatch of $2v_{os}$ between the magnitudes of the dc reference voltages $+V_d$ and $-V_u$ and can be analysed along the same lines as in the previous section. Thus, by taking $\eta = 2v_{os}/V_u$, the ensuing error in the output can be computed using expression (6.9). For the prototype, utilising the opamp OP07 which has a maximum offset voltage of 25 μV, equation (6.9) yields a worst case error of only 0.004 %.

The offset voltage of the comparator (v_{oc}) has the effect of shifting the reference point of the comparator by an amount equal to v_{oc}. As long as the offset voltage of OC remains constant during a complete conversion period, it has negligible effect on the final output. A typical opamp like the OP07 has a offset voltage stability of 1 μV/month and a maximum offset voltage drift of 1.3 μV/^{o}C. Hence, a comparator with very low offset voltage drift during the conversion period is sufficient to keep the output error insignificant.

6.4.3 Effect of ON resistance of the switches

In the proposed scheme, the ON resistance, r_1, of switch S_1 is in series with R_1 while the ON resistance r_2 of switch S_2 is in series with R_2. It is equivalent to a change in the values of sensor resistances R_1 and R_2 with the new values as $(R_1 + r_1)$ and $(R_2 + r_2)$, respectively. In this condition, equation (6.4) gets modified as

$$\left(N_{(1)} R_1 + N_{(1)} r_1 - N_{(0)} R_2 - N_{(0)} r_2\right) \le \left(R_1, R_2\right)_{max}, \tag{6.10}$$

leading to

$$\left(1 - 2\bar{y}\right) = \pm kx \left(\frac{1}{1 + \frac{r_1 + r_2}{R_o}} \right) - \left(\frac{r_1 - r_2}{R_o + r_1 + r_2} \right). \tag{6.11}$$

A comparison of expressions (6.6) and (6.11) indicates that the switch ON resistances contribute to a gain error as well as an offset in the output. If we employ identical switches for S_1 and S_2, then $r_1 \approx r_2$ and the offset will be zero. As can be seen

from the above expression, the gain error can be made negligible by ensuring $R_o >> (r_1 + r_2)$. For the prototype, the MAX4680 with $r = 1.25\,\Omega$ was used for the switches, resulting in a worst case gain error of -0.42 % and an offset of 0.08 % (with $R_o = 600\,\Omega$ and $\Delta r = 0.5\,\Omega$). The gain error and the offset, if present, can be easily minimised by suitable compensation.

6.4.4 Effects of switch leakage currents

Leakage currents between nodes 1 and 2 of switches S_1 and S_2, flow from the dc reference sources to the circuit ground and hence do not charge or discharge C_F. When S_1 is at position 2, leakage current (say, I_{L1}) exists between nodes 1 and A. In this condition, the resistance between node A and node 2 is r_1. As $r_1 << R_o$, a large portion of the leakage current I_{L1} flows to circuit ground via node 2 and a negligible amount of current - $\left(I_{L1}\left[r_1/(r_1 + R_1)\right]\right)$ - compared to the sensor current (V_u/R_1), flows through R_1. Similar conditions are applicable for S_2. For the prototype (using the MAX4680) the maximum leakage current was 5 nA. When compared to the minimum sensor current of 2.8 mA (for $R_o = 600\,\Omega$, $V_u = 2.5$ V and $kx = 0.5$), the leakage current was only 6.2 pA, indicating that in practice, the switch leakage currents have little or no effect on the performance of the circuit.

6.4.5 Effect of the bias current of the opamp OA

Depending on its polarity, the opamp bias current (I_B) of OA charges the capacitor C_F, in the same direction throughout a typical conversion time. The bias current manifests as a change in the charging currents as $\left(-\frac{V_u}{R_1} \pm I_B\right)$ and $\left(\frac{V_d}{R_2} \mp I_B\right)$ through the sensor resistances R_1 and R_2, respectively. It can also be represented as a change in the magnitude of the dc reference voltage, equal to either $I_B R_1$ *or* $I_B R_2$. Thus, it can be

treated as equivalent to a mismatch between reference voltages and the ensuing worst case error due to the bias current of the opamp OA can be computed using equation (6.9), by substituting for $\eta = \frac{I_B}{V_u}(R_1 + R_2) = 2\frac{I_B R_o}{V_u}$. The effect can be made insignificant by selecting an opamp OA with very low I_B such that $I_B << \frac{V_u}{R_o}$. The maximum input bias current of the opamp OP07 used in the prototype, is only 3 nA and hence its effect on the output is insignificant.

6.4.6 Effect of stray capacitances

In practice, it may well be that the sensor head is located far from the signal conditioning unit and that the electrical connections between these units are made using shielded cables. Distributed capacitances will exist between the live conductor of each cable and its grounded shield. This effect can be represented by lumped stray capacitances as shown in Fig. 6.3. Stray capacitances C_{AG}, C_{BG} and C_{CG} exist from nodes P, COM and S, respectively to ground. C_{AG} charges to $-V_u$, when S_1 is at

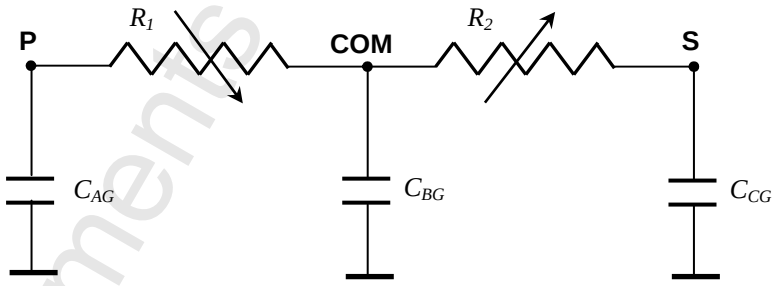


Fig. 6.3 Possible stray capacitances for the differential resistive sensor

position 1. Similarly, C_{BG} charges to $+V_d$, when S_2 is at position 2. Whenever S_1 is switched to position 2 and S_2 to position 1, the charge acquired by the corresponding capacitances C_{AG} and C_{BG} discharges to ground through the low impedance path offered by the switch ON resistance. As long as the time constant $r_1 C_{AG} << R_1 C_{AG}$ and

$r_1 C_{BG} << R_2 C_{BG}$, the stray capacitances C_{AG} and C_{BG} will have negligible effect on the operation of the circuit. As node COM is always at virtual ground, the value of C_{CG} will not affect the output.

6.5 Simulation studies

Before prototyping the circuit, it was simulated using OrCAD PSpice (v 16.2). Since a PSpice model of the digital filter AD1556 was not available, the average of the bit stream ***y*** was indirectly obtained, employing precision reference voltages cascaded to a second order, low-pass filter with cut-off frequency$y << f_c$, where $f_c = 1/T_c$. The resistance of the differential resistive sensor was varied in a range of ± 50 % of its nominal value of 600 Ω, in steps of ± 5 %. A resistor of 1.25 Ω was included in series with the sensor resistances to simulate the effect of the switch resistances (r_1 and r_2). The output was sampled after the simulation was allowed to run for 200 ms, to ensure that all transients die out. Initially, the resistances were varied linearly as given by equation (1.5). The output of the low-pass filter was measured and the value of *kx* was calculated using expression (6.6). The output and error for this case are plotted in Fig. 6.4. A similar simulation was run for a sensor with inverse characteristics of the form given by equation (1.6), the results of which are shown in Fig. 6.5. The errors are predicted to be a maximum of ±0.02 %. It has to be mentioned that the simulations were run without accounting for any of the non-idealities discussed above.

The circuit was again simulated with the switch resistances suitably modified, in order to determine the effect of mismatch in r_1. It was found that the worst possible error in the output, for a mismatch of 100 % was only 0.51 %. Similarly, the magnitudes of the reference voltages were altered to understand their influence on the output. A 1 % mismatch in the magnitudes of the reference voltages produced a maximum error of 4.12 % in the output and was the largest source of error in the circuit.

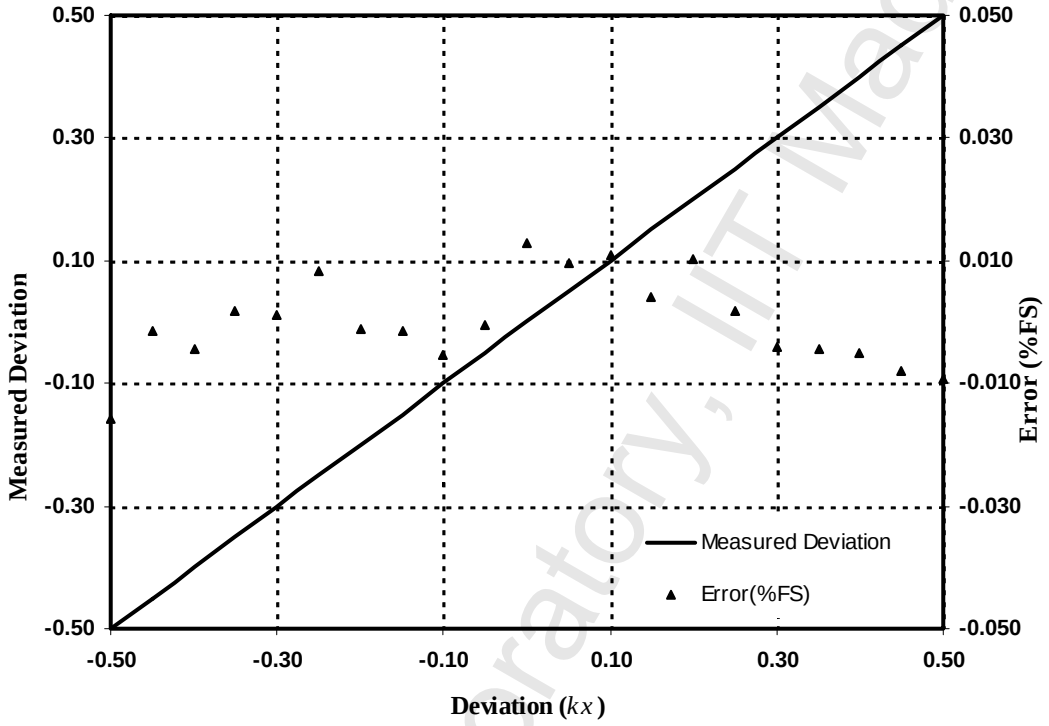


Fig. 6.4 Performance of a sensor with linear characteristics (Simulation Study)

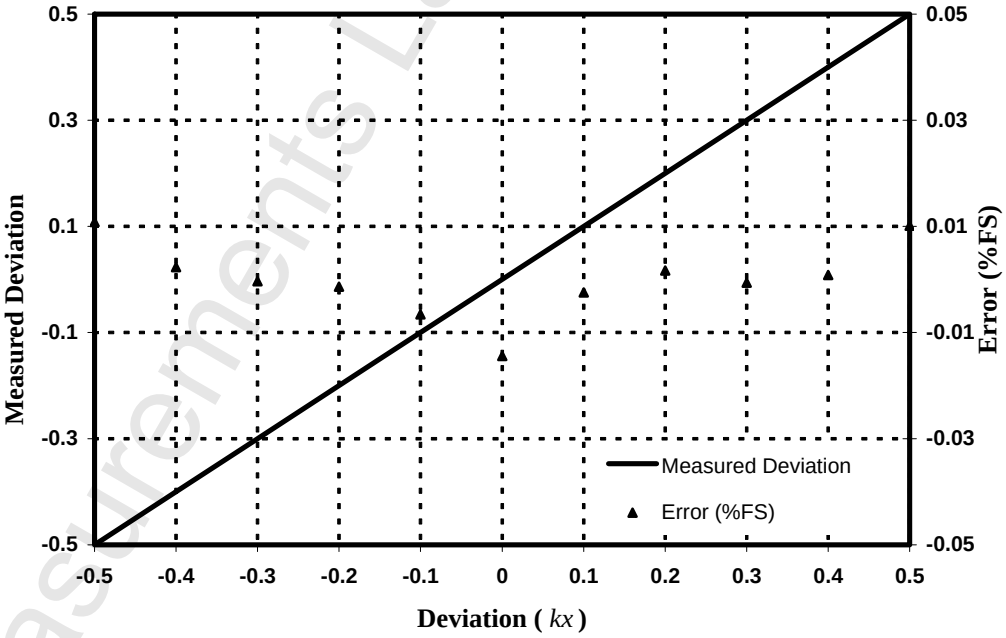


Fig. 6.5 Performance of a sensor with inverse characteristics (Simulation Study)

6.6 Experimental results

A prototype Σ-Δ resistance to digital converter based on the proposed technique was built and tested in the laboratory. The reference voltage $+V_d$ was generated using the reference diode LM385-2.5, buffered with a voltage follower (opamp OP07). $-V_u$ was obtained with the help of a unity gain inverter realized with a second OP07. The magnitude of $-V_u$ was trimmed to obtain a match (up to 5 digits) between the magnitudes of $+V_d$ and $-V_u$. The MAX4680 (possessing a low ON resistance of 1.25 Ω) was employed for the SPDT switches. A third OP07 served as the opamp OA. The value of the feedback capacitor was chosen as 0.33 μF, to limit the maximum change in the integrator voltage per clock cycle to be less than the slew rate of the OP07. An LM311 served as the comparator (OC) and the CD4013 [106] was used for the D-flip-flop. To extract the average of the bit-stream ($\bar{y}$), the IC AD1556 was employed.

The AD1556 implements a Finite Impulse Response (FIR), linear phase, equi-ripple, low-pass filter and decimator [107]. The decimation ratio for the first stage is 128 while for the second stage it is 8. A clock of 1.024 MHz is specified for the AD1556. Taking into consideration the slew rate of the OP07 used in the circuit, it was however decided to operate at a much lower frequency of 80 kHz, which was felt to be quite sufficient for our requirements. The digital filter used this clock and also provided an output clock which was $0.25*(f_{in})$ = 20 kHz. This signal was used to trigger the D-flip-flop.

A suitable program was written and burnt into a PIC16F877A microcontroller to read the output $\bar{y}$ from the AD1556, compute and then, display $(1-2\bar{y})$ on a 5-digit seven segment display. The conversion time of the prototype Σ-Δ RDC was typically 40 ms.

The prototype developed was tested with resistive sensors possessing linear as

well as inverse characteristics. The sensor resistances were set up using two, precision decade resistance boxes from Otto Wolff, Germany, having a resolution of 1 Ω and an accuracy of ± 0.01 %. The nominal value of the resistances was selected as 600 Ω and R_1 and R_2 were varied up to 300 Ω in steps of 6 Ω, to simulate a kx variation in the range of ± 0.5, with increments of + 0.01. The SDRDC was found to provide a linear digital output in both cases. Typical waveforms obtained from the prototype, at the outputs of the integrator and the D-flip-flop (***y***) are shown in Fig. 6.6. The average of ***y*** was computed and the corresponding value of kx was calculated. The output characteristic along with the relative error of the prototype SDRDC is depicted in Fig. 6.7. The worst case, full-scale error was found to be less than ± 0.08 %, validating the analysis as well as the simulation study.

Development of new resistive sensors and associated signal conditioning circuits has been discussed in this and the previous four chapters. The concluding chapter briefly summarises the contributions in the thesis and outlines the scope for further research in this area.

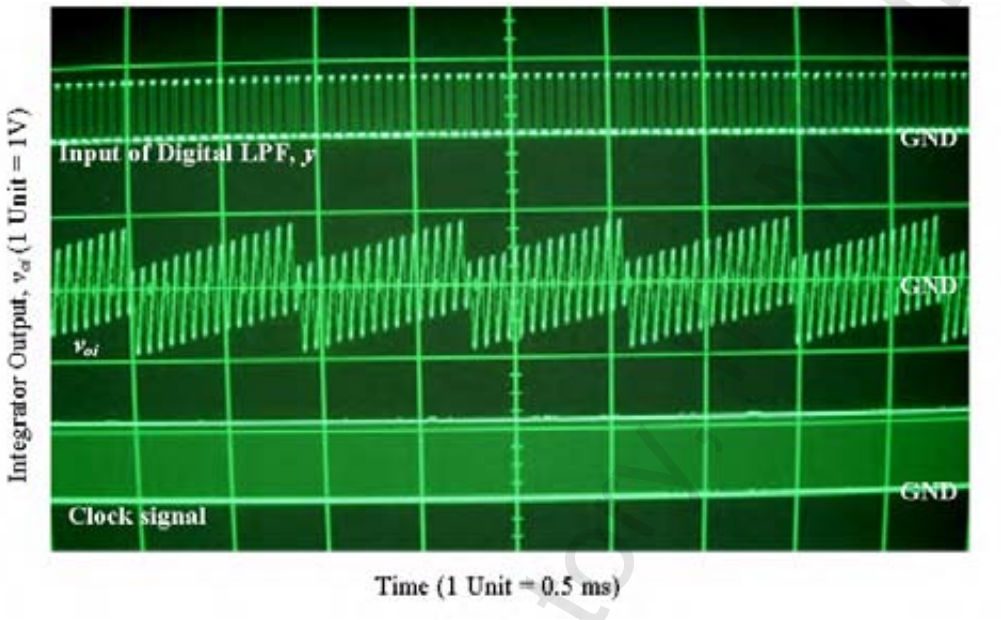


Fig. 6.6 Output of the D Flip-flop (y) and the integrator (v_{oi}) along with the clock signal – from the prototype SDRDC

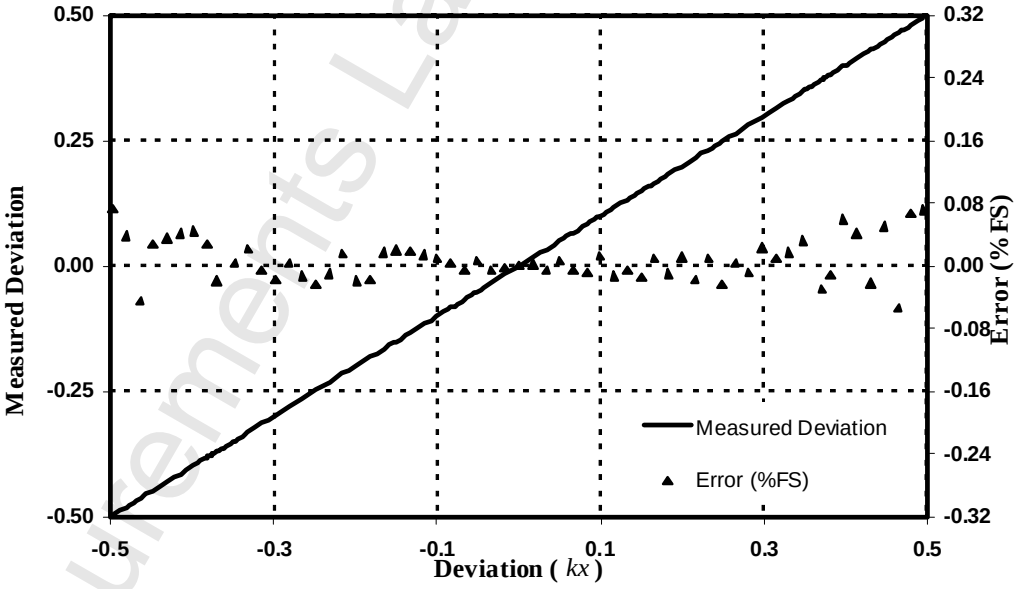


Fig. 6.7 Output and error characteristics of the prototype SDRDC

7.Summary and Conclusions

7.1 Thesis summary

Resistive type transducers are widely used in control and instrumentation applications due to their simplicity, ease of operation as well as the stable nature of their input-output characteristics. In a typical resistive type transducer, which could be of the single element or of the differential kind, the resistance of the sensor varies in proportion to the changes in the measurand. Signal conditioning circuits which can convert this change in resistance directly into a digital output would be highly desirable. It would be advantageous if this aim could be accomplished without major modifications to existing infrastructure. The research reported in this thesis is in this direction.

The problem of a nonlinear characteristic, which is one of the major disadvantages of a traditional Wheatstone bridge based signal conditioning circuit employed with a single element resistive sensor, has been taken up first and dealt with in Chapter 2. This drawback is overcome by making use of a novel feedback compensation scheme, which senses the output of the bridge and utilises a part of it to excite the bridge so as to significantly reduce the nonlinearity. The scheme is first simulated and then prototyped, both with and without feedback compensation, to demonstrate that the proposed scheme delivers results which are more than an order of magnitude better than those obtained without compensation. The feedback compensation scheme presented also compares very favourably with other methods which are presently available. An added advantage is that the proposed circuit does not modify an existing Wheatstone bridge circuit, but simply makes use of an additional summer. The circuit was analysed for major sources of errors and it was demonstrated that the precision with which the circuit is compensated was the largest single source of

error in the circuit.

The digitisation of the output of a single element resistive sensor like the RTD was taken up next, in Chapter 3. The common dual slope integrating analog to digital converter is suitably modified to accept the resistive sensor to provide a digital output which is linear with the measurand. By appropriately switching reference voltage supplies of the required polarity to the resistive sensor, an output is obtained in terms of a measured time period, which is directly proportional to the measurand. Major sources of errors in the circuit were identified and expressions obtained to quantify their effects. The dual slope resistance to digital converter was simulated before being prototyped. The results of both the simulation as well as the experiments conducted on the prototype are presented.

Chapter 4 dealt with the problem of the simultaneous linearisation and digitisation of the output of a nonlinear but popular resistive sensor, namely, the thermistor. Assuming an inverse exponential temperature-resistance characteristic for the thermistor, it was incorporated into a logarithmic amplifier, the output of which was then manipulated to obtain a temperature to time converter such that the time period was linear with the temperature being measured. The circuit was analysed and the stability of the reference voltages was determined to be the major source of error in the output. The linearising digital converter for thermistors was simulated and then tested by building a prototype unit. The results of the experiments conducted on the prototype, both over a large dynamic range of the temperature and a shorter range with smaller increments establish the practicality of the proposed technique.

Direct resistance to digital converters suitable for a differential resistive sensor are presented and discussed in the next two chapters with Chapter 5 dealing with the dual slope integrating technique. The conventional dual slope ADC is modified to accept a

differential resistive sensor as part of the integrator. Suitable logic circuitry have been used to sequence and switch the appropriate reference voltage to the sensor so that the final output which is a measured time period, is directly proportional to the measurand. An analysis of the circuit identifies the major sources of error in the output. Results of simulation as well as experiments conducted on a prototype have been presented.

To handle rapidly changing inputs, a modified sigma-delta analog to digital converter has been proposed to digitise the output of a differential resistive sensor. The details are presented in Chapter 6. The integrator of a normal sigma-delta converter has been modified so that it included the elements of the differential resistive sensor. The output of the integrator is oversampled and then filtered to remove the high frequency components so that a digital output which is proportional to the quantity being measured is obtained. The circuit was thoroughly investigated for errors, including stray capacitances. It was then simulated before being prototyped using the characteristics of a regular strain gage sensor. Both the simulation results and prototype characteristics are presented for analysis.

All the circuits designed have been prototyped using off-the-shelf, inexpensive and easily available components and have been rigorously tested. The maximum errors produced by the prototype resistance to digital converters are listed below:

Type of Resistance to Digital Converter	Maximum Error (% FS)
Single Element type	± 0.20 %
Thermistor	± 0.20 %
Differential type	± 0.35 %
Sigma-Delta Converter	± 0.08 %

The maximum nonlinearity in the Wheatstone bridge with a single element resistive sensor after it has been feedback compensated is reduced to ± 0.04 %.

The principle of the dual slope integrator has been judiciously employed in order to overcome any errors due to component variations. The error analysis of all the

circuits presented in the thesis indicates that the mismatch in the magnitudes of the reference voltages constitutes one of the biggest sources of error. It can therefore be concluded that the use of reference voltage sources with high stability, of the order of parts per million, that are easily available today as well as proper circuit layout practices will go a long way towards improving the performance of the circuits developed. Components used in the circuits should be of better tolerances in order to ensure that the circuits conform to specifications.

The table below compares the results obtained using the circuits presented in the thesis with those reported in literature. As can be seen, even with the rudimentary practises used, the signal conditioning circuits described in this thesis, produce comparable, if not better, results.

	Best Results	
	Thesis	**Literature**
Wheatstone Bridge Linearisation	Nonlinearity = 0.04%	Non-linearity = 0.0025% *[19]
Thermistor Linearisation	Error = 0.2%	Error = 0.35% [80]
DSRDC for Single Sensor	Error = 0.2%	Error = 1%
DSRDC for Differential Sensor	Error = 0.35%	Error = 0.2% (with three slopes)
Sigma-Delta RDC	Error = 0.08%	No data for comparison

* Results for a Strain Gage Signal Conditioning IC which can only handle bridges with $\gamma = 1$.

7.2 Conclusions

The research reported in this thesis establishes that it is possible to :

(i) Linearise the output of a Wheatstone bridge based analog signal conditioning circuit operating with a single element resistive sensor by using the feedback compensation scheme.

(ii) Combine the analog signal conditioning aspect of a resistive transducer

with the requirement of analog to digital conversion and obtain a less complex solution in the form of a "direct resistance digital converter".

(iii) Suitably modify the popular dual slope as well as sigma-delta type analog to digital converters and realize appropriate "direct resistance to digital converters" suitable for single element as well as differential types of resistive sensors.

(iv) Suitably modify the popular dual slope analog to digital converter and realize a "linearising direct resistance to digital converter" suitable for a thermistor.

(v) Appropriately modify the Σ-Δ ADC to obtain a direct resistance to digital converter for a differential resistive sensor.

7.3 Publications

The work presented in this thesis has resulted in the following publications :

Journals :

Mohan N.M., George B., and Kumar V.J., "Direct Digital Converter for a Single Element Resistive Sensor", *IEEE Trans. Instrum. Meas*. (Accepted for publication).

Mohan N.M., George B. and Kumar V.J., "Analysis of a Sigma-Delta Resistance to Digital Converter for Differential Resistive Sensors", *IEEE Trans. Instrum. Meas.*, vol. 58, # 5, May 2009, pp. 1617-1622.

Conferences :

Mohan N.M., Venmathi G., Vani M., Sankaran P. and Kumar V.J., "Linearising Resistance to Digital Converter suitable for Thermistors", *27th IEEE International Instrumentation and Measurement Technology Conference (I^2MTC)*, Austin, Texas, May 2010. (Accepted for publication)

Mohan N.M. and Kumar V.J., "Direct Digital Converter for Single Active Element Resistive Sensor", *Proc. 26th IEEE International Instrumentation and Measurement Technology Conference (I^2MTC)*, Singapore, May 5-7, 2009, pp. 828-831.

Mohan N.M., Geetha T., Sankaran P. and Kumar V.J., "Linearisation of the Output of a Wheatstone Bridge for a Single Active Sensor", *Proc. 16th IMEKO TC4 Symposium*, Florence, Italy, September 12-14, 2008, pp. 25-29.

Mohan N.M., George B. and Kumar V.J., "A Sigma-Delta Resistance to Digital Converter for Differential Resistive Sensors", *Proc. 25th IEEE International*

Instrumentation and Measurement Technology Conference (I^2MTC), Victoria Island, Canada, May 12-15, 2008, pp.1159-1161.

Mohan N.M., George B., and Kumar V.J., "Dual Slope Resistance to Digital Converter", *Proc. 24th IEEE Instrumentation and Measurement Technology Conference (IMTC)*, Poland, May 1-3, 2007, pp.1-5.

7.4 Scope for further work

One of the reasons for the low errors reported with the digital converters discussed in this thesis is the relatively long, fixed integration periods used in the process. While time periods in the range of 100 ms may not hinder the converters in handling the inputs from the resistive sensors in most of the cases, there may arise occasions when the measurand changes rapidly. Under such circumstances, a digital converter with a fixed time period of 100 ms would not be an acceptable solution. It would be fruitful to work on a direct resistance to digital converter that would be able to accept such rapid changes in the input signal, without sacrificing either accuracy or resolution. It might also be worthwhile to extend the idea of direct digital converters to inductive transducers like the linear variable differential transformers.

A major area of application of resistive sensors is in biomedical instrumentation and devices, where the emphasis is on low power budgeting and miniaturisation, in order to pack the maximum functionality in the limited space available. It would be interesting to work on developing a low cost, integrated, system-on-a-chip, digital converter which could accept inputs from resistive sensors and provide a linear digital output over the entire dynamic range of the sensor.

A rewarding line of research would be to develop a direct digital converter which could handle both single element and differential type resistive sensors, with minimum external components. Moreover, a converter which uses only one reference voltage in the conversion process would go a long way towards ensuring better performance as it has been determined that the mismatch in the magnitudes of the reference voltages is the

major source of error in the direct digital converters presented in this thesis. It is expected that further work along these lines would lead to compact instrumentation systems built around resistive transducers which possess a basic advantage of infinitesimally small resolution.

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Curriculum – Vitae

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