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Design and Implementation of a Signal Conditioning Operational Amplifier for a Reflective Object Sensor

Ankit Master
University of Tennessee - Knoxville, amaster@utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Ankit Master entitled "Design and Implementation of a Signal Conditioning Operational Amplifier for a Reflective Object Sensor." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Syed K. Islam, Aly E. Fathy

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Design and Implementation of a Signal Conditioning Operational Amplifier for a Reflective Object Sensor

A Thesis Presented for the
Master of Science Degree
The University of Tennessee, Knoxville

Ankit Chandrakant Master
December 2010

Thank you Chandra!

ABSTRACT

Industrial systems often require the acquisition of real-world analog signals for several applications. Various physical phenomena such as displacement, pressure, temperature, light intensity, etc. are measured by sensors, which is a type of transducer, and then converted into a corresponding electrical signal. The electrical signal obtained from the sensor, usually a few tens mV in magnitude, is subsequently conditioned by means of amplification, filtering, range matching, isolation etc., so that the signal can be rendered for further processing and data extraction.

This thesis presents the design and implementation of a general purpose op amp used to condition a reflective object sensor's output. The op amp is used in a non-inverting configuration, as a current-to-voltage converter to transform a phototransistor current into a usable voltage. The op amp has been implemented using CMOS architecture and fabricated in a 0.5-µm CMOS process available through MOSIS.

The thesis begins with an overview of the various circuits involving op amps used in signal conditioning circuits. Owing to the vast number of applications for sensor signal conditioning circuits, a brief discussion of an industrial sensor circuit is also illustrated. This is followed by the complete design of the op amp and its implementation in the data acquisition circuit. The op amp is then characterized using simulation results. Finally, the test setup and the measurement results are presented. The thesis concludes with an overview of some possible future work on the sensor-op amp data acquisition circuit.

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CHAPTER I Introduction

1.1 Motivation

A sensor is a device that receives a signal or stimulus and responds with an electrical signal. Sensors are often used to measure various physical properties such as temperature, force, position, pressure, light intensity, etc. These signals act as stimulus to the sensor, and the sensor output is conditioned and processed to provide the corresponding measurement of the physical property. The full-scale outputs of most sensors are relatively small voltages, currents, or resistance changes, and therefore their outputs must be properly conditioned before further analog or digital processing can occur. Another important reason for the need for signal conditioning blocks in any data acquisition or measurement system is the non-linearity of the sensor outputs with respect to the applied stimulus. Some of the most fundamental signal-conditioning functions include amplification, level translation, linearization, filtering, impedance transformation and range matching.

Industrial processes often employ sensors in process control systems as a means to measure physical quantities. Conditioning the signal obtained from the sensor is of utmost importance for achieving maximum information out of the signal. In spite of the variety of sensors and their outputs, the ever-so versatile operational amplifiers (op amps) successfully serve as an efficient signal conditioning circuit in most analog/mixed-signal systems. Op amp characteristics such as high input impedance, low input bias current, minimal common-mode gain, high gain-bandwidth, low operating power, low output impedance, and the flexibility offered by this device make it highly conducive for using it as a signal conditioning element. Also, higher levels of integration now allow ICs to incorporate more complex circuits on a single chip. Integrating an op amp with high performance ADCs is relatively easy thereby facilitating the need to have outputs in a digitized format for processing/storage by a computer or a processing unit. The flexibility of op amps thus helps in minimizing the external conditioning circuit inventory. With this motivation, an op amp is the ultimate choice to function as a signal conditioning block for fine-tuning the output of a reflective object sensor and subsequently interfacing it with an ADC to obtain a digitized output for valuable data extraction and interpretation.

1.2 Scope of the Thesis

The purpose of this work is to design and implement an operational amplifier that functions as a signal conditioning circuit for a reflective object sensor's output signal. Specifically, the op amp is designed to be a general purpose signal conditioning block in any measurement or process control system. The op amp configuration and performance in the circuit will be governed by the electrical character of the sensor and its output. Thus, for instance, high impedance sensors such as reflective object sensors, using the op amp as a current-to-voltage converter will prove to be a better signal processing circuit whereas implementing an instrumentation amplifier will be useful for resistive bridge sensors. However, in both cases, assuming that the op amp parameters like gain, slew rate, bandwidth, and offset voltage requirement is the same, then the op amp design remains invariably the same but just the manner in which it is configured will be different for different sensors. Table 1.1 lists the requirements set for the design of this op amp.

1.3 Organization of the Thesis

Chapter 2 commences with a brief overview of the fundamentals of operational amplifiers. It is further supplemented by some circuits denoting the use of op amps in various configurations depending upon the electrical characteristics of the sensor and its output.

Chapter 3 outlines the complete schematic of the designed op amp in detail. The operation of the complete op amp is discussed along with the different circuits used for its characterization. The characterization is documented by means of simulation and the results are shown.

Parameter	Specification
Gain Bandwidth	> 1 MHz
Capacitive Load	50 pF
Minimum Input Common Mode Voltage	0 V
CMRR	> 60 dB
PSRR	> 60 dB
Slew Rate	> 1 V/μs
Open Loop Voltage Gain (A_{OL})	> 80 dB

Table 1.1 Op amp Specifications

Chapter 4 presents the measured results of the op amp as well as those of the complete system. The test setup for each measurement is also described in this section.

Chapter 5 discusses the system application of the data processing system. The sensor is interfaced with the op amp, configured as an I-to-V converter. The output of the op amp is an amplified signal of the low sensor output signal. This op amp signal is hence useful for further digital processing through the use of ADCs.

Chapter 6 concludes the thesis highlighting the results and also describing some future work that can be done for improving the system.

CHAPTER II Sensor Signal Conditioning

This chapter begins with an overview of the fundamentals of the operational amplifier and its performance parameters. It is followed by a detailed discussion of the application of op amps in different sensor signal conditioning circuits. The purpose of this discussion is to highlight the flexibility and versatility of op amps as universal analog signal conditioning blocks. The chapter is concluded by a brief overview of an industrial sensor employed for the purpose of position/distance measurement.

2.1 Operational Amplifiers – Fundamentals

Ideal operational amplifiers are functional blocks that are characterized by infinite voltage gain, infinite input resistance, zero output resistance, infinite bandwidth and zero input bias current [1]. However, in real world applications, practical op amps can only approach these characteristics. Circuits built using an op amp operate in a stable closed loop configuration by utilizing the advantages of negative feedback efficiently. Fig. 2.1 illustrates a functional block diagram of a basic operational amplifier. The input stage, a differential pair, provides the required gain to the input signal and feeds the output signal to the subsequent gain stage of the op amp. The output of the differential stage can be single-ended or differential. The second stage is usually an inverting stage and can offer high gain as well as differential-to-single ended conversion (if necessary). Occasionally, some op amps also have a buffer/output stage that is used to drive resistive loads and high capacitive loads. If included, this stage determines the output swing of the ultimate output signal produced by the op amp. The biasing circuitry provides a stable, quiescent operating point for the entire circuit. Although negative feedback ensures stable operation of the op amp, compensation is used to ensure frequency stability, and improve the op amp characteristics as desired.

Several parameters help us characterize the op amp. Open-loop gain, small-signal bandwidth, settling time, slew rate, PSRR, and CMRR are some of the parameters that give us a measure of the performance of the op amp. The ability of the op amp to provide an accurate closed-loop gain is governed by the open-loop gain (A_{OL}).

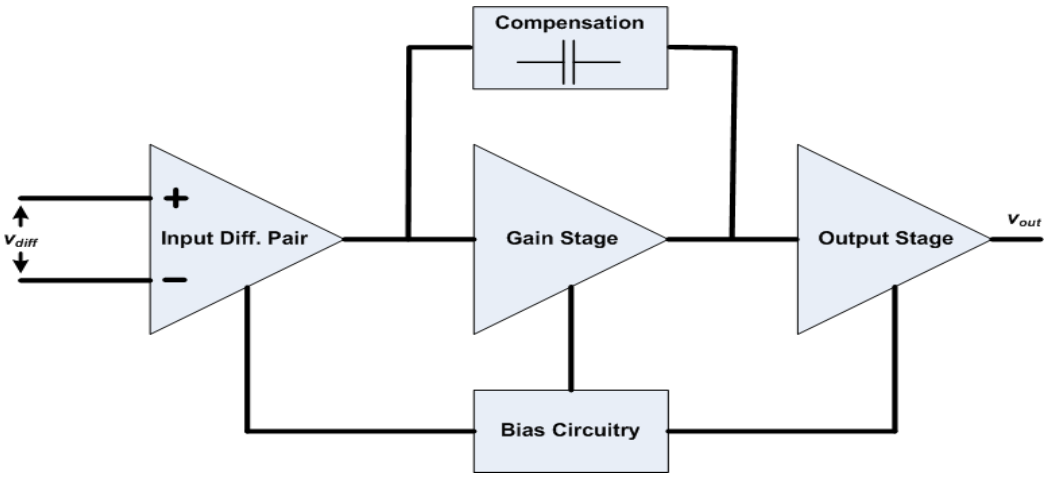

Figure 2.1 Basic operational amplifier

Slew Rate is the maximum rate of change of output voltage. PSRR indicates the ability of an op amp to withstand the variation in power supply voltage. The frequency response of a circuit is characterized by the small-signal bandwidth, phase margin, settling time, and the large signal bandwidth. All these parameters including several others are discussed in the following chapters in detail.

2.2 Signal Conditioning Applications

Different applications often require the need to measure different physical entities from the real world. Examples include distance, position, light intensity, and temperature. Every class of sensor has different electrical characteristics than the other. Also, the form of output may also vary, i.e. some may have a current output while some may generate voltage. However, one aspect shared by all sensors is the weak output signal generated by them. Sensor outputs usually range from few hundreds of μV/μA to tens of mV/mA. Such weak signals need to be conditioned before which they can be utilized to generate useful data. The versatility and flexibility of op amps make them a valuable component of signal conditioning circuits for such weak output signals obtained from sensors.

As stated earlier, the electrical nature of the sensor output differs from one sensor to the other. In most cases, the principle of operation of the sensor determines the nature of sensor output. The nature of the sensor output determines the op amp requirement. Thus, depending on the sensor

output, an op amp can be designed in different configurations to achieve the maximum information out of the sensor output. The following examples are an attempt to understand this very fact.

2.2.1 Semiconductor Temperature Sensors

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about -55°C to +150°C. Typically, semiconductor temperature sensors make use of the relationship between a bipolar junction transistor's (BJT) base-emitter voltage to its collector current [2],

$$V_{BE} = \frac{kT}{q} ln\left(\frac{I_C}{I_S}\right) \tag{2.1}$$

Where k is the Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, and I_S is a current related to the geometry and temperature of the transistors. (This equation assumes a voltage of at least a few hundred mV on the collector and ignores Early effect.) The dependence of the base-emitter voltage on I_S, and hence temperature renders the direct application of this equation useless [2]. However, if we take 'N' transistors identical to the first as seen in Figure 2.2, and allow equal currents flowing in one BJT, as well as the N similar BJTs, then the difference between the respective base-emitter voltages (or ΔV_{BE}) is proportional to absolute temperature and is independent of I_S [2].

$$\Delta V_{BE} = V_{BE} - V_N = \frac{kT}{q}\left[ln\left(\frac{I_C}{I_S}\right) - ln\left(\frac{I_C}{N*I_S}\right)\right] \tag{2.2}$$

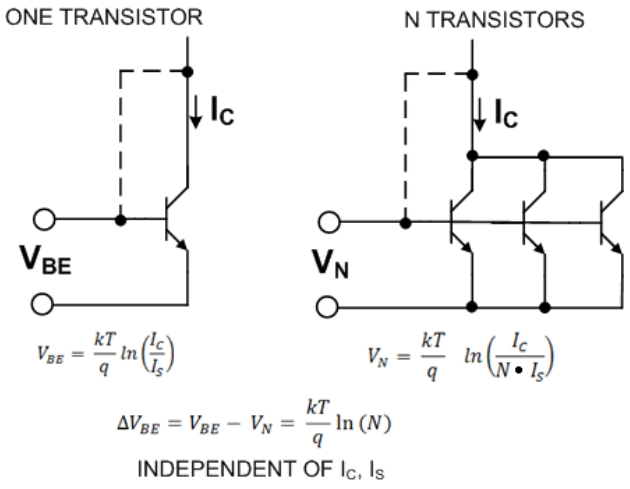

Figure 2.2 Basic Relationships for BJT-based semiconductor temperature sensors

$$\Delta V_{BE} = V_{BE} - V_N = \frac{kT}{q} ln \left[\left(\frac{I_C}{I_S} \right) \Big/ \left(\frac{I_C}{N * I_S} \right) \right] = \frac{kT}{q} ln\,(N) \tag{2.3}$$

As evident from the equation above, ΔV_{BE} is dependent only on the transistor emitter area ratio N and the absolute temperature T. The only variable here being T as N is fixed for a given design. The equation above is implemented as shown in the Figure 2.3 and is popularly known as the "Brokaw Cell", after its inventor [2].

As seen in the circuit across resistor R_2,

$$\Delta V_{BE} = V_{BE} - V_N \tag{2.4}$$

and the emitter current through Q_2 is $\Delta V_{BE}/R_2$. The op amp's servo loop and the two resistors 'R' force an identical current to flow through Q_1.

The corresponding voltage developed across R_1 is V_{PTAT}, a voltage proportional to absolute temperature (PTAT). This is given by,

$$V_{PTAT} = 2\frac{R_1}{R_2}(V_{BE} - V_N) = 2\frac{R_1}{R_2}\frac{kT}{q}\ln(N) \tag{2.5}$$

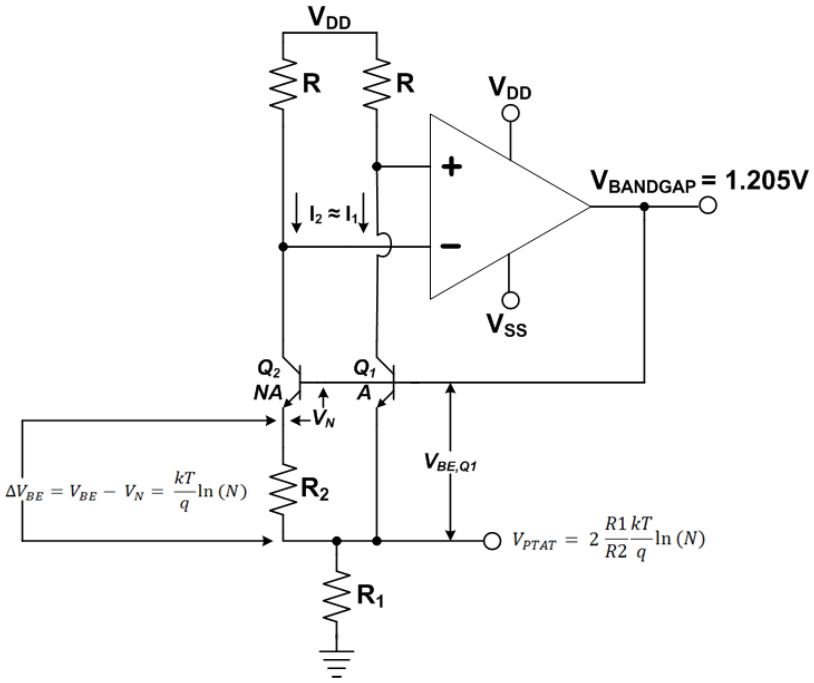

Figure 2.3 Brokaw Cell [2]

As seen from the circuit [2], $V_{BANDGAP}$ which appears at the base of Q_1 is the sum of $V_{BE(Q1)}$ and V_{PTAT}. The voltage $V_{BE(Q1)}$ is complementary to absolute temperature (CTAT), and summing it with a properly proportioned V_{PTAT} across R_1 gives a bandgap voltage approximately constant with respect to temperature. If designed appropriately – proper choice of $\frac{R_1}{R_2}$ ratio and N – such that $V_{BANDGAP}$ is equal to the silicon bandgap voltage of 1.205 V, then the voltage is independent of temperature. Note that this circuit is useful as a basic silicon-based temperature sensor taking direct or scaled use of the V_{PTAT} voltage.

2.2.2 High Impedance Charge Output Sensors

Piezoelectricity is the ability of some materials to generate an electric field in response to applied mechanical strain. Sensors operating on this piezoelectric effect are called piezoelectric sensors. These are high impedance transducers and require an amplifier that converts a transfer of charge into a voltage change. Thus, depending on the nature of the output of the piezoelectric sensor, an op amp is configured as a charge sensitive amplifier as shown in Figure 2.4.

As seen from the circuit diagram, the op amp is, simply stated, an inverting integrator. Connecting the op amp as an integrator helps perform a time integration of the electric current, thus measuring a total electric charge. It acts as an amplifier whose equivalent input impedance is a capacitive reactance that is very high at low frequencies. Thus, the current integrator basically obtains a voltage proportional to the charge and provides a low output impedance.

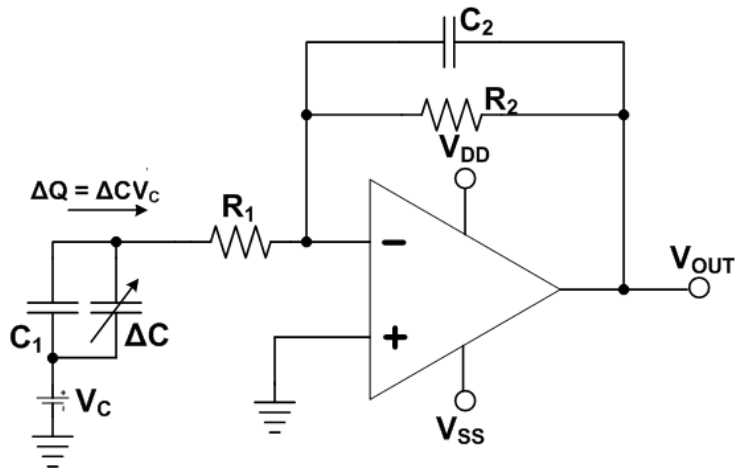

Figure 2.4 Charge Amplifier [2]

There are two types of charge transducers: capacitive and charge-emitting [2]. In a capacitive transducer, the voltage across the capacitor (V_C) is held constant. The change in capacitance, ΔC, produces a change in charge, given by [2]

$$\Delta Q = \Delta C \bullet V_C \tag{2.6}$$

This charge is transferred to the op amp as a voltage, given by

$$\Delta V_{OUT} = \frac{-\Delta Q}{C_2} = \frac{-\Delta C \cdot V_C}{C_2} \tag{2.7}$$

Charge-emitting transducers produce an output charge, ΔQ, and their output capacitance remains constant. This charge would normally produce an open-circuit output voltage $\Delta Q/C$ [2]. However, due to virtual ground effect of the op amp, the charge transferred to capacitor C_2 produces an output voltage given by [2]

$$\Delta V_{OUT} = \frac{-\Delta Q}{C_2} \tag{2.8}$$

The upper cut-off frequency is dominated by the feedback *RC* network while the lower cut-off frequency is dominated by the input *RC* network.

$$f_2 = \frac{1}{2\pi R_2 C_2} \tag{2.9}$$

$$f_1 = \frac{1}{2\pi R_1 C_1} \tag{2.10}$$

2.2.3 Resistive Bridge Sensors

Resistive elements are some of the most common sensors. They are inexpensive and relatively easy to interface with signal-conditioning circuits. Resistive elements can be made sensitive to temperature, strain, and light. Thus, physical phenomena such as fluid or mass flow, dew-point humidity, etc. can be measured using resistive elements. The most common and easiest method for measuring small resistance changes accurately is by the use of a resistance bridge. A basic Wheatstone bridge is a prime example of a resistance bridge [2].

A basic bridge amplifier, as shown in Figure 2.5, may be used to amplify the output of a single-element varying resistive bridge. This circuit is relatively simple wherein the output from two nodes of the balanced bridge is fed differentially to the op amp. Under balanced condition, assuming matched resistors, the common-mode signal should be rejected by the op amp resulting in zero output at the op amp [2].

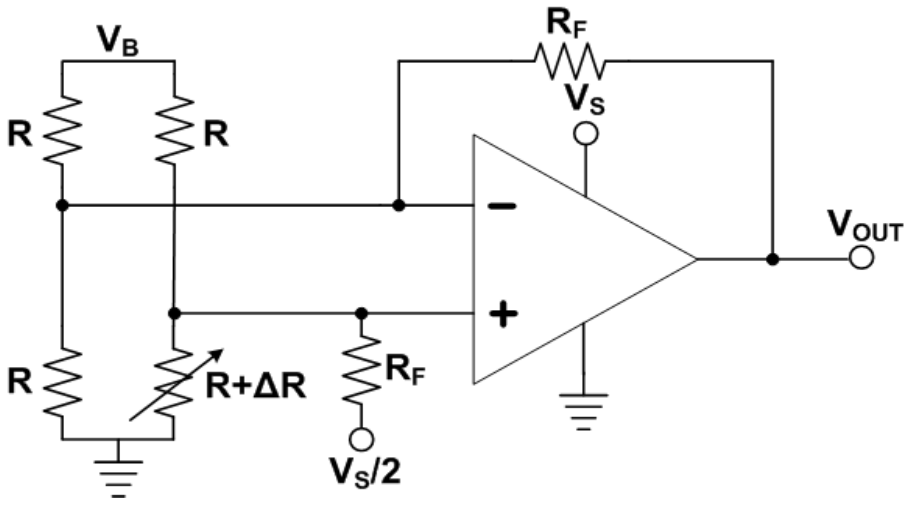

Figure 2.5 a single op amp Bridge Amplifier [2]

However, resistor matching is difficult to achieve resulting in poor common mode rejection (CMR). Also, loading due to R_F and the op amp bias current also results in poor accuracy. Dependance of gain upon the bridge resistances and R_F results in non-linear output [2].

A much better approach is to use an instrumentation amplifier for the required gain, as shown in Figure 2.6 [2]. The gain of the op amp is set with a single resistor, R_G. Since, the amplifier provides dual, high-impedance loading to the bridge nodes, it does not unbalance or load the bridge. This circuit not only provides better accuracy but also helps the common mode rejection.

Using Kirchoff's current law around the resistive bridge, the output voltage for the bridge can be found. This output voltage of the resistive bridge when fed to the input of the op amp is amplified by the gain of the op amp to yield the output signal,

$$V_{OUT} = \frac{V_B}{4}\left[\frac{\Delta R}{R+\frac{\Delta R}{2}}\right][Gain] \tag{2.11}$$

The bridge, as seen from the figure, is voltage driven by the voltage V_B [2]. This voltage can optionally be used for an ADC reference voltage, in which case it also is an additional output, V_{REF} [2].

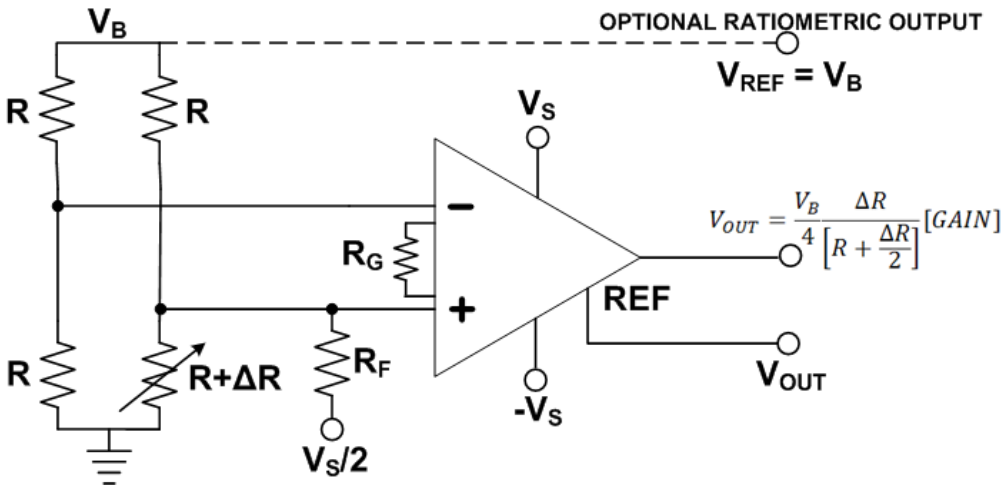

Figure 2.5 Instrumentation amplifier used for Bridge network [2]

2.3 Industrial Sensor Illustration

This section gives an example of an industrial sensor being employed in the industry currently for the purpose of distance measurement. Different modules operate simultaneously along the assembly line in order to build a final product. Consider a production plant involved in the manufacturing of the Pull-Ups® Training pants. The product manufacturing involves the base outer cover poly running along the conveyor from the start of the machine line. Different modules like the Super-Absorbent Material (SAM), fluff forming module, waist elastic applicator module, along with several others, then perform operations on the poly to ensure smooth build-up of the product, layer-by-layer. The final product is then packaged at the end of the line and delivered in boxes. However, in order to ensure flawless manufacturing of the product, the raw materials flowing along the conveyor have to be monitored continuously so as to adhere to the standards of the product. This monitoring involves the use of distance measurement sensors, infrared sensors, gray checkers, and opacity sensors.

A distance measurement sensor is illustrated in the Figure 2.6 [3] below. A short electrical pulse drives a semiconductor laser diode to emit a pulse of light. The emitted light is collimated through a lens, which produces a very narrow laser beam. The laser beam bounces off the target, scattering some of its light through the sensor's receiving lens to a photodiode, which creates an electrical pulse [3]. The time interval between the transmitted and received electrical pulses is used to calculate the distance to the target, using the speed of light as a constant [3].

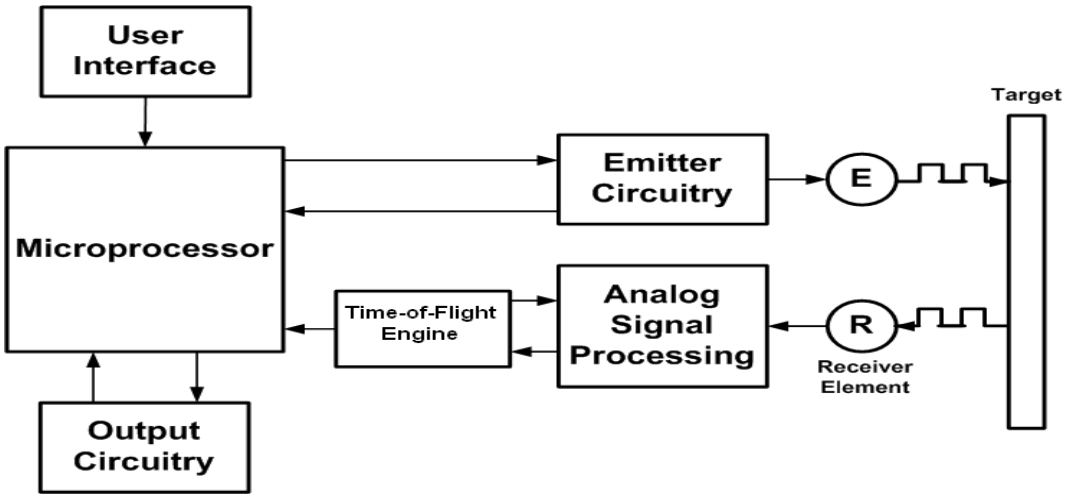

Figure 2.6 Time-of-Flight Sensor (Distance Measurement) [3]

This measurement technique is used to control the rate for unwinding the outer cover poly of the spindle. Assuming that the sensor is situated somewhere along the rim of the disc, longer the time required by the laser beam to reflect back from the circumference of the cloth poly implies a smaller diameter of the cloth unwind and hence lower the rate of rotation of the spindle. As seen from the example above, industrial applications often employ sensors to measure different physical phenomena for process control. Also, as shown in the previous sections of this chapter, an op amp is a highly versatile and flexible component which can be utilized for the implementation of such data acquisition systems easily. Thus, the following chapter discusses the design of such an op map which is used for processing the signal obtained from a reflective object sensor.

CHAPTER III Op Amp Design

This chapter discusses the design and implementation of the general purpose op amp in full detail. The chapter begins with an analysis of the complete op amp schematic which is followed by the derivation and explanation of the various performance parameters of the op amp. The last section of the chapter consists of the simulation results and presents the layout and implementation of the design.

3.1 Op Amp Architecture

The ultimate goal of any system is for it to produce the desired end results which are termed as specifications or design requirements. For an op amp design, the procedure is an iterative process which involves selection of an appropriate architecture followed by correct device sizing. The design is then tested rigorously via simulation to ensure that it is achieving its goal of meeting the required specifications. The design requirements listed in Table 1.1 are considered in detail to devise the architecture.

3.1.1 Input Stage

The input stage of any op amp is usually dictated by noise, input common-mode range and gain. The purpose of this op amp is to serve as a signal conditioning component in process control systems or data acquisition systems. Thus, the architecture was attempted to be as simple as possible so as to meet the specifications for the design. Topologies such as single-ended stage, simple differential stage, differential-cascode and folded-cascode are commonly used as input stages.

Bearing in mind the principal function of the op amp being to sense the weak sensor signal, it is logical for the CMOS differential input pair to be ground sensing. Since the PMOS device is a true-ground device, the op amp should have a PMOS input pair to ensure a minimum input common range voltage of 0 V. Although various input stages comprising of differential cascode and folded cascode offer advantages such as high output impedance, high gain and good ICMR, wide output swing, respectively, repetitive iterations of the op amp schematic with a simple single-ended output for the input stage helped us achieve all the specifications that were laid out before the start of the design.

Thus, after meeting all the requirements of the design and keeping simplicity in focus, a single-ended PMOS differential input pair was selected as the input stage of the op amp.

3.1.2 Output Stage

The important criteria for designing an output stage are good current driving capability, low power dissipation, high gain delivering ability, and good stability. The output stage used in this op amp employs a single output NMOS transistor driven by two PMOS transistors in the output leg of the op amp. It is a class-A type of output stage. Pole splitting [4] has been used as the compensation technique for asserting the dominant pole of the system. Since the introduction of additional capacitance on the output transistor introduces a virtual zero due to Miller capacitance, an NMOS-modeled resistor is also connected in the feedback path of the output transistor. The op amp is designed to drive a load of 50 pF.

3.1.3 Current Mirror

The current mirror used in this op amp is a wide-swing cascode circuit known as the Sooch current mirror (named after its inventor). Refer Figure 3.1 for the Sooch current mirror. The major advantages of using this current mirror is the elimination of the possibility of mismatch between the two branch currents and thus, reduce power consumption. This is achieved by maintaining the desired difference between the gate voltages of P_7 and P_8 of one overdrive voltage, V_{ov}. In order to achieve this, it is required to bias M_1 at the active region and subsequently requiring gate voltages of P_7 and P_8 to be $V_t + V_{ov}$ and $V_t + 2V_{ov}$ respectively [5]. As shown in Figure 3.1, since P_{12} is diode connected, it operates in the saturation region. Since the gate-source voltage of P_{12} is equal to the gate-drain voltage of P_{11}, a channel exists at the drain of P_{11} when it exists at the source of P_{12}. In other words, P_{12} forces P_{11} to operate in the triode region [5].

To obtain the drain-source voltage of P_{11} to be V_{ov}, we need to design the aspect-ratio of the transistors appropriately. Since P_{12} operates in the active region,

$$I_{BIAS} = \frac{k'}{2}\left(\frac{W}{L}\right)_{12}(V_{GS12} - V_t)^2 \tag{3.1}$$

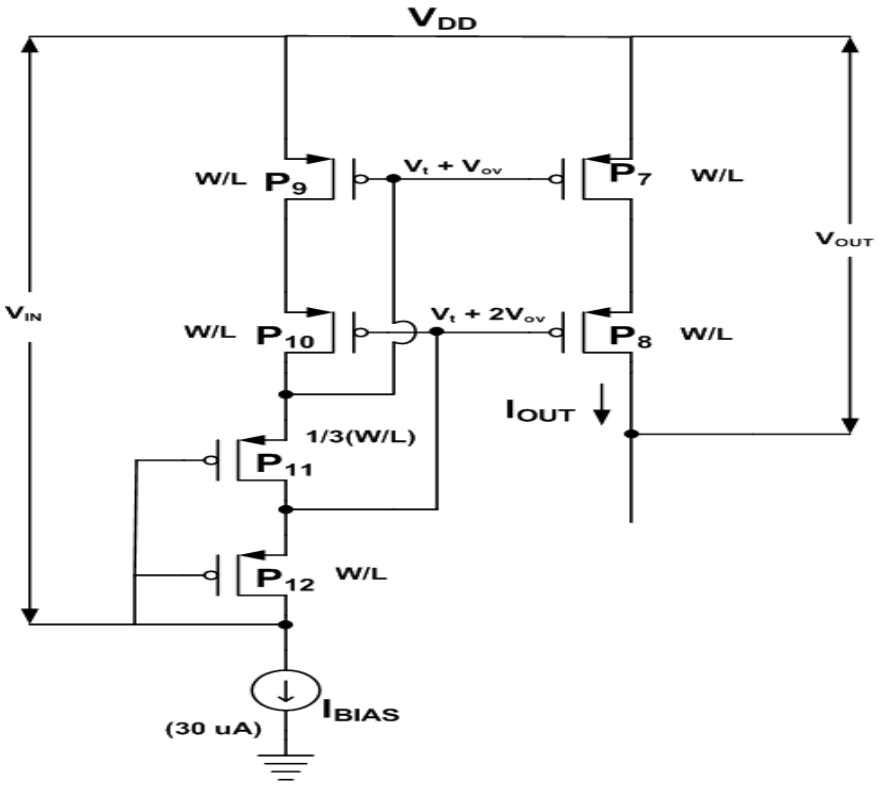

Figure 3.1 Sooch current mirror [5]

Since P_{11} operates in the triode region,

$$I_{BIAS} = \frac{k'}{2}\left(\frac{W}{L}\right)_{11}\left((V_{GS12} - V_t)V_{DS11} - (V_{DS11})^2\right) \tag{3.2}$$

The goal is to set [5]

$$V_{DS11} = V_{ov} \tag{3.3}$$

when

$$V_{GS12} = V_t + V_{ov} \tag{3.4}$$

From eqn. (3.3) and (3.4),

$$V_{GS11} = V_{GS12} + V_{DS11} = V_t + 2V_{ov} \tag{3.5}$$

Substituting eqn. (3.2) – (3.5) into eqn. (3.1) gives,

$$\frac{k'}{2}\left(\frac{W}{L}\right)_{12}(V_{ov})^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_{11}(2(2V_{ov})V_{ov} - (V_{ov})^2) \tag{3.6}$$

which is further simplified to [5],

$$\left(\frac{W}{L}\right)_{11} = \frac{1}{3}\left(\frac{W}{L}\right)_{12} \tag{3.7}$$

3.2 Complete Schematic

The complete schematic of the designed op amp is shown in figure 3.2. The input stage of the op amp consists of PMOS differential input pair transistors P_1 and P_2 loaded by current mirror N_2 and N_3. A cascode tail current source consisting of PMOS transistors P_5 and P_6 is utilized for the differential input pair. The external current bias of 30 µA is used to set the current in the reference branch of the Sooch current mirror. The op amp has a class-A output stage consisting of a simple common-source amplifier with a cascode current source load. The output transistor N_1 is biased by the output of the input stage. Frequency compensation is implemented using Miller capacitor C_1 and its corresponding zero-nulling active resistor N_6. This tracking compensation is biased by NMOS transistors N_4 and N_5. The performance parameters of the op amp are analyzed in this section.

3.2.1 Open-loop Gain

An expression for the mid-band gain of the op amp can be derived by considering the gain of the individual stages such as the input and output stages. The mid-band gain seen by the inputs to the input stage is symmetrical and can be expressed as,

$$A_{V1} = -(g_{m,P2})(r_{o,P2} \,||\, r_{o,N2}) \tag{3.8}$$

Due to the matching of P_1 and P_2,

$$g_{m,P1} = g_{m,P2} \tag{3.9}$$

The output impedance of the output stage is given as,

$$r_{out,cascode} = (g_{m,P4})(r_{o,P4})(r_{o,P3}) \tag{3.10}$$

The voltage gain of the output stage is thus given by,

$$A_{V2} = -(g_{m,N1})(r_{out,cascode} \,||\, r_{o,N1}) \approx -(g_{m,N1})(r_{O,N1}) \tag{3.11}$$

Thus, the overall mid-band gain offered by the op amp is equal in magnitude for both differential inputs and the overall gain is given by,

$$|A_{V,total}| = |A_{V1}A_{V2}| = (g_{m,P2})(g_{m,N1})(r_{o,N1})(r_{o,P2} \,||\, r_{o,N2}) \tag{3.12}$$

Using appropriate values for g_m and r_o, the open loop-gain of the op amp is calculated in Appendix, A.1.

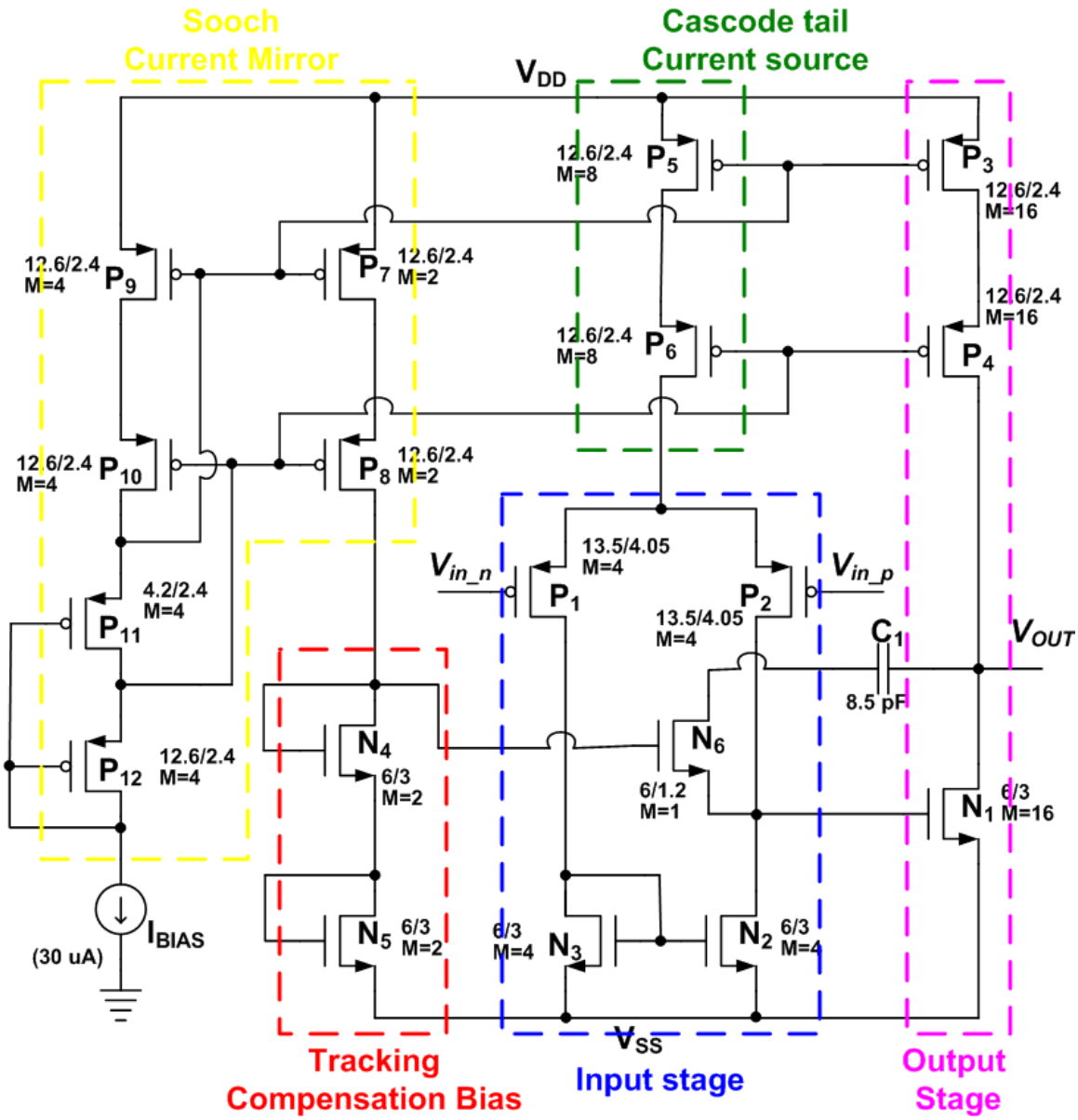

Figure 3.2 Complete schematic of the op amp

3.2.2 Frequency Compensation

As seen in figure 3.2, the op amp has bandwidth-limiting pole at the drain of N_1/P_4. Frequency compensation is provided using a pole-splitting Miller capacitor and its corresponding zero-nulling MOS active resistor. The value of the compensation capacitor is found using the requirement for frequency stability, as in [6]

$$C_C = \sqrt{\frac{g_{m,N1}}{g_{m,P4}} C_{d,N1,P4} C_L} \tag{3.13}$$

where $g_{m,N1}$ and $g_{m,P4}$ are the transconductances of the output drivers, $C_{d,N1,P4}$ is the output node capacitance and C_L is the load capacitance. The value of the zero-nulling resistor needs to be maintained across any variation in process, temperature, and supply voltage (PTS) in order to ensure that the pole-zero doublet does not adversely impact the settling time of the op amp [7, 8]. The tracking compensation implemented here [7] enables effective biasing of the active resistor across any variation in PTS. The value of the active resistor is made to track the g_m of N_1. This is achieved through careful device sizing and careful device matching of N_1, N_2, and N_4 with N_6. The pole-zero cancellation is a function of device sizes and the relative values of the bias currents and capacitors that can be controlled by careful matching. Hence, the value of the active resistor is independent of variations in process, temperature, and supply voltage.

3.2.3 Input Common Mode Range

The PMOS differential input pairs provide the feasibility to extend the lower ICMR to VSS. This is of prime importance in this application considering that the op amp is designed to sense the very low output signals of sensors. Connecting the substrates of the input devices to V_{DD} also improves the ICMR by increasing the threshold devices due to body effect. The minimum value of the input common mode range is given by,

$$\begin{aligned} V_{ICMR,min} &= V_{SS} + V_{SG,P1} - V_{SD,P1} - V_{GS,N3} \\ &= V_{SS} + |V_{TH,P1}| + V_{SD,P1} - V_{SD,P1} - V_{GS,N3} \\ &= V_{SS} + |V_{TH,P1}| - V_{TH,N3} - V_{OV,N3} \end{aligned} \tag{3.14}$$

From (3.14), it is evident that threshold voltage impacts the lower limit of ICMR. Note that $V_{ICMR,min}$ approaches V_{SS}.

The maximum limit of ICMR is determined by the V_{SG} of the input pair and the tail current source bias. It can be expressed as,

$$V_{ICMR,max} = V_{DD} - V_{SG,P1} - V_{SDsat,P5} - V_{SDsat,P6}$$

$$V_{ICMR,max} = V_{DD} - \left(V_{SDsat,P1} + |V_{TH,P1}|\right) - V_{SDsat,P5} - V_{SDsat,P6} \quad (3.15)$$

For a 5-V V_{DD}, $V_{ICMR,max}$ should exceed mid-supply.

3.2.4 Noise

The input stage dominates the noise of the op amp. PMOS devices offer lower flicker noise which is advantageous in our op amp design. Also, the noise component of the load devices is scaled by the ratio of their transconductance to that of the input pair devices. So, the transconductance of the input differential pair needs to be larger than that of the load pair in order to ensure low input-referred noise. There exists a trade-off between noise and the output swing of the stage. Generally, the overdrive voltage of the current loads is minimized to realize a wide output swing, but for a fixed current bias this increases the transconductance (due to increased W) and thereby results in a larger input-referred noise.

A quick estimate on the equivalent input noise of the op amp can be performed by considering the noise of the input stage. The noise generated by subsequent stages is reduced by the gain of the differential-input stage when referred to the input. Those noise stages can therefore be neglected for hand analysis. Referring to Figure 3.2, considerable noise is contributed by the input devices of P_1 and P_2 and the current loads of N_2 and N_3, while the tail current source noise is neglected in the differential-mode analysis. The total thermal and flicker noises of the devices is referred to the input to obtain the equivalent input noise as [7, 9],

$$\overline{V_{n,in}^{\,2}} = 8kT\left[\frac{2}{3g_{m,P1}} + \frac{2g_{m,N2}}{3g_{m,P1}^{\,2}}\right] + \frac{2}{f}\left[\frac{K_N}{C_{OX}W_NL_N}\frac{g_{m,N2}^{\,2}}{g_{m,P1}^{\,2}} + \frac{K_P}{C_{OX}W_PL_P}\right] \quad (3.16)$$

where k is the Boltzmann constant, T is the absolute temperature, $g_{m,P1}$ and $g_{m,N2}$ are the transconductances of the transistors P_1 and N_2 respectively, K_N and K_P are the process-dependant flicker noise coefficients of NMOS and PMOS devices respectively and W, L is the width and length of P_1 and N_2.

3.2.5 Slew Rate

The Slew Rate of the op amp can be represented as [7],

$$SR = \frac{I_{tail}}{C_C} \tag{3.17}$$

where I_{tail} is the total current supplied to the input differential pair and C_C is the compensation capacitor.

3.3 Simulation Results

Simulations were performed using Spectre in order to verify and characterize the performance of the op amp. The circuits used for each characterization are identical to those used in testing and are discussed in-depth in Chapter 4. The results presented here are from simulations of the extracted layout, with a 50 pF load, using the BSIM3v3 typical corner models for this 0.5-µm process and with a supply voltage of 5 V.

Figure 3.3 presents the ICMR variation plot across the input voltage. The op amp is in unity-gain non-inverting configuration and V_{DD}/V_{SS} is ± 2.5 V. It can be seen that the op amp is ground sensing and the upper ICMR value decreases with increasing input voltage. Figure 3.4 shows the open-loop gain and the phase plot for the frequency compensated op amp. As seen from the figure, the A_{OL} is 88 dB with a UGBW of 3 MHz and a phase margin of 86°. The response to small-signal transient inputs is presented in Figure 3.5 and Figure 3.6. The simulated rise time and fall time are 165 ns and 139 ns respectively. Figure 3.7 and Figure 3.8 show the large-signal response of the op amp.

Op amp characterizations such as offset voltage, PSRR, and CMRR can also be done using BSIM3 models for this 0.5-µm process. However, the simulation results obtained will be highly optimistic values rather than being realistic. Monte Carlo simulations with a ±3σ variation in the threshold and process parameters should be performed to get those results. However, due to the unavailability of such models for this process, these simulations have not been shown here.

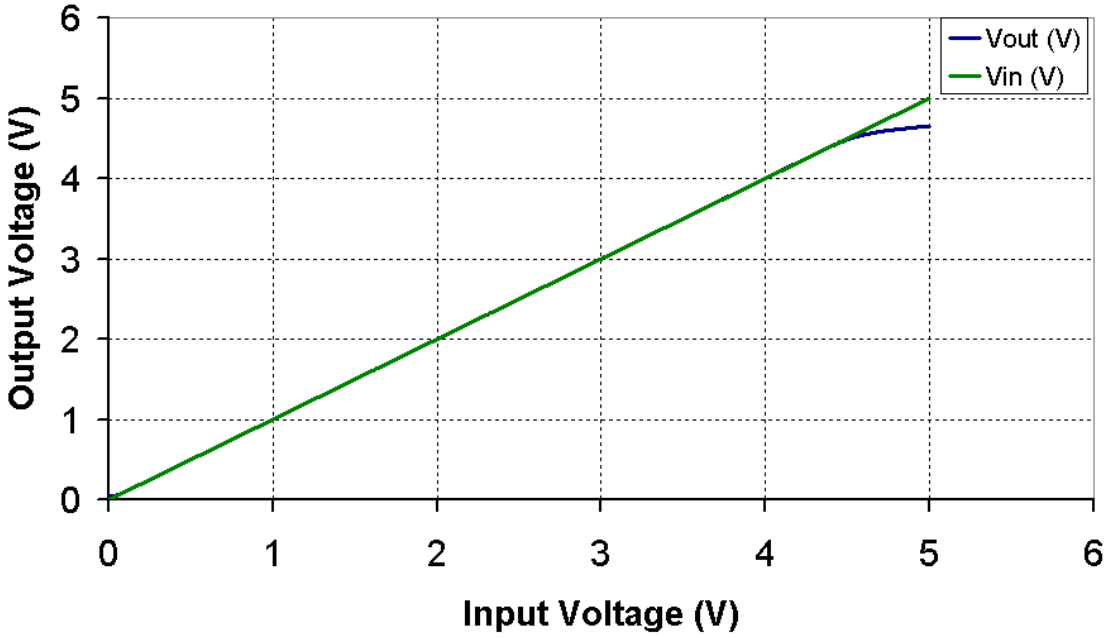

Figure 3.3 Simulation result for ICMR

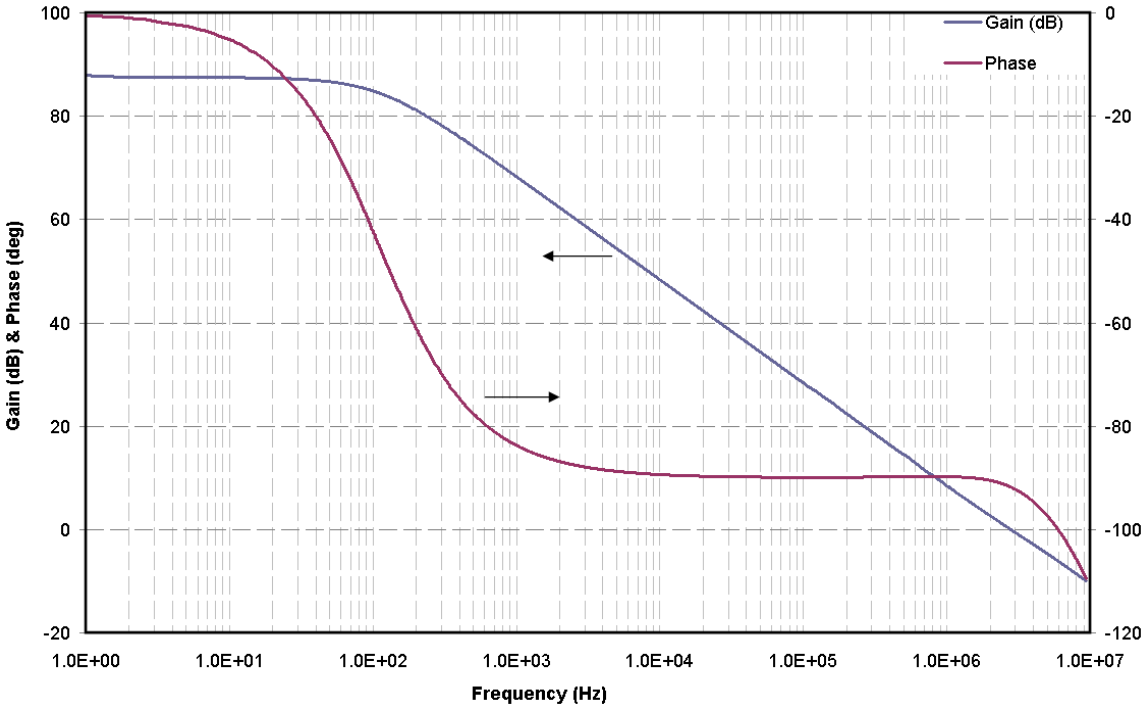

Figure 3.4 Simulation result for open-loop gain and phase

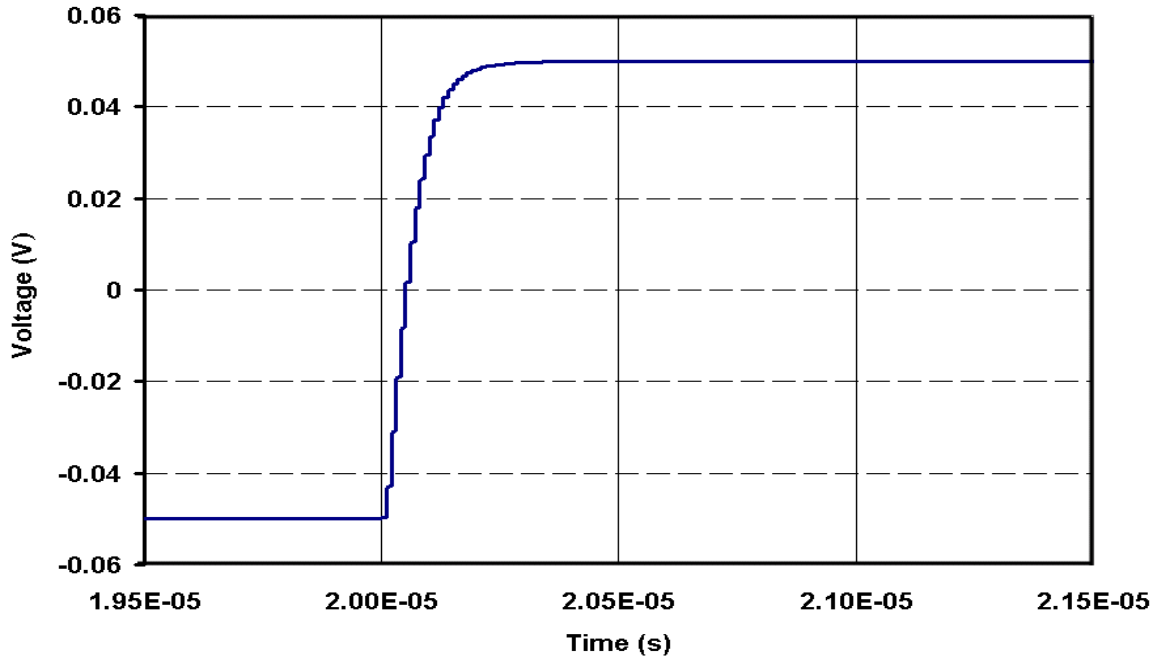

Figure 3.5 Simulation result for small-signal rise time

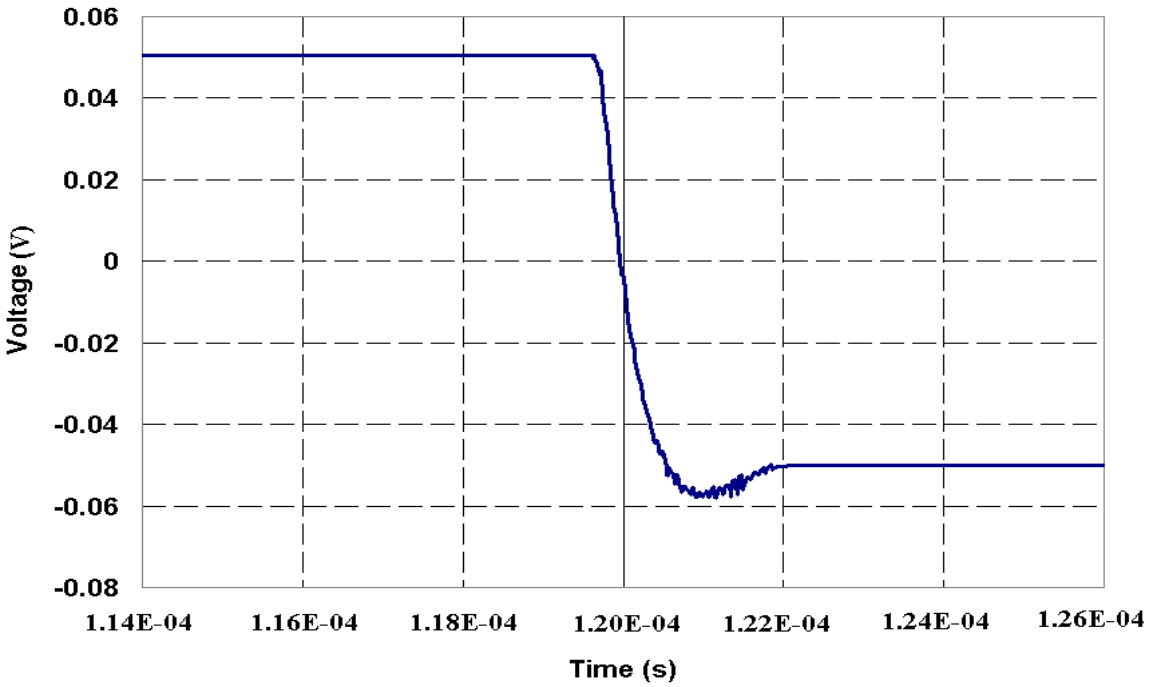

Figure 3.6 Simulation result for small-signal fall time

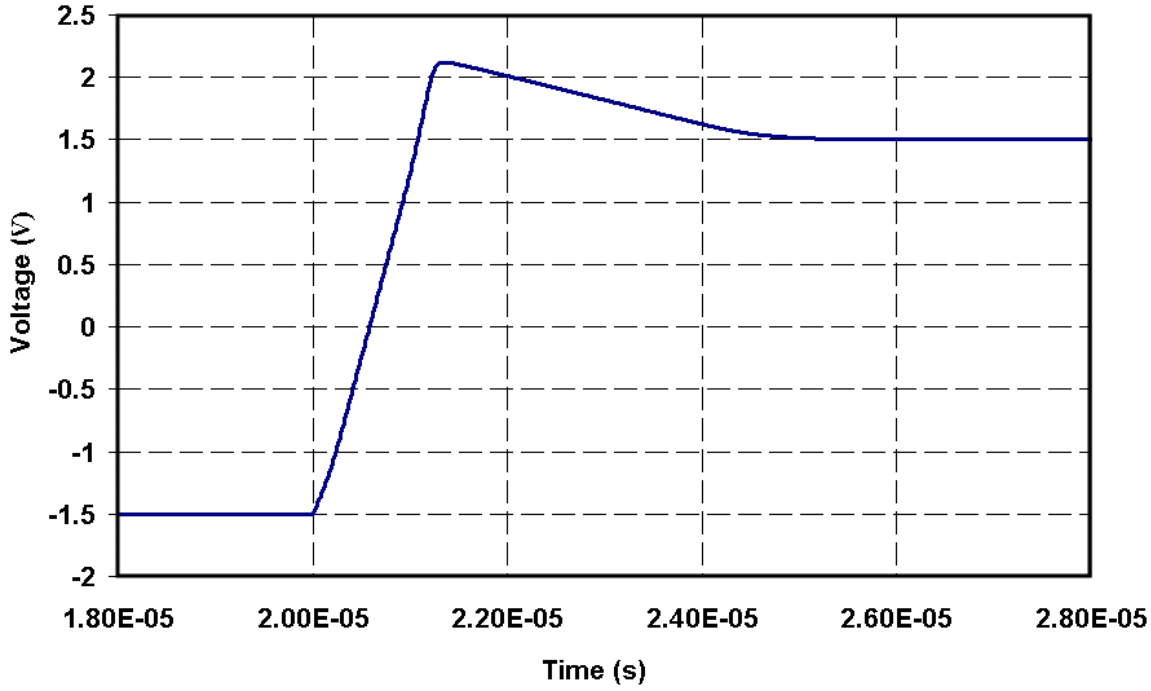

Figure 3.7 Simulation result for positive-going large-signal slewing

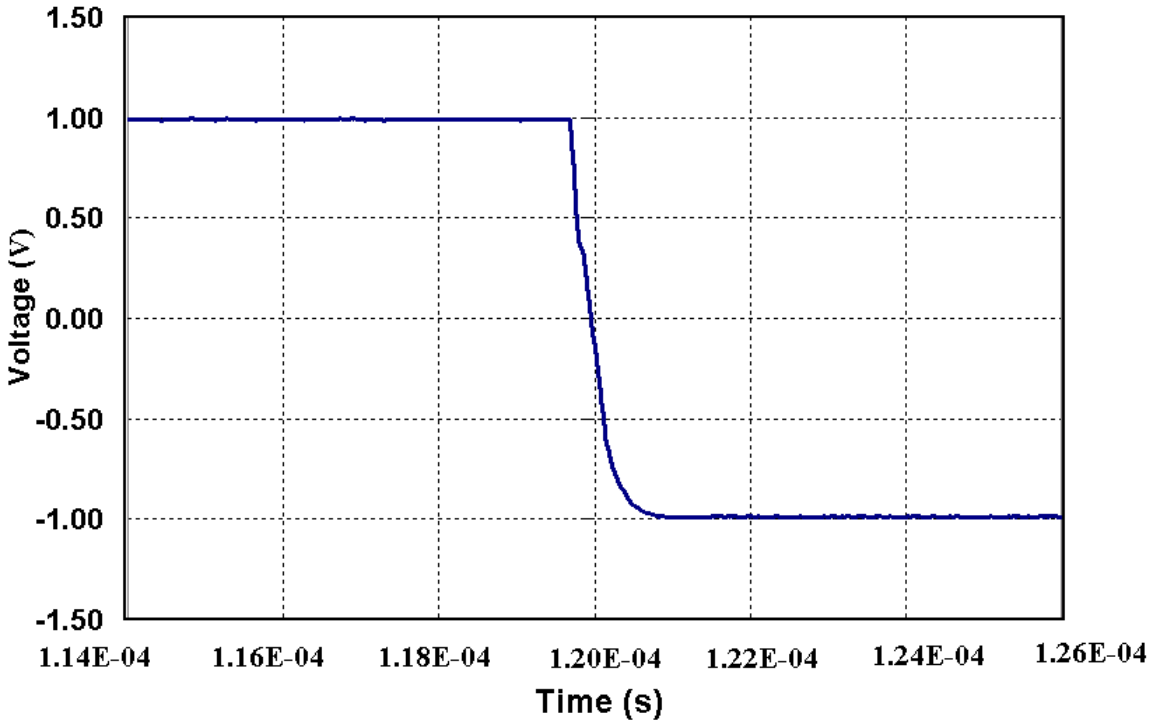

Figure 3.8 Simulation result for negative-going large-signal slewing

3.4 Layout and Implementation

The performance of the op amp could be altered due to the presence of parasitics in the circuit layout. Therefore careful layout techniques are required in order to minimize the effect of parasitics such as capacitances, resistances, parasitic transistors, latch-up etc. Guard rings with numerous substrate/well contacts around the transistors were used to reduce the substrate/well resistance. Doing this prevents the parasitic transistors from turning ON and thus reduces the susceptibility to latch up. Also, the generous use of substrate/well contacts minimizes the substrate noise by providing a low impedance path for the substrate noise to ground. Further, the random thermal noise due to gate resistance is also reduced by using multi-fingered gates in the transistors.

The highly symmetrical input stage and the current mirrors require good matching between the transistors. This is achieved by the use of common centroid layout technique to match these transistors. Figure 3.9 presents the layout of the op amp. Note that the input differential pair P_1–P_2 is matched in common centroid. In the output stage, the transistors N_2, N_3, and N_5 and the output transistor N_1 are matched together. Also, the current mirror transistors of P_9, P_7, P_3, and P_5 are matched.

The design was implemented in a commercial 0.5-μm CMOS process. The op amp had 6 dedicated pins for V_{IN+}, V_{IN-}, V_{OUT}, I_{BIAS} and power supply pins. Figure 3.9 shows the layout of the general-purpose op amp. Figure 3.10 presents the die photograph of the fabricated chip. The op amp occupies an area of 0.04 mm^2.

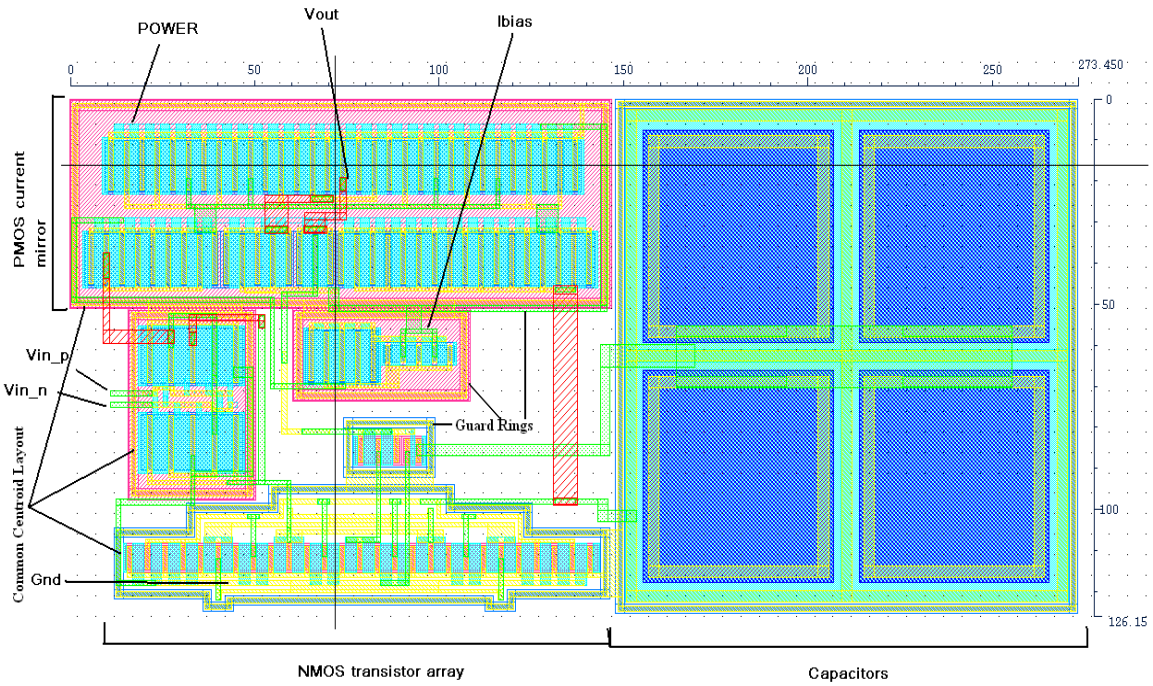

Figure 3.9 Layout of the general-purpose op amp

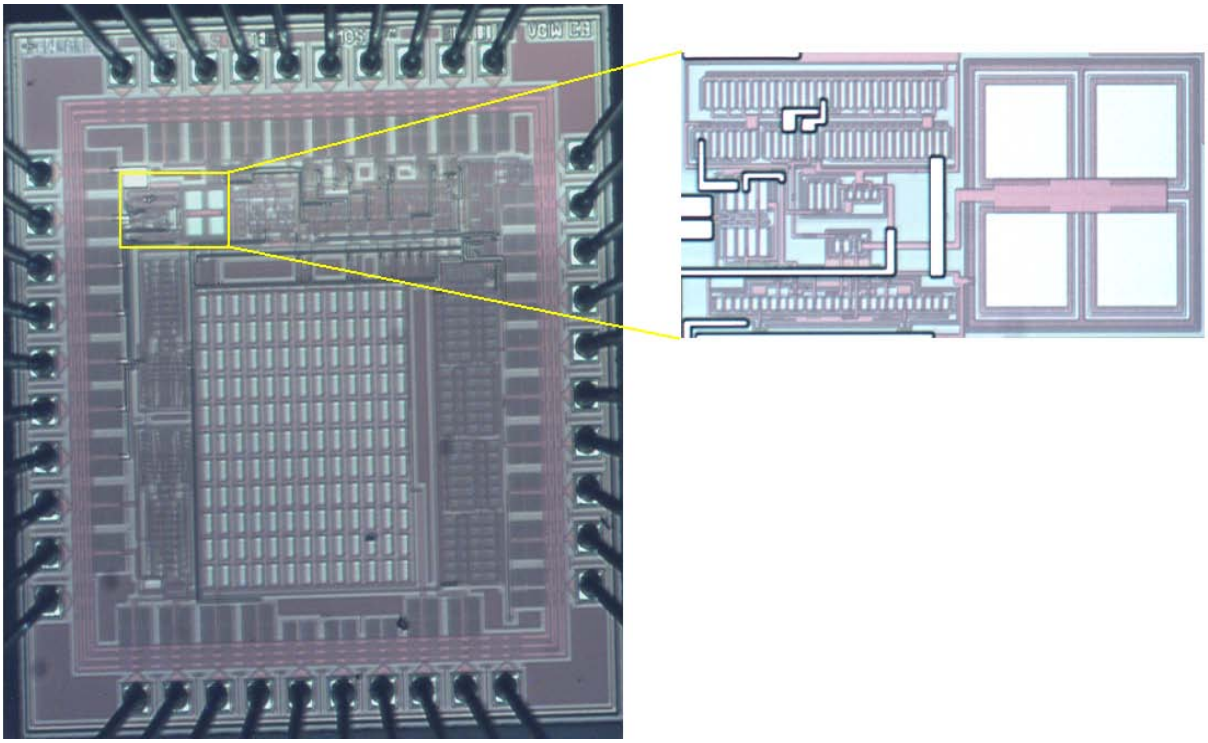

Figure 3.10 Die photo of the general-purpose op amp

CHAPTER IV Op Amp Measurement Results

This chapter presents the measurement techniques and test results obtained for the signal conditioning operational amplifier. The following section illustrates the test setup and discusses the measurement results.

4.1 Test Setup

The test circuits necessary for characterizing the op amp were built on a printed circuit board, shown in the Appendix, Figure A.1, and used to test the op amp. Complementary supply voltages of ±2.5 V, from an Agilent E3631A, were used to simplify testing by referencing the signals to a mid-supply voltage of ground. Power supply bypassing capacitors were placed close to the supply pins of the op amp to dampen any ac ripple and power supply noise. To filter out the power supply noise over a wide bandwidth, an array of capacitors comprising of a tantalum 1 μF and ceramic 0.1 μF were used. The op amp was biased by a 30 μA current sink which was provided by an external current source. An effective load capacitance of about 50 pF was connected to the op amp's output for all test configurations. An oscilloscope probe with a load of 15 pF, 10x attenuation, and 1 MΩ impedance was used for all measurements (included in the 50 pF load estimate). A sample of 5 chips was used for testing and the measurements results obtained show consistent trend in the changes across the temperature range.

4.1.1 Input common-mode range

The ICMR is measured by configuring the op amp as a non-inverting unity-gain buffer as shown in Figure 4.1. A linear input ranging from V_{SS} to V_{DD} is applied to the op amp and the output voltage is monitored. The range of input voltages for which the slope of the output voltage is unity represents an optimistic estimate of the ICMR. The lower range of ICMR extends to ground consistently for all 5 chips.

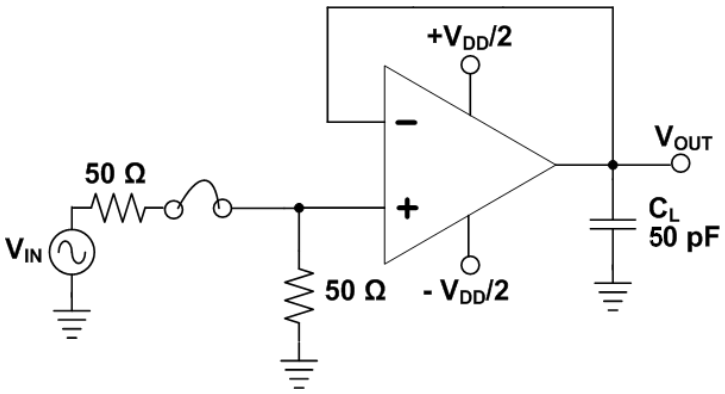

Figure 4.1 Measurement setup for ICMR

4.1.2 Open-loop gain

The open loop gain of the op amp is defined as

$$A_{OL} = \frac{V_{OUT}}{v_{\epsilon}} \tag{4.1}$$

where V_{OUT} is the op amp's output voltage, which is assumed to be zero when no input is applied and v_{ε} is the feedback error voltage, which is the input differential voltage applied to the amplifier [10]. Due to the very high differential gain of the op amp, measuring the gain using an open-loop configuration is very difficult, so the op amp is kept in a closed-loop configuration.

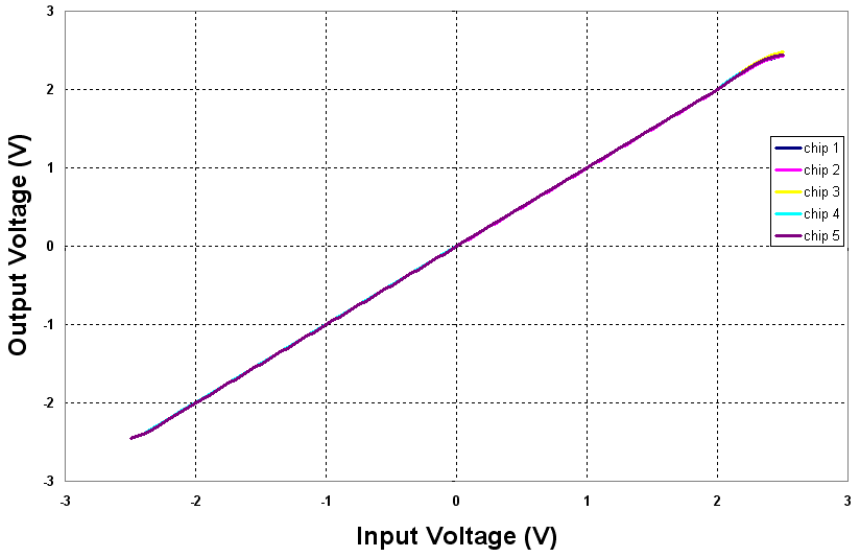

Figure 4.2 Measured ICMR for 5 chips

Figure 4.3 presents the setup used for the open-loop gain measurement where the op amp is configured as a unity-gain inverting amplifier. The signal is applied to the negative input terminal through the *RC* network while the positive input is grounded, thereby maintaining a fixed common-mode voltage of ground, and therefore the finite open-loop gain can be differentiated from the finite CMRR [10]. A large feedback resistor is chosen to prevent dc loading of the op amp's output. The probing of the error voltage v_ε at the negative input terminal of the op amp introduces capacitance at the node which, along with the large input resistance, would form a low-frequency pole and thereby cause instability. Capacitor C_1 fixes the location of the input pole and capacitor C_F adds a zero to improve the stability of the system.

An SR770 network analyzer, which provides high resolution voltage measurements, was used for the AC voltage measurements. The network analyzer has an internal sine-wave synthesizer which is perfectly synchronized with the timing window of its FFT analyzer. Using this sinewave as the op amp's input prevents any spectral leakage during the FFT analysis of the op amp's output and thereby gives an accurate measurement. A nominal input of 200 mV was applied for the measurements. The SR770 has a frequency limit of 100 kHz, so the op amp's open-loop gain was characterized for this range and unity gain bandwidth (UGBW) is derived by extrapolating the plot with a – 20 dB/decade slope to cross the 0 dB line. Figure 4.4 shows the measured open-loop gain of the op amp. The measured low frequency A_{OL} is 84 dB (close to the simulated value of 86 dB). The measured UGBW being 3.5 MHz is also close to the simulated value of 3 MHz.

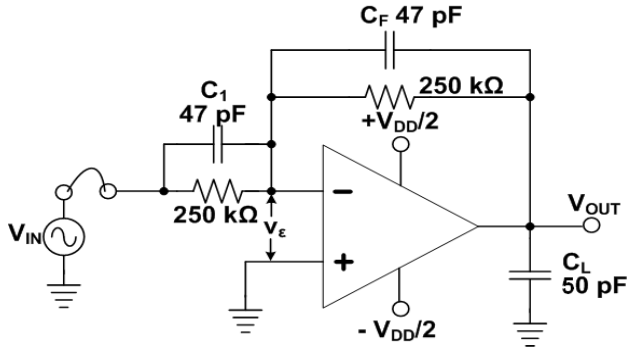

Figure 4.3 Open-loop gain measurement circuit

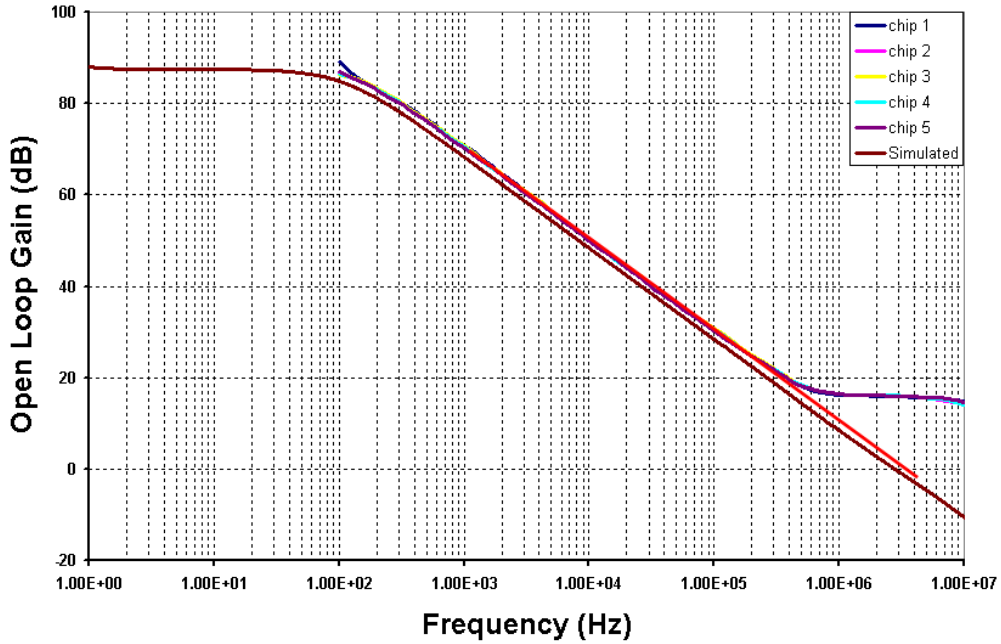

Figure 4.4 Measured open-loop gain (A_{OL}) for 5 chips

4.1.3 Small-signal analysis

The op amp's response to small-signal and large-signal transient inputs is essential in determining the rise time, fall time and slew rate of the op amp. To perform transient analysis, the op amp is configured as a unity-gain non-inverting buffer as shown in Figure 4.1. For small-signal analysis, a square wave of 100 mV_{pp} is input to the op amp and the rise, fall times along with the respective overshoots are measured. The small-signal BW, which is the UGBW, is derived from the rise time using the second-order system approximation of [11],

$$UGBW = \frac{0.35}{t_{rise(10\%-90\%)}} \tag{4.2}$$

The average rise time for the op amp over all 5 chips was 172 ns. The fall time recorded for the same was 147 ns. Thus, the UGBW obtained by using the rise time in equation 4.2 is 2.03 MHz, reasonably close to the 3 MHz UGBW obtained by extrapolating the open-loop gain characteristics of the op amp. Figure 4.5 and 4.6 shows the small-signal rise time and fall time respectively.

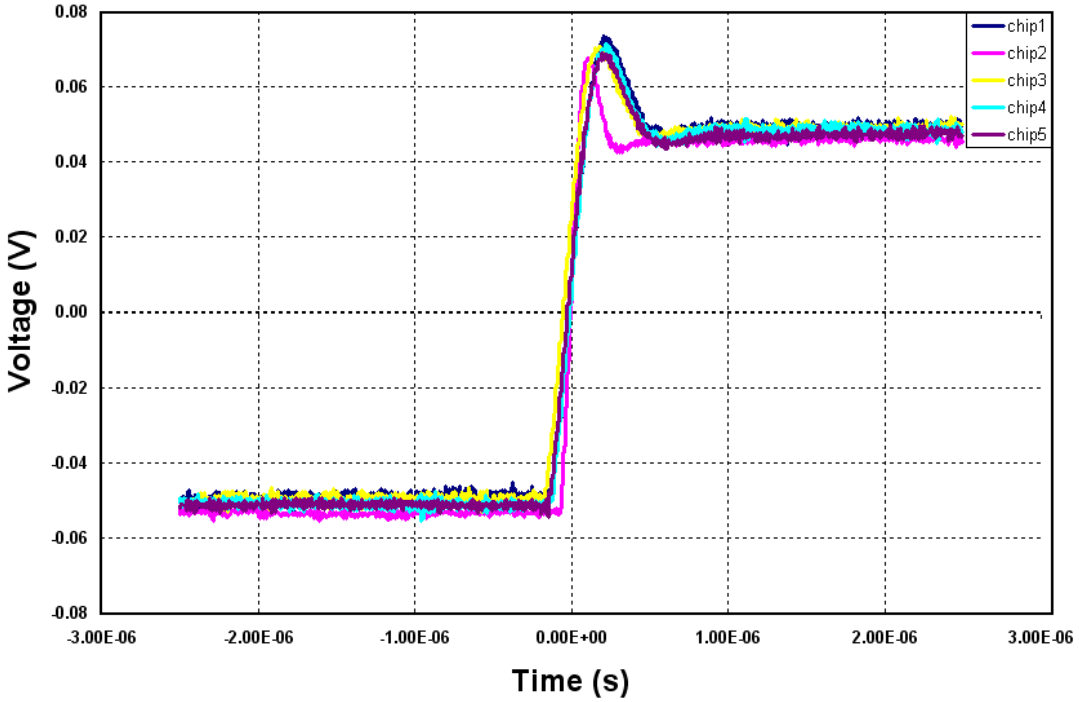

Figure 4.5 Measurement results for small-signal rise time for 5 chips

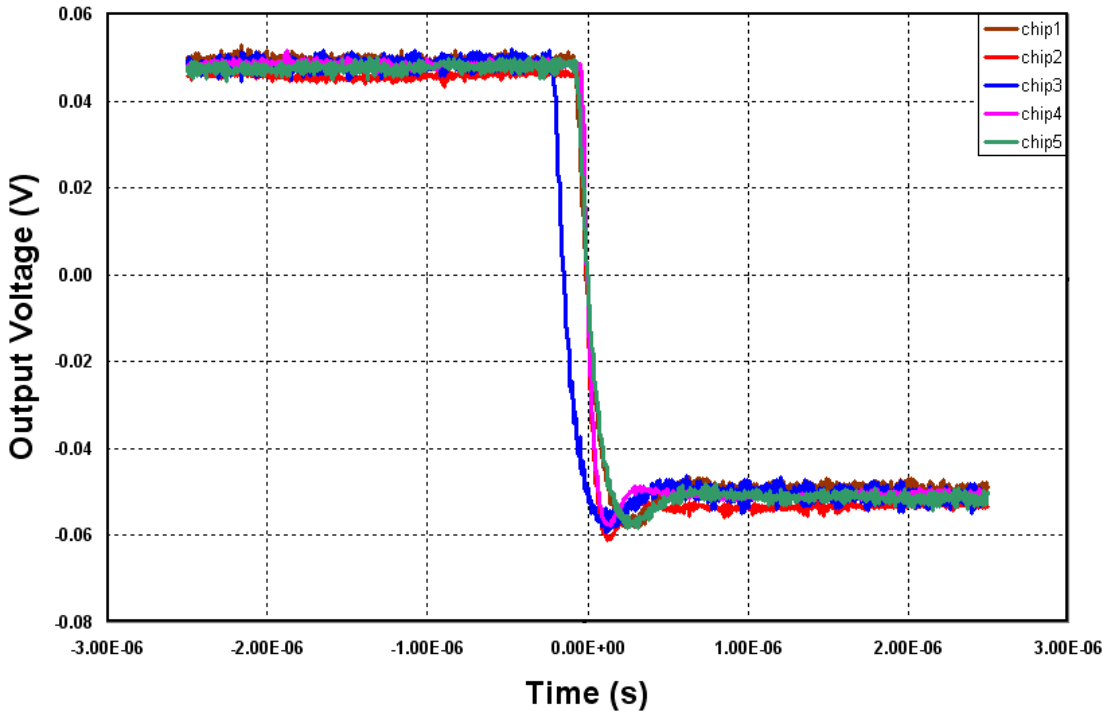

Figure 4.6 Measurement results for small-signal fall time for 5 chips

4.1.4 Large-signal analysis (Slew rate)

Slew Rate (SR) is measured using large-signal analysis by applying a 1 V_{pp} input at 1 kHz to the op amp, which is configured as a unity-gain non-inverting buffer. Figure 4.7 and Figure 4.8 present the positive and negative slewing signals of the large-signal analysis. The measured positive-edge slewing and negative-edge slewing was found to be 1.04 V/μs and 6.01 V/μs, respectively. These values match reasonably well with the simulated 3.53 V/μs slew rate.

4.1.5 Input-referred noise

The input-referred noise of an op amp can be measured using the schematic as in Figure 4.7. The output noise of the op amp is amplified by a low-noise preamplifier (Perkin Elmer 5183) and the output noise spectral density is measured using the HP3985A network analyzer. The preamplifier provides a gain of 60 dB, a usable bandwidth limit of 1 MHz, and a typical input referred noise of 2 nV√Hz at 1 KHz. Hence the op amp is the dominant noise source in this setup. Noise measurements were performed for a frequency range of 10 Hz to 1 MHz, with an average of 50 data points per decade for frequencies above 10 KHz. The network analyzer was configured and the data was processed using software based on Lab View. In order to verify the accuracy of the measurement setup, the noise voltage for 1 KΩ resistor was measured. The measured noise floor was 4 nV/√Hz which is the expected thermal noise voltage for the resistor.

The measured input referred noise of the op amp is shown in Figure 4.10. The noise characteristic is consistent across the 5 chips. The input referred noise at 100 KHz is about 300 nV/√Hz.

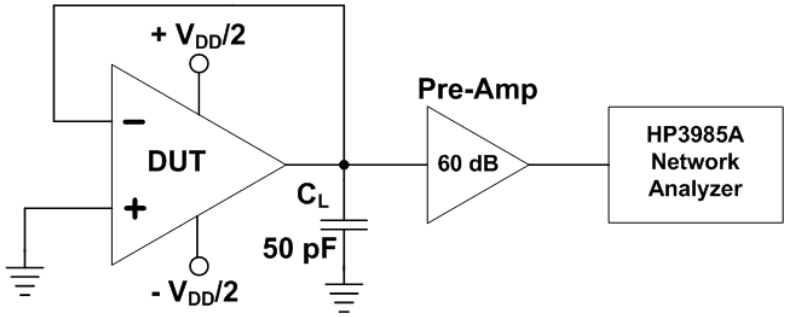

Figure 4.7 Setup for noise measurement

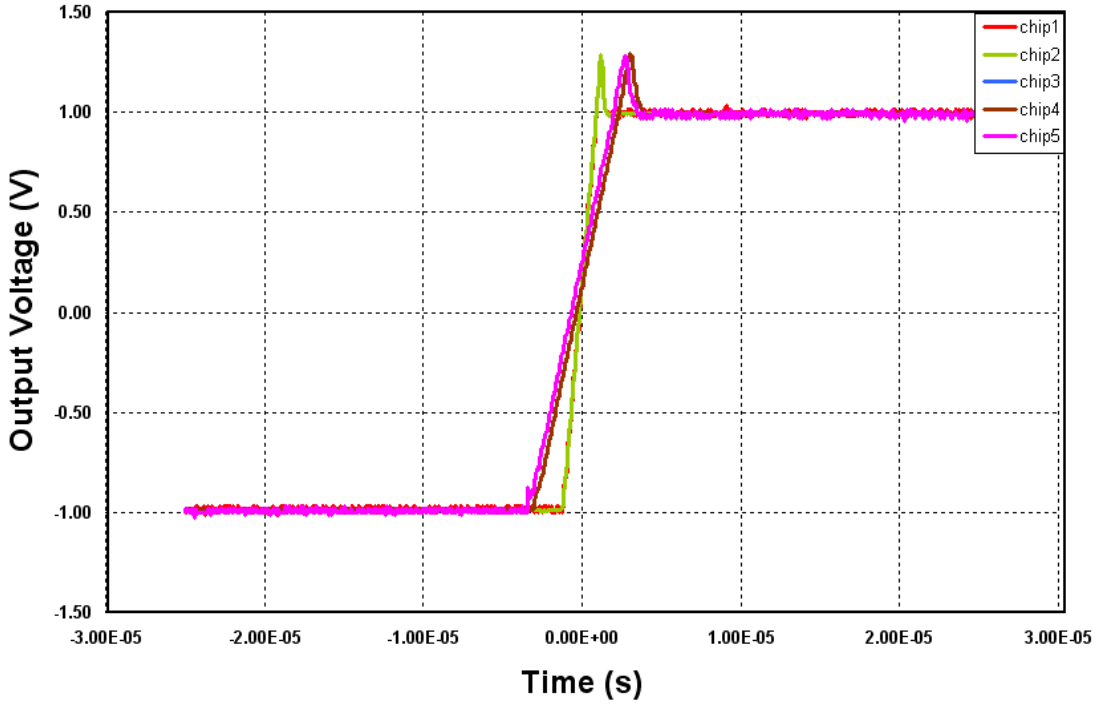

Figure 4.8 Measured positive-edge slewing for 5 chips

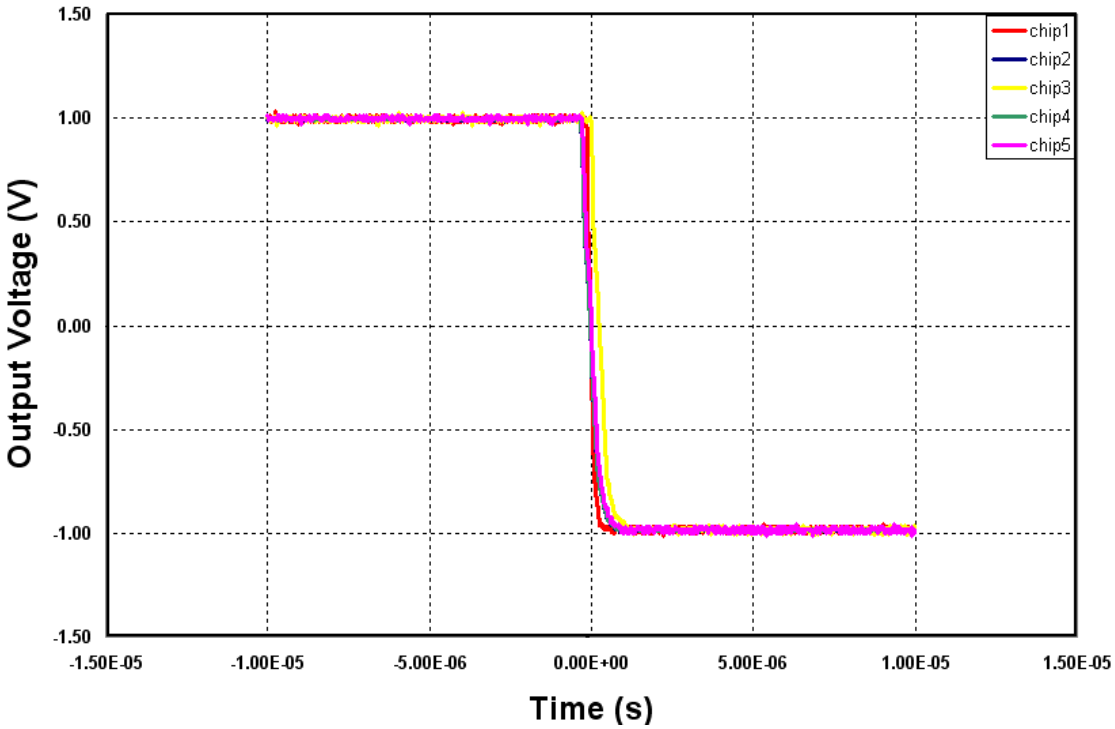

Figure 4.9 Measured negative-edge slewing for 5 chips

4.1.6 PSRR

PSRR is represented as the ratio of change in power supply voltage to the change in the op amp's output, caused by the power supply change. This change in the output can be attributed to the bias point variation with the power supply changes, causing a change in the offset voltage. Thus PSRR can be measured as [1]

$$PSRR = \frac{\Delta V_{PS}}{\Delta V_{OUT}} = \frac{\Delta V_{PS}}{\Delta V_{OS}} \tag{4.3}$$

The schematic in Figure 4.11 presents the measurement method to characterize the DC PSRR. The op amp is powered with complementary power supplies and is configured in unity-gain mode with the common-mode voltage set at mid-supply voltage of ground. To determine the PSRR, the supply voltages are varied and the V_{OS} that is the output of the op amp is measured at each point and PSRR is computed using equation (4.3). The average PSRR for the op amp based on measurements from all 5 chips was 68 dB.

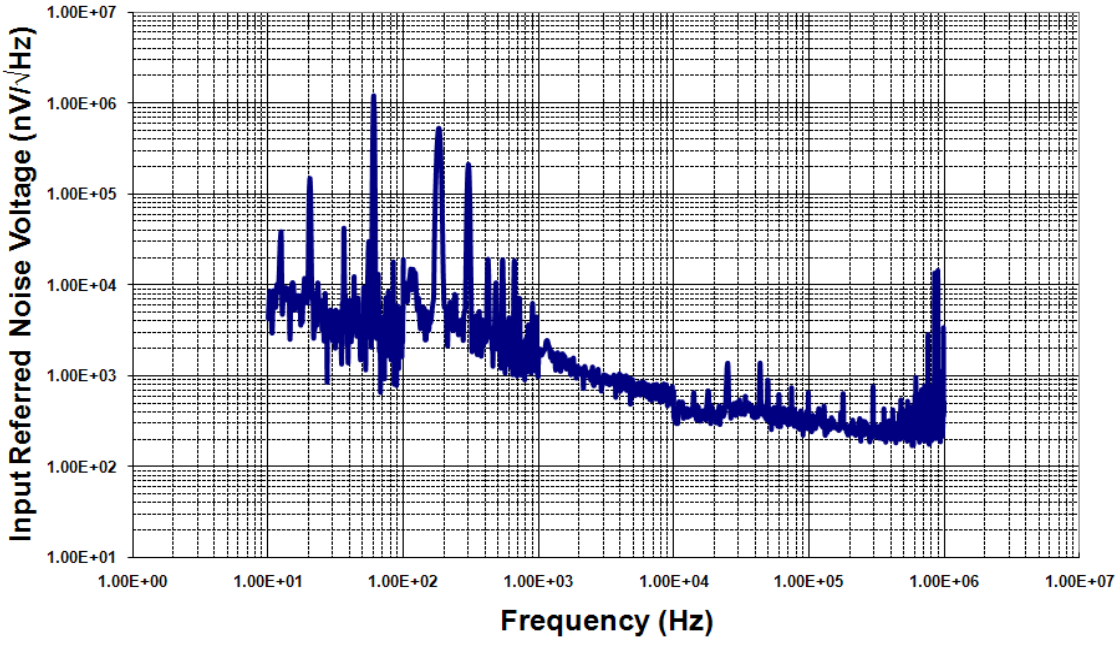

Figure 4.10 Measured input referred noise

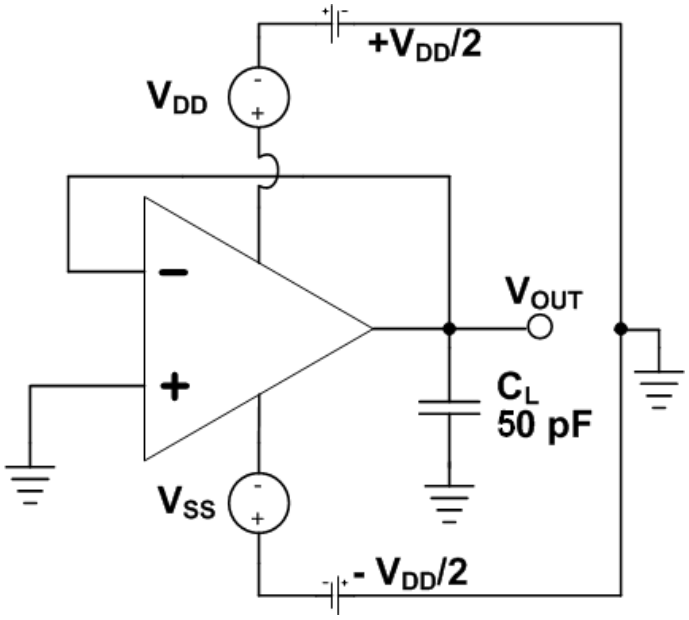

Figure 4.11 PSRR Measurement setup

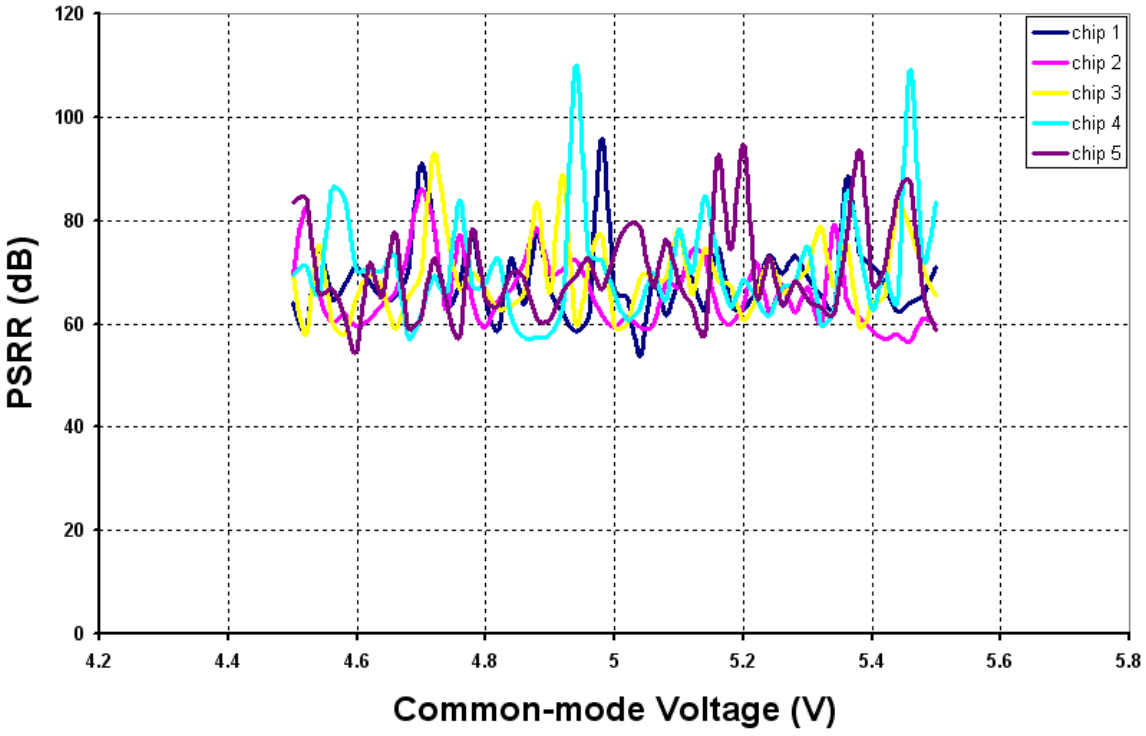

Figure 4.12 Measured PSRR for 5 chips

4.1.7 CMRR

CMRR is defined as the ratio of the voltage gain for a differential-mode input signal to the voltage gain for a common-mode input signal, and can be stated as [1]

$$CMRR = \frac{A_{DM}}{A_{CM}} = \left[\frac{\frac{\Delta V_{OUT}}{\Delta V_{IND}}}{\frac{\Delta V_{OUT}}{\Delta V_{INCM}}}\right] = \frac{\Delta V_{INCM}}{\Delta V_{IND}} \tag{4.4}$$

Therefore, measuring the dc CMRR involves determining the change in the offset voltage due to any change in the applied common-mode voltage. But, power supply voltage variation may affect the output as well as the offset voltage. In order to ensure that the measured change in the offset voltage is only due to a change in common-mode input voltage, the output voltage of the op amp is maintained at a fixed voltage for the complete test sequence. Figure 4.12 illustrates the test circuit used in the measurement [10]. The driver maintains the op amp's output voltage at ground, irrespective of the value of the power supply or the common-mode input voltage. The common-mode voltage, V_{CM} is varied across the op amp's ICMR range and the change in offset voltage is captured. Figure 4.13 presents the CMRR across the common-mode voltage variations. The average CMRR across 5 chips was measured to be 58 dB at room temperature.

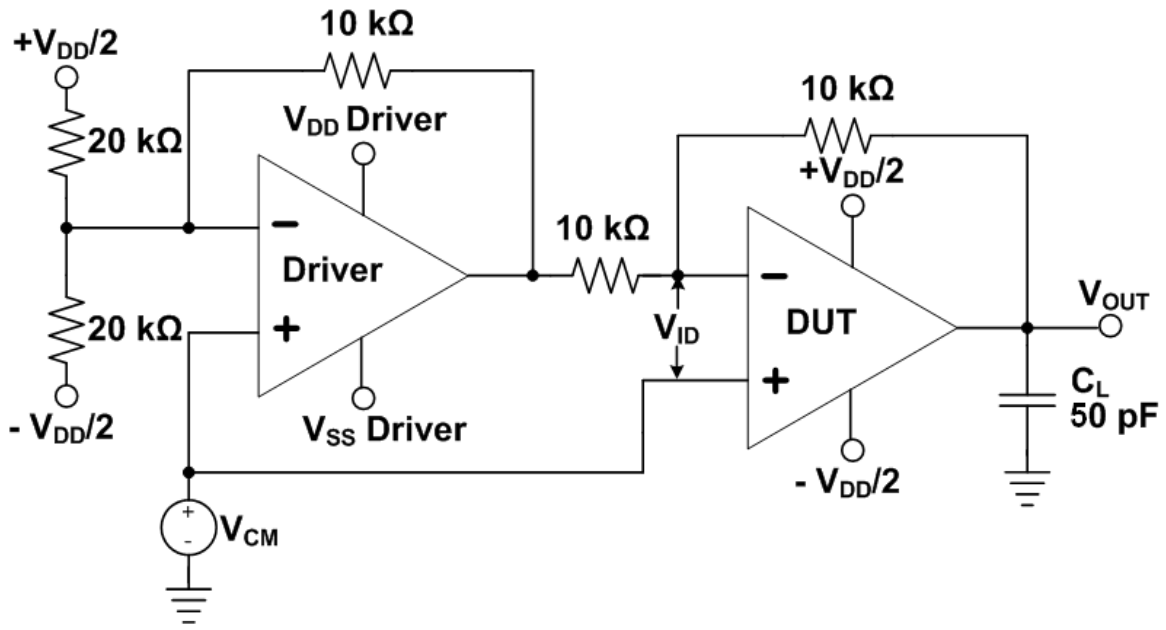

Figure 4.13 CMRR Measurement circuit

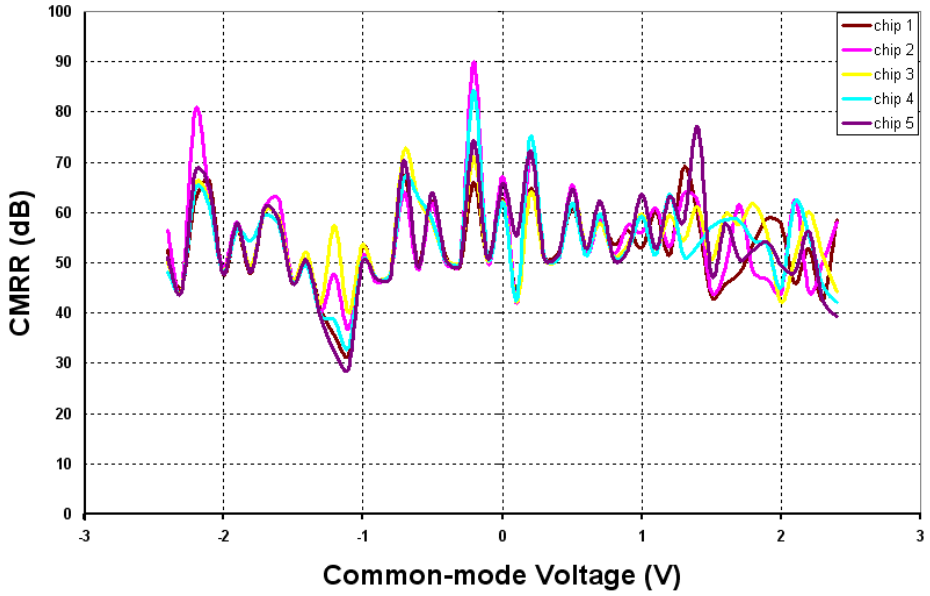

Figure 4.14 Measured CMRR for 5 chips

4.2 Summary

The table below summarizes the performance of the op amp. As seen from the table, the op amp has been able to meet almost all the specifications for the design. Overall, with such results, the op amp should perform well for the targeted application.

Parameter	Specification	Simulated	Measured
Open-loop gain (A_{OL})	> 80 dB	88 dB	86 dB
Gain Bandwidth (GBW)	> 1 MHz	3 MHz	2.8 MHz
Minimum input common mode voltage	0 V	0 V	0 V
PSRR	> 60 dB	*	68 dB
CMRR	> 60 dB	*	58 dB
Slew Rate	> 1 V/µs	2.2 V/µs	1.04 V/µs

Table 4.1 Summary of measured results

***** Due to the unavailability of appropriate models for AMI 0.5 µm technology, Monte-Carlo analysis was not performed to obtain the realistic simulated values of these parameters.

CHAPTER V System Application

This chapter discusses the application of the op amp within an instrumentation system. The op amp is interfaced with a reflective object sensor and used as a current-to-voltage converter. The primary application of the system level circuit is width measurement of thin layers of cloth or material in general. The phenomenon of reflectivity is used to achieve this. The op amp in this circuit amplifies the output signal of the sensor and matches its range with the input span of an off-the-shelf commercial ADC.

5.1 Width Measurement

A reflective object sensor consists of a light emitting source, usually an LED which is electrically and optically isolated from the phototransistor. It should be noted, however, that both the LED and the phototransistor are in the same package. There are small windows on the top surface of the reflective object sensor's IC package which allow the light emitted by the LED to pass through it. When the sensor is powered ON and the diode is forward biased, it emits light out of the package. This light can be reflected back into the package to bias the phototransistor with the aid of a reflective surface positioned over the sensor. The amount of current conducted by the transistor varies according to the proximity of the reflective surface to the sensor and the reflectivity of the material used. For the same distance of the material from the sensor, a single layer of reflective surface will reflect more light back to the phototransistor than two layers of the same material stacked together. This is because the addition of an extra layer of material causes the reflective surface to become more opaque relative to the single layer of material. This results in lower reflection of incident light by the reflective surface. Lower reflected light will consequently force the phototransistor to draw less current. This variation in current can be utilized to correlate or characterize the width or thickness of the reflective surface.

5.2 System level Circuit Setup

Figure 5.1 illustrates the setup of the reflective object sensor interfaced with a signal conditioning op amp. The op amp is configured as a non-inverting I-to-V converter which samples the current output of the sensor and generates a voltage.

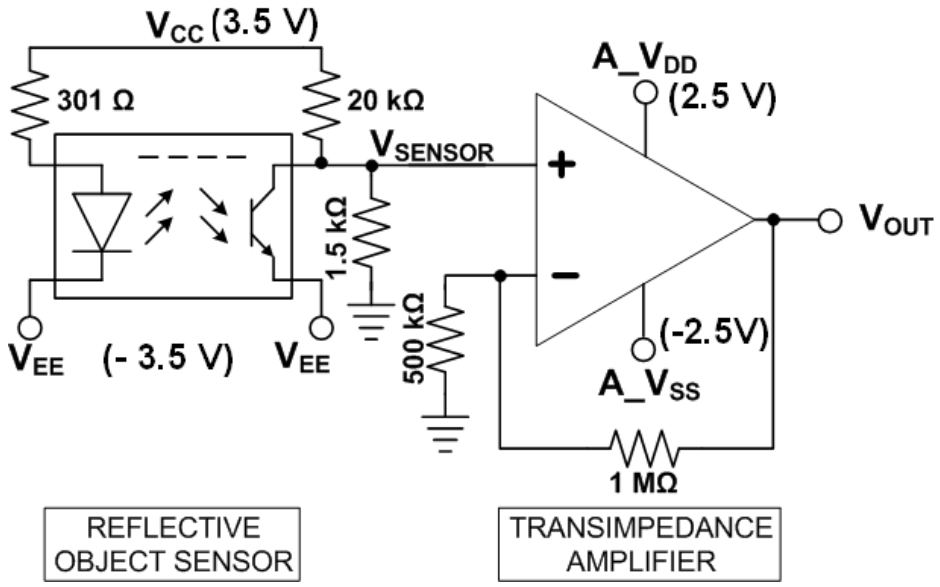

Figure 5.1 System level circuit consisting of reflective object sensor and op amp

The biasing of the sensor is crucial for this application and is biased based on the datasheet information [12]. The values of the biasing resistors and the load resistor have been calculated for a forward current of 20 mA through the diode and 0.4 V_{CE} for the phototransistor for a load of approximately 1 kΩ. A dual power supply of ±3.5 V has been used for the sensor. The op amp is used in a non-inverting configuration providing a closed-loop gain of 3 V/V. A high value of feedback resistor is used to minimize the loading effects on the op amp.

Table 5.1 details the operation of the circuit for different reflective surfaces. The test procedure followed for obtaining these results will now be described. Using the test board shown in Appendix A.2, different reflective surfaces like a white sheet of paper, two white sheets of paper, aluminum foil, etc. were passed over the sensor at a distance of 1 mm from its top surface. The corresponding sensor output voltages and op amp output voltages were noted.

As evident from Table 5.1, ΔV_{sensor} (mV) is the difference in the sensor output voltage when there is no reflective surface (phototransistor OFF) and in the presence of a reflective surface (phototransistor ON). The sensor output voltage is amplified (with a gain of 3) by the op amp.

Reflecting material	V_{sensor} (V)	ΔV_{sensor} (mV)	$V_{op\ amp}$ (V)	ΔV_{opamp} (mV)
No Reflection	0.800	-	2.424	-
One white sheet	0.405	39.500	1.266	115.820
Two white sheets	0.529	27.100	1.582	84.200
Yellow paper	0.559	24.070	1.624	80.000
Aluminum foil	0.501	29.860	1.239	118.540
Black paper	0.798	0.220	2.419	0.540

Table 5.1 System level circuit measurement results (width measurement)

The gain provided by the op amp proves highly useful to read small difference voltages provided by the sensor between different reflective materials.. The first two rows depicting the difference in output voltage for one and two white sheets illustrates that this method can be used for the intended application of width measurement.

5.3 System noise floor

Noise is an important parameter that is useful in characterizing any circuit. For this system level circuit, the worst case signal-to-noise ratio can be determined when the sensor is OFF. Figure 5.2 shows the input-referred noise equivalent circuit [1] for the system level circuit of Figure 5.1. In this analysis, an equivalent noise source e_n for the op amp is connected to the non-inverting terminal and simultaneously considering the op amp to be noiseless. The resistors will contribute thermal noise to the circuit given by [1],

$$e_{n,thermal} = \sqrt{4kTR} \tag{5.1}$$

where k is the Boltzmann constant, T is the absolute temperature, and R is the value of the resistor. All the noise sources shown for the resistors represent this thermal noise source for the resistors. In order to calculate the total noise floor of the circuit, each voltage source will be multiplied by a gain factor depending upon its location within the op amp circuit. The total input-referred noise for the circuit will be given as [1],

$$e_o{}^2 = e_n{}^2 \left(1 + \frac{R_f}{R_1}\right)^2 + e_{RL}{}^2 \left(1 + \frac{R_f}{R_1}\right)^2 + e_{R1}{}^2 \left(\frac{R_f}{R_1}\right)^2 + e_{RF}{}^2 \tag{5.2}$$

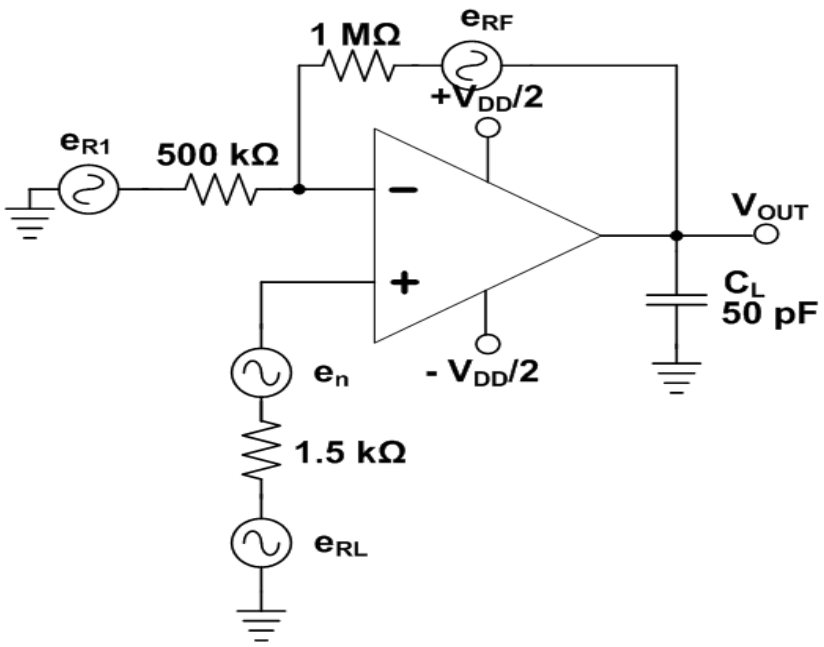

Figure 5.2 Input-referred noise equivalent model of the system level circuit

Using eqn. 5.1 at a temperature of 300 K, and the measured value of the op amp noise at 100 kHz of 300 nV/√Hz, eqn. 5.2 provides the noise floor of the system to be 362.3 nV/√Hz and the total input referred noise e_{ni} is 120.76 nV/√Hz.

CHAPTER VI Conclusions

This thesis presents the design and analysis of a general purpose op amp suitable as an analog signal conditioning block. The op amp was characterized for different parameters and also integrated on a system level to verify its performance for its intended application.

From the measured results, it is illustrated that the op amp provides high gain, has ground sensing ICMR, and high PSRR. It has also met its desired requirement to act as an analog signal conditioning amplifier for a reflective object sensor. The relatively simple design and satisfactory performance make the op amp suitable to be used as a general purpose op amp.

6.1 Future Work

The future work on this thesis can be aimed at understanding certain aspects of the circuit and also enhancing the characterization of the op amp for different parameters. The following steps outline the possible enhancements to this work.

Certain aspects of the circuit such as CMRR and noise can be investigated further to better understand the circuit. Also, there is room for the overall improvement on certain other parameters of the op amp could result in overall better performance of the system level circuit. A shunt feedback capacitor could be added to the op amp's feedback network to reduce the system's noise bandwidth.

The op amp along with the sensor can be connected to an ADC to digitize the output values of obtained from the op amp. Digitizing these values will not only be helpful for further processing and analysis of the information gathered, but will also facilitate easy storage of the information. This enhanced data acquisition system could act as a standalone system for any process control system in which measurement of thickness or width would be essential.

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APPENDIX

A.1 Calculation of Open-Loop Gain

The overall gain of the op amp was derived in Section 3.2.1 and is given by equation (3.12) which is,

$$|A_{V,total}| = |A_{V1}A_{V2}| = (g_{m,P2})(g_{m,N1})(r_{o,N1})(r_{o,P2} \,||\, r_{o,N2}) \quad \text{(A.1)}$$

The approximate value of the A_{OL} can be estimated from this equation. The transconductance is given by,

$$g_m = \sqrt{2\beta I_D} \quad \text{(A.2)}$$

$$g_{m,P2} = \sqrt{2 \times 40 \times 10^{-6} \times \frac{13.5}{4.05} \times 30 \times 10^{-6}} = 109.44 \times 10^{-6} S$$

$$g_{m,N2} = \sqrt{2 \times 120 \times 10^{-6} \times \frac{16 \times 17}{3} \times 120 \times 10^{-6}} = 2370 \times 10^{-6} S$$

The output resistance of each device can be found using,

$$r_o = \frac{1}{\lambda I_D} \quad \text{(A.3)}$$

Thus the output impedance of the first stage becomes,

$$r_{o,P2} \,||\, r_{o,N2} = \frac{1}{0.015 \times 30 \times 10^{-6}} \,||\, \frac{1}{0.032 \times 30 \times 10^{-6}} = 1.27 \times 10^{6} \Omega \quad \text{(A.4)}$$

The output impedance of the output stage becomes,

$$r_{o,N1} = \frac{1}{0.032 \times 120 \times 10^{-6}} = 260\ k\Omega \quad \text{(A.5)}$$

And now the approximate A_{OL} can be found as,

$$|A_{V,total}| = |A_{V1}A_{V2}| = 109.44 \times 10^{-6} \times 2370 \times 10^{-6} \times 1.27 \times 10^{6} \times 260 \times 10^{3}$$

$$A_{V,total} = 89.7 \text{ dB} \quad \text{(A.6)}$$

A.2 Test Board

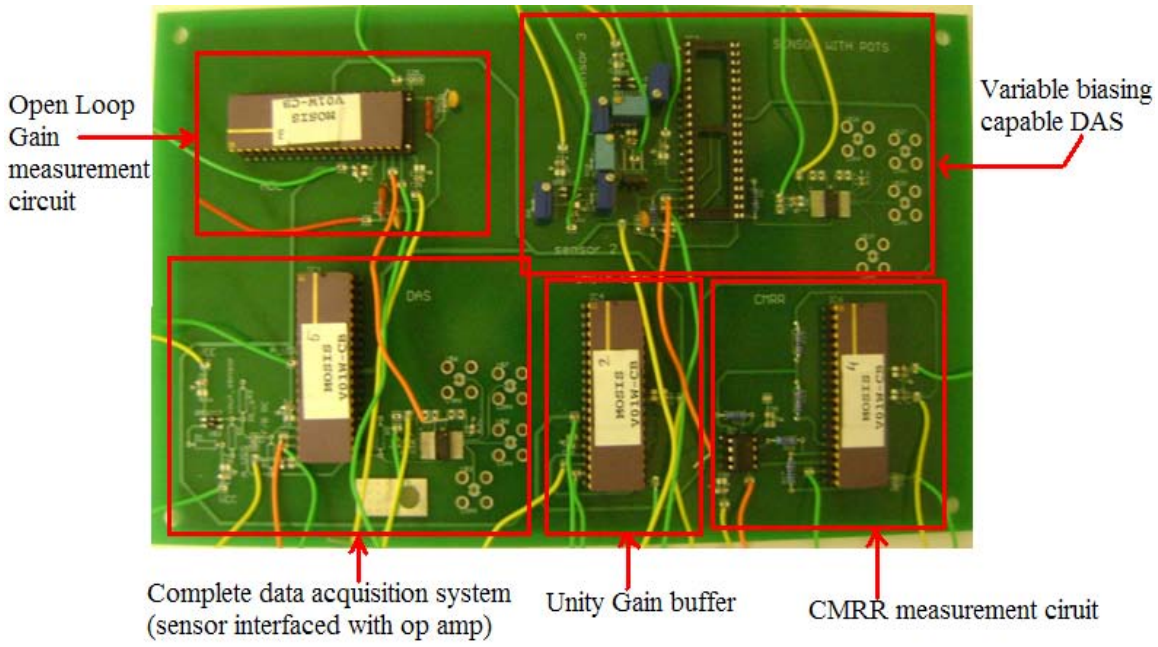

Figure A.2 Picture of Test Board

VITA

Ankit Master was born in Mumbai, India. He pursued his undergraduate degree in the field of Electronics and Telecommunication Engineering at the University of Mumbai, India. In 2007, he moved to the University of Tennessee, Knoxville to further his education and obtain a Master's degree in Electrical Engineering. After completing his current Master's program, Ankit intends to obtain another graduate degree in Business Administration.