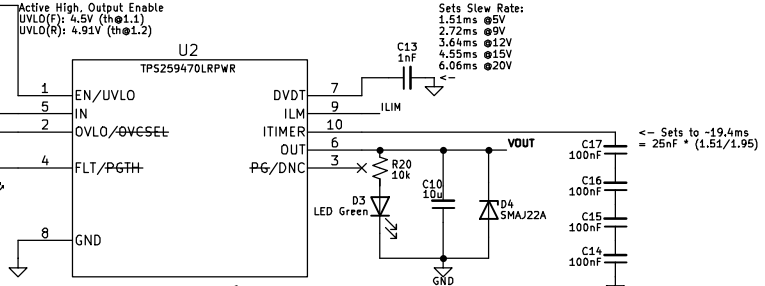
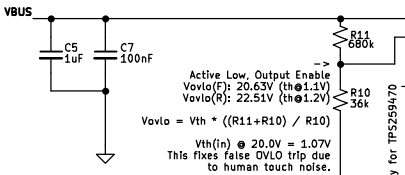
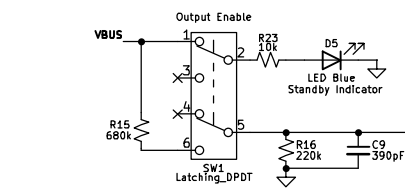
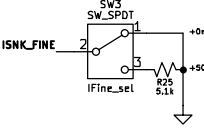
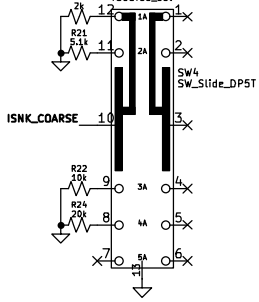
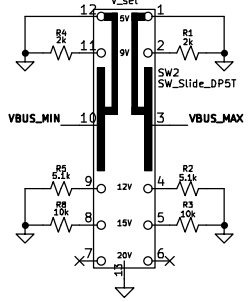
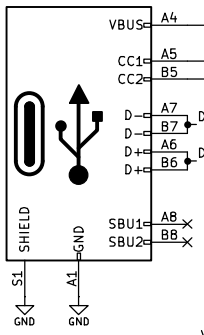
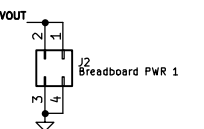
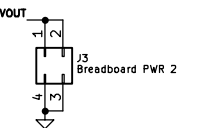
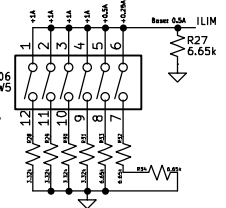


Revisions:  
 - D5 polarity correction.  
 - Part # cleanup.  
 - FLT LED to 3v3 Instead of VBUS.  
 - OVLO thresh changed from 21V to 22.5V to prevent false OVLO trip.  
 - Reduced UVLO, OVLO resistors to reduce noise.  
 - Changed selector to slide switches.

J1  
 USB\_C\_Receptacle\_USB2.0\_16P



Effective Rlim: 6.65kΩ to 632.6Ω  
 Trip current range: 0.58A to 5.27A  
 Step size of 0.25A  
 Ilim (A) = 3334/Rlim [TPS25947X]  
 Example  
 SW: 1 2 3 4 5 6  
 IL: 1 0 0 1 1 (2.25A)  
 IL: 1 1 0 0 1 (3.8A)



Rishik Tiwari (rishik@auriva.tech)		
Brand: MAKING by Auriva		
Auriva Technologies (OPC) Private Limited, India.		
Sheet: /		
File: power-module-v1r1.kicad_sch		
<b>Title: PowerBaby 100W USB PD Sink Module (v1)</b>		
Size: A4	Date: 2025-07-08	Rev: 1
KiCad E.D.A. 8.0.6		Id: 1/1