

→ Counters:

Counter is an sequential circuit capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. A specified sequence of states appears as the counter output.

A register is used for storing and shifting data which is in the form of 1's and/or 0's, entered from an external source.

A counter that follows the binary sequence is called a "binary counter". An  $n$ -bit binary counter consists of  $n$ -flip flops and can count in binary from 0 to  $2^n - 1$ . It is also called as modulus counter or MOD-N counter where  $N = \text{number of states at the counter output} = 2^n$ .

→ Types of counters

Counters are classified into two types.

- \* Asynchronous or non-synchronous or Ripple or serial counters.
- \* Synchronous or parallel counters.

In Synchronous counter, the common clock input is connected to all the flip flop and thus they are clocked simultaneously.

In Asynchronous counter, the first flip flop is clocked by the external clock pulse and then each successive flip flop is clocked by the Q and  $\bar{Q}$  output of the previous flip-flop.

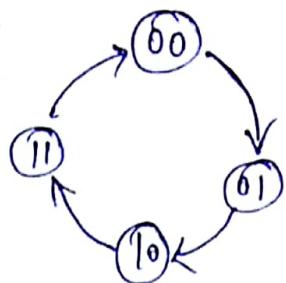
∴ In an Asynchronous counter, the flip-flops are not clocked simultaneously.

→ Asynchronous counter:

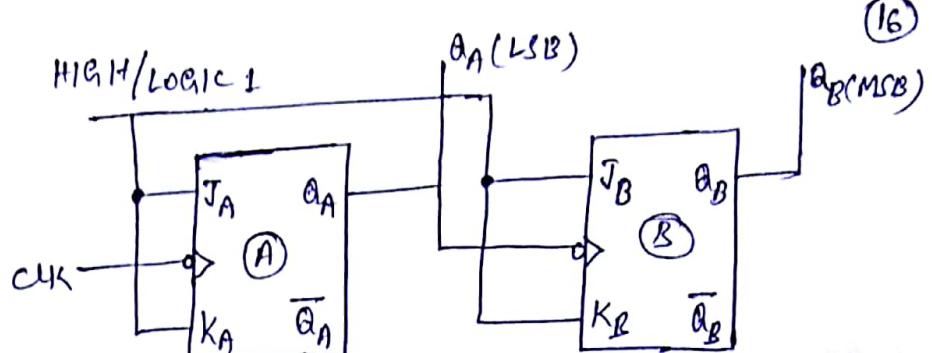
To design the ripple counter, the number of flip flops required depends on the number of states. The number of the output states of the counter is called 'Modulus' (MOD) of the counter. The maximum number of states of a counter is  $2^n$ , where n is the number of flip-flops in the counter. If we have two flip-flops, then the maximum possible number of output states of the counter is  $2^2$  i.e. 4. We can name that counter as MOD-4 or Modulus-4 counter.

→ MOD - 4 or 2-bit Asynchronous Counter:

MOD-4 counter is a 2-bit asynchronous counter which consists of four states due to its two number of flip-flops. The state diagram and logic diagram of 2-bit ripple counter is shown in figure.



Fig(i) State diagram



Fig(ii) Logic diagram

The clock is connected to the clock input of first flip flop. The clock input of the second stage flip flop is triggered by the  $Q_A$  output of the first stage. Note that the flip flop changes its state only when triggered by negative edge of the each clock pulse, but the second flip-flop changes its state only when triggered by the negative going transition of the  $Q_A$  output.

$\therefore$  The two flip-flops are never simultaneously triggered which results in asynchronous counter operation.

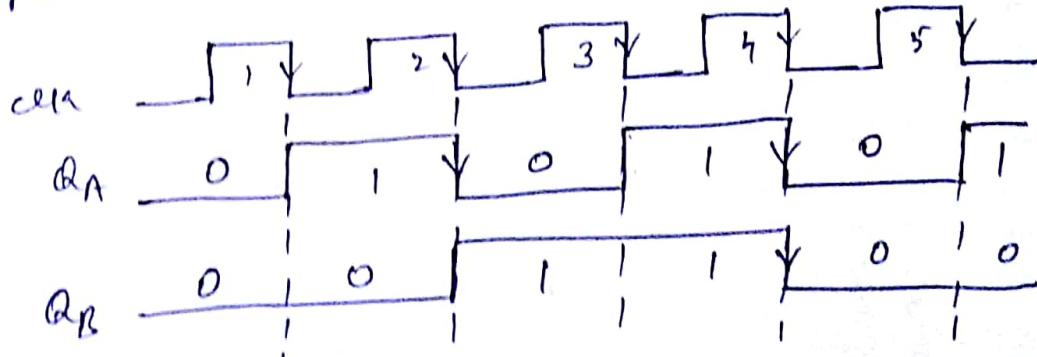


Fig:- Timing diagram of 2-bit ripple counter.

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→ Mod 8 - or 3-bit Ripple counter or Asynchronous counter

It is a 3-bit asynchronous counter, the count sequence starts from 000 to 111 and uses three flip flops.

Fig shows the state diagram of the 3-bit ripple counter. In this diagram, each binary states are indicated inside the circles and directed line between the circles are indicated by the state transitions.

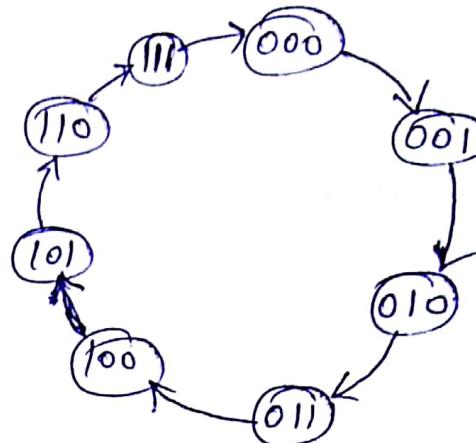


Fig: State diagram of 3-bit ripple counter.

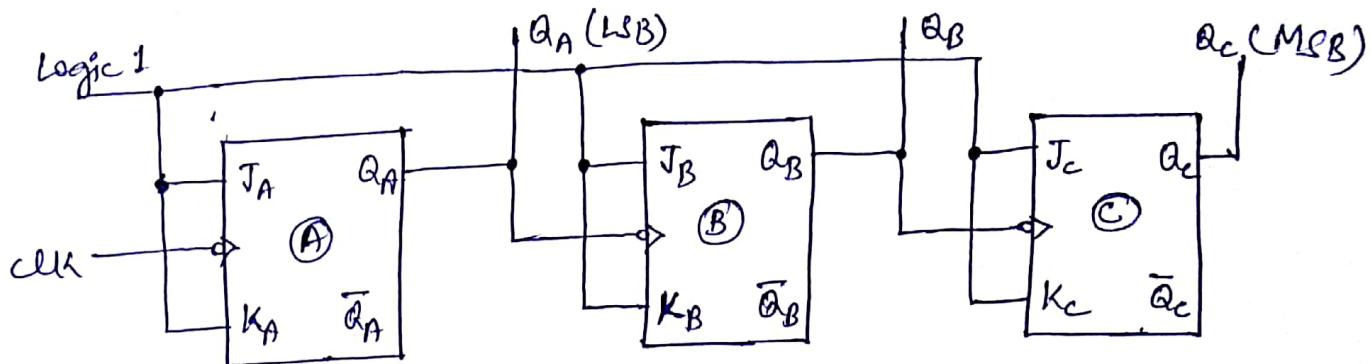


Fig: Logic diagram for 3-bit ripple counter.

The 3-bit ripple counter with 3 JK flip flops named as A, B and C, where C output represents the most significant bit of the count and the A flip flop o/p indicates the least significant bit of the count.

Here, first flip flop (A) is triggered by the clk which is holding the least significant bit. The second flip flop (B) is triggered by  $Q_A$  output of first flip flop. The third flip flop (C) is triggered by the  $Q_B$  output of the second flip flop.

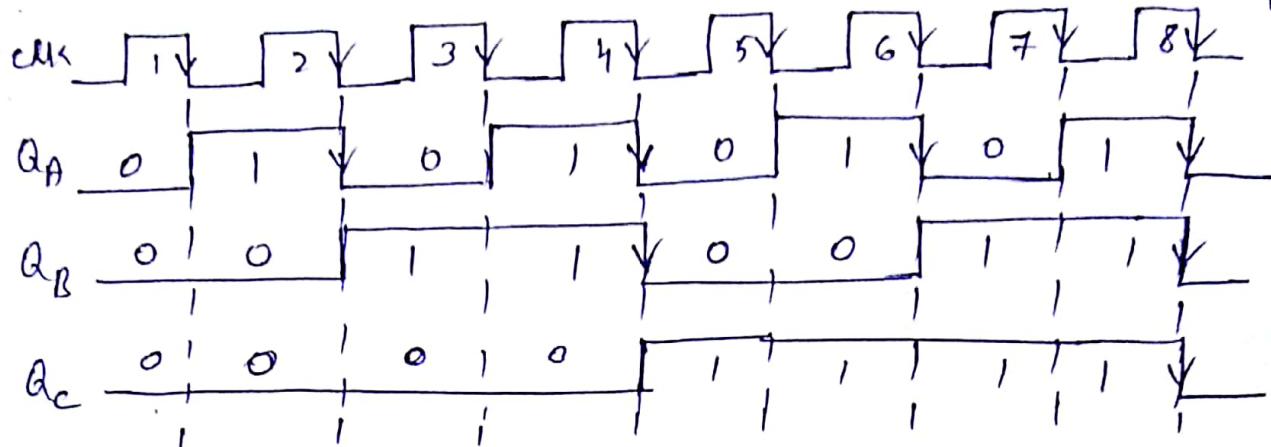


Fig:- Timing diagram of 3-bit. Ripple counter.

→ Counters with MOD numbers less than  $2^n$   
 counters can also be designed to have a number of states in these, sequence less than  $2^n$ . The resulting sequence is called a "truncated sequence". To obtain the truncated sequence, it is necessary to force the counter to recycle before going all of its normal states.

The basic counter is modified to produce the required MOD number less than  $2^n$  by allowing the counter to "skip states" that are to part of the counting sequence. One of the most common method for doing this is making all flip flops to reset after the counter  $N$  with the help of feedback gate in the circuit. Such feedback is provided by a NAND gate, in which the output provides all clear inputs in parallel.

→ Design of Divide-by- $N$  Ripple Counter:

The general procedure for the design of a divide-by- $N$  ripple counter using JK flip flop with clear ( $\overline{CLR}$ ) input.

- \* Determine the number  $n$  flip flop required based on number  $N$  ( $N \leq 2^n$ ).
- \* Connect the  $n$ -flip flops as a ripple counter.
- \* Find the binary representation of  $N$ .
- \* Connect all flip-flops outputs that are 1 at the count  $N$  of the counter, as an input to the NAND gate.
- \* Connect the NAND gate output to the clear inputs of all the flip flops.

→ MOD-6 Ripple Counter or Synchronous counter

Here  $N=6$  and the number of flip-flops required is  $n=3$  ( $N \leq 2^3$ ). Use of 3 JK flip-flops is necessary and they are named as A, B and C.

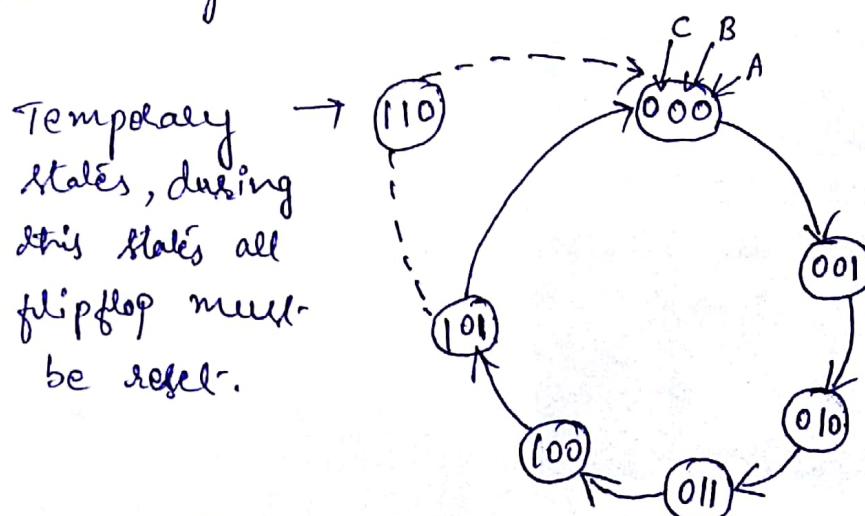


Fig: State diagram of MOD-6 counter.

When starting count of 000, the diagram shows that the states of the counter changes normally until the count of 100. When the

next clock pulse occurs, the counter temporarily goes to the 110 count before going to the stable 000 count.

We can consider that counter goes directly from 101 to 000 count. Note that the 111 state was never reached, not even temporarily.

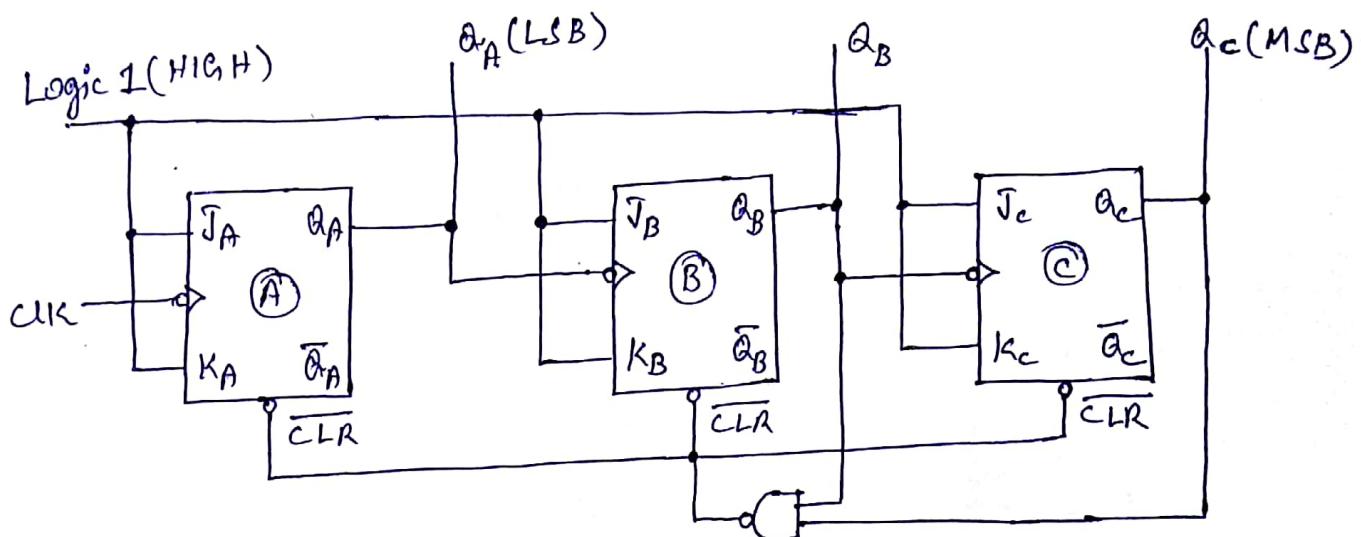


Fig: Logic diagram of MOD-6 ripple counter

→ MOD - 10 Ripple counter or Decade counter or BCD counter or synchronous counter:

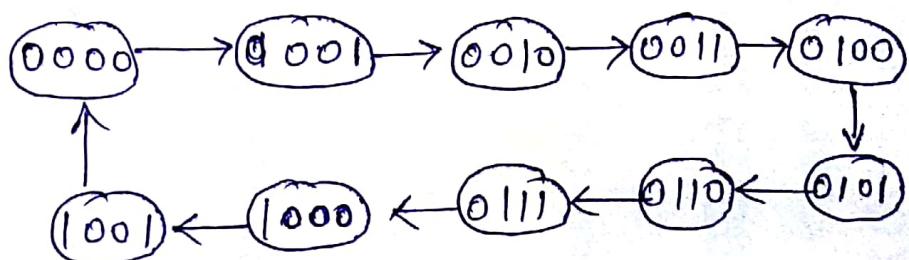


Fig: State diagram of a BCD counter.

A decimal counter follows a sequence of ten states and returns to '0' after the count of 9. These counters are useful in display applications where BCD is required for conversion to a decimal readout.

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A counter with a count sequence of 0 (0000) through 9 (1001) is called a BCD counter because its ten states sequence is the BCD code.

To design a BCD counter, we need 4 flip flops and the 4-bit asynchronous decade counter with four JK flip flops.

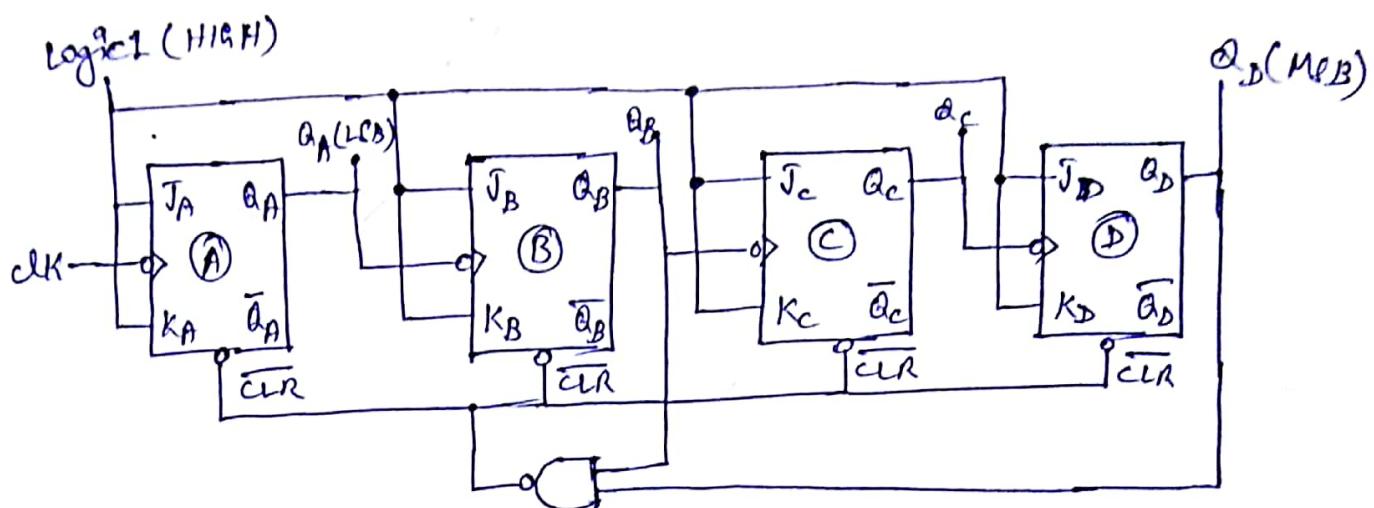


Fig: MOD-10 Ripple counter.

The clock input is connected to the first flip flop only. The second, third and fourth flip flops are triggered by the outputs  $Q_A$ ,  $Q_B$  &  $Q_C$  respectively.

When the counter goes to count 1010, the NAND output goes low and all flip flops are in clear condition. Thus, when 10<sup>th</sup> clock pulse occurs, the counter output  $Q_D\ Q_C\ Q_B\ Q_A = 0000$  instead of 1010.

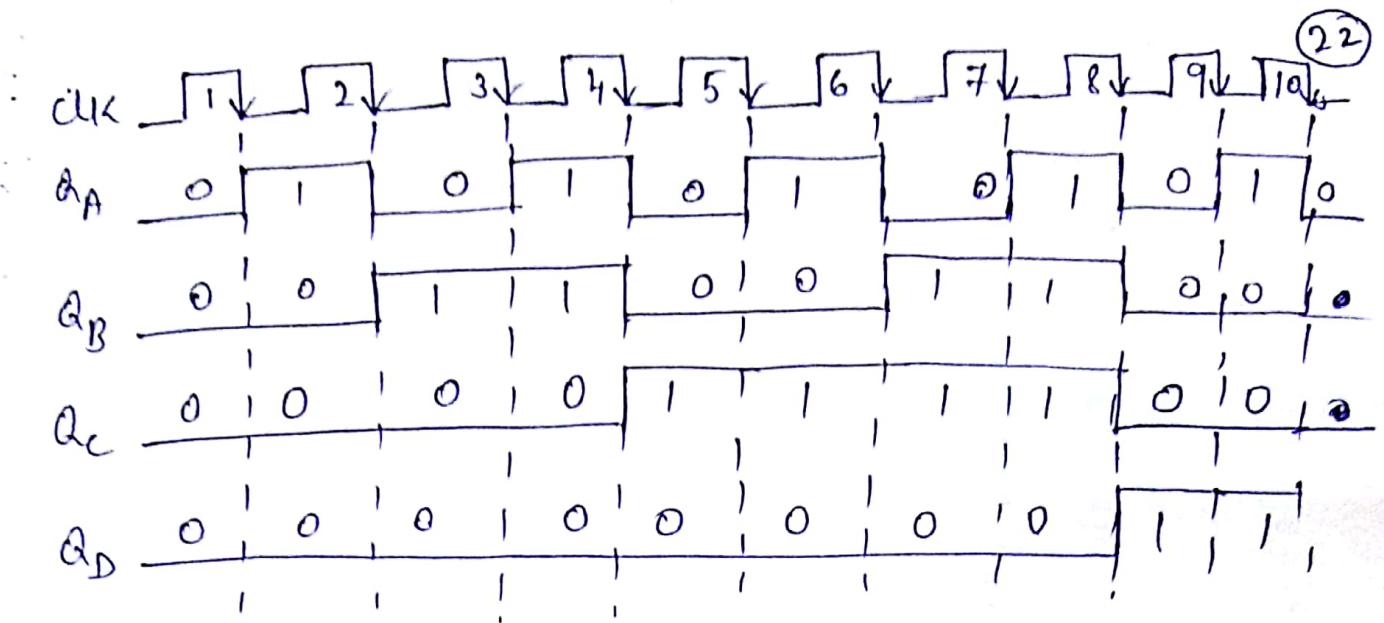


Fig: Timing diagram of BCD Counter.

→ Synchronous counter

In a Synchronous counter, all the flip flops change their state simultaneously, the operation of each stage being initiated by the clock.

In a Synchronous counter, we must note the following:

- \* clock pulse is applied common to all flip flops.
- \* The flip flop in the lower-order position is complemented with every clock pulse and the JK inputs are maintained at logic 1. (to get the toggling action).

→ 2-Bit Synchronous Binary counter

If has two JK flip-flops. These flip flops are negative edge triggered flip flops.

Here, the clock signal is connected in parallel to clock inputs of both the flip flop.

But the Q<sub>p</sub> output of the first stage is used to derive the T and K inputs of second stage.

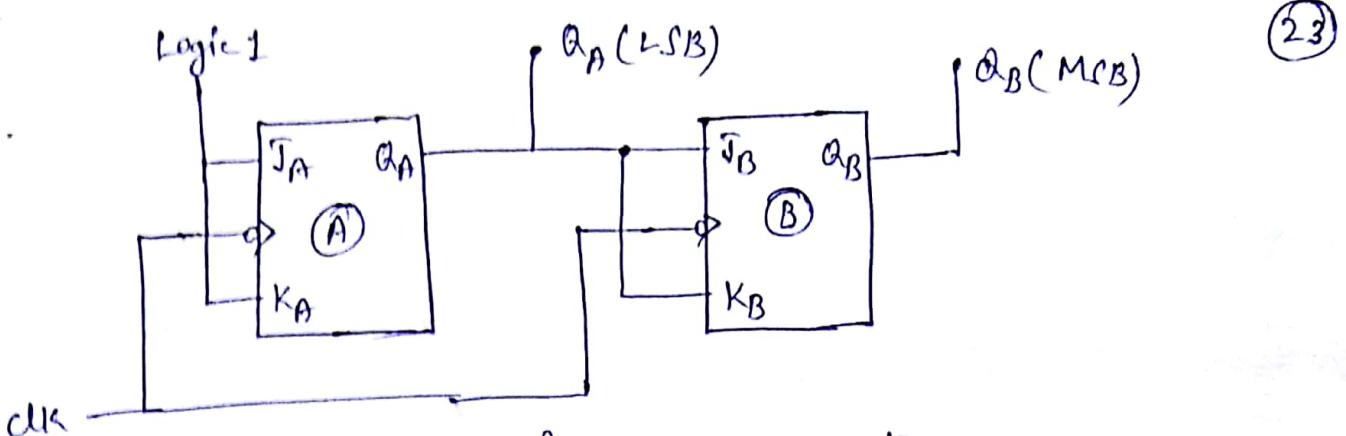


Fig: Two-Bit Synchronous counter.

### Operation

Initially assume that  $Q_A = Q_B = 0$ . For the first clock pulse negative edge, the flip flop A will toggle, because  $J_A = K_A = 1$  whereas flip flop B output will remain zero, because  $J_B = K_B = 0$  and  $Q_A = 1$  at the end of the pulse, i.e. -ve edge of the pulse. So after the first clock pulse  $Q_A = Q_B = 1$ .

At the negative edge of the second clock pulse, both flip flop will toggle because they both have a toggle condition on their J and K inputs. Thus after second clock pulse  $Q_A = 0$  and  $Q_B = 1$ .

At the negative edge of the third clock pulse, flip flop A toggles making  $Q_A = 1$ , but flip flop B remains set i.e.  $Q_B = 1$ . Hence, at the end of the third clock pulse  $Q_A = Q_B = 1$ .

Finally, at the negative edge of the fourth clock pulse, both flip flops toggle as their JK inputs are all logic 1. This results in  $Q_A = Q_B = 0$  and the counter is recycled back to its original state.

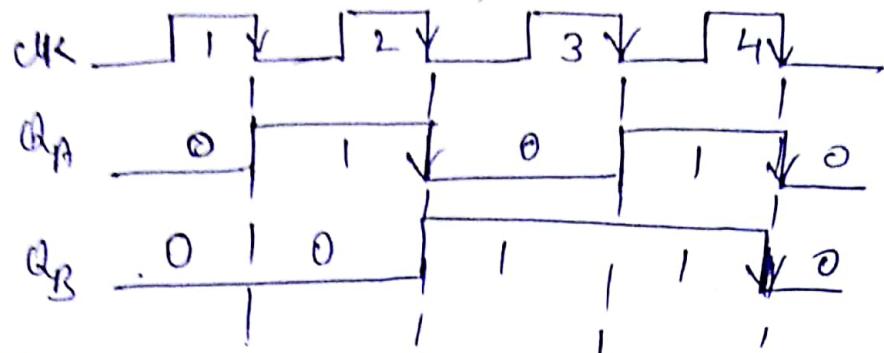


Fig: Timing diagram of 2-bit synchronous counter  
 → 3-bit synchronous binary counter in

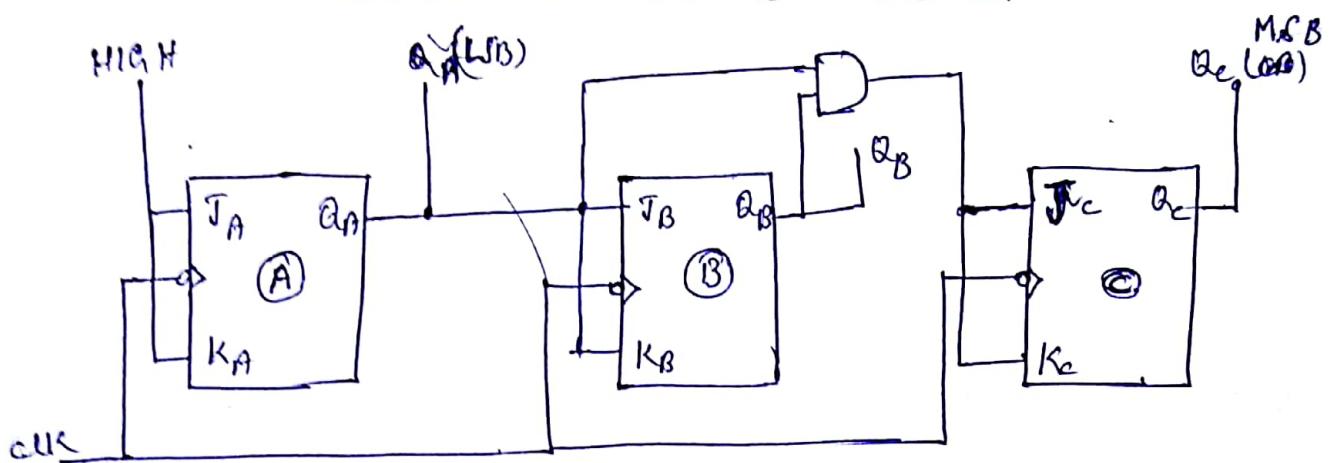


Fig:- Logic diagram of 3-bit synchronous counter

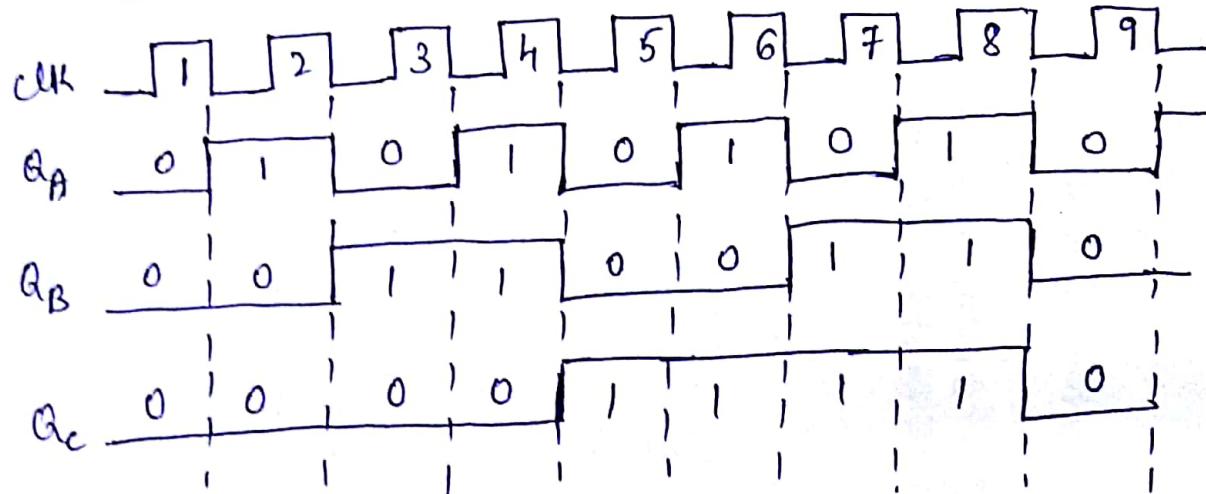


Fig: Timing diagram of 3-bit synchronous counter

Table: State Sequence of 3-bit Synchronous counter

clk	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

we can notice that flip flop C has to change its state only when Q<sub>A</sub> and Q<sub>B</sub> both are at logic 1. This condition is detected by AND gate and applied to the J<sub>C</sub> and K<sub>C</sub> inputs of flip flop C. whenever both Q<sub>A</sub> and Q<sub>B</sub> are HIGH, the output of the AND gate makes the J and K inputs of the flip flop C HIGH and flip flop C toggles on the clock pulse.

other than Q<sub>A</sub> = Q<sub>B</sub> = 1, the J and K inputs of flip flop C are held low by the AND gate output and the flip flop does not change its state.

→ Comparison between Synchronous Versus Asynchronous counter.

#### Synchronous counter

- \* In this type of counters there is no connection of first flip flop output to clock input of the next flip flop.
- \* All the flip flops are clocked simultaneously

#### Asynchronous counter

- \* In this counter flip flops are connected in such a way that the first flip flop output is the clock for the next flip flop.
- \* All the flip flops are not clocked simultaneously.

- \* Complex logic circuits for more number of states
- \* High Speed when compared to asynchronous counter
- \* Design is very simple even for more number of states.
- \* Low Speed.

→ Design procedure of Synchronous counter

Step 1 Obtain the number of states from the given information.

Step 2 Determine the number of required flip flops.

Step 3 Write the Excitation table of above obtained flip flop.

Step 4 Develop the circuit state table by using Excitation table.

Step 5 Use K-map to find the Expression for corresponding input function of counter.

Step 6 Draw the Counter circuit by using flip flop and required gates, from the above obtained Boolean Expression.

→ Modulus N counter

Defn. Modulus: The number of states through which a counter sequences before repeating.

Modulo-n (or Mod -n) counter: A counter with a modulus of n states.

The counter with n flip flop has maximum mod number ~~2^n~~  $2^n$

Eg 4 bit binary counter is mod 16 counter  
 $(2^4 = 16)$

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The required flip flop for counter must satisfy  
satisfy the following relation.

$$2^n \geq N$$

where  $n$  - Number of bit from ~~the~~ is equal to  
number of required flip flop (one flip flop  
store one bit)

$N$  - Total number of states.

Eg) Design Mod 4 Synchronous counter using JK  
flip flops and implement it.

Solution MOD 4 counter

Step 1: Here 4 indicates total number of states (0, 1, 2  
and 3)

Step 2: The required flip flop

$$2^n \geq N$$

$$2^n \geq 4$$

$$\boxed{n = 2}$$

Two flip flops are required to design MOD 4 counter.  
The flip flops are labelled as A and B.

Step 3: Excitation table for  
JK flip flop.

present state	Next State	Flip flop inputs	
$Q_n$	$Q_{n+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth table JK flip flop						
PS	NS	J	K	Qn	Qn+1	State
0	0	0	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	1	1	0	1
1	0	1	1	0	1	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0

Reset  
Set  
Toggle

~~Step 4:-~~ Step 4:- State table or transition table.

Present state		Next state		Flip flop inputs			
$Q_A$	$Q_B$	$Q_{A+1}$	$Q_{B+1}$	$J_A$	$K_A$	$J_B$	$K_B$
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

Step 5: K-map Simplification

For  $J_A$

$Q_A$	$Q_B$	0	1
0	0	0	1
1	X	X	1

$$J_A = Q_B$$

For  $K_A$

$Q_A$	$Q_B$	0	1
0	0	X	0
1	0	1	1

$$K_A = Q_B$$

For  $J_B$

$Q_A$	$Q_B$	0	1
0	1	0	X
1	1	X	1

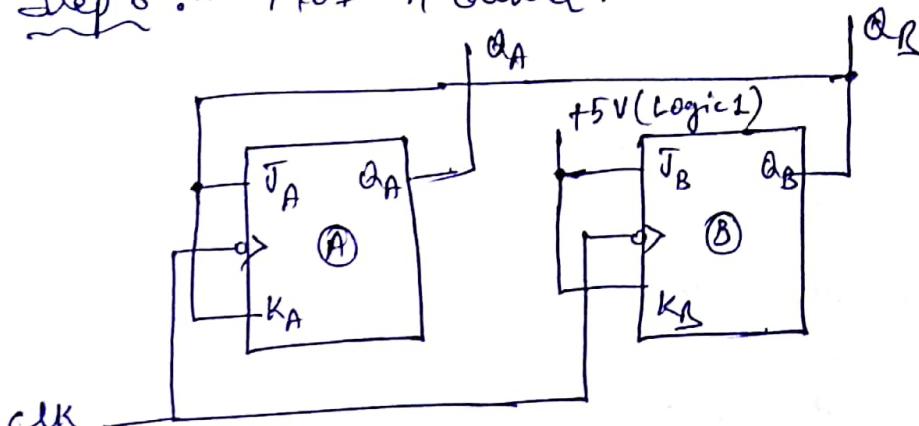
$$J_B = 1$$

For  $K_B$

$Q_A$	$Q_B$	0	1
0	X	0	1
1	X	1	1

$$K_B = 1$$

Step 6: in MOD 4 counter.



2) Design Mod 5 counter using JK flip-flops and implement it.

Soln:- MOD 5 counter

Step 1:- Here 5 indicates total number of states (0, 1, 2, 3 and 4)

Step 2:- The required flip flop

$$2^n \geq N$$

$$2^n \geq 5$$

$$n=3$$

Three flip flops are required to design Mod 5 counter. (29)  
The flip flops are labeled as A, B and C.

Step 3: Excitation table for JK flip flop

Present state	Next state	Flip flop inputs	
$Q_n$	$Q_{n+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 4: State table or Transition table.

The skipped states are 101, 110, 111. Enter the 'X' for these states.

Present state			Next state			Flip flop inputs					
$Q_C$	$Q_B$	$Q_A$	$Q_{C+1}$	$Q_{B+1}$	$Q_{A+1}$	$J_C$	$K_C$	$J_B$	$K_B$	$J_A$	$K_A$
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Step 5: K-map simplification

For  $J_C$

$Q_B Q_A$	00	01	11	10
$Q_C$	0	0, 1	1, 0	0, 2
	0	$X_4$	$X_5$	$X_7$
	1			$X_6$

$J_C = Q_A Q_B$

For  $K_C$

$Q_B Q_A$	00	01	11	10	
$Q_C$	0	$X_0$	$X_1$	$X_3$	$X_2$
	1	$X_4$	$X_5$	$X_7$	$X_6$

$K_C = 1$

(30)

For  $J_B$

$Q_B Q_A$	00	01	11	10	
$Q_C$	0	0	1	$X_3$	$X_2$
	1	$X_4$	$X_5$	$X_7$	$X_6$

$$J_B = Q_A$$

For  $K_B$

$Q_B Q_A$	00	01	11	10	
$Q_C$	0	$X$	$X$	1	0
	1	$X$	$X$	$X$	$X$

$$K_B = \bar{Q}_A$$

For  $J_A$

$Q_B Q_A$	00	01	11	10	
$Q_C$	0	1	$X$	$X$	1
	1	0	$X_4$	$X_5$	$X_7$

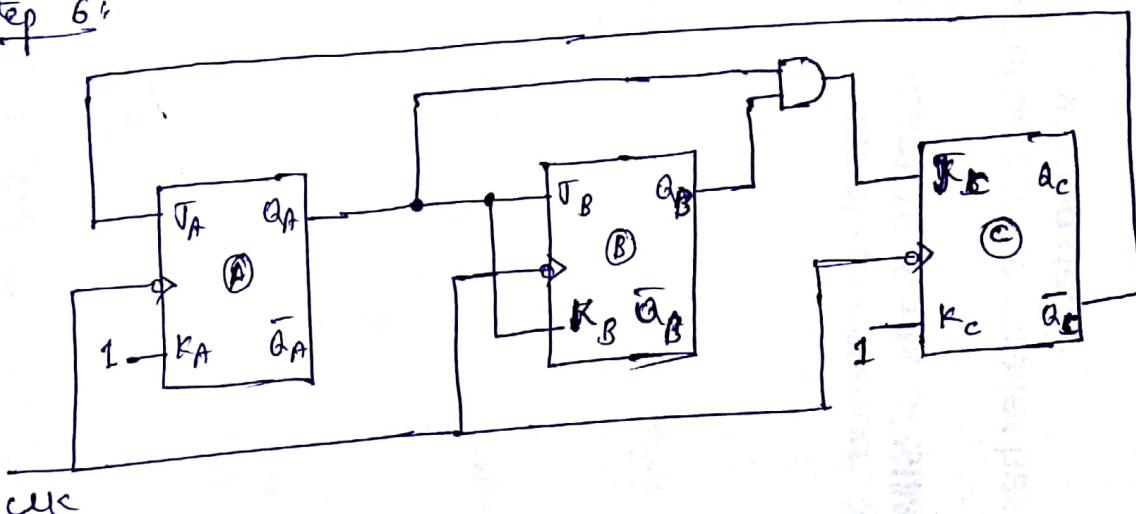
$$J_A = \bar{Q}_C$$

for  $K_A$

$Q_B Q_A$	00	01	11	10	
$Q_C$	0	$X_6$	1	1	$X_2$
	1	$X_4$	$X_5$	$X_7$	$X_6$

$$K_A = 1$$

Step 6:



→ Up / Down Synchronous Counter

Defn: Up counter :- A counter with an ascending sequence

Down counter :- A counter with an descending sequence.

\* An up/down counter is one that is capable of progressing progressing in ascending order or descending order through a certain sequence.

\* An up/down counter is also called bidirectional counter.

- \* Usually up/down operation of the counter is controlled by UP/DOWN signal.
- \* When this signal is HIGH, counter goes through UP sequence, i.e. 0, 1, 2, 3, ..., n. When UP/DOWN signal is LOW counter follows reverse sequence i.e. n, n-1, n-2, ..., 1, 0.

For 3-bit counters these sequences are:

0, 1, 2, 3, 4, 5, 6, 7 for up sequence and 7, 6, 5, 4, 3, 2, 1, 0 for down sequence.

State table for Three bit up/down Counter

CP	UP	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

- i) Design a Synchronous Gray code MOD 6 up counter using JK flip flop and Implement it.

Sdn: MOD 6 up counter

Step 1: Here 6 indicates total number of states (0, 1, 2, 3, 4 and 5)

Step 2: The required flip flop

$$2^n \geq N$$

$$2^n \geq 6$$

$$\boxed{n = 3}$$

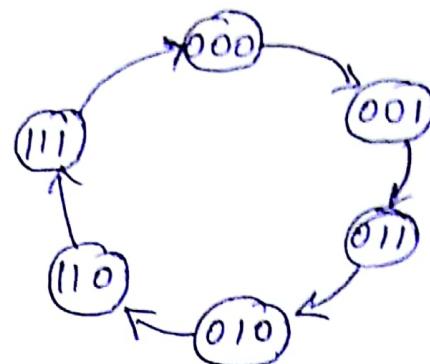
Three flip flops are required to design MOD 6 counter.

MOD-6  
Straight binary

000	(0)	000	(0)
001	(1)	001	(1)
010	(2)	011	(3)
011	(3)	010	(2)
100	(4)	110	(6)
101	(5)	111	(7)

MOD-6  
Gray code

State diagram



Step 4: State table

Present state			Next state			Flip flop. Inputs					
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$\bar{J}_A$	$K_A$	$\bar{J}_B$	$K_B$	$\bar{J}_C$	$K_C$
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	1	1	0	1	X	X	0	0	X
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

(The unused states are 100, 101)

Step 3: Excitation table for JK flip flop.

present state		next state		flip flop inputs	
$Q_n$	$Q_{n+1}$	$Q_n$	$Q_{n+1}$	J	K
0	0	0	0	0	X
0	1	1	1	1	X
1	0	0	1	X	1
1	1	1	1	X	0

Step 5: K-map simplification

		$Q_B Q_C$	
		00	01
$Q_A$	0	0, 0	1, 0
	1	X, 1	X, 0

$$\bar{J}_A = Q_B Q_C$$

		$Q_B Q_C$	
		00	01
$Q_A$	0	X, 0	X, 1
	1	0, 1	X, 0

$$K_A = Q_C$$

For  $J_B$ 

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	0, 0	1, 1	$X_3$	$X_2$	
1	$X_4$	$X_5$	$X_4$	$X_6$	

$$\bar{J}_B = Q_C$$

For  $J_C$ 

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	1, 0	$X_1$	0, 3	$X_2$	
1	1, 1	$X_5$	$X_7$	$X_6$	

$$\bar{J}_C = Q_B$$

For  $K_B$ 

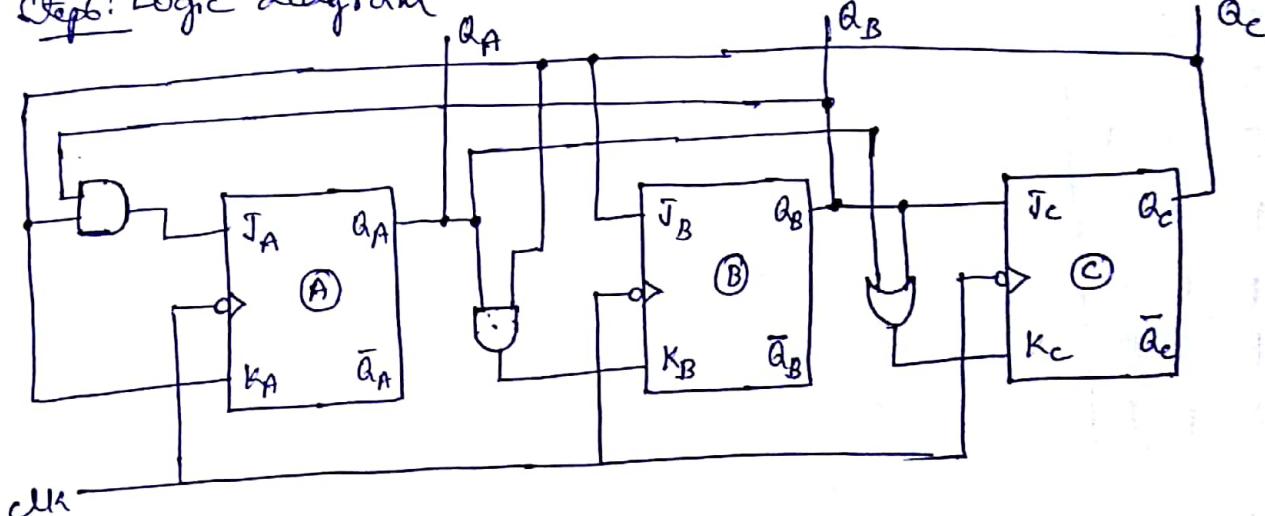
$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	$X_0$	$X_1$	0, 3	$X_2$	
1	0, 4	1, 5	$X_7$	$X_6$	

$$K_B = Q_A Q_C$$

For  $K_C$ 

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	$X_0$	0, 1	$X_3$	1	
1	$X_4$	1, 5	$X_7$	$X_6$	

$$K_C = Q_A + Q_B$$

Step 1: Logic diagram

- 2) Design a synchronous binary MOD 6 counter using JK flip flop and Implement it.

Solution Step 1:- Here 6 indicates total number of states (0, 1, 2, 3, 4 and 5)

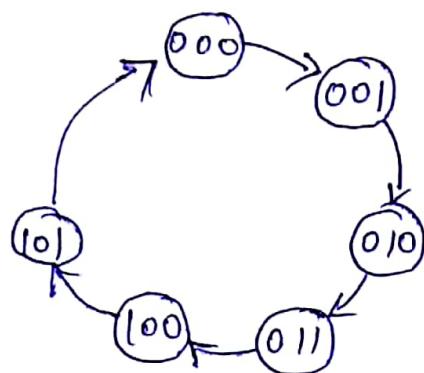
Step 2: The required flip flop

$$2^n \geq N$$

$$2^n \geq 6$$

$$n=3$$

Three flip flops are required to design MOD 6 counter.

state diagramTruth table J K flip flop

J	K	$Q_n$	$Q_{n+1}$	State
0	0	0	0	
0	0	1	1	NC
0	1	0	0	
0	1	1	0	Reset.
1	0	0	1	
1	0	1	1	Sel.
1	1	0	1	
1	1	1	0	Toggle

Step 3 :- Excitation table for JK flip flop.

present state	next state		flip flop inputs	
	$Q_n$	$Q_{n+1}$	J	K
0	0	0	0	X
0	0	1	1	X
1	0	0	X	1
1	0	1	X	0

Step 4 :- State table

present state	next state			flip flop inputs								
	$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	J <sub>A</sub>	K <sub>A</sub>	J <sub>B</sub>	K <sub>B</sub>	J <sub>C</sub>	K <sub>C</sub>
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	0	1	0	0	X	1	X	X	1
0	1	0	0	0	1	1	0	X	X	0	1	X
0	1	1	0	1	0	0	1	X	X	1	X	1
1	0	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	0	X	1	0	X	X	1
1	1	0	0	X	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X	X

## Step 5 K-map simplification

for  $J_A$

		Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	
		00	01	11	10
		0	0, 0	1 <sub>3</sub>	0 <sub>2</sub>
0	0	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>
1	1				

$$J_A = Q_B \bar{Q}_C$$

For  $K_A$

		Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>
		00	01	11	10
		0	X <sub>0</sub>	X <sub>1</sub> , X <sub>3</sub>	X <sub>2</sub>
0	0	0	1 <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
1	1	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$$K_A = Q_C$$

For  $J_B$

		Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>
		00	01	11	10
		0	0, 0	1 <sub>1</sub> , X <sub>3</sub>	X <sub>2</sub>
0	0	0	1 <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
1	1	0 <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$$J_B = \bar{Q}_A Q_C$$

For  $K_B$

		Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>
		00	01	11	10
		0	X <sub>0</sub>	X <sub>1</sub> , 1 <sub>3</sub>	0 <sub>2</sub>
0	0	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>
1	1				

$$K_B = Q_C$$

For  $J_C$

		Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>
		00	01	11	10
		0	1 <sub>0</sub>	X <sub>1</sub> , X <sub>3</sub>	X <sub>2</sub>
0	0	1 <sub>0</sub>	X <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
1	1	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

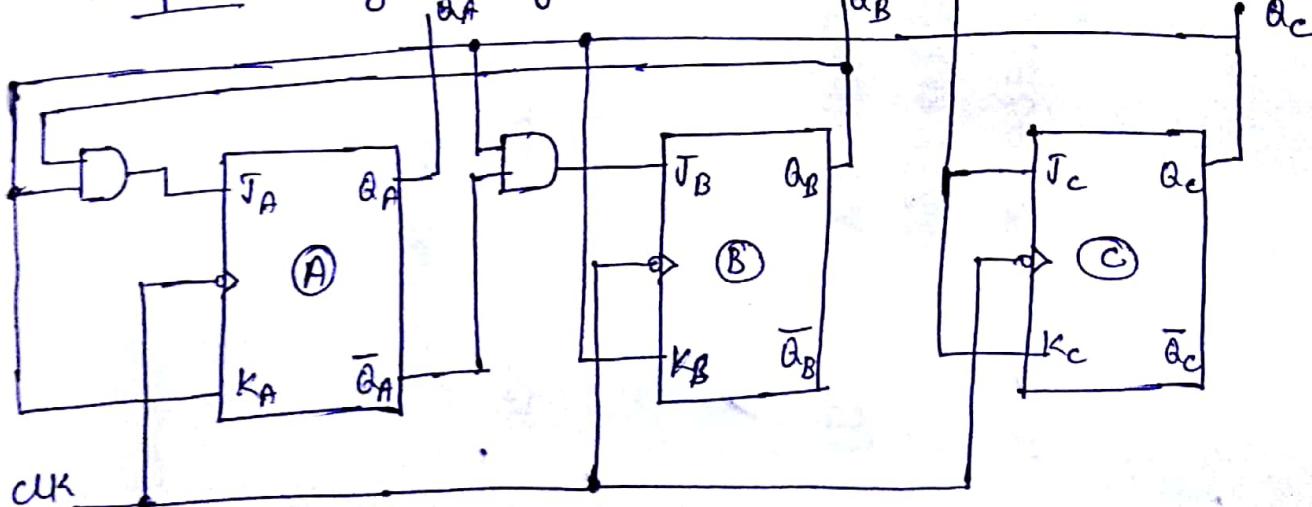
$$J_C = 1$$

For  $K_C$

		Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>	Q <sub>B</sub> Q <sub>C</sub>
		00	01	11	10
		0	X <sub>0</sub>	1 <sub>1</sub> , 1 <sub>3</sub>	X <sub>2</sub>
0	0	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>
1	1				

$$K_C = 1$$

## Step 6 Logic diagram



3) Design MOD 6 Synchronous counter using clocked D flip flop.

John: Here 6 indicates total no. of states (0, 1, 2, 3, 4 and 5)

Step 1:- Find the number of flipflops to build the counter.

Flip flops required are

$$2^n \geq N$$

$$2^n \geq 6$$

$$\boxed{n=3}$$

Three flip flops are required to design MOD 6 counter.

Step 3 in Excitation table for D flip flop

Present state	Next state	Flip flop inputs
$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

Truth table of D flip flop

D	$Q_n$ PS	$Q_{n+1}$ NS	State
0	x	0	Reset
1	x	1	Set
x	x	$Q_n$	NC

Step 4: State table or transition table

Present state			Next state			Flip flop inputs		
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$D_A$	$D_B$	$D_C$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	0	0	0	0	0	0
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

Step 5 : K-map Simplification

		$Q_B Q_C$	00	01	11	10
		$Q_A$	0	0	1	0
$Q_A$	$\bar{Q}_B \bar{Q}_C$	0	0	0	1	0
		1	1	0	X	X

$$D_A = Q_B Q_C + Q_A \bar{Q}_C$$

		$Q_B Q_C$	00	01	11	10
		$Q_A$	0	0	1	0
$Q_A$	$\bar{Q}_B \bar{Q}_C$	0	0	1	0	1
		1	0	0	X	X

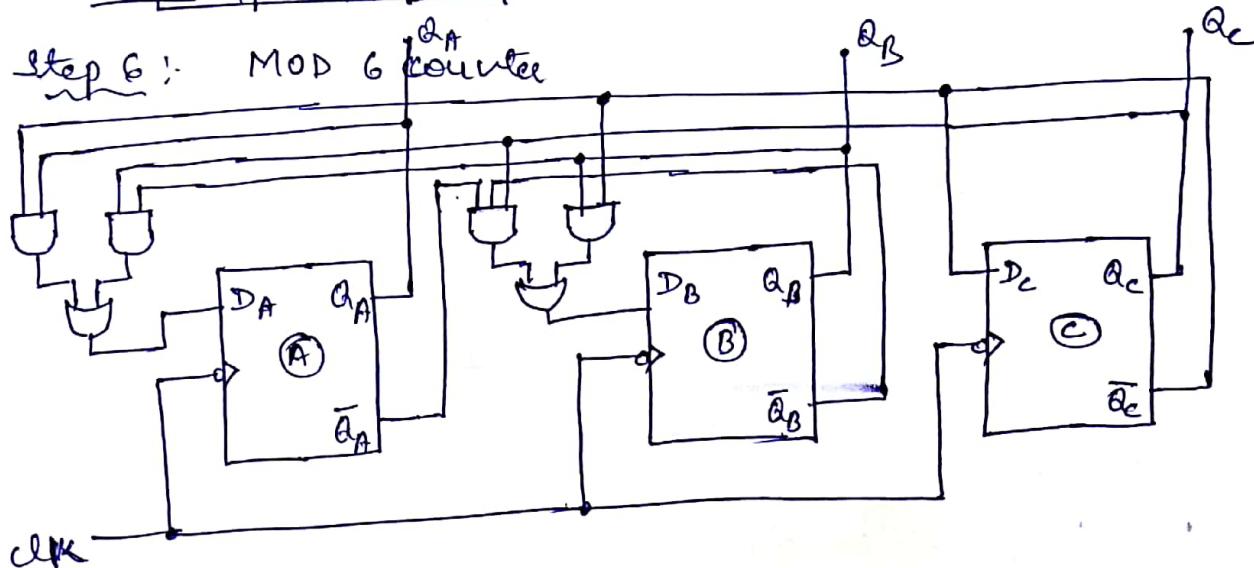
$$D_B = \bar{Q}_A \bar{Q}_B Q_C + Q_A \bar{Q}_C$$

For  $D_C$

		$Q_B Q_C$	00	01	11	10
		$Q_A$	0	0	1	0
$Q_A$	$\bar{Q}_B \bar{Q}_C$	0	1	0	0	1
		1	1	0	X	X

$$D_C = \bar{Q}_C$$

Step 6 : MOD 6 counter



→ Design MOD 6 Synchronous counter using clocked T flip flop.

Step 1 : Here 6 indicates total number of states ( $0, 1, 2, 3, 4$  and  $5$ )

Step 2 : Flip flops required are

$$2^n \geq N$$

$$2^n \geq 6$$

$$\boxed{n=3}$$

∴ Three flip flops are required to design MOD 6 counter.

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Step 3: in Excitation table for T flip flop.

present state	Next state	Flip flop Inputs
$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Truth table of  
T flip flop

P.S	$Q_n$	T	N.S	State
			$Q_{n+1}$	
	0	0	0	NC
	0	1	1	
	1	0	1	
	1	1	0	Toggle

Step 4: in State table or Transition table

present state			Next state			Flip flop inputs		
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$T_A$	$T_B$	$T_C$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X

Step 5: K-map simplification

For $T_A$		
$Q_A$	$Q_B Q_C$	
0	00 01 11 10	
1	04 15 X7 X6	

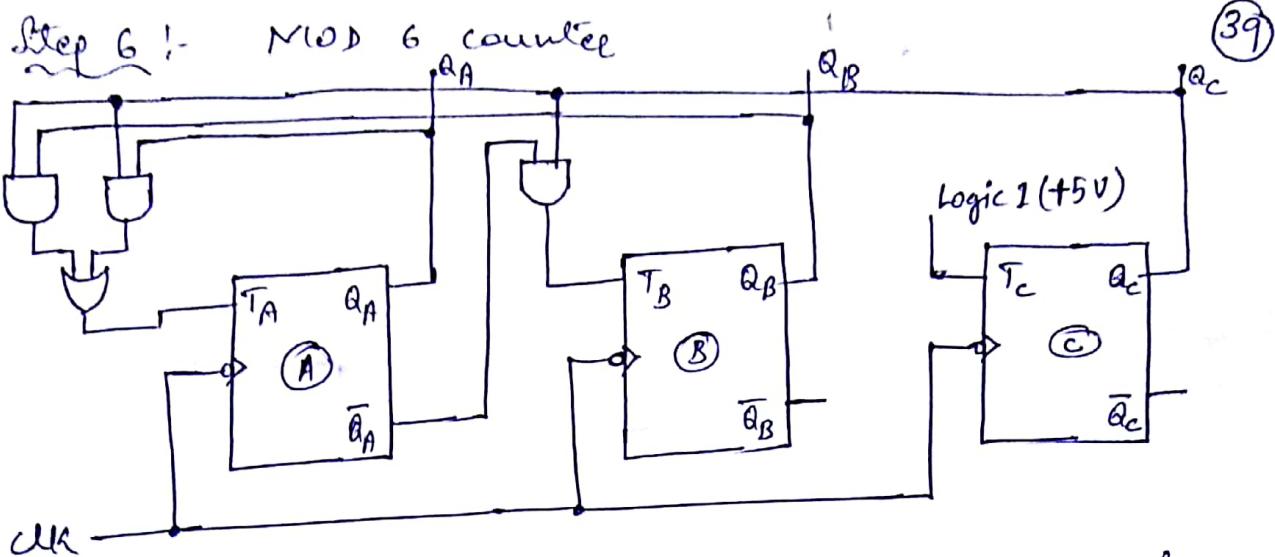
$$T_A = Q_B Q_C + Q_A Q_C$$

For $T_B$		
$Q_A$	$Q_B Q_C$	
0	00 01 11 10	
1	04 15 X7 X6	

$$T_B = \bar{Q}_A Q_C$$

For $T_C$		
$Q_A$	$Q_B Q_C$	
0	00 01 11 10	
1	14 15 X7 X6	

$$T_C = 1$$



5) Design MOD 6 synchronous counter using clocked SR flipflop.

Soln: Step 1 :- Here 6 indicates total number of states ( $0, 1, 2, 3, 4$  and  $5$ )

Step 2 :- Flip flops required are

$$2^n \geq N$$

$$2^n \geq 6$$

$$\boxed{n=3}$$

Totally Three flip flops required to design MOD 6 counter.

Step 3 :- Excitation table for SR flip flop.

Present State	Next State	Flip flop Inputs	
$Q_n$	$Q_{n+1}$	$S$	$R$
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Truth table of SR flip flop

S	R	$Q_n$ P.S	$Q_{n+1}$ N.S	State
0	0	0	0	
0	0	1	1	NC
0	1	0	0	
0	1	1	0	Reset
1	0	0	1	
1	0	1	1	Set
1	1	0	X	Indeterminate
1	1	1	X	Or unpredictable

Step 4 :- State table or Transition table.

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Present state			Next state			Flip flop inputs					
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$S_A$	$R_A$	$S_B$	$R_B$	$S_C$	$R_C$
0	0	0	0	0	1	0	X	0	X	1	0
0	0	1	0	1	0	0	X	1	0	0	1
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	0	0	1	0	0	1	0	1
1	0	0	1	0	1	X	0	0	X	1	0
1	0	1	0	0	0	0	1	0	X	0	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Step 5 :- K-map Simplification

For  $S_A$

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	0, 0, 1, 0	0, 0	1, 0	0, 2	
1	X, 0, X, X	X, 1	X, 1	X, 0	

$$S_A = Q_B \bar{Q}_C$$

For  $R_A$

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	0, X, X, X	0, X	X, 1	0, 3	X, 2
1	X, 0, 1, X	0, 4	1, 5	X, 7	X, 6

$$R_A = \bar{Q}_B \bar{Q}_C$$

For  $S_B$

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	0, 0, 0, 1	0, 0	0, 3	X, 2	
1	0, 1, X, X	0, 4	0, 5	X, 7	X, 6

$$S_B = \bar{Q}_A \bar{Q}_B \bar{Q}_C$$

For  $R_B$

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	X, 0, 0, 1	0, 0	0, 3	1, 2	
1	X, X, X, X	X, 4	X, 5	X, 7	X, 6

$$R_B = Q_B \bar{Q}_C$$

For  $S_C$

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	1, 0, 0, 1	0, 0	0, 3	1, 2	
1	1, X, X, X	1, 4	0, 5	X, 7	X, 6

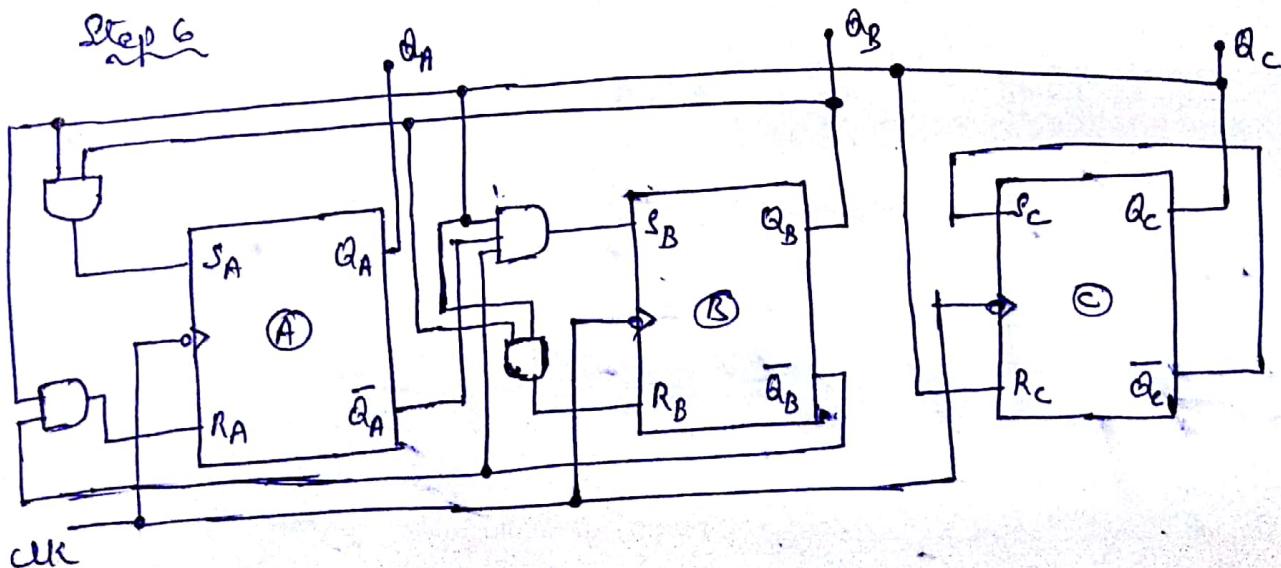
$$S_C = \bar{Q}_C$$

For  $R_C$

$Q_A$	$\bar{Q}_B \bar{Q}_C$	00	01	11	10
0	0, 0, 1, 1	0, 0	1, 1	1, 0	
1	0, 1, X, X	0, 4	1, 5	X, 7	X, 6

$$R_C = Q_C$$

Step 6



6) Design a counter with the irregular binary count sequence of 1, 2, 5 and 7. ... using T flipflop. (H1)

Soln:

There are only four states, a 3 bit counter is required to implement this sequence because the maximum binary count is seven.

Since the required sequence does not include all the possible binary states, the invalid states (0, 3, 4 and 6) can be treated as don't care in the design.

Unused states are (000, 011, 100, 110)

Step 1: Here 8 ~~8~~ indicates total number of states (1, 2, 5 and 7)

Step 2: Flip flop required are

$$2^n \geq N$$

$$2^n \geq 8 \quad 2^n \geq 2^3$$

$$\boxed{n=3}$$

Totally three flip flops are required to design MOD 8 counter.

Step 3: Excitation table for T flip flop

present state	Next State	Flip flop inputs
$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4 : State table

(42)

Present state			Next state			Flip flop Inputs		
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$T_A$	$T_B$	$T_C$
X	X	X	X	X	X	X	X	X
0	0	1	0	1	0	0	1	1
0	1	0	1	0	1	1	1	1
X	X	X	X	X	X	X	X	X
X	X	X	X	X	X	X	X	X
1	0	1	1	1	1	0	1	0
X	X	X	X	X	X	X	X	X
1	1	1	0	0	1	1	1	0

Step 5 : K-map Simplification

For  $T_A$

$Q_A$	$Q_B Q_C$	00	01	11	10
0	$Q_A$	X	0	X	1
1	$\bar{Q}_A$	X	0	1	X

$$\therefore T_A = Q_B$$

For  $T_B$

$Q_A$	$Q_B Q_C$	00	01	11	10
0	$Q_A$	X	1	X	1
1	$\bar{Q}_A$	X	1	1	X

$$T_B = 1$$

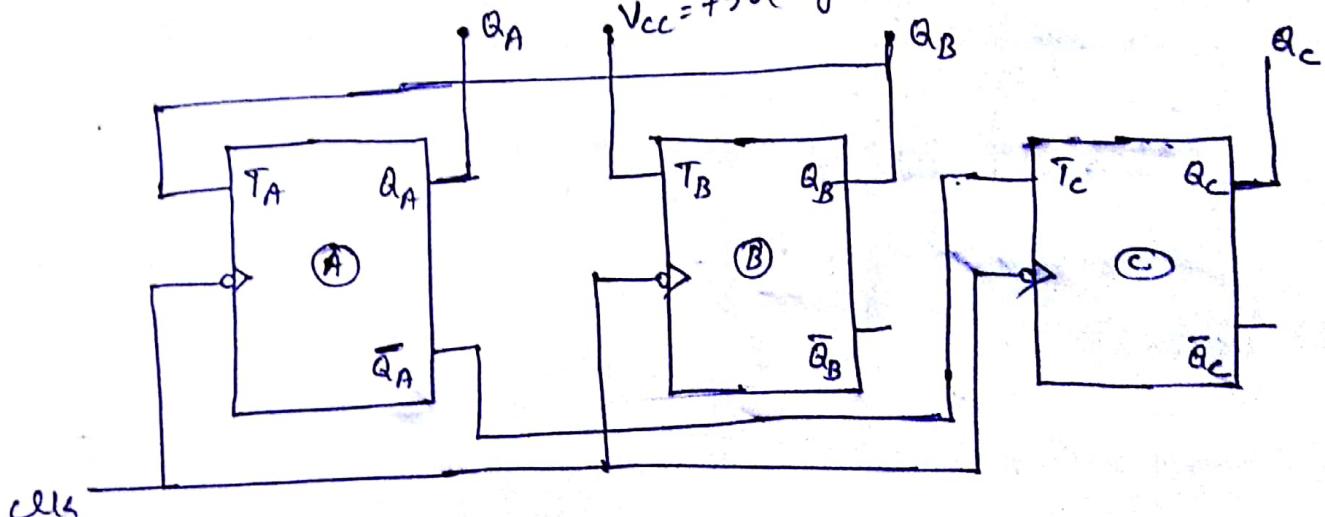
For  $T_C$

$Q_A$	$Q_B Q_C$	00	01	11	10
0	$Q_A$	X	1	X	1
1	$\bar{Q}_A$	X	0	0	X

$$T_C = \bar{Q}_A$$

Step 6 : MOD-8 counter

$V_{CC} = +5V$  (Logic 1 at HIGH)



clk

7) Design a MOD-8 synchronous counter using T flip flop.

Soln:-

Step 1 :- Here 8 indicates total number of states ( $0, 1, 2, 3, 4, 5, 6$  and  $7$ )

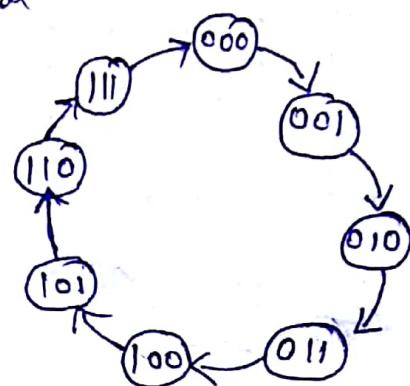
Step 2 :- Flip flops required are

$$2^n \geq N$$

$$2^n \geq 8$$

$$\boxed{n = 3}$$

State diagram



Totally three flip flops are required to design MOD 8 counter.

Step 3 :- Excitation table for T flip flops.

present state	Next state	Flip flop inputs
$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4 :- State table

present state			Next state			Flip flop inputs		
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$T_A$	$T_B$	$T_C$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Step 5 : ~ K-map simplification

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For  $T_A$

		Q <sub>B</sub> Q <sub>C</sub>	00	01	11	10
		Q <sub>A</sub>	0	0	1	0
		0	0	0	1	0
		1	0	0	1	0
		1	4	5	7	6

$$T_A = Q_B Q_C$$

For  $T_B$

		Q <sub>B</sub> Q <sub>C</sub>	00	01	11	10
		Q <sub>A</sub>	0	0	1	0
		0	0	0	1	0
		1	0	1	1	0
		1	4	5	7	6

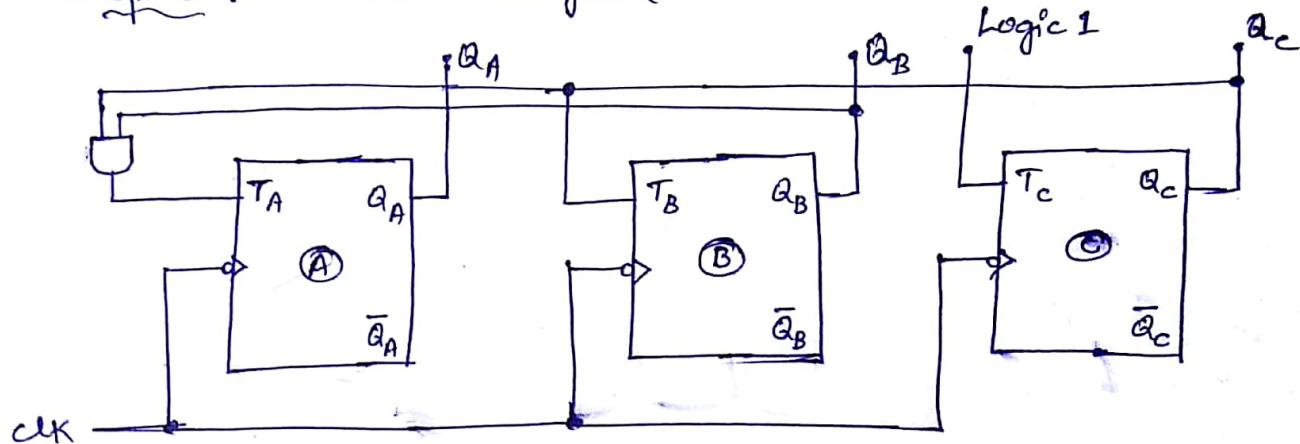
$$T_B = Q_C$$

For  $T_C$

		Q <sub>B</sub> Q <sub>C</sub>	00	01	11	10
		Q <sub>A</sub>	0	0	1	0
		0	1	1	1	1
		1	1	1	1	1
		1	4	5	7	6

$$T_C = 1$$

Step 6 : ~ State diagram



Design a counter with T flip flops that goes through the following binary repeated sequence : 0, 1, 3, 7, 6, 4.

Note: The states 2 and 5 are considered as don't care conditions.

Step 1:- Here 8 indicates total no. of states  
(0, 1, 3, 7, 6, 4)

Step 2:- Flip flops required are.

$$2^n \geq N$$

$$2^n \geq 8$$

$$n = 3$$

Three flip flops are required to design MOD 8 counter.

Step 3:- Excitation table of T flip flop.

present state	Next state	Flipflop inputs
$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4:- State table

present state	Next state	Flipflop inputs
A B C	A B C	$\bar{T}_A$ $T_B$ $T_C$
0 0 0	0 0 1	0 0 1
0 0 1	0 1 1	0 1 0
0 1 0	X X X	X X X
0 1 1	1 1 1	1 1 0
1 0 0	0 0 0	1 1 0
1 0 1	X X X	X X X
1 1 0	1 0 0	0 1 0
1 1 1	1 1 0	0 0 1

Step 5 :- K-map simplification

		For $T_A$				
		00	01	11	10	
		0	0	0	1	X
		1	X	0	0	

		For $T_B$				
		00	01	11	10	
		0	0	1	1	X
		1	D	X	0	1

		For $T_C$				
		00	01	11	10	
		0	1	0	0	X
		1	0	X	1	0

$$T_A = \bar{A}B + A\bar{B}$$

$$T_A = A \oplus B$$

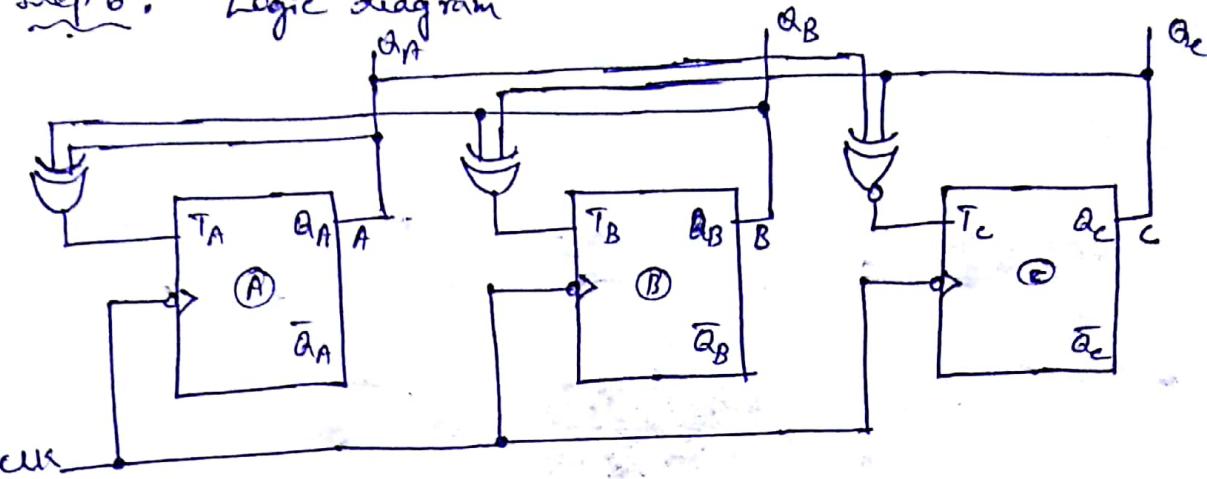
$$T_B = \bar{A}C + A\bar{C}$$

$$T_B = A \oplus C$$

$$T_C = AC + \bar{A}\bar{C}$$

$$T_C = A \oplus C$$

Step 6: Logic diagram



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2) Design a counter with the following repeated binary sequence: 1, 2, 3, 4, 5, 6 use JK flip flops.

Solution Step 1: Here 6 indicates total no. of states  
(1, 2, 3, 4, 5, 6)

Step 2: - Flip flops required are

$$2^n \geq N$$

$$2^n \geq 6$$

$$\boxed{n = 3}$$

Three flip flops are required to design MOD 6 counter.

Step 3: - Excitation table of JK flip flops

present state	Next State	Flip flop Input	
$Q_n$	$Q_{n+1}$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Step 4: State table

present state	Next State			Flip flop inputs							
	A	B	C	$J_A$	$K_A$	$J_B$	$K_B$	$J_C$	$K_C$		
000	0	0	0	x	x	x	x	x	x	x	x
001	0	0	1	0	x	1	x	x	x	x	1
010	0	1	0	0	x	x	0	1	x	x	x
011	0	1	1	1	x	x	1	x	x	x	1
100	1	0	0	x	0	0	x	1	x	x	1
101	1	0	1	x	0	0	x	1	x	x	x
110	1	1	0	x	0	1	x	x	1	x	x
111	1	1	1	x	x	x	x	x	x	x	x

### Step 5: K-map simplification

		For $J_A$					
		BC	00	01	11	10	
A			0	X <sub>0</sub>	0	1 <sub>B</sub>	0 <sub>A</sub>
1			1	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$$J_A = BC$$

		For $K_A$					
		BC	00	01	11	10	
A			0	X <sub>0</sub>	X <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
1			1	0 <sub>4</sub>	0 <sub>5</sub>	X <sub>7</sub>	1 <sub>6</sub>

$$K_A = B$$

		For $J_B$					
		BC	00	01	11	10	
A			0	X <sub>0</sub>	1	X <sub>3</sub>	X <sub>2</sub>
1			1	0 <sub>4</sub>	1	X <sub>7</sub>	X <sub>6</sub>

$$J_B = C$$

		For $K_B$					
		BC	00	01	11	10	
A			0	X <sub>0</sub>	X <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
1			1	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$$K_B = C + A$$

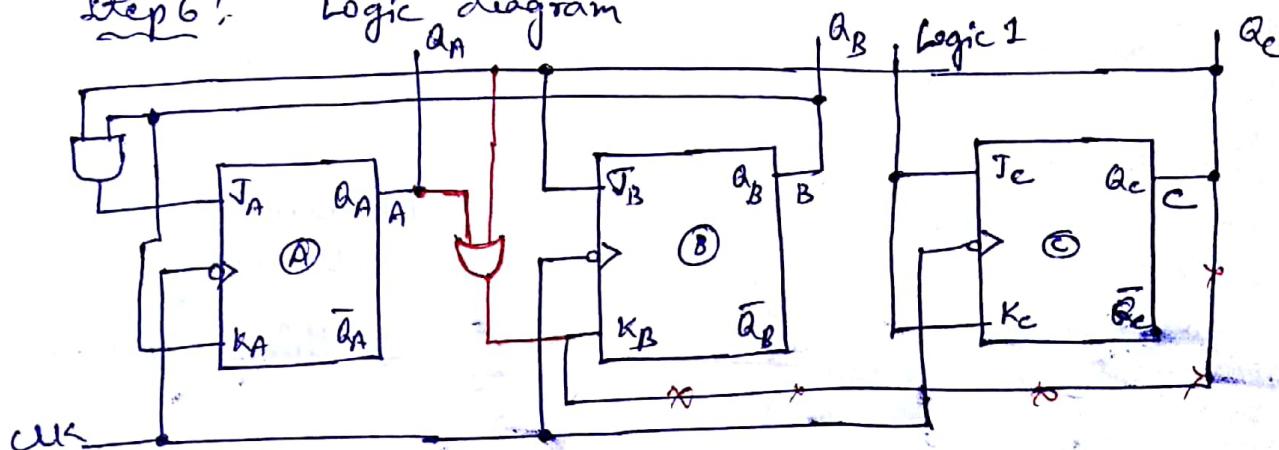
		For $J_C$					
		BC	00	01	11	10	
A			0	X <sub>0</sub>	X <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>
1			1	1 <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	1 <sub>6</sub>

$$J_C = 1$$

		For $K_C$					
		BC	00	01	11	10	
A			0	X <sub>0</sub>	1	1 <sub>3</sub>	X <sub>2</sub>
1			1	X <sub>1</sub>	1	X <sub>7</sub>	X <sub>6</sub>

$$K_C = 1$$

### Step 6: Logic diagram



3) Design a counter with the following repeated binary sequence 0, 1, 2, 4, 6 use D flip flops.

Step 2 Excitation table for D flip flop

present state	next state	FFifp
$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

### State table

present state	next state	FFifp's		
		A	B	C
000	001	0	0	1
001	010	0	1	1
010	100	1	0	0
011	XXX	X	X	X
100	110	1	1	0
101	XXX	X	X	X
110	000	0	0	0
111	XXX	X	X	X