PLANAR HKMG CMOS
PART C: DECK OVERVIEW

ECE 595 Semiconductor Device Integration Through Simulation

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Planar HKMG CMOS Flow: <output_root>_<index>_process.results file

```
output root: pcmos
index: 1
load point: 0
load file: NONE
mc_implant n.ions: N/A
```

simulation descriptors

```
z_depth: 0.2
z_height: 0.3
z_channel_offset: 0.0005
z_halo_depth: 0.012
poly_width: 0.028
iso_width: 0.03
iso_to_poly_width: 0.041
nisi_to_iso_width: 0.005
well_overlap: 0
sti_depth: 0.035
sti_angle: 85
t_ox_implant: 0.003
t_gox_sac: 0.001
t_ox_poly: 0.002
t_gox_sio2: 0.001
t_gox_hfo2: 0.002
t_tin: 0.002
t_nit_spacer: 0.01
t_nit_spacer_oe: 0.005
pwell_energy: 4
pwell_dose: 7e+12
nvt_energy: 4
nvt_dose: 6.9e+12
nwell_energy: 10
nwell_dose: 6.3e+12
pvt_energy: 10
pvt_dose: 2.4e+12
nhalo_energy: 3
nhalo_dose: 1.4e+13
phalo_energy: 8
phalo_dose: 1.8e+13
next_energy: 1.2
next_dose: 1e+15
pext_energy: 1.4
pext_dose: 2e+14
nsd_energy: 3
nsd_dose: 3e+15
psd_energy: 2
psd_dose: 7e+15
well_diff_temp: 1000
well_diff_time: 14
ext_diff_temp: 1000
ext_diff_time: 0.02 (seconds)
sd_diff_temp: 1000
sd_diff_time: 0.02 (seconds)
```

process input parameters

```
start: Fri Sep  6 17:59:40 UTC 2024

ext_depth_n: 0.00698898451
ext_depth_p: 0.00774702909
sd_depth_n: 0.0170415257
sd_depth_p: 0.019818278
leffj_n: 0.0245174904
lext_n: 0.0037412548
lmetal_n: 0.0259954244
overlap_n: 0.000738967
leffj_p: 0.0244574686
lext_p: 0.0037712657
lmetal_p: 0.02599542
overlap_p: 0.0007689757

end: Fri Sep  6 18:10:43 UTC 2024
```

extracted physical dimensions

e.g. "cmos_1_process.results"

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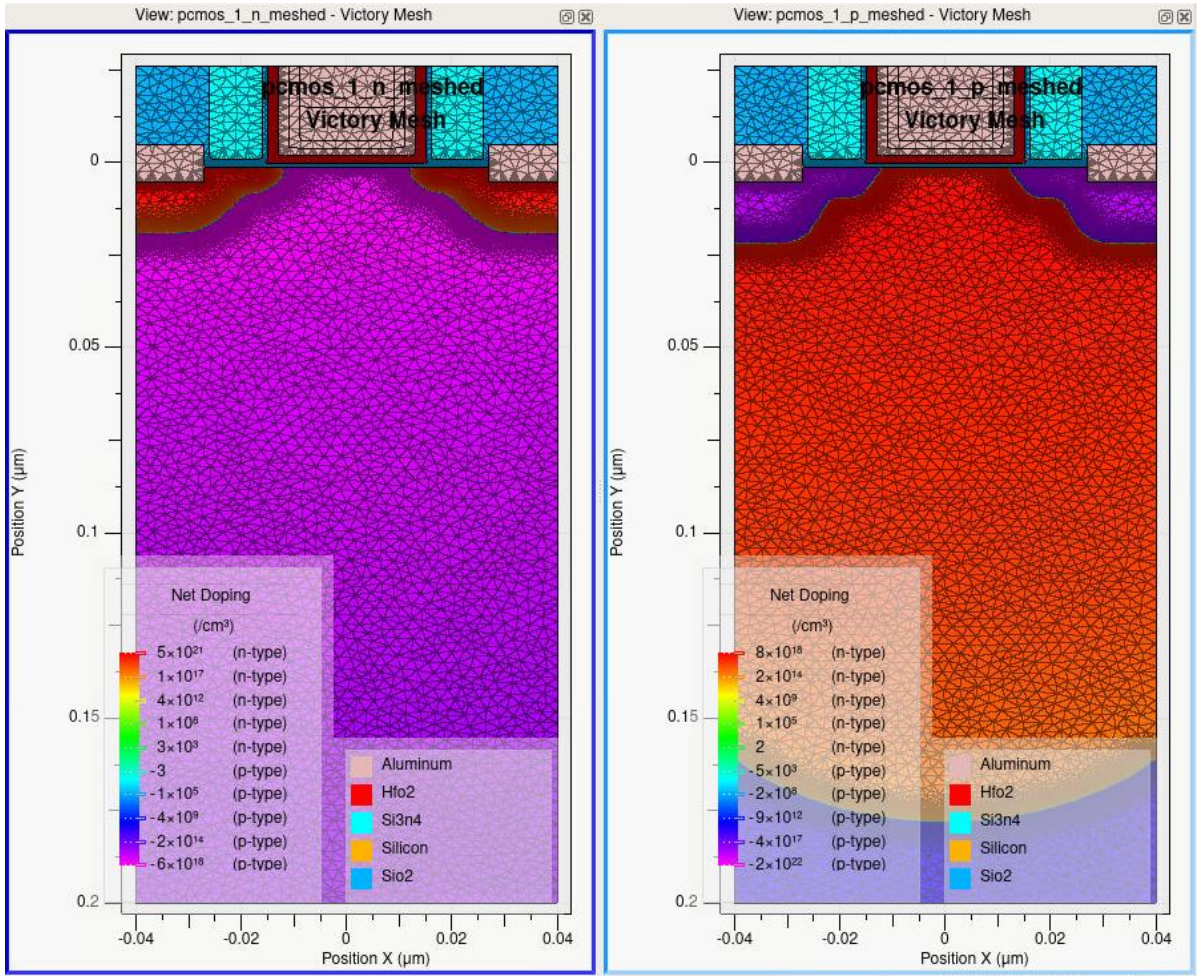
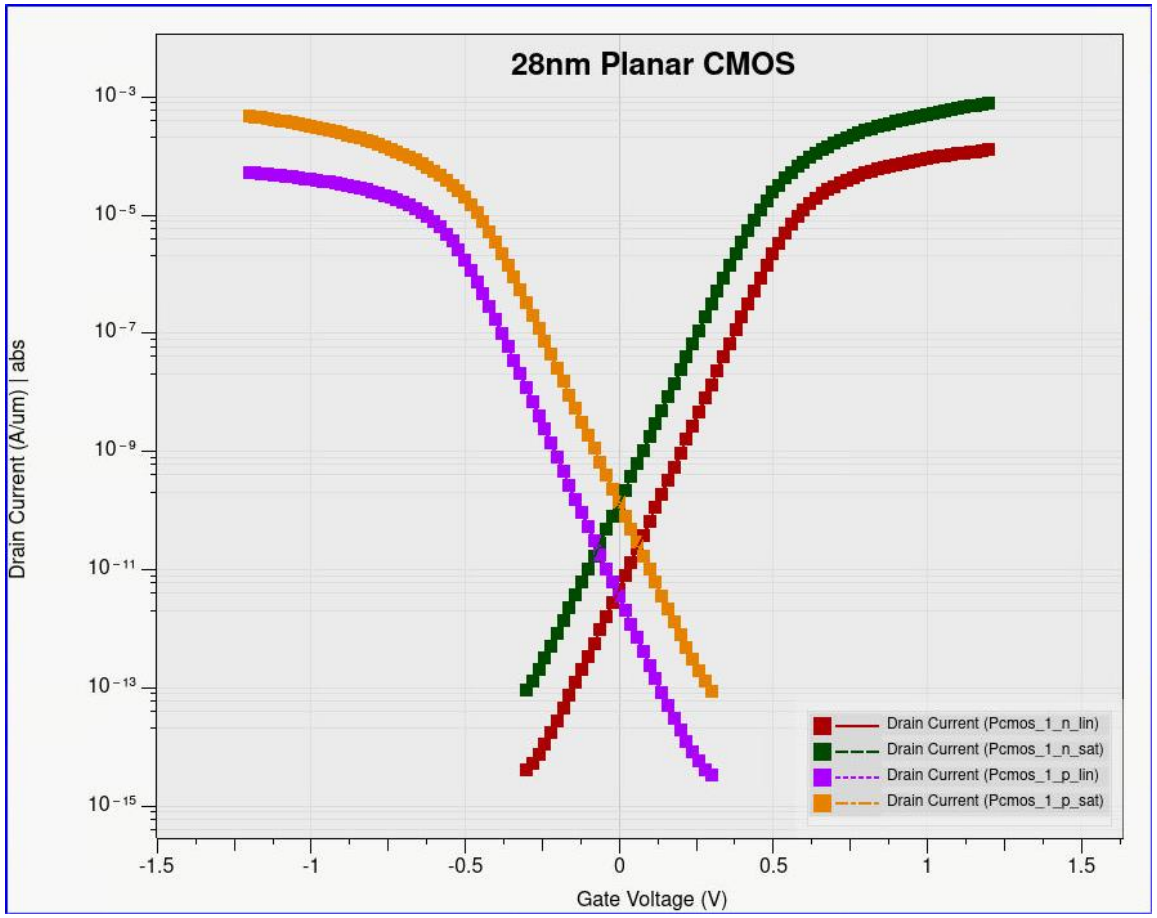
Planar HKMG CMOS Flow: Cropping and Meshing for Electrical Simulation



To allow electrical simulation with Victory Device, the individual N and P transistors are cropped, mirrored, translated, and re-meshed using Victory Mesh.

Planar HKMG CMOS Flow: Electrical Simulation Output



	N	P
Linear Threshold Voltage (Vg for Id=100nA/um, Id=0.05)	0.375	0.380
Saturation Threshold Voltage (Vg for Id=100nA/um, Id=0.05)	0.255	0.252
Idlin (Vd=1.2, Vg=0.05) uA/um	123.6	51.78
Idsat (Vd=Vg=1.2V) uA/um	759.3	468.9
Subthreshold Slope (mV/decade) linear (Vd=0.05)	87.5	88.5
Subthreshold Slope (mV/decade) saturation (Vd=1.2)	89.4	89.6
Off-State Leakage (nA/um) linear (Vd=0.05, Vg=0)	0.00456	0.00348
Off-State Leakage (nA/um) saturation (Vd=1.2, Vg=0)	0.131	0.136
Drain-Induced Barrier Lowering (mV)	120	128

The resulting device characteristics are well matched and well behaved.

Gate workfunctions set to 4.4eV and 5eV for n-channel and p-channel, respectively. Generation lifetimes of 100ps assumed for electrons and holes, with contact resistance of 10^{-10} ohm-cm^2.

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Planar HKMG CMOS Flow: Electrical Simulation Results Files

cmos_1_n_lin.results:

```
index: 1
device: n
bias: lin

structure width: 0.08
workfunction: 4.4
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*1
drain bias: 0.05*1
minimum gate voltage: -0.3*1
maximum gate voltage: 1.2*1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep  6 18:13:48 UTC 2024

Vth_[V]=0.37532027

Id_[uA/um]=123.563068

Ileak_[nA/um]=0.00456331986

slope=11.4277097

ss_[mV/dec]=87.5065981

vtgmax=0.55259331

end: Fri Sep  6 18:15:41 UTC 2024
```

cmos_1_n_sat.results:

```
index: 1
device: n
bias: sat

structure width: 0.08
workfunction: 4.4
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*1
drain bias: 1.2*1
minimum gate voltage: -0.3*1
maximum gate voltage: 1.2*1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep  6 18:16:08 UTC 2024

Vth_[V]=0.255489571

Id_[uA/um]=759.241263

Ileak_[nA/um]=0.130946582

slope=11.1821198

ss_[mV/dec]=89.4284821

vtgmax=0.634296593

end: Fri Sep  6 18:18:09 UTC 2024
```

cmos_1_p_lin.results:

```
index: 1
device: p
bias: lin

structure width: 0.08
workfunction: 5
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*-1
drain bias: 0.05*-1
minimum gate voltage: -0.3*-1
maximum gate voltage: 1.2*-1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep  6 18:18:37 UTC 2024

Vth_[V]=-0.380041581

Id_[uA/um]=-52.3006066

Ileak_[nA/um]=-0.00348364983

slope=-11.3024544

ss_[mV/dec]=-88.4763578

vtgmax=-0.515151573

end: Fri Sep  6 18:21:57 UTC 2024
```

cmos_1_p_sat.results:

```
index: 1
device: p
bias: sat

structure width: 0.08
workfunction: 5
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*-1
drain bias: 1.2*-1
minimum gate voltage: -0.3*-1
maximum gate voltage: 1.2*-1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep  6 18:22:24 UTC 2024

Vth_[V]=-0.251754859

Id_[uA/um]=-469.747069

Ileak_[nA/um]=-0.136159708

slope=-11.1564715

ss_[mV/dec]=-89.6340747

vtgmax=-0.622715814

end: Fri Sep  6 18:26:07 UTC 2024
```

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