PLANAR HKMG CMOS
PART A: BASELINE DESCRIPTION

ECE 595 Semiconductor Device Integration Through Simulation

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Planar HKMG CMOS Flow: Textbook Example

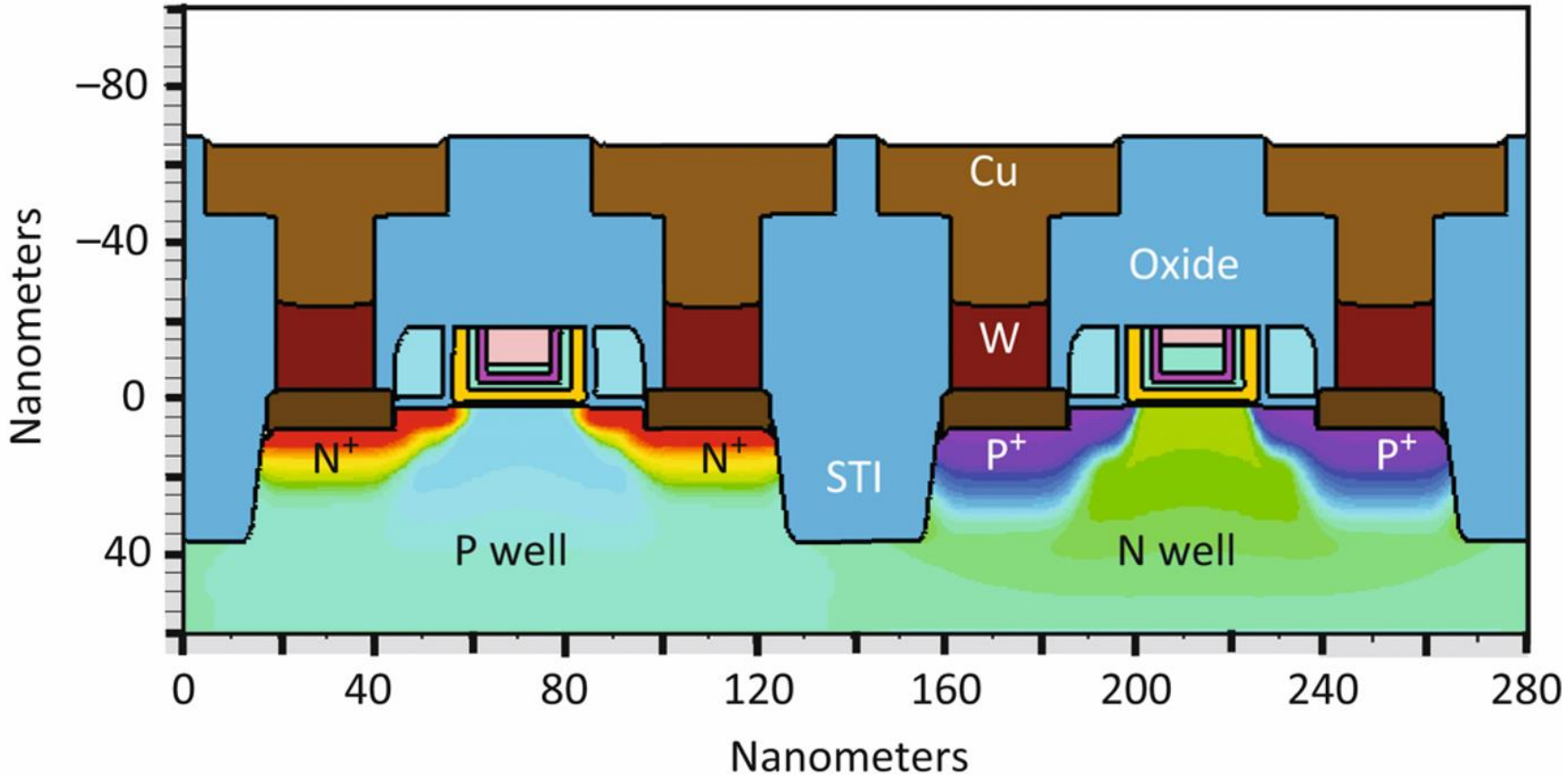


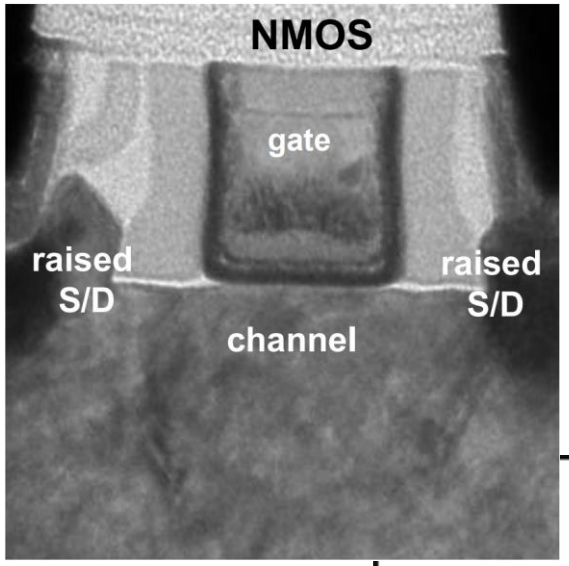
Figure 2.2 from ICFS&T (reversed)

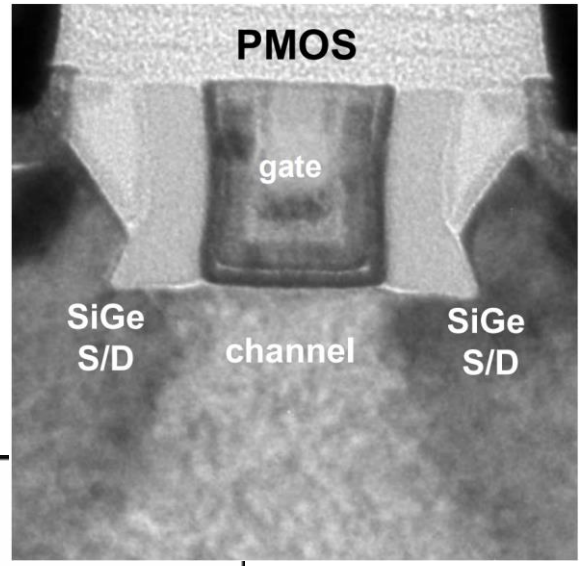
28nm Gates (poly), 30nm Isolation, 140nm N-P space

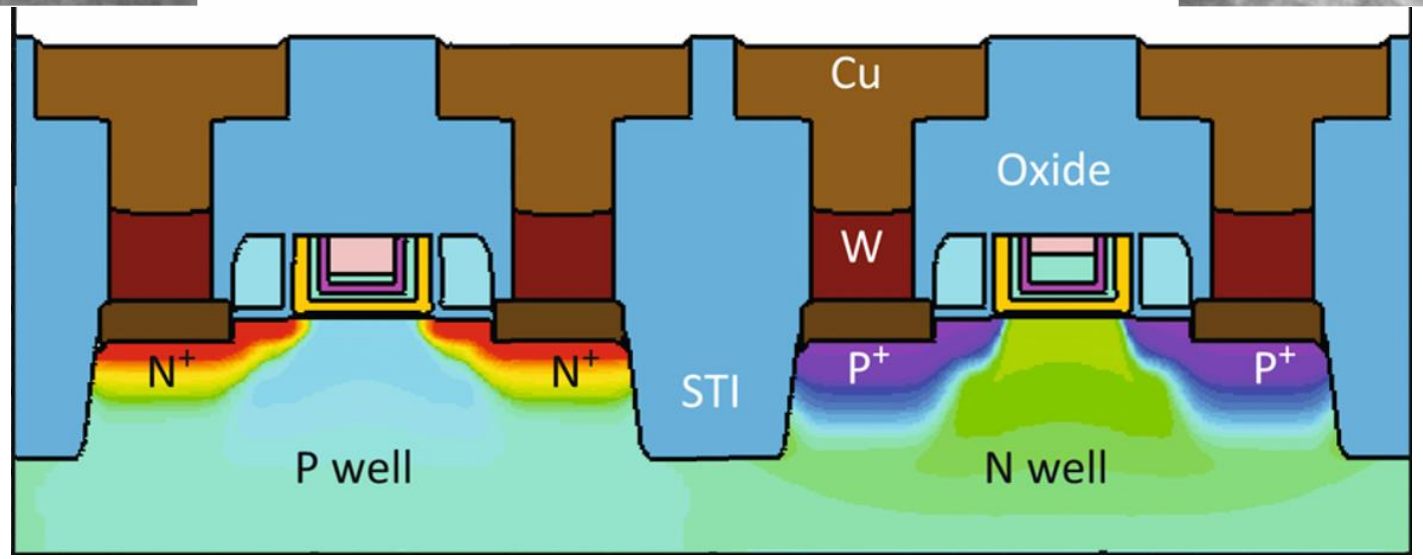
1nm SiO_2 with 3nm HfO_2 (gate metal length ~21nm)

Integrated Circuit Fabrication, Science and Technology, Figure 2.2 (reversed)

Planar HKMG CMOS Flow: Comparison with SEM Cross-Sections







Cross-sections from "High Performance 32nm Logic Technology Featuring2nd Generation High-k + Metal Gate Transistors", Intel, IEDM 2009

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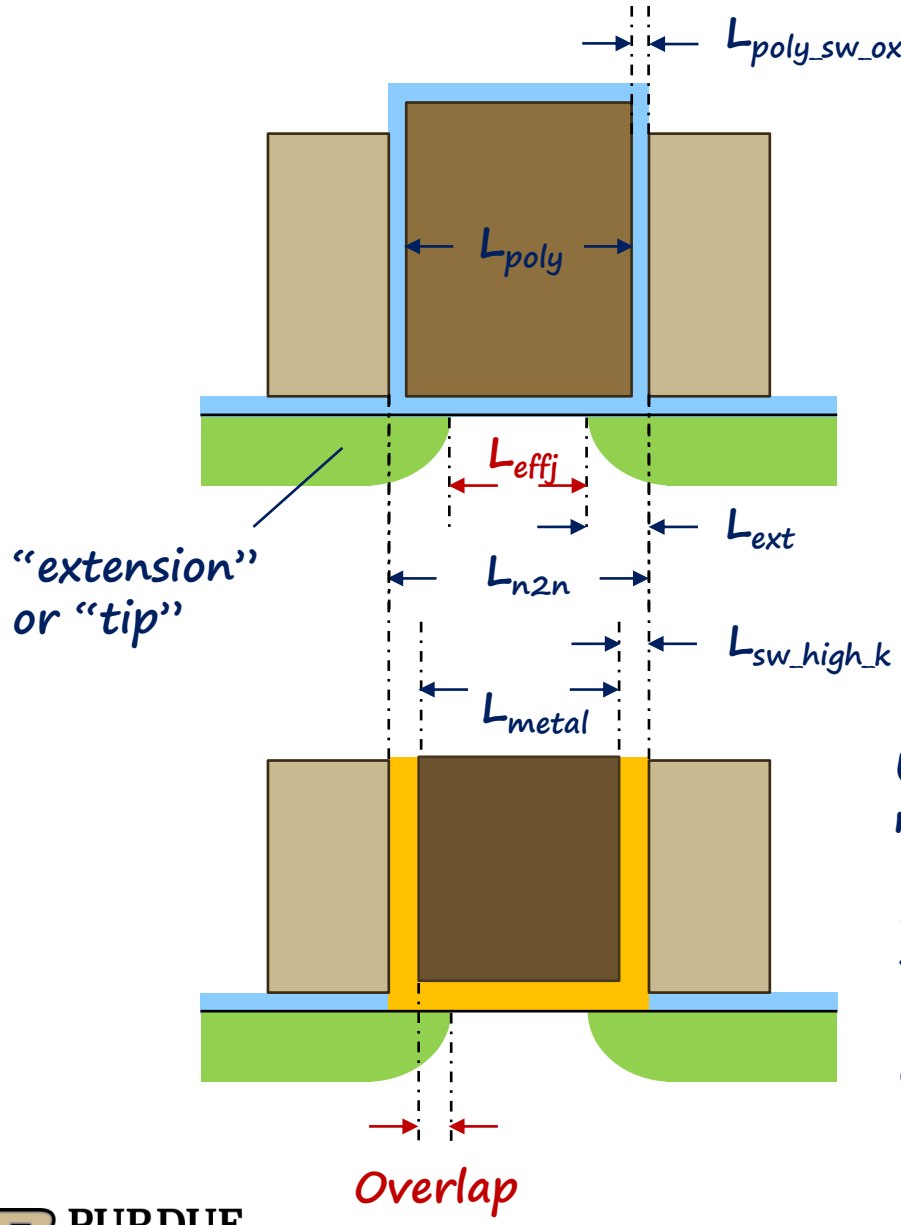
Planar HKMG CMOS Flow: Replacement Metal Gate Geometry



Nitride-to-nitride = $L_{n2n} = L_{poly} + 2 * L_{poly\_sw\_ox}$

Tip-to-tip = $L_{effj} = L_{n2n} - 2 * L_{ext}$

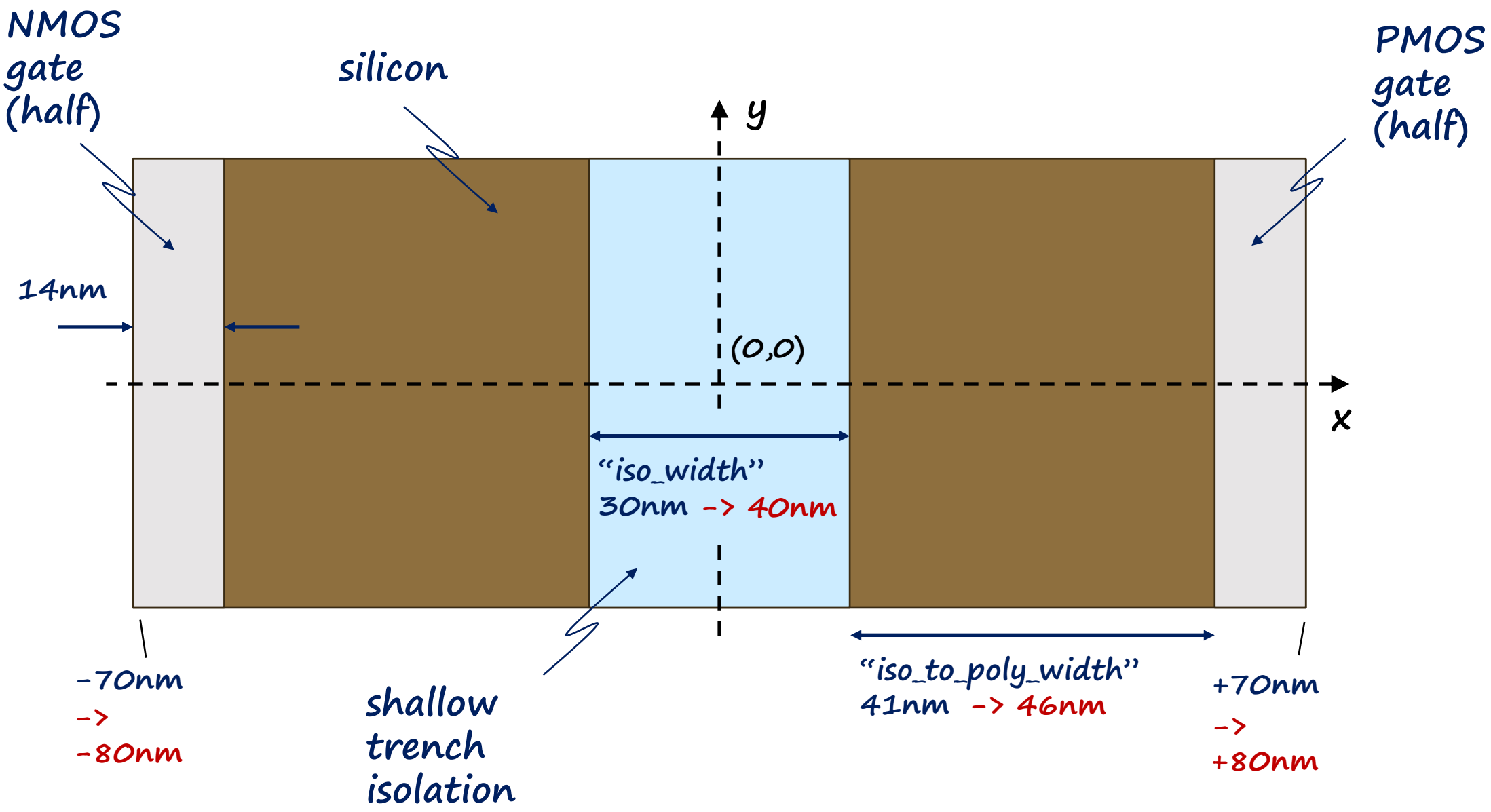
$L_{metal} = L_{n2n} - 2 * L_{sidewall\_high\_k}$

Overlap = $0.5 * (L_{metal} - L_{effj}) = L_{sidewall\_high\_k} - L_{ext}$

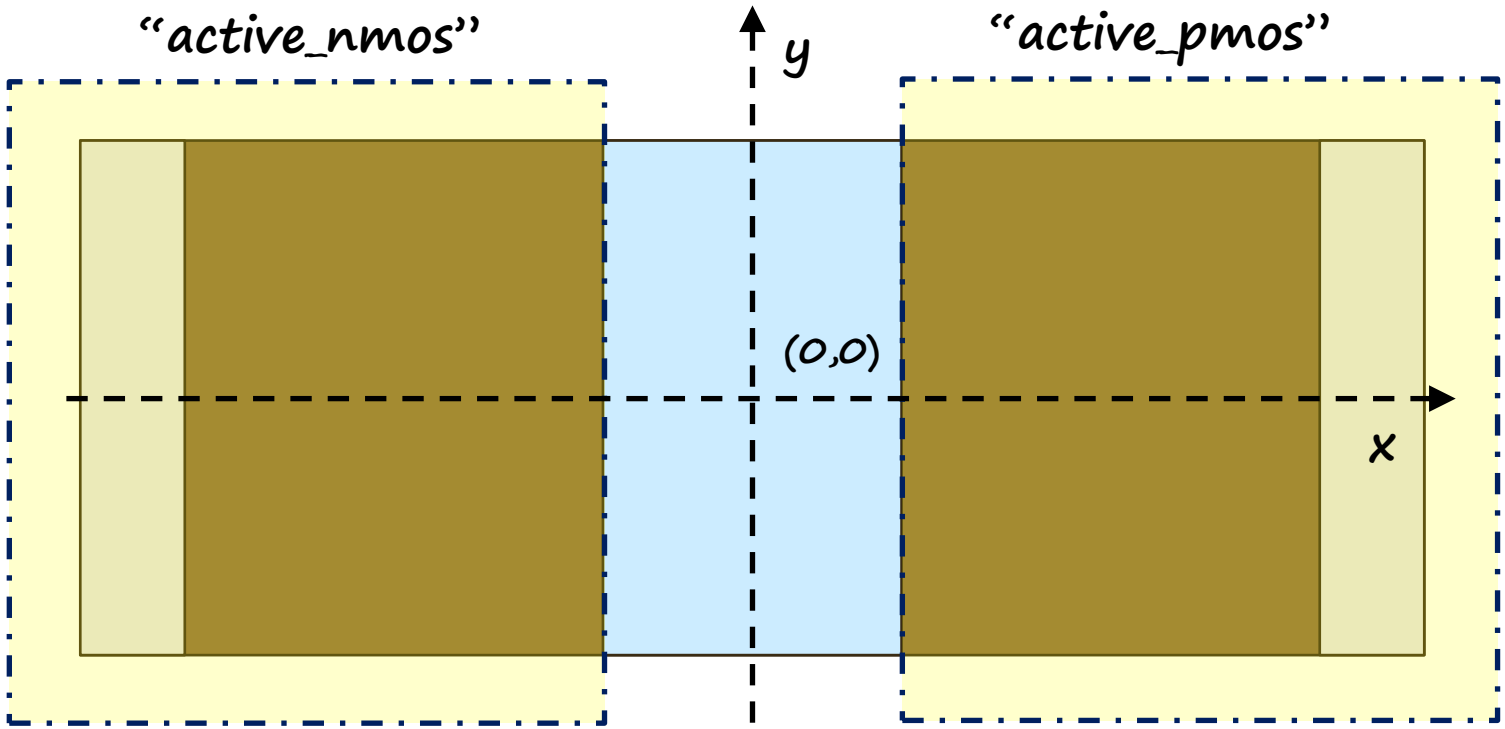
Unlike the case of a poly gate, the overlap does not depend on the poly sidewall oxide thickness.

Once an overlap target is set, the sidewall thickness of the dielectric stack determines the required extension side diffusion (and thus extension depth), or vice-versa.

Planar HKMG CMOS Flow: Layout



Planar HKMG CMOS Flow: Active Area Mask

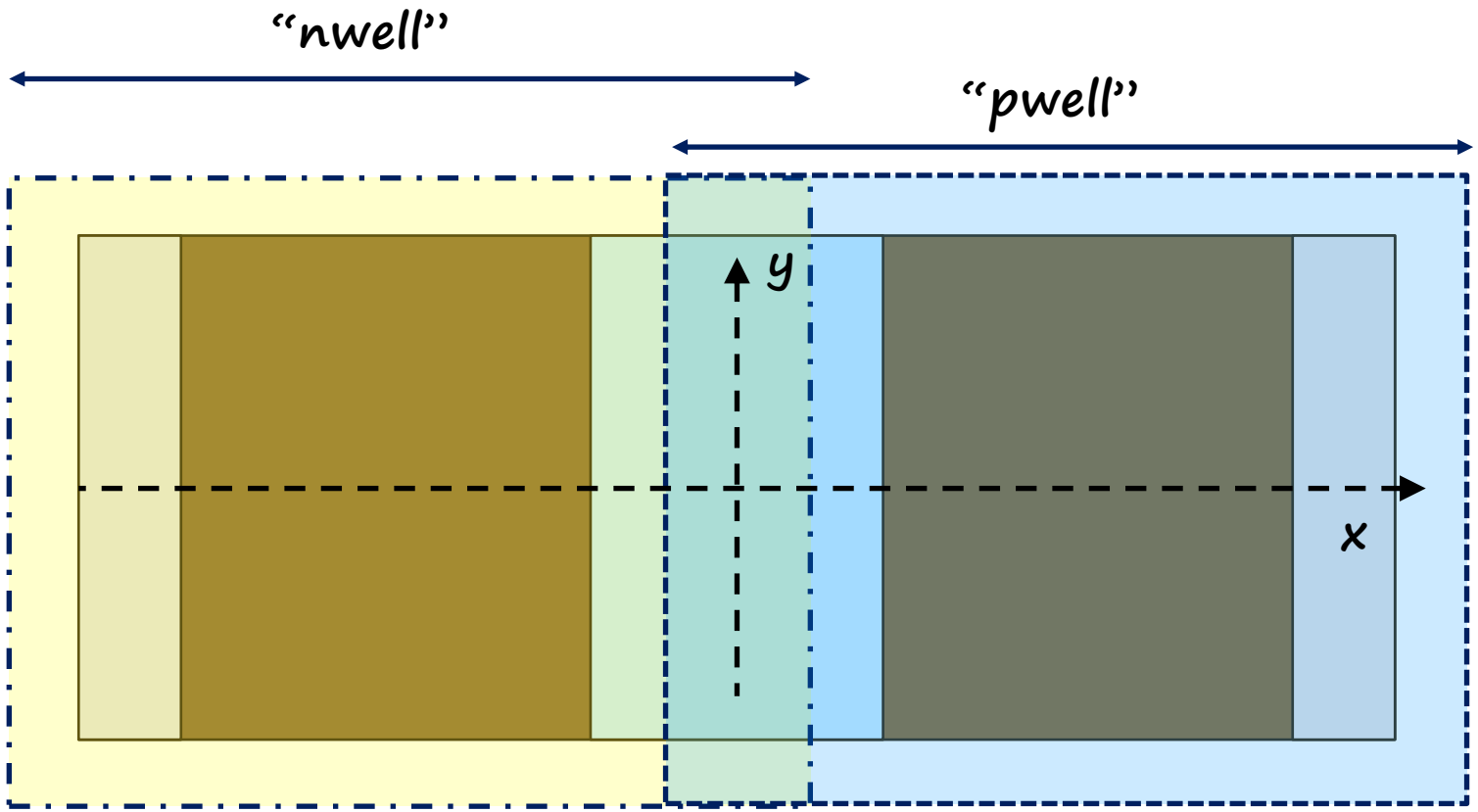


Note: 2D simulation in X-Z plane; y-dimension is arbitrarily set to +/- 0.1 (must enclose y=0)

Active Area mask, "active", is the Boolean "or" of two rectangles, "active_nmos" and "active_pmos"

(Resist will cover the areas to be protected from STI silicon etch.)

Planar HKMG CMOS Flow: Well Masks



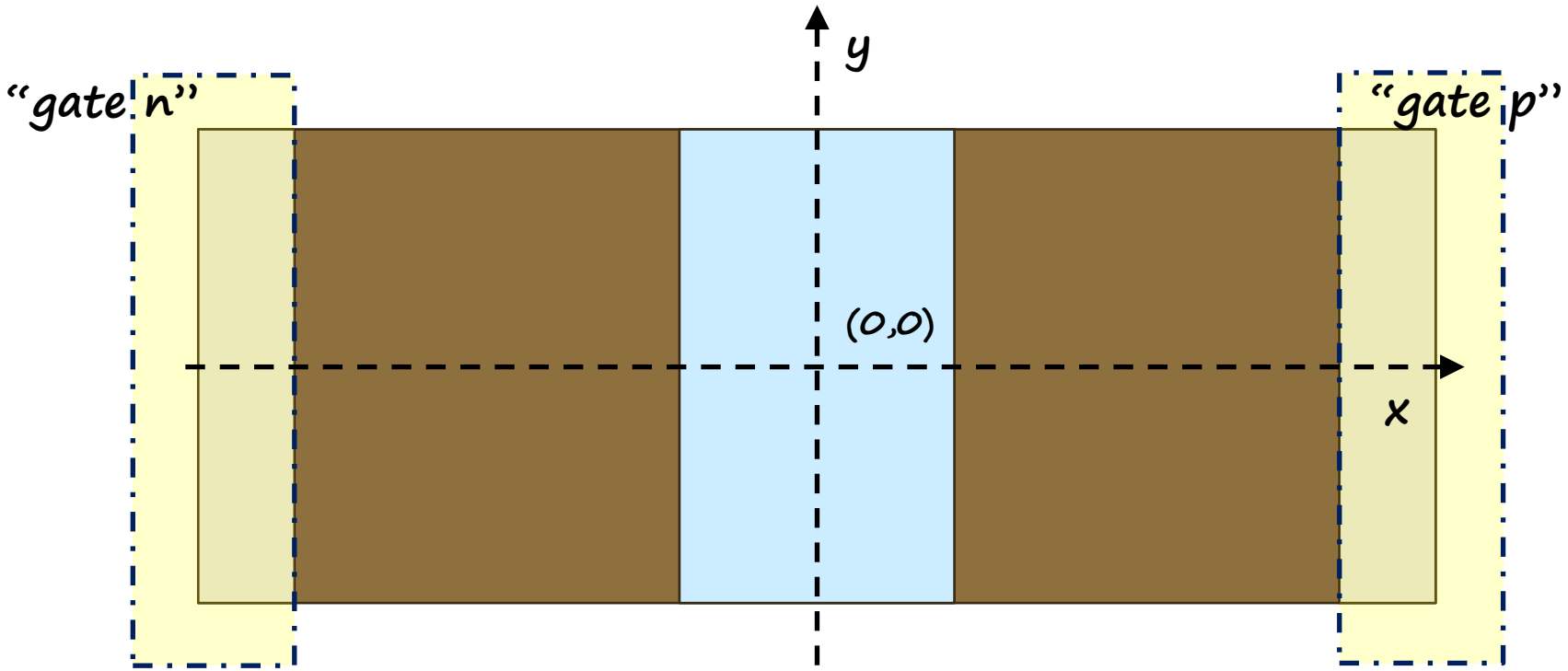
Masks can overlap in the center region to increase margin for lateral dopant diffusion.

Overlap is controlled by a parameter named "well_overlap" ; originally set to zero, but increasing to 10nm.

N-well implant (phosphorus) goes into the PMOS side; resist rectangle covers NMOS side (negative x)

P-well implant (boron) goes into the NMOS side; resist rectangle covers PMOS side (positive x)

Planar HKMG CMOS Flow: Gate Mask



Gate mask, "gate" is the boolean "or" of two rectangles, "gate_n" and "gate_p"

Planar HKMG CMOS Flow: Process Sequence with Load Points

oxide/nitride hardmask dep
hardmask nitride etch
  using active mask
oxide and silicon etch
  based on nitride hardmask

liner oxidation (800C 30m dry)
- first load point (stiliner)
conformal oxide deposition (150nm)
CMP into nitride
nitride strip
oxide wet etch and re-oxidation
- second load point (sti)

P well mask and implant
N well mask and implant
well diffusion
- third load point (well)
N vt mask and implant
P vt mask and implant
- fourth load point (vt)
oxide etch

sacrificial gate oxide deposition
poly gate deposition
poly CMP
nitride hardmask deposition
hardmask patterning with gate mask
poly etch
poly re-oxidation (deposited)
- fifth load point (polyreox)

mask, nhalo and ntip implants
mask, phalo and ptip implants
anneal
- sixth load point (flash)
spacer deposition and etch

mask, N source/drain
mask, P source/drain
anneal
- seventh load point (sd)

silicide (silicon etch and NiSi deposition)
oxide deposition and CMP
poly pull
sacrificial gate etch

high-k gate deposition
TiN/TaN deposition
TiN deposition
- eigth load point (highk)

masked TiN partial etch
aluminum deposition
metal gate CMP

Planar HKMG CMOS Flow: Simulation Output

tedungan@nanohub-2449665-123:~/planar/cmos_shallow

```
[tedungan@nanohub-2449665-123 cmos_shallow]$ ls
oxidationtime.log       pcmos_1_29.str          sv_pcmos_1_polyreox.lay
pcmos_1_01.str          pcmos_1_30.str          sv_pcmos_1_polyreox.ppc
pcmos_1_02.str          pcmos_1_31.str          sv_pcmos_1_polyreox.prp
pcmos_1_03.str          pcmos_1_32.str          sv_pcmos_1_polyreox.run
pcmos_1_04.str          pcmos_1_33.str          sv_pcmos_1_polyreox.svf
pcmos_1_05.str          pcmos_1_34.str          sv_pcmos_1_sd.dop
pcmos_1_06.str          pcmos_1_35.str          sv_pcmos_1_sd.lay
pcmos_1_07.str          pcmos_1_36.str          sv_pcmos_1_sd.ppc
pcmos_1_08.str          pcmos_1_37.str          sv_pcmos_1_sd.prp
pcmos_1_09.str          pcmos_1_38.str          sv_pcmos_1_sd.run
pcmos_1_10.str          pcmos_1_39.str          sv_pcmos_1_sd.svf
pcmos_1_11.str          pcmos_1_40.str          sv_pcmos_1_sti.dop
pcmos_1_12.str          pcmos_1_41.str          sv_pcmos_1_sti.lay
pcmos_1_13.str          pcmos_1_final.dop       sv_pcmos_1_stiliner.dop
pcmos_1_14.str          pcmos_1_final.lay       sv_pcmos_1_stiliner.lay
pcmos_1_15.str          pcmos_1_final.ppc       sv_pcmos_1_stiliner.ppc
pcmos_1_16.str          pcmos_1_final.prp       sv_pcmos_1_stiliner.prp
pcmos_1_17.str          pcmos_1_final.run       sv_pcmos_1_stiliner.run
pcmos_1_18.str          pcmos_1_final.svf       sv_pcmos_1_stiliner.svf
pcmos_1_19.str          pcmos_1_process.results sv_pcmos_1_sti.ppc
pcmos_1_1d_h_ch.str     planar_cmos_1.in        sv_pcmos_1_sti.prp
pcmos_1_1d_h_halo.str   runtimeinfo.txt         sv_pcmos_1_sti.run
pcmos_1_1d_v_ch_n.str   sv_pcmos_1_flash.dop    sv_pcmos_1_sti.svf
pcmos_1_1d_v_ch_p.str   sv_pcmos_1_flash.lay    sv_pcmos_1_vt.dop
pcmos_1_1d_v_ext_n.str  sv_pcmos_1_flash.ppc    sv_pcmos_1_vt.lay
pcmos_1_1d_v_ext_p.str  sv_pcmos_1_flash.prp    sv_pcmos_1_vt.ppc
pcmos_1_20.str          sv_pcmos_1_flash.run    sv_pcmos_1_vt.prp
pcmos_1_21.str          sv_pcmos_1_flash.svf    sv_pcmos_1_vt.run
pcmos_1_22.str          sv_pcmos_1_highk.dop    sv_pcmos_1_vt.svf
pcmos_1_23.str          sv_pcmos_1_highk.lay    sv_pcmos_1_well.dop
pcmos_1_24.str          sv_pcmos_1_highk.ppc    sv_pcmos_1_well.lay
pcmos_1_25.str          sv_pcmos_1_highk.prp    sv_pcmos_1_well.ppc
pcmos_1_26.str          sv_pcmos_1_highk.run    sv_pcmos_1_well.prp
pcmos_1_27.str          sv_pcmos_1_highk.svf    sv_pcmos_1_well.run
pcmos_1_28.str          sv_pcmos_1_polyreox.dop sv_pcmos_1_well.svf
```

output from running process portion of deck

green: sequential 2D structure files
purple: final 1D cutline files
brown: load point files
gold: final save for use by mesh and device

tedungan@nanohub-2449665-123:~/planar/cmos_shallow

```
[tedungan@nanohub-2449665-123 cmos_shallow]$ ls
oxidationtime.log       pcmos_1_37.str          sv_pcmos_1_highk.lay
pcmos_1_01.str          pcmos_1_38.str          sv_pcmos_1_highk.ppc
pcmos_1_02.str          pcmos_1_39.str          sv_pcmos_1_highk.prp
pcmos_1_03.str          pcmos_1_40.str          sv_pcmos_1_highk.run
pcmos_1_04.str          pcmos_1_41.str          sv_pcmos_1_highk.svf
pcmos_1_05.str          pcmos_1_final.dop       sv_pcmos_1_polyreox.dop
pcmos_1_06.str          pcmos_1_final.lay       sv_pcmos_1_polyreox.lay
pcmos_1_07.str          pcmos_1_final.ppc       sv_pcmos_1_polyreox.ppc
pcmos_1_08.str          pcmos_1_final.prp       sv_pcmos_1_polyreox.prp
pcmos_1_09.str          pcmos_1_final.run       sv_pcmos_1_polyreox.run
pcmos_1_10.str          pcmos_1_final.svf       sv_pcmos_1_polyreox.svf
pcmos_1_11.str          pcmos_1_n_lin.dat       sv_pcmos_1_sd.dop
pcmos_1_12.str          pcmos_1_n_lin.log       sv_pcmos_1_sd.lay
pcmos_1_13.str          pcmos_1_n_lin.results   sv_pcmos_1_sd.ppc
pcmos_1_14.str          pcmos_1_n_lin_vg0.str   sv_pcmos_1_sd.prp
pcmos_1_15.str          pcmos_1_n_lin_vgmax.str sv_pcmos_1_sd.run
pcmos_1_16.str          pcmos_1_n_meshed.str    sv_pcmos_1_sd.svf
pcmos_1_17.str          pcmos_1_n_sat.dat       sv_pcmos_1_sti.dop
pcmos_1_18.str          pcmos_1_n_sat.log       sv_pcmos_1_sti.lay
pcmos_1_19.str          pcmos_1_n_sat.results   sv_pcmos_1_stiliner.dop
pcmos_1_1d_h_ch.str     pcmos_1_n_sat_vg0.str   sv_pcmos_1_stiliner.lay
pcmos_1_1d_h_halo.str   pcmos_1_n_sat_vgmax.str sv_pcmos_1_stiliner.ppc
pcmos_1_1d_v_ch_n.str   pcmos_1_p_lin.dat       sv_pcmos_1_stiliner.prp
pcmos_1_1d_v_ch_p.str   pcmos_1_p_lin.log       sv_pcmos_1_stiliner.run
pcmos_1_1d_v_ext_n.str  pcmos_1_p_lin.results   sv_pcmos_1_stiliner.svf
pcmos_1_1d_v_ext_p.str  pcmos_1_p_lin_vg0.str   sv_pcmos_1_sti.ppc
pcmos_1_20.str          pcmos_1_p_lin_vgmax.str sv_pcmos_1_sti.prp
pcmos_1_21.str          pcmos_1_p_meshed.str    sv_pcmos_1_sti.run
pcmos_1_22.str          pcmos_1_process.results sv_pcmos_1_sti.svf
pcmos_1_23.str          pcmos_1_p_sat.dat       sv_pcmos_1_vt.dop
pcmos_1_24.str          pcmos_1_p_sat.log       sv_pcmos_1_vt.lay
pcmos_1_25.str          pcmos_1_p_sat.results   sv_pcmos_1_vt.ppc
pcmos_1_26.str          pcmos_1_p_sat_vg0.str   sv_pcmos_1_vt.prp
pcmos_1_27.str          pcmos_1_p_sat_vgmax.str sv_pcmos_1_vt.run
pcmos_1_28.str          planar_cmos_1.in        sv_pcmos_1_vt.svf
pcmos_1_29.str          runtimeinfo.txt         sv_pcmos_1_well.dop
pcmos_1_30.str          sv_pcmos_1_flash.dop    sv_pcmos_1_well.lay
pcmos_1_31.str          sv_pcmos_1_flash.lay    sv_pcmos_1_well.ppc
pcmos_1_32.str          sv_pcmos_1_flash.ppc    sv_pcmos_1_well.prp
pcmos_1_33.str          sv_pcmos_1_flash.prp    sv_pcmos_1_well.run
pcmos_1_34.str          sv_pcmos_1_flash.run    sv_pcmos_1_well.svf
pcmos_1_35.str          sv_pcmos_1_flash.svf
pcmos_1_36.str          sv_pcmos_1_highk.dop
[tedungan@nanohub-2449665-123 cmos_shallow]$
```

after device portion of deck

blue: output from IV characterization

red: input parameters and extracted dimensions

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