

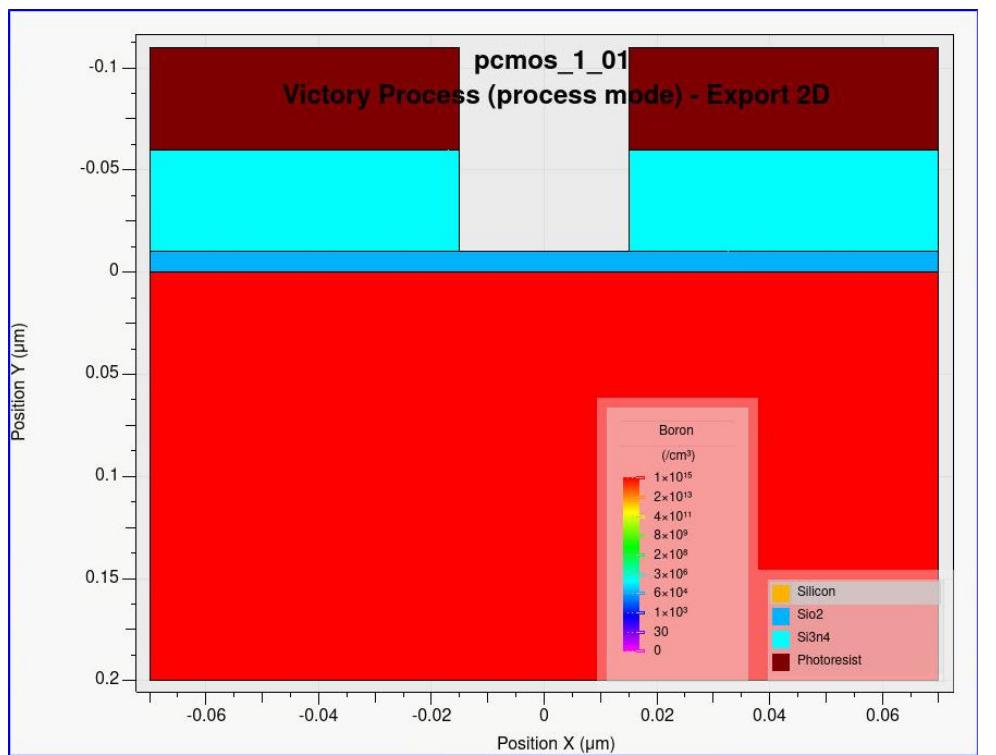
PLANAR HKMG CMOS

PART B: SEQUENTIAL CROSS-SECTIONS

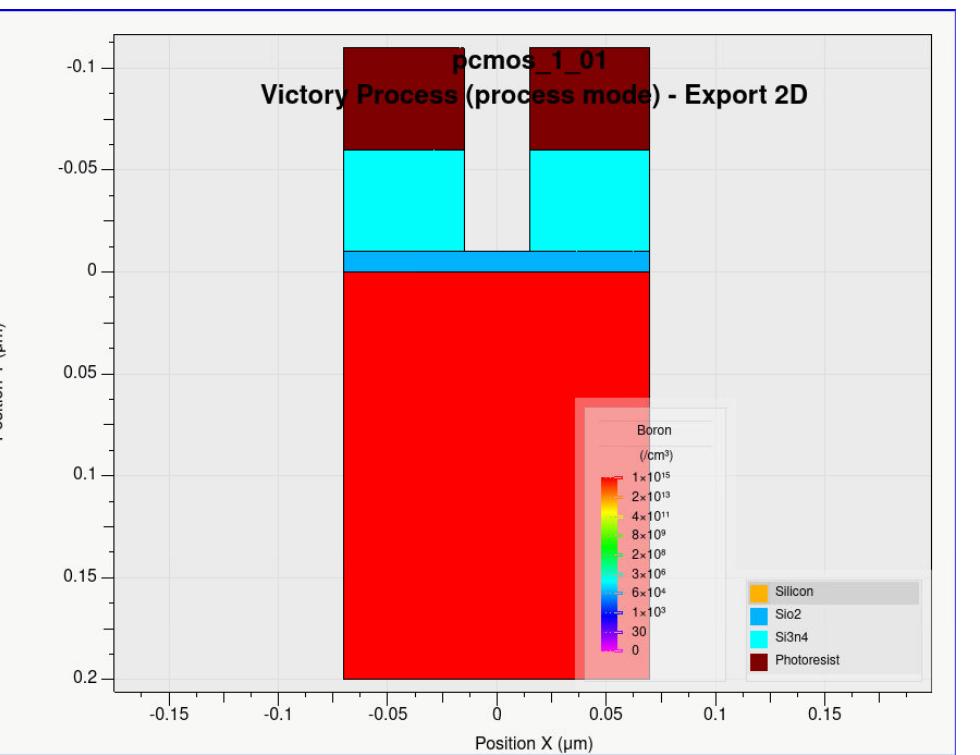
ECE 595 Semiconductor Device
Integration Through Simulation

Tom Dungan

Planar HCKMG CMOS Flow: STI Hardmask Etch



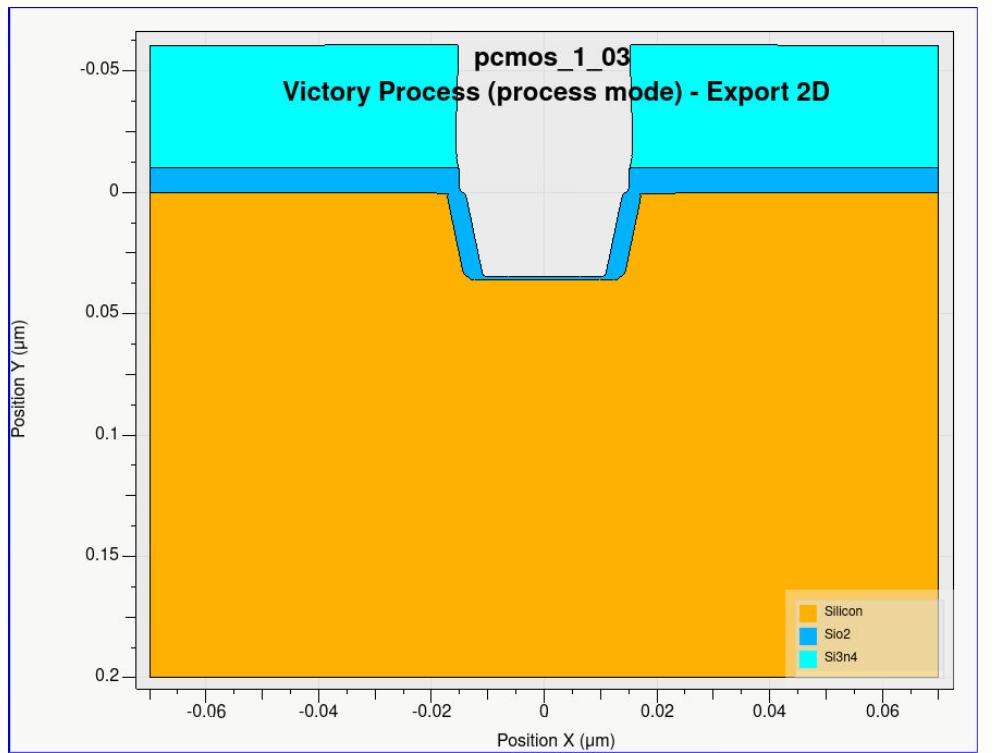
The red color of the silicon indicates a uniform background starting doping of $1\text{e}15/\text{cm}^3$ in the silicon epi layer (the substrate below would be much more heavily doped).



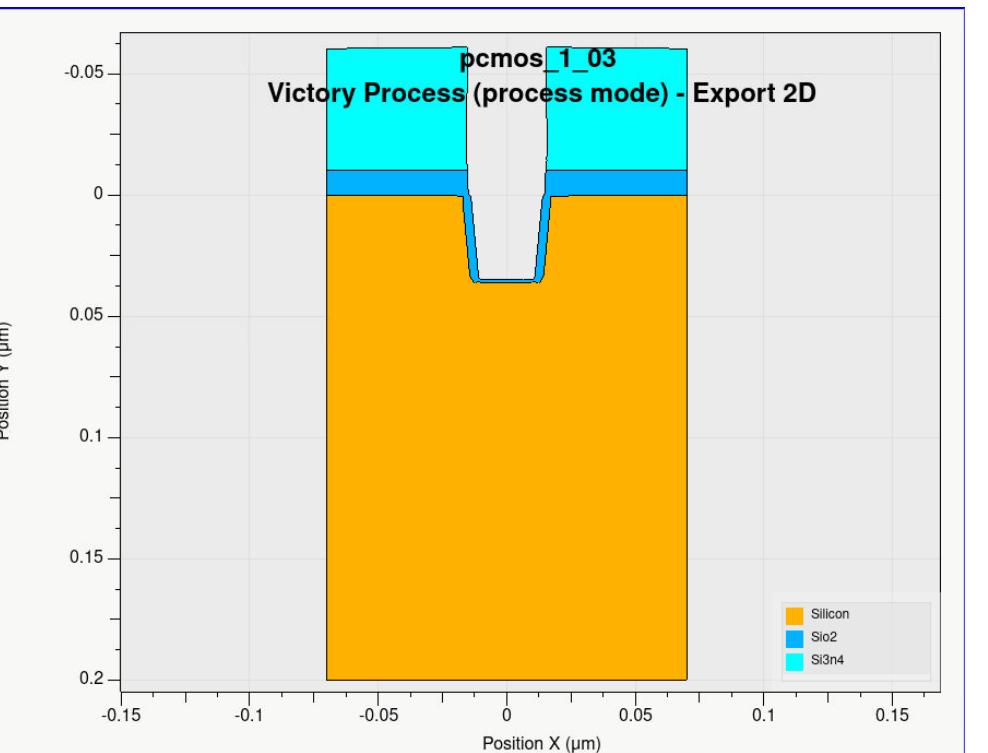
The same structure in an orthographic view to indicate the high aspect ratio of these devices.



Planar HKMG CMOS Flow: STI Liner Oxidation



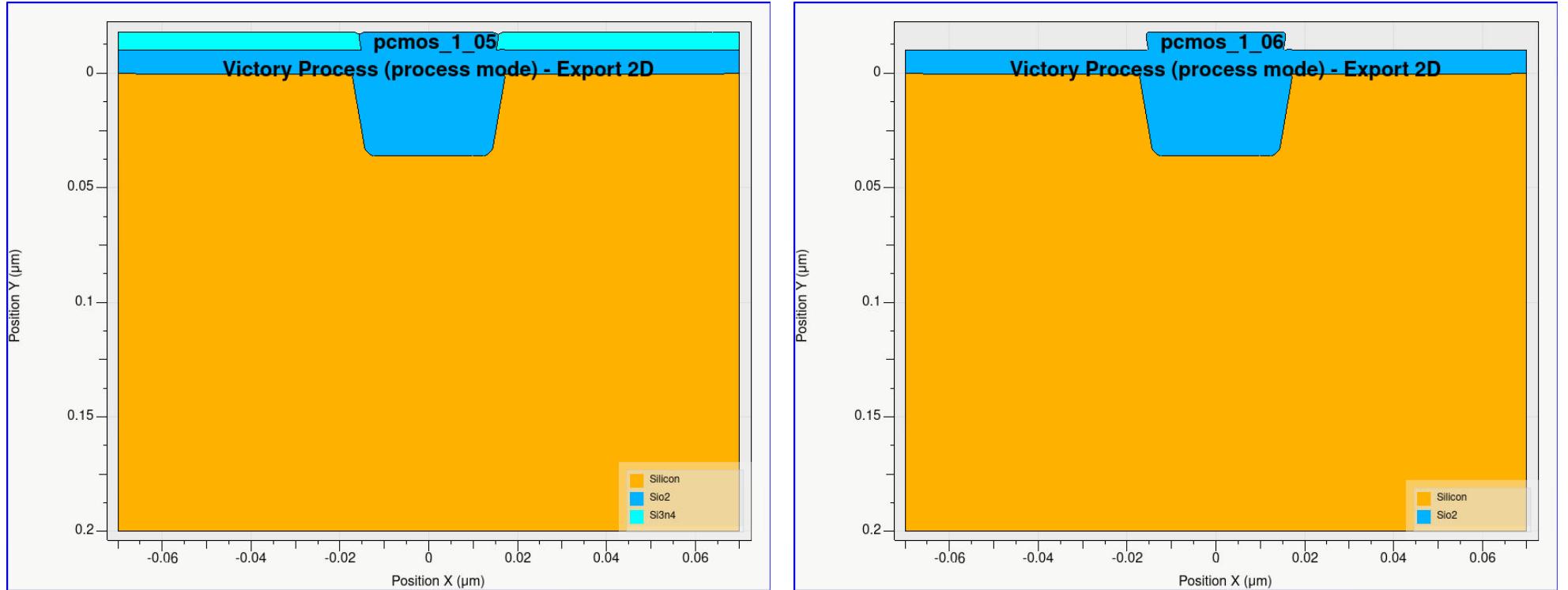
Trench structure after thermal liner oxide growth. Note the deformation of the hardmask and rounding of the trench corners.



Oxide is thicker on sloped trench sidewalls. Growth of thin oxide layers on non-planar structures is one of the more challenging tasks for accurate simulation.

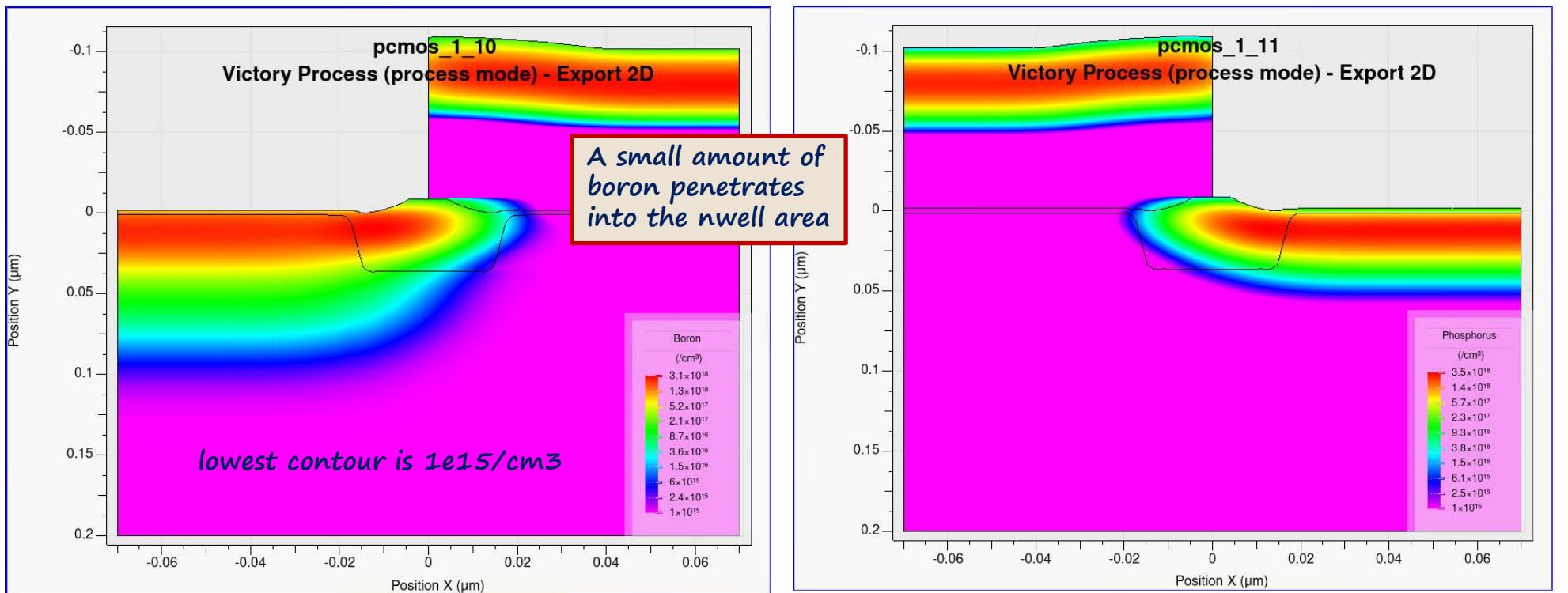


Planar HCKMG CMOS Flow: STI CMP and Hardmask Strip



The depth control of the CMP step determines the variability in the oxide protrusion remaining after nitride strip, which in turn affects final field planarity for poly transitions onto field areas.

Planar HKMG CMOS Flow: Well Implants



Pwell implant for nmos transistor:

boron 3KeV, $8e12/\text{cm}^2$, 7-degree tilt, 22-degree rotation
100nm resist (50nm might work)

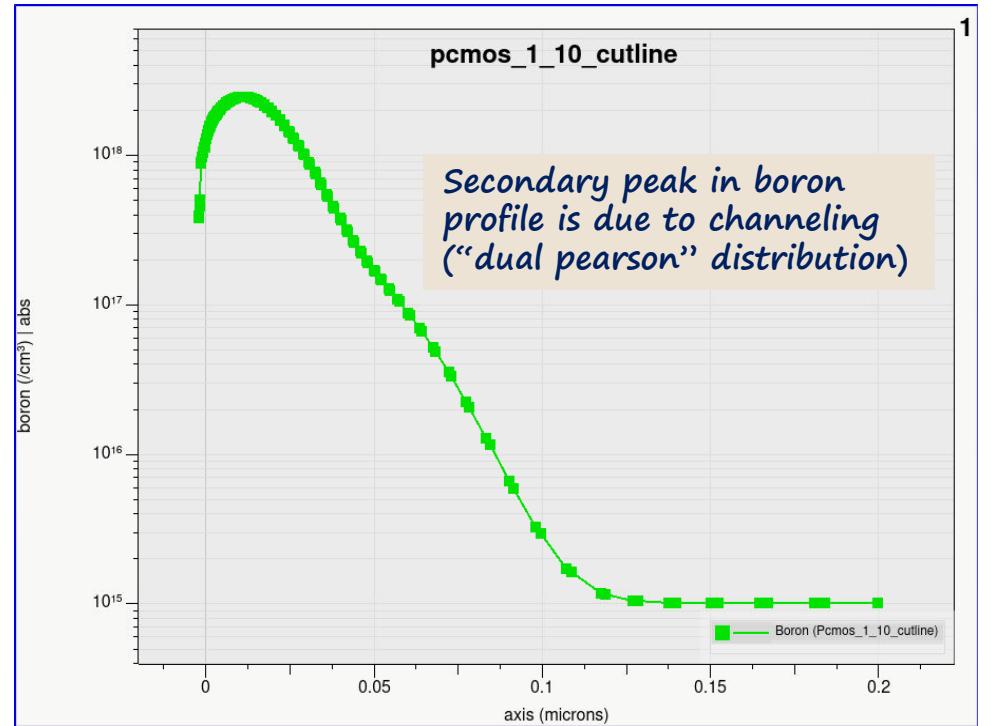
Nwell implant for pmos transistor:

phosphorus 10KeV, $6.3e12/\text{cm}^2$, 7-degree tilt, 22-degree rotation
100nm resist (50nm might work)

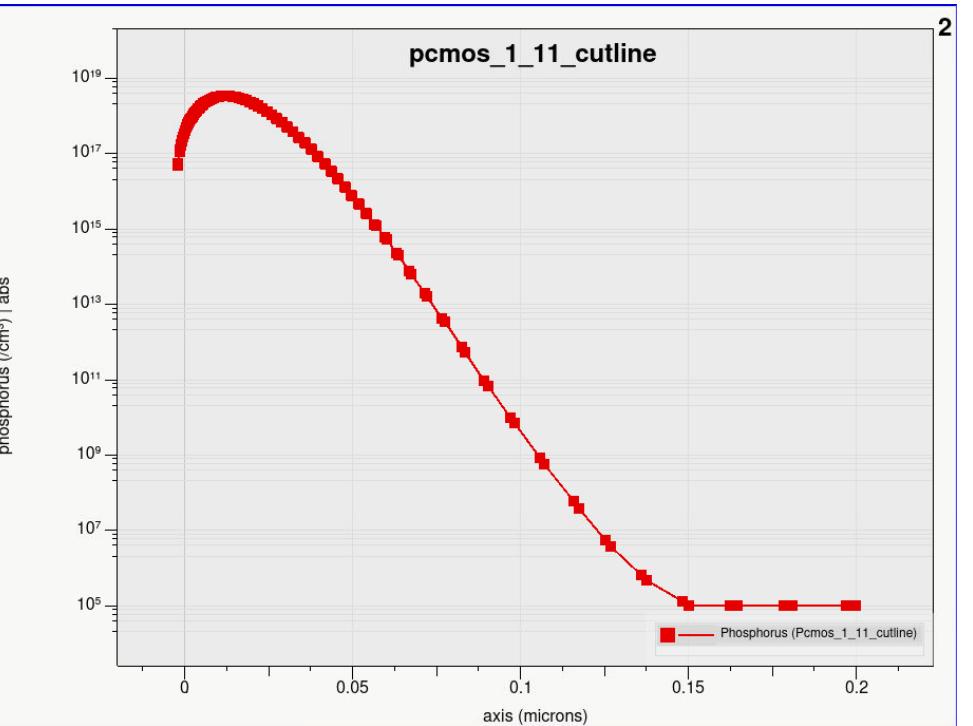
The masks are centered on the STI ("well_overlap" = 0) ... adding an overlap would provide some margin against implant spillover, but the choice of overlap must observe overlay registration tolerances



Planar HCKG CMOS Flow: Doping Profiles after Well Implants



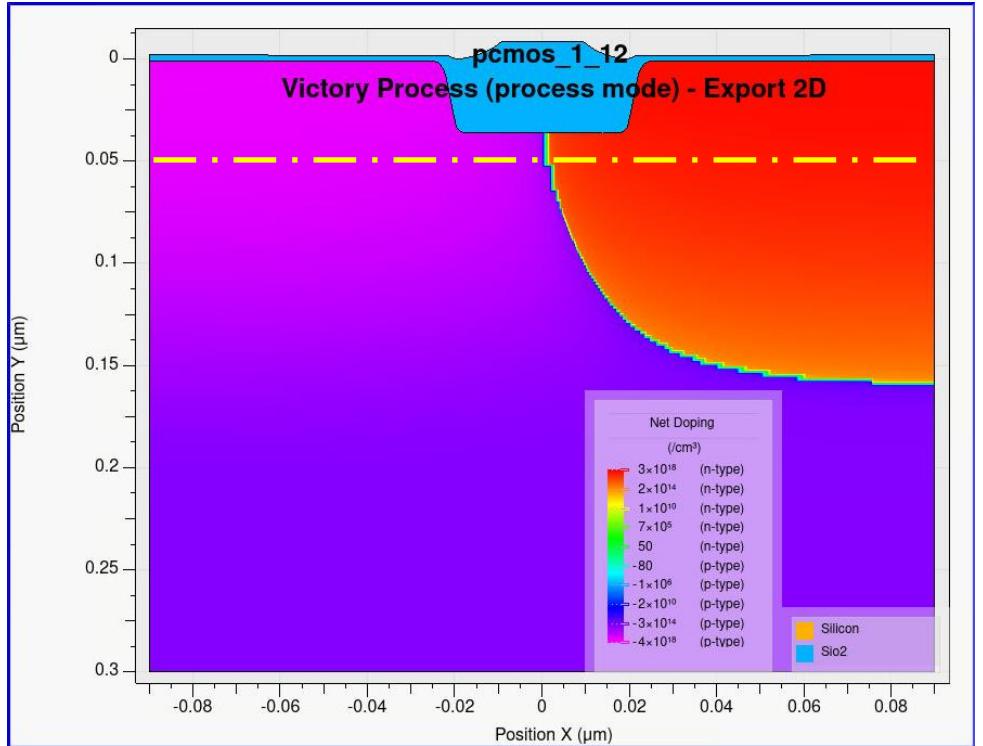
Boron profile in pwell ($x=-0.065\mu\text{m}$)
after as implanted prior to well drive



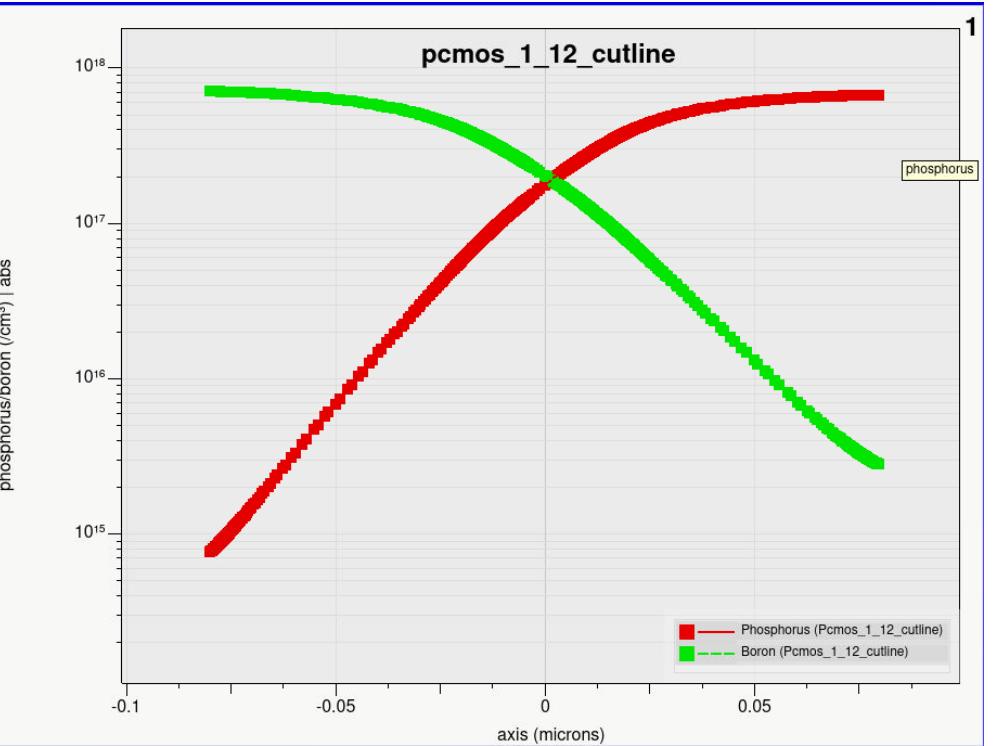
Phosphorus profile in nwell ($x=+0.065\mu\text{m}$)
as implanted prior to well drive



Planar HCKMG CMOS Flow: Net Doping after Well Drive



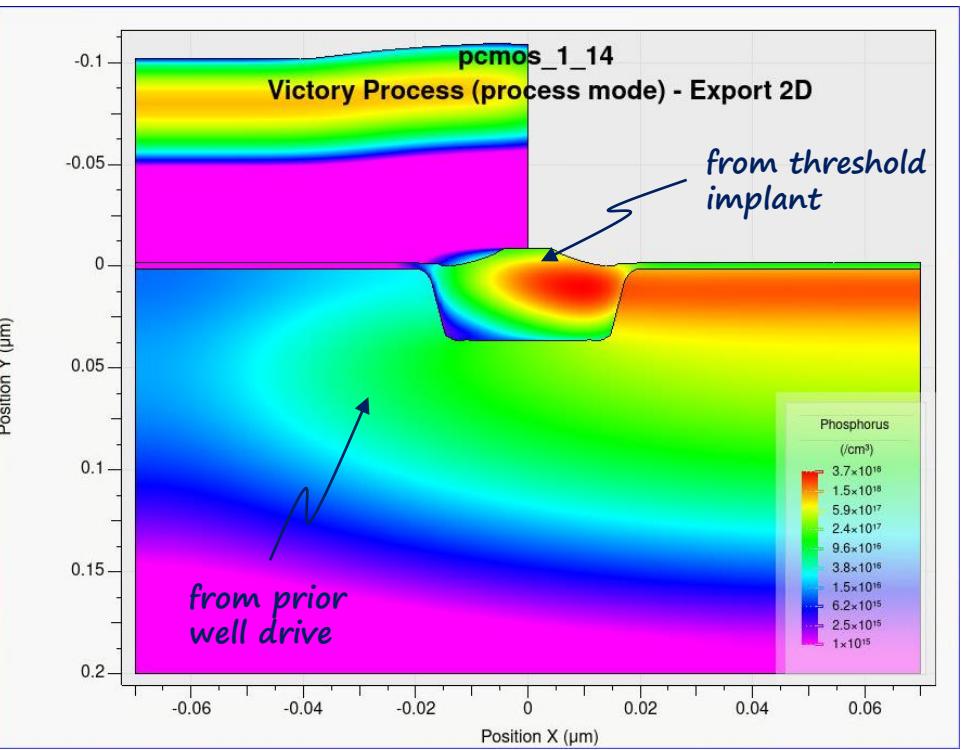
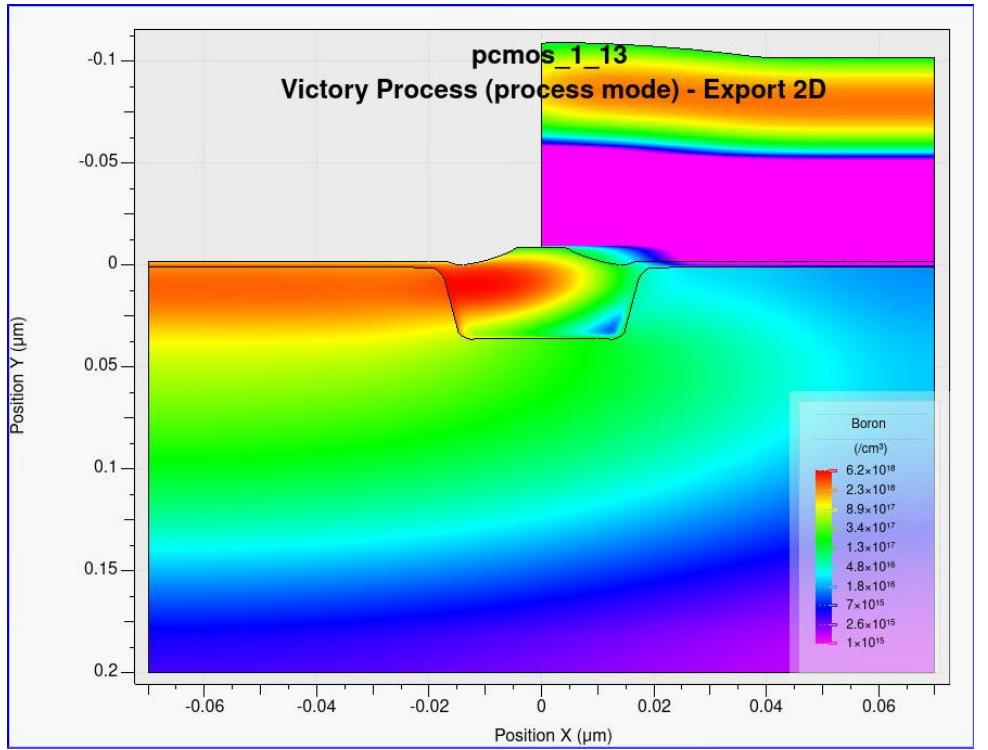
Net doping after well drive.



Horizontal Cut line at " y "=0.05 (really z), just below STI



Planar HCKMG CMOS Flow: Threshold-Adjust Implants

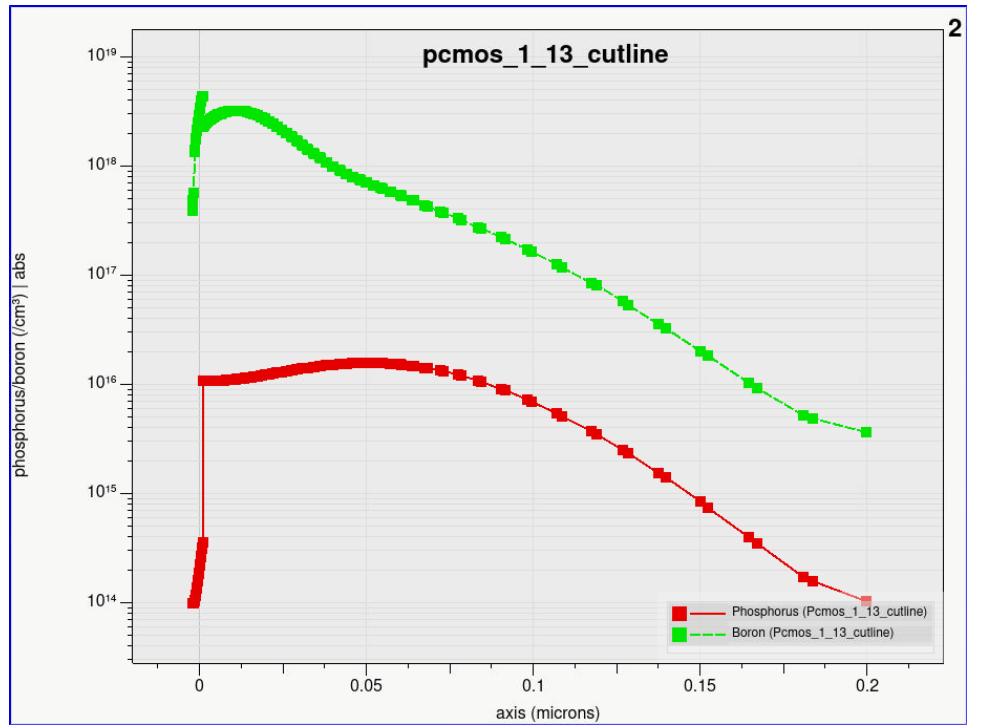


Threshold-adjust implant for nmos transistor:
boron 4KeV, $6.9 \times 10^{12}/\text{cm}^2$, 7-degree tilt, 22-degree rotation
100nm resist (50nm might work)

Threshold-adjust implant for pmos transistor:
phosphorus 10KeV, $2.5 \times 10^{12}/\text{cm}^2$, 7-degree tilt, 22-degree rotation
100nm resist (50nm might work)

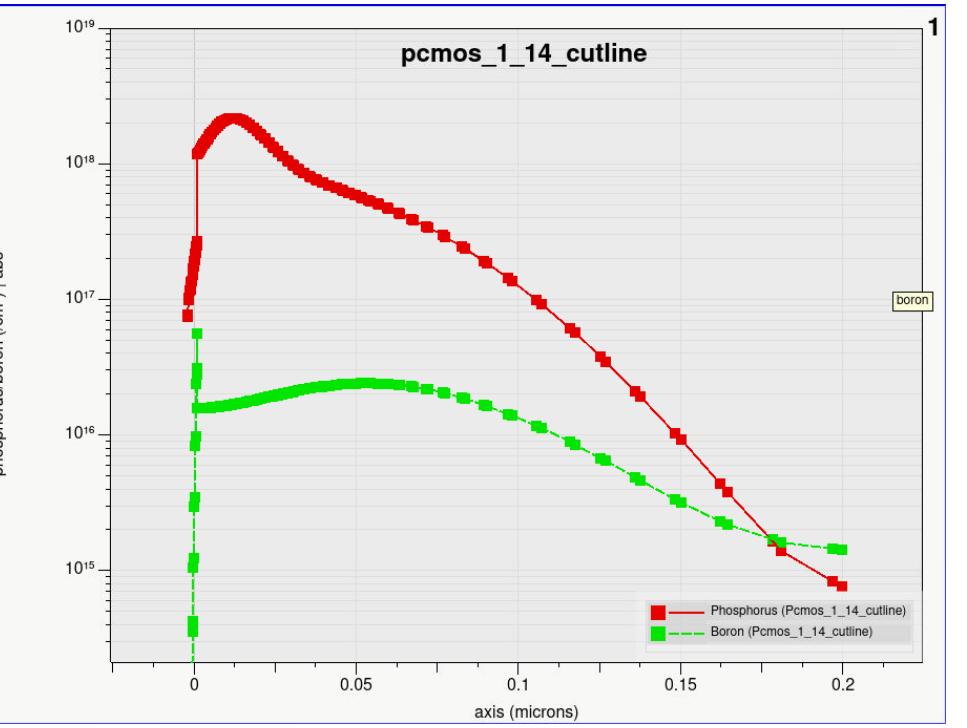
Note that it appears as if these implants have an exaggerated range, but that is because the profile includes the previously-driven well implants.

Planar HCKMG CMOS Flow: Threshold-Adjust Implants



Boron profile in nmos pwell ($x=-0.065\mu m$) after well drive and n-channel threshold implant (with phosphorus laterally diffused from pmos device).

Boron peak is about $3.19e18/\text{cm}^3$.

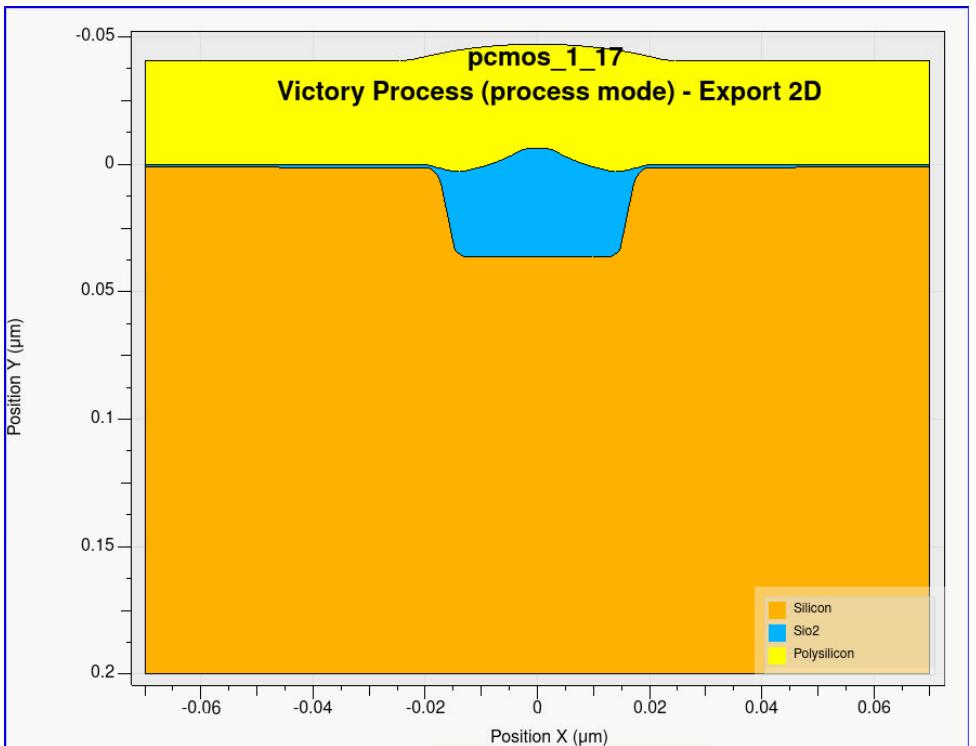


Phosphorus profile in pmos nwell ($x=+0.065\mu m$) after well drive and p-channel threshold implant (with boron laterally diffused from nmos device).

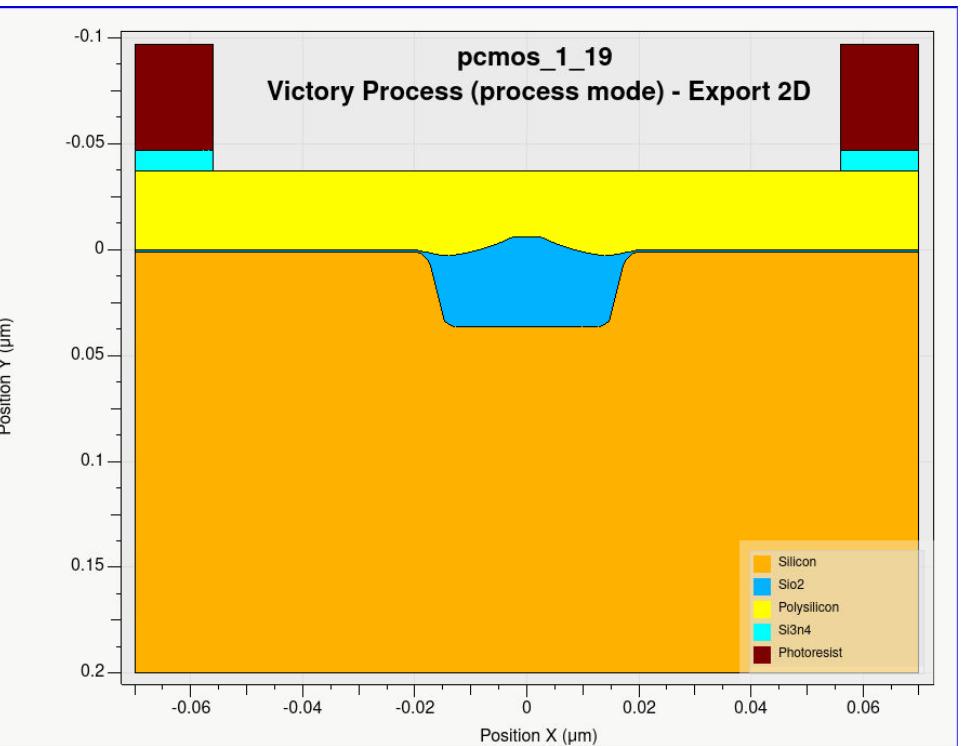
Phosphorus peak is about $2.14e18/\text{cm}^3$.



Planar HCKMG CMOS Flow: Gate Deposition, Polish, and Hardmask



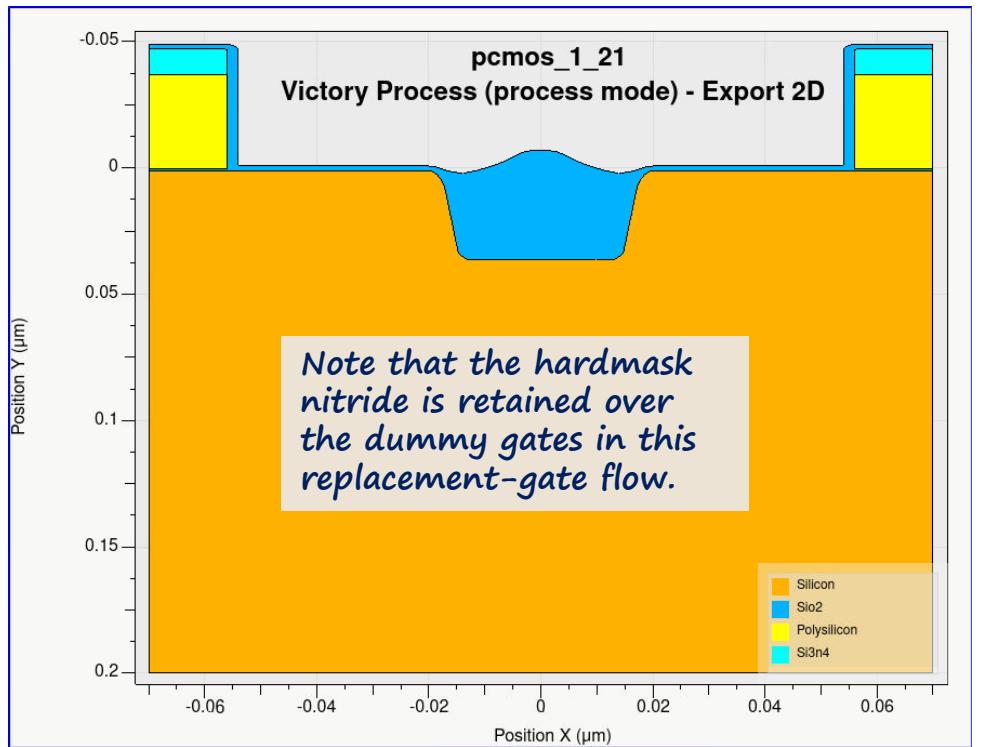
After oxide strip and redeposition of a 1nm dummy gate oxide, polysilicon is deposited to form the dummy gates.



The polysilicon is flattened by CMP, and nitride is deposited, masked and etched to serve as a hardmask for gate etch (note that this might be done with an SADP or SAQP process).



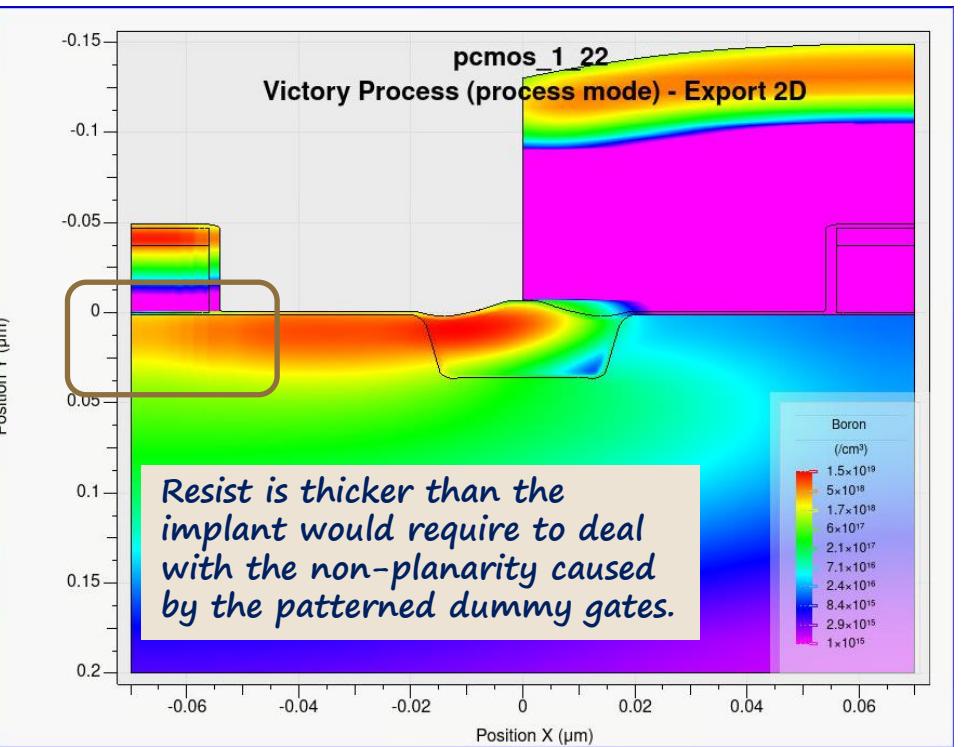
Planar HCKMG CMOS Flow: Poly "Reox" and N-Channel Halo



A 2nm oxide layer is deposited over the gates.

The extension (or tip) implants will be performed through this oxide.

The oxide also acts as a mini spacer between the extension implants and the edge of the poly – but in the replacement gate process, this layer will later be replaced with the ALD gate dielectric, so the spacer effect on underlap of the final metal gate edge gets cancelled out.



Shown after nmos halo implant, 1.4×10^{13} boron at 3KeV and 25-degree tilt, but simulated as 10-degree tilt because the analytical implant model cannot handle 25-degree tilt (see later short-loop slide).

4 rotations at 0, 90, 180, 270-degrees to channel.

The contours are shown with $1 \times 10^{15}/\text{cm}^3$ minimum as in the prior implant slides, but it is difficult to distinguish the effect of the halo implant with this scale.



Planar HCKMG CMOS Flow: Halo "Short Loops"

To understand the behavior of a specific aspect of the process flow, it is often useful to define a “short loop” that creates a simpler structure that can be evaluated more quickly.

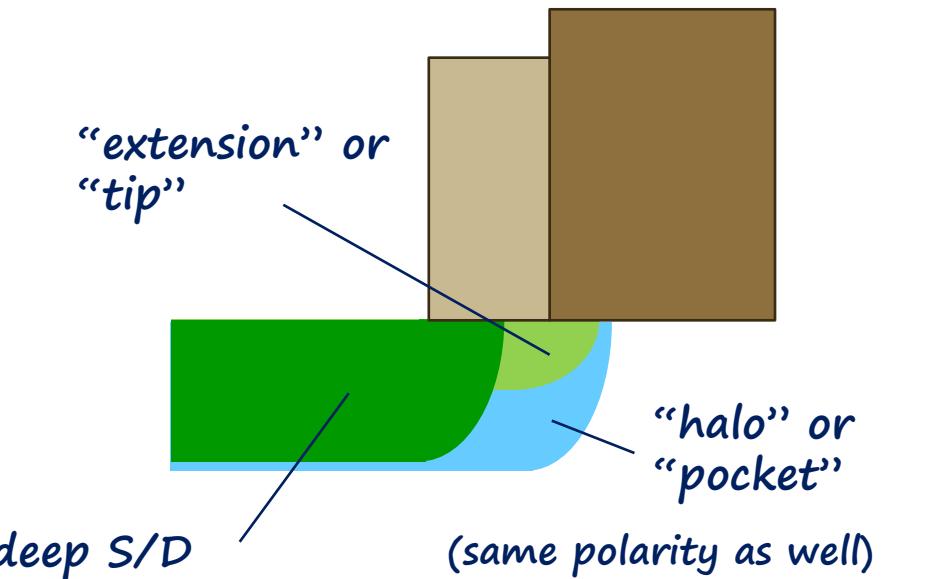
Such “Short Loop” flows are useful in physical process development and in simulation.

An example where a short loop is important to our simulation is in the selection of the halo (or “pocket”) implant parameters.

The halo implants are complex, because they add implant angle as a parameter.

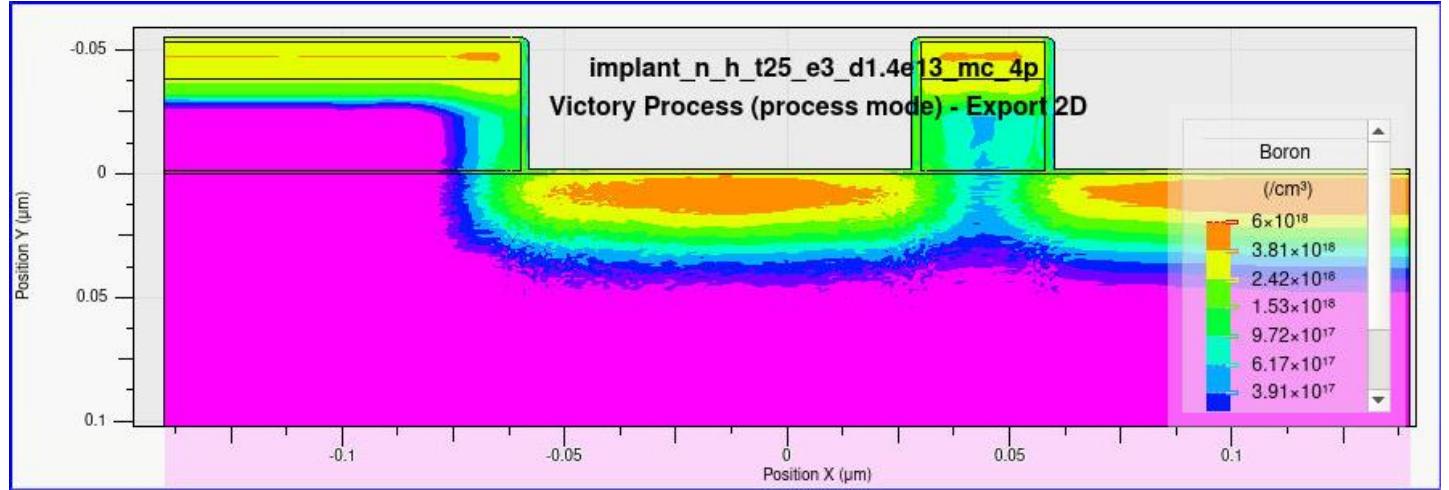
Higher-angle implants are typically used with halos to controllably push the edge of the halo just out beyond the edge of the s/d extension, with much lower dose.

The halo is designed to contain the field from the drain, without unduly increasing the threshold or the s/d capacitance.



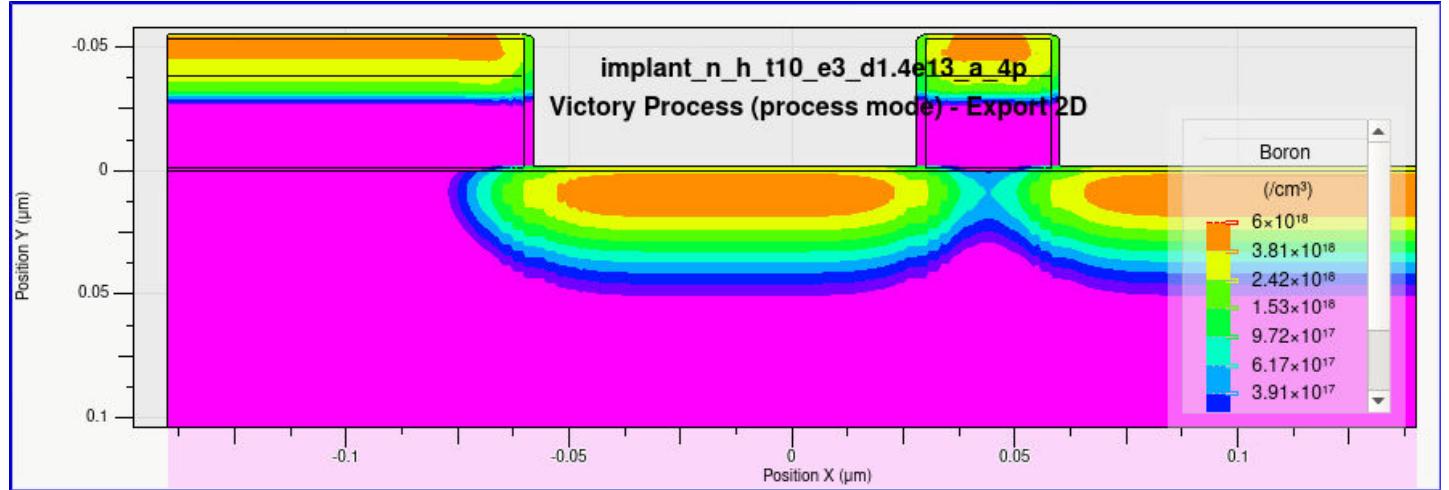
Planar HCKMG CMOS Flow: N-Channel Halo Short Loop

To understand the behavior of a specific aspect of the process flow, it is often useful to define a “short loop” that creates a simpler structure that can be evaluated more quickly.



Results from nmos boron halo short loop comparing monte carlo with analytic approximation.

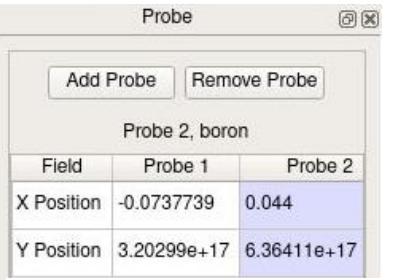
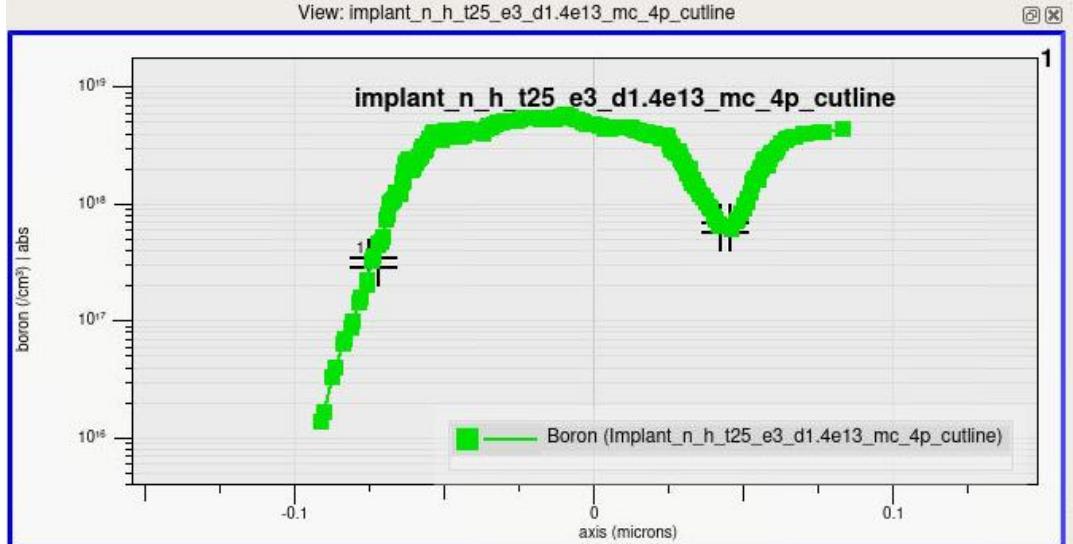
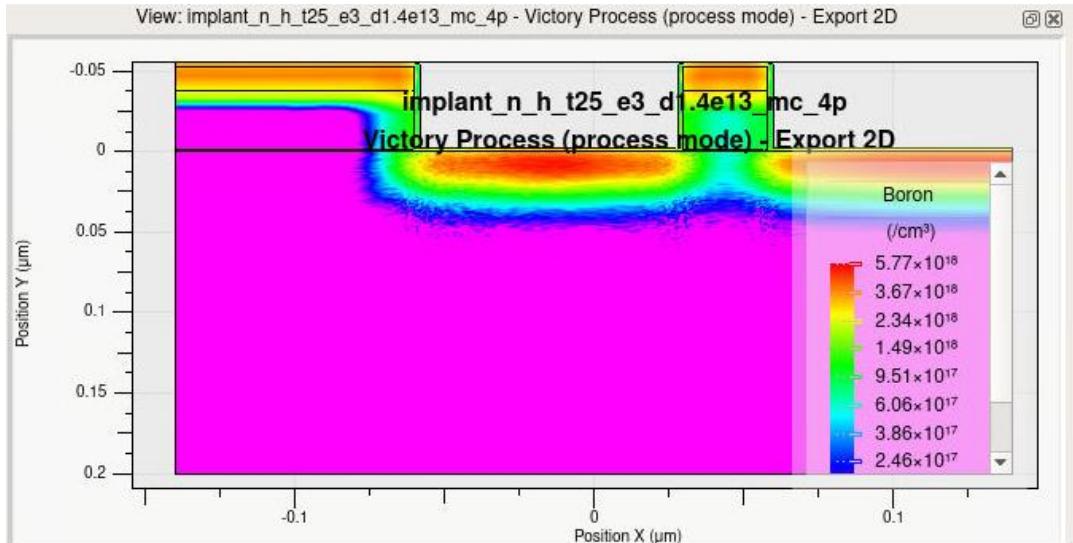
Implant is 1.4×10^{13} a 3KeV with 25-degree tilt and 22-degree rotation, in 4 passes.



Analytic approximation must use 10-degree tilt, because 25-degree does not work (produces vanishingly shallow result).



Planar HCKMG CMOS Flow: N-Channel Halo and Reverse Short Channel Effect



The cutline shows the doping profile at the depth of the peak of the profile, with a long channel compared to a short channel.

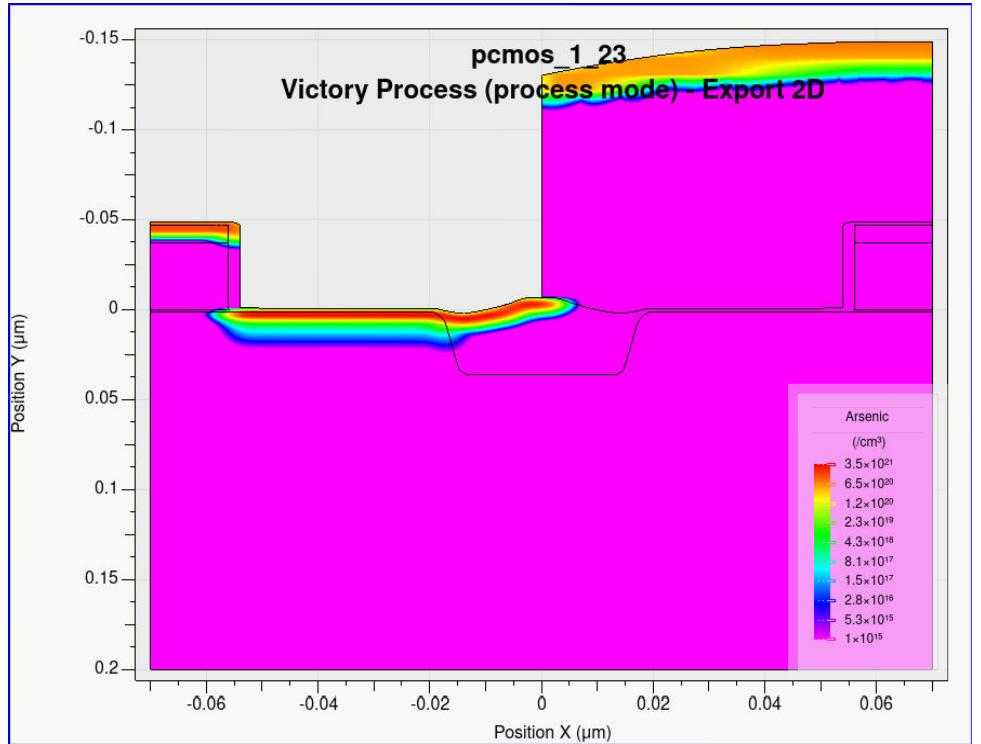
The probe results show that the doping from the halo is nearly twice as high in the center of the short channel, compared to the same distance into the long channel.

This merging of halos in short channels is the cause of the reverse short channel effect, where threshold rises for short channels.

The merged peak ($\sim 6.4 \times 10^{17}$) needs to be small compared to the peak (annealed) threshold adjust doping ($\sim 3.2 \times 10^{18}$ from profile on previous slide).

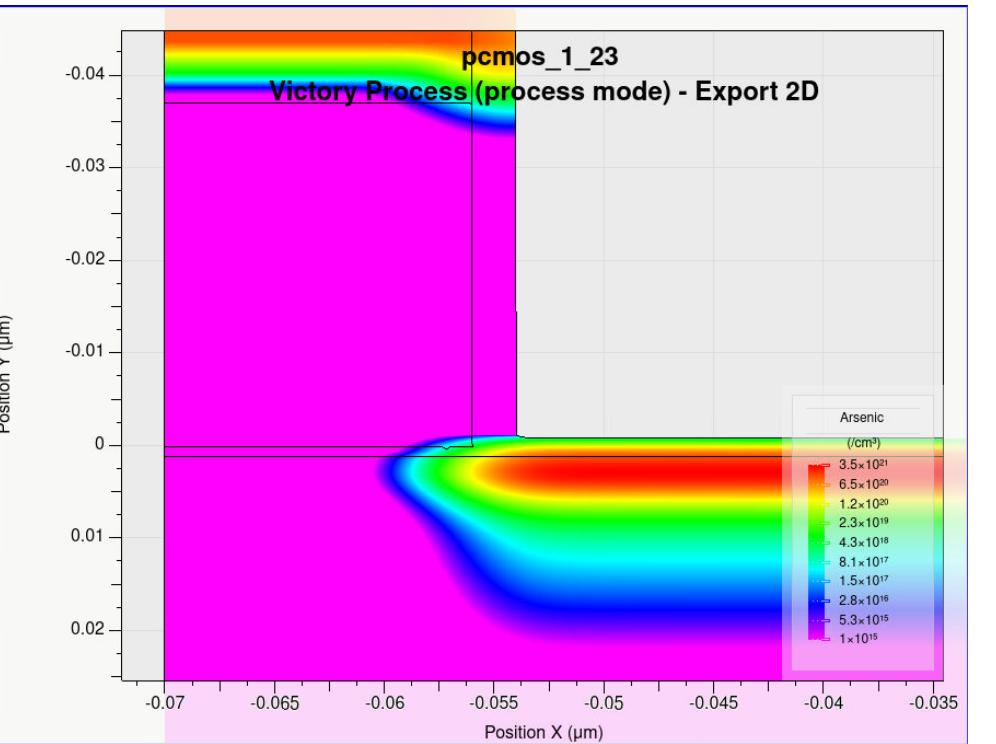


Planar HCKMG CMOS Flow: N-Channel Extension Implant



After arsenic extension implant into n-channel device.
1.2KeV, $1\text{e}15/\text{cm}^2$, 7-degree tilt, 22-degree rotation,
4 passes

Again, resist is thicker than the implant would require
to deal with the non-planarity caused by the patterned
dummy gates.

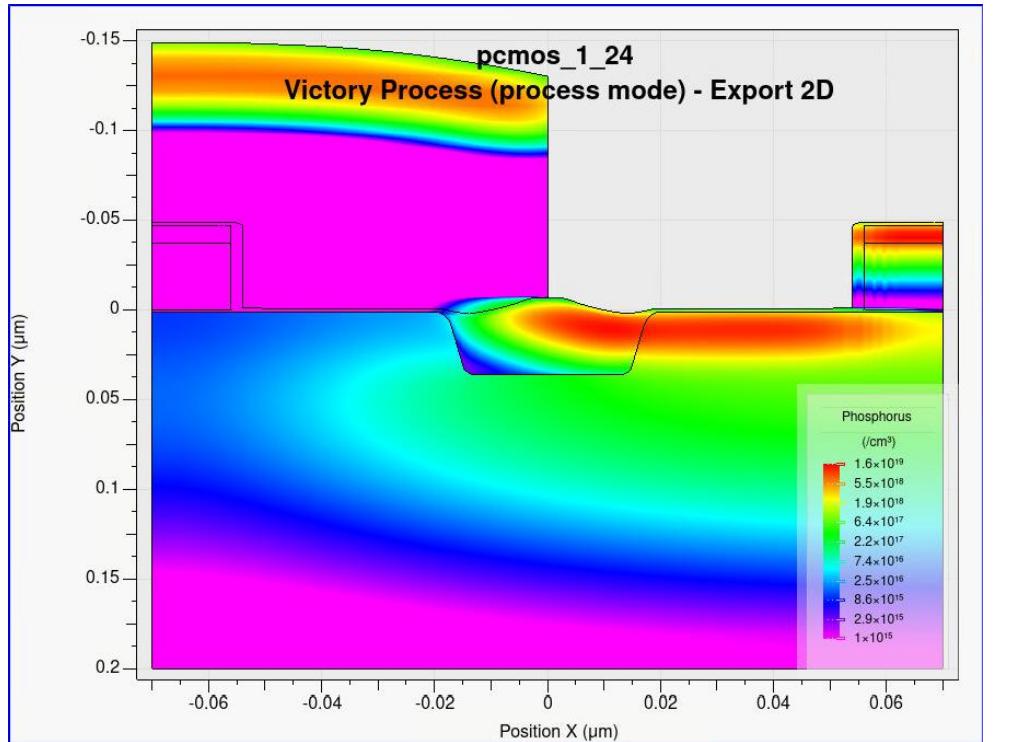


Closer view of tip region, verifying that the bulk of the implant is within the silicon.

Screen oxide is 2nm thick both on silicon surface and
on poly sidewall (vertical and horizontal dimensions not
to scale).



Planar HCKMG CMOS Flow: P-Channel Halo



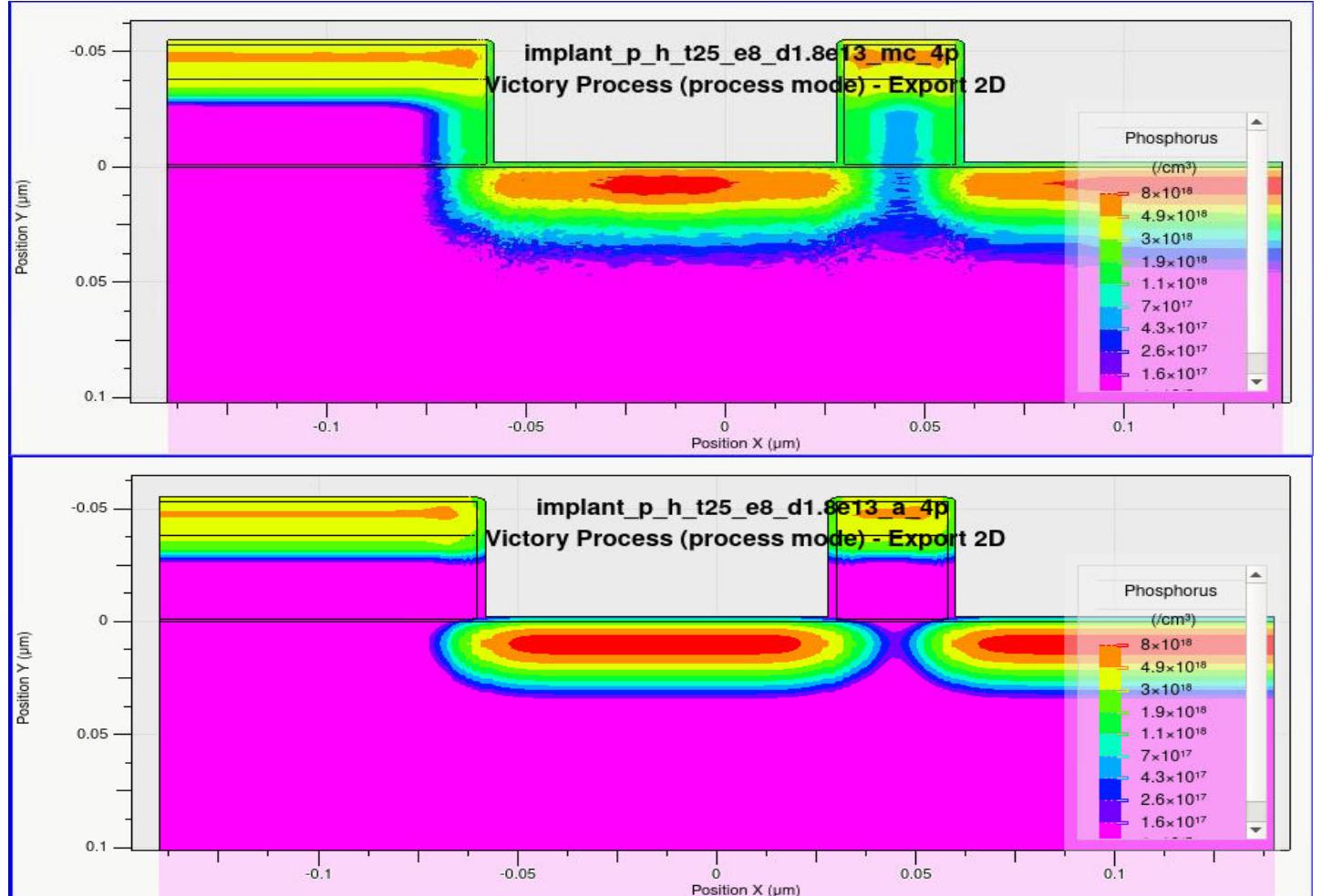
After phosphorus p-channel halo implant.

8KeV, $1.8 \times 10^{13}/\text{cm}^2$, 25-degree tilt;
0, 90, 180, 270-degrees rotation

Note that there is not much margin in the poly/nitride gate stack to block this implant.

Planar HCKMG CMOS Flow: P-Channel Halo Short Loop

Phosphorus halo short loop for the P-channel device:

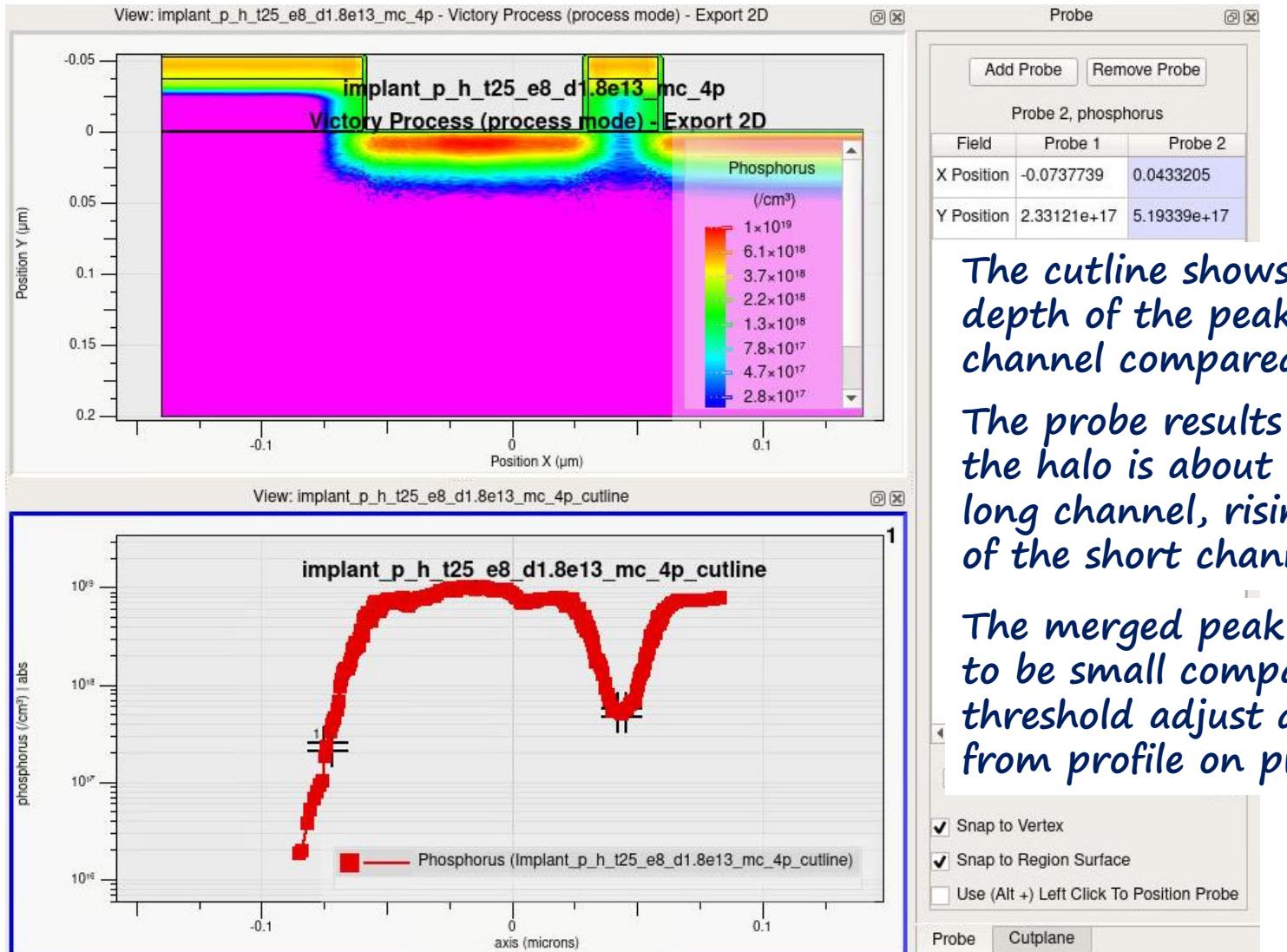


Results from pmos boron halo short loop comparing monte carlo with analytic approximation.

Implant is 1.8×10^{13} at 8KeV with 25-degree tilt and 22-degree rotation, in 4 passes.

For phosphorus, the 25-degree tilt analytic approximation produces a profile.

Planar HCKG CMOS Flow: PMOS Halo Implant and Reverse Short Channel Effect

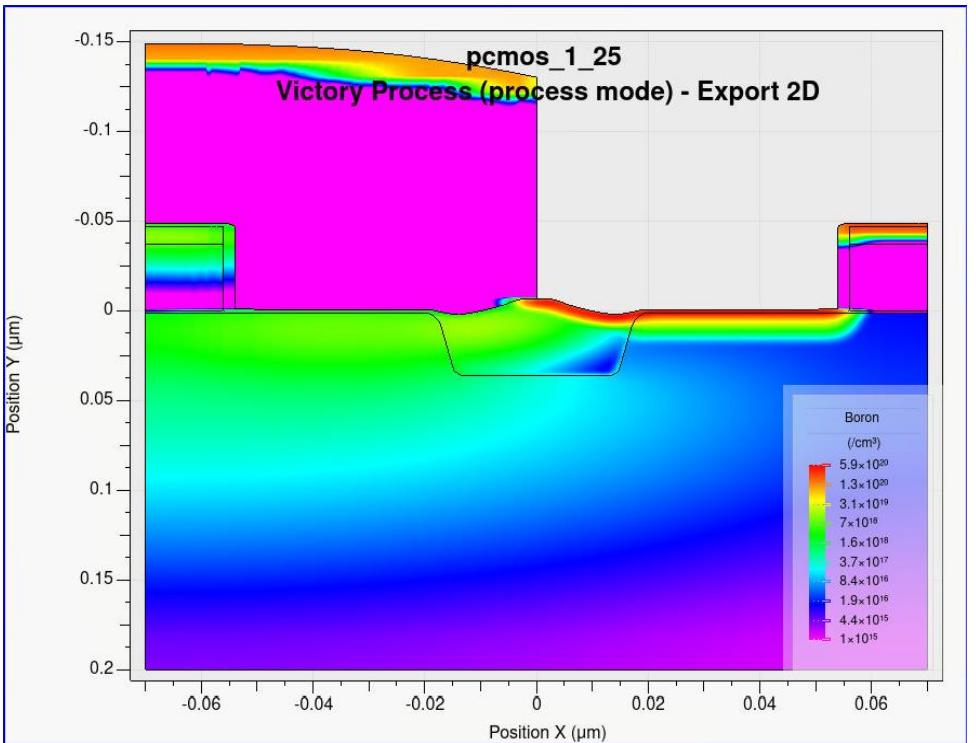


The cutline shows the doping profile at the depth of the peak of the profile, with a long channel compared to a short channel.

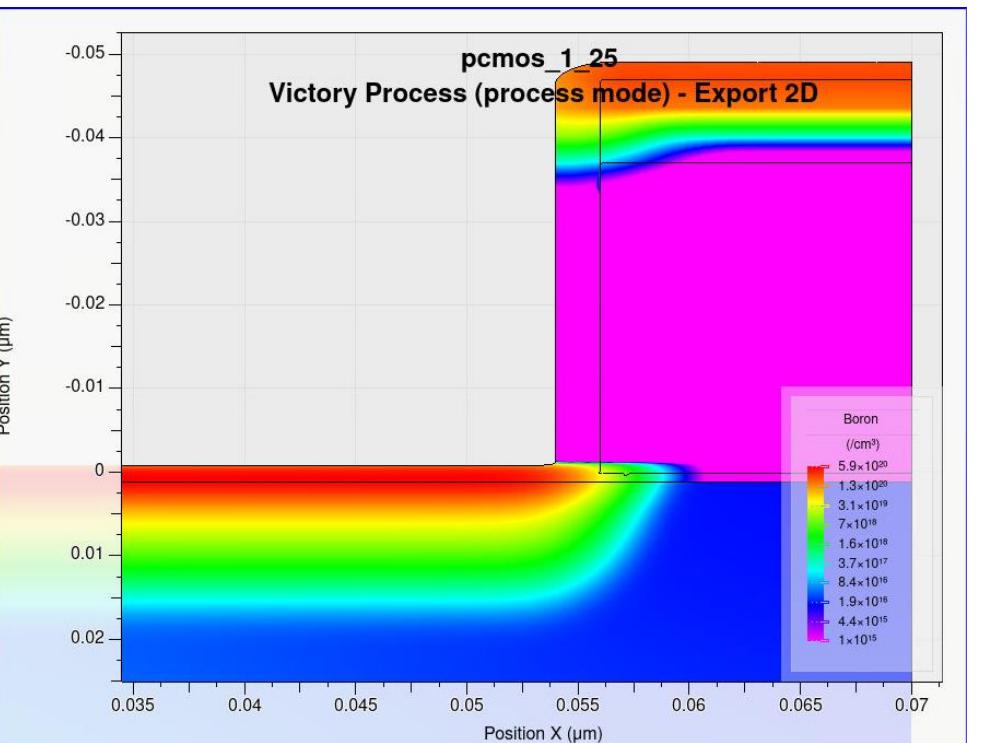
The probe results show that the doping from the halo is about 2.3×10^{17} at 0.14nm into the long channel, rising to 5.2×10^{17} in the center of the short channel.

The merged peak ($\sim 5.2 \times 10^{17}$) needs to be small compared to the peak threshold adjust doping ($\sim 2.1 \times 10^{18}$ from profile on previous slide).

Planar HCKMG CMOS Flow: P-Channel Extension Implant



After BF_2 extension implant into p-channel device.
1.4KeV, $2e14/\text{cm}^2$, 7-degree tilt, 22-degree rotation,
4 passes



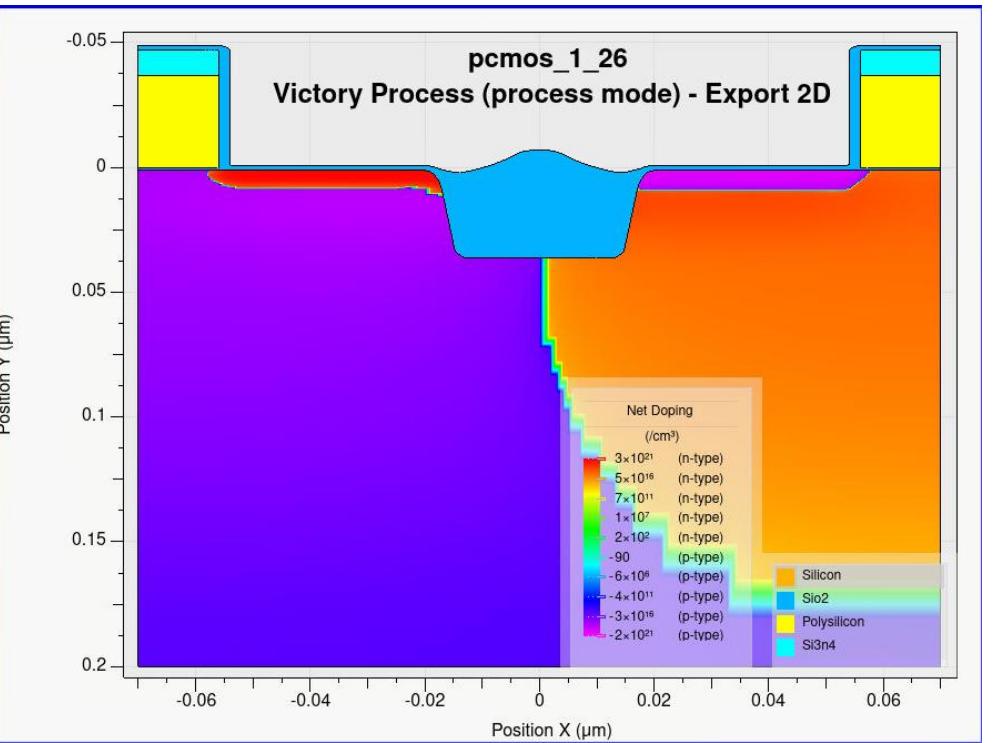
Closer view of tip region, showing that barely half of the implant makes it into the silicon.

Screen oxide is 2nm thick both on silicon surface and on poly sidewall (vertical and horizontal dimensions not to scale).

Thickness control of the screen oxide would be critical to the effective length of the p-channel devices.

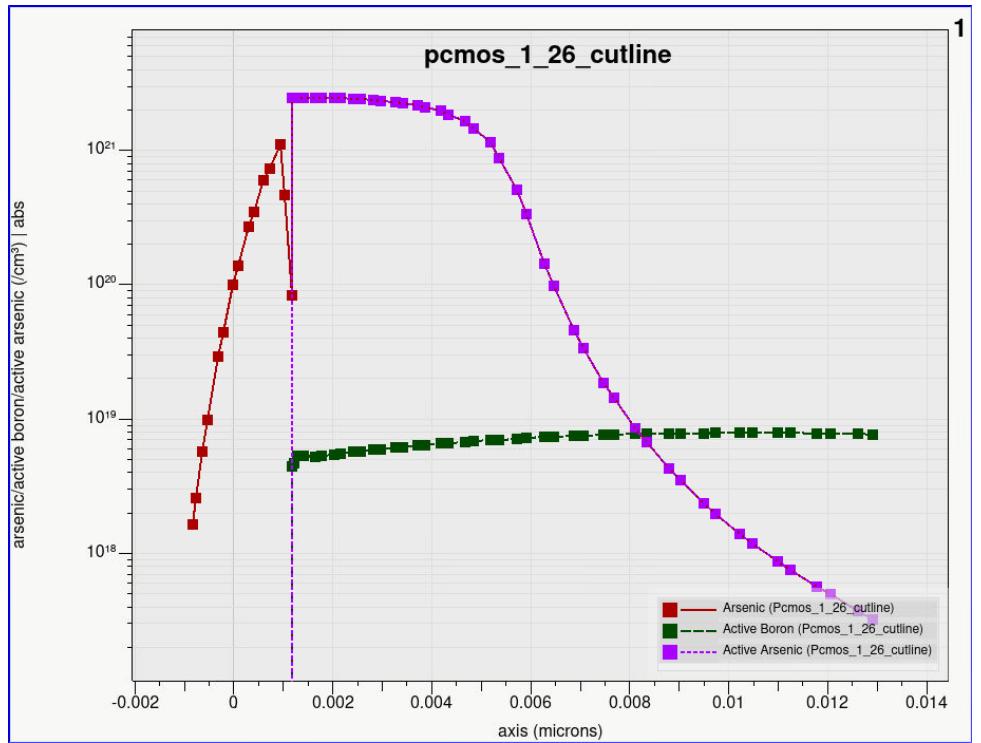


Planar HCKMG CMOS Flow: Extension Anneal

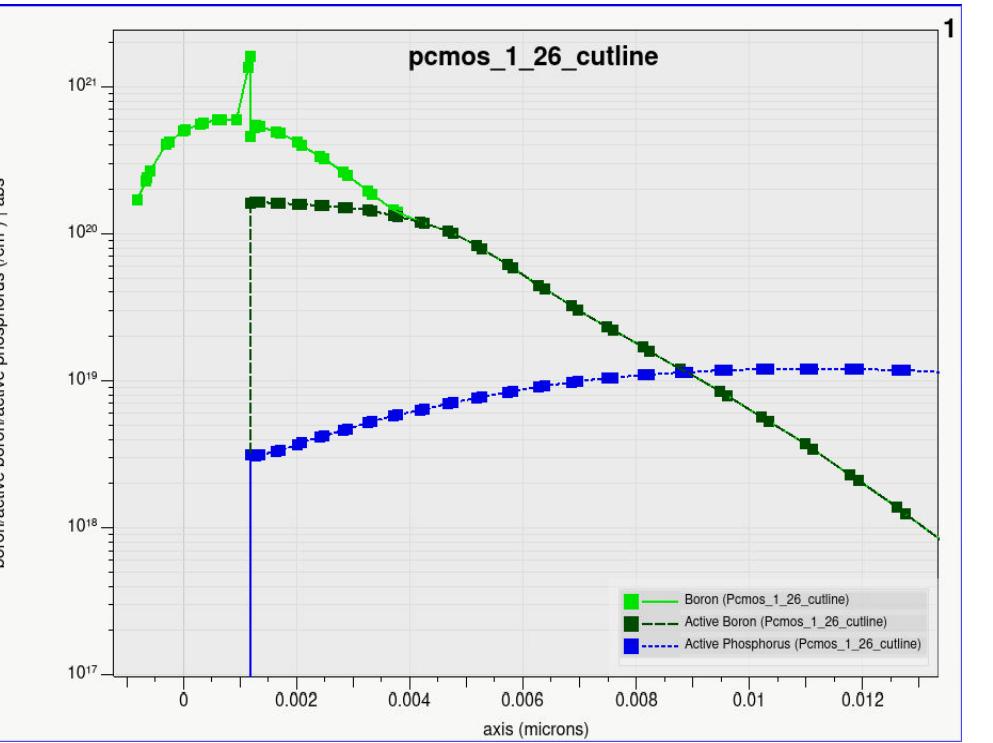


Net profile of active dopants after extension anneal.

Planar HCKMG CMOS Flow: Activated Extension Comparison



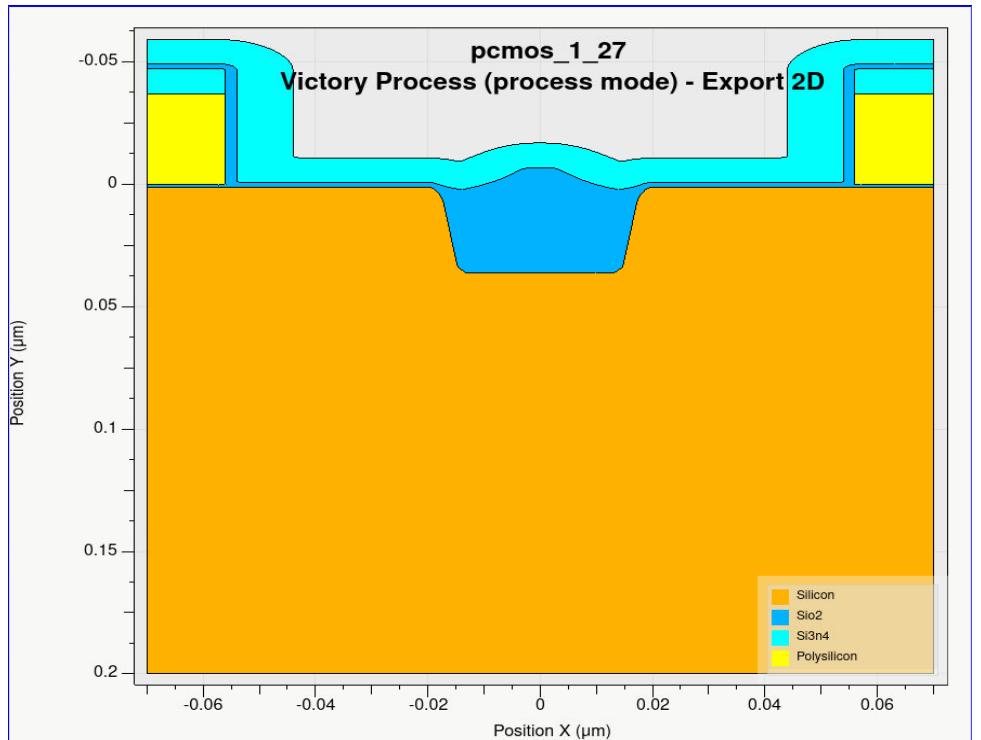
Arsenic activates to a high level ($>10^{21}$) and tends to distribute at the limit, creating a desirable "squared-off" profile.



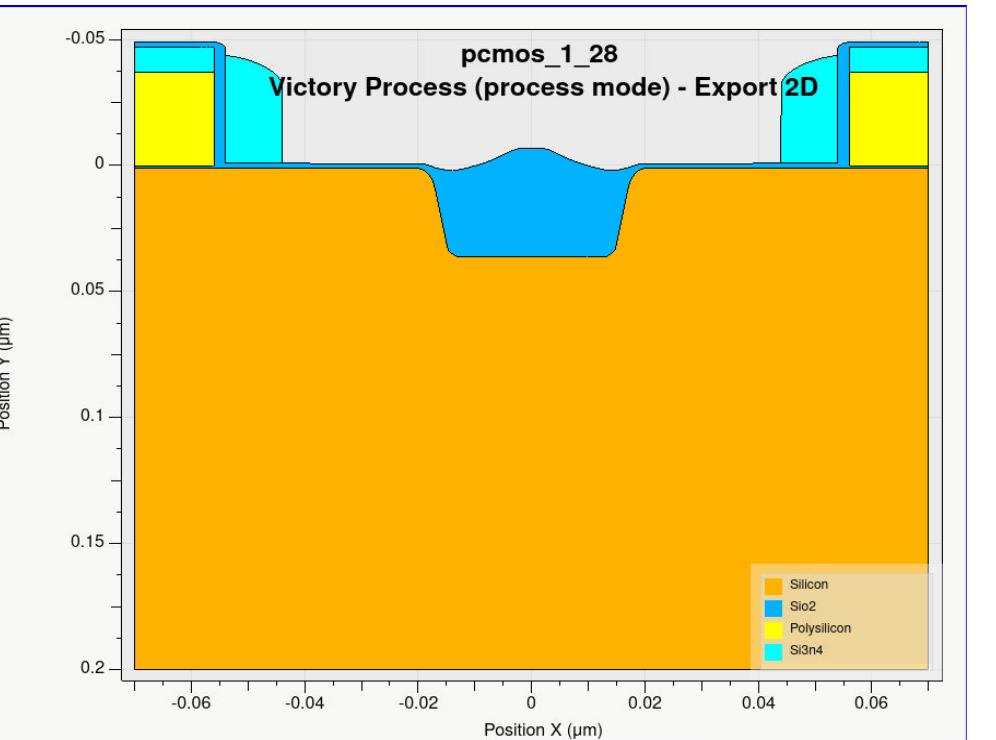
Activation limit for boron is lower ($\sim 2 \times 10^{20}$), and profile is more dispersed.

Note that a minimum extension depth is required for the tip to overlap the metal gate – the minimum tip lateral diffusion is set by the sidewall thickness of the deposited high-k gate stack.

Planar HCKMG CMOS Flow: Spacer Nitride Deposition and Etch



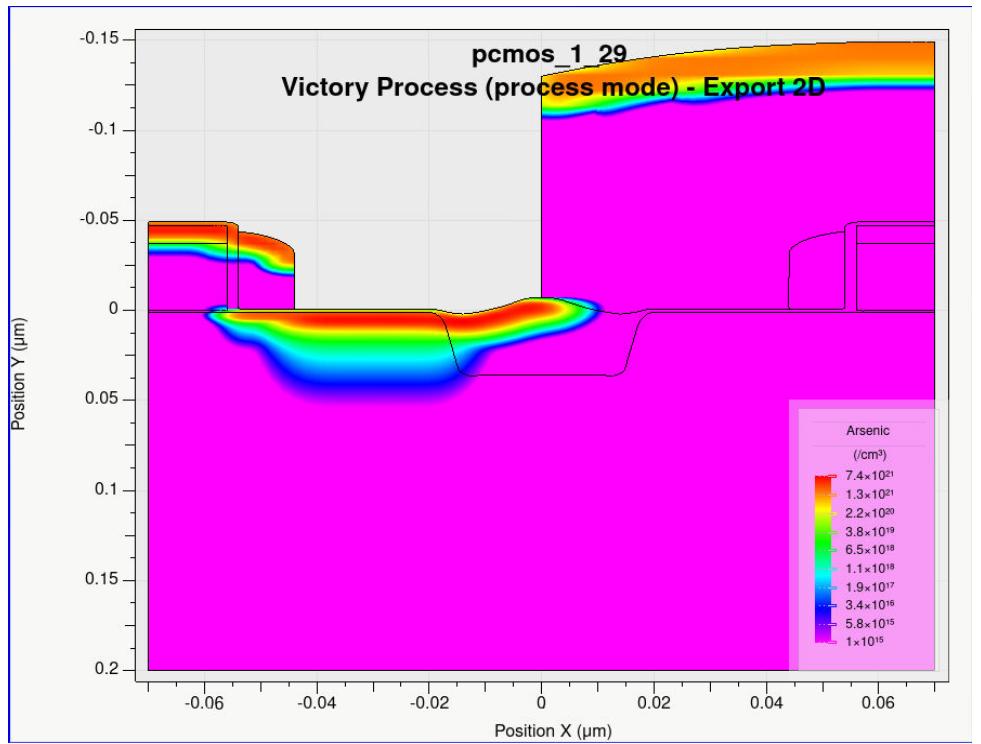
After deposition of 10nm conformal spacer nitride.



After spacer etch, selective to 2nm oxide.

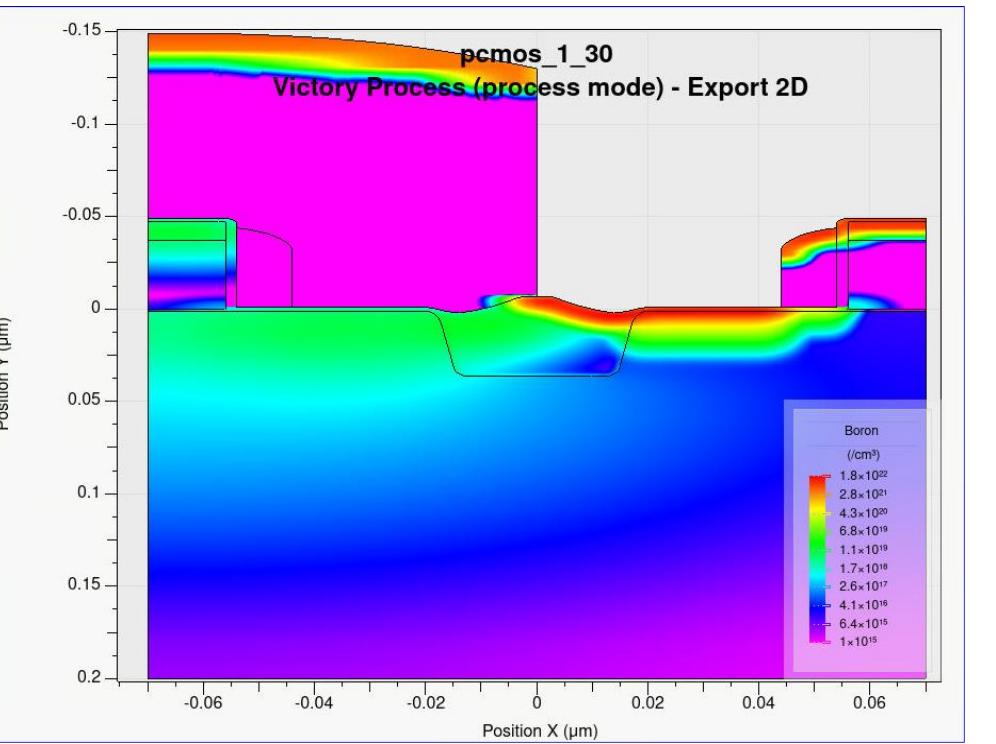
The lateral thickness of the nitride on the dummy gate sidewalls controls the deep source/drain spacing from the channel. Conformality of the deposition and isotropy (and selectivity) of the etch must be carefully controlled.

Planar HCKMG CMOS Flow: Deep Source/Drain Implants



After n-channel deep S/D arsenic implant:

3KeV, $3e15/\text{cm}^2$, 7-degree tilt, 22-degree rotation,
4 passes

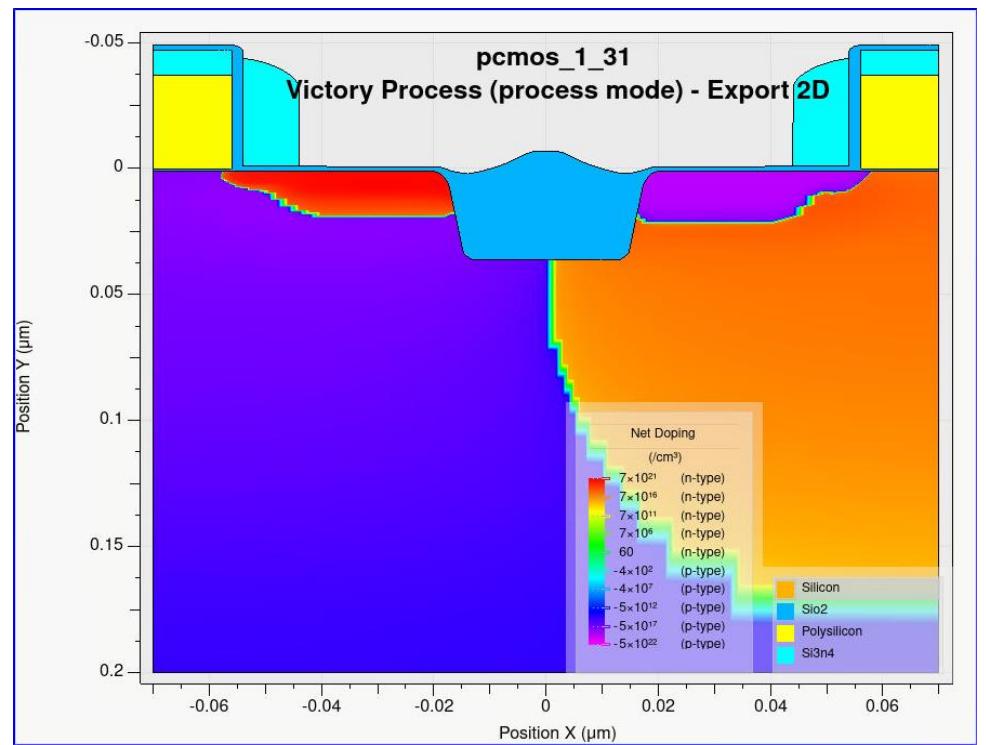


After p-channel deep S/D BF₂ implant:

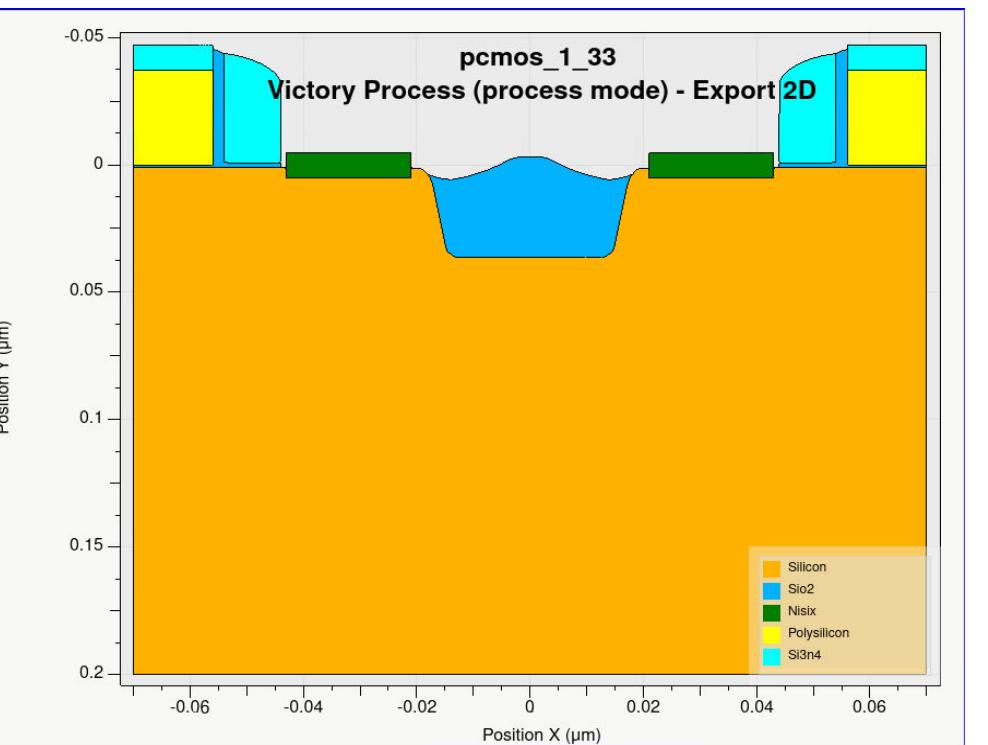
3KeV, $3e15/\text{cm}^2$, 7-degree tilt, 22-degree rotation,
4 passes



Planar HCKMG CMOS Flow: After S/D Anneal and Silicide

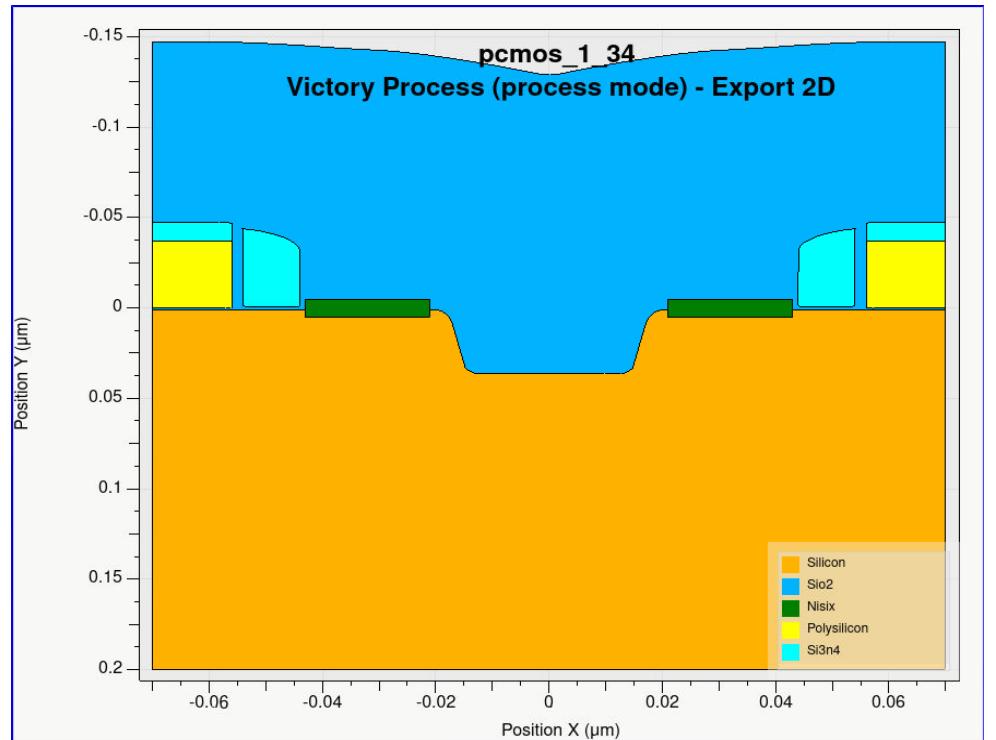


Active dopant contours after s/d anneal

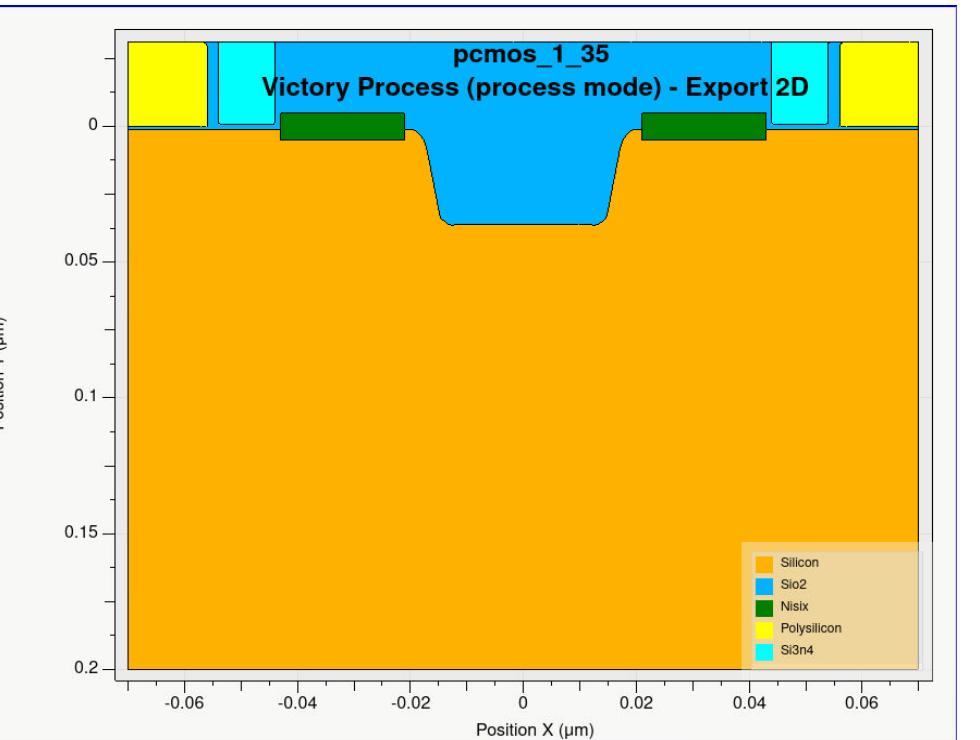


Nickel salicide process is performed, but only approximated in simulation. Because the nitride remains over the poly gates, the silicide will only form on the source and drain surfaces.

Planar HKMG CMOS Flow: Oxide Overcoat and CMP

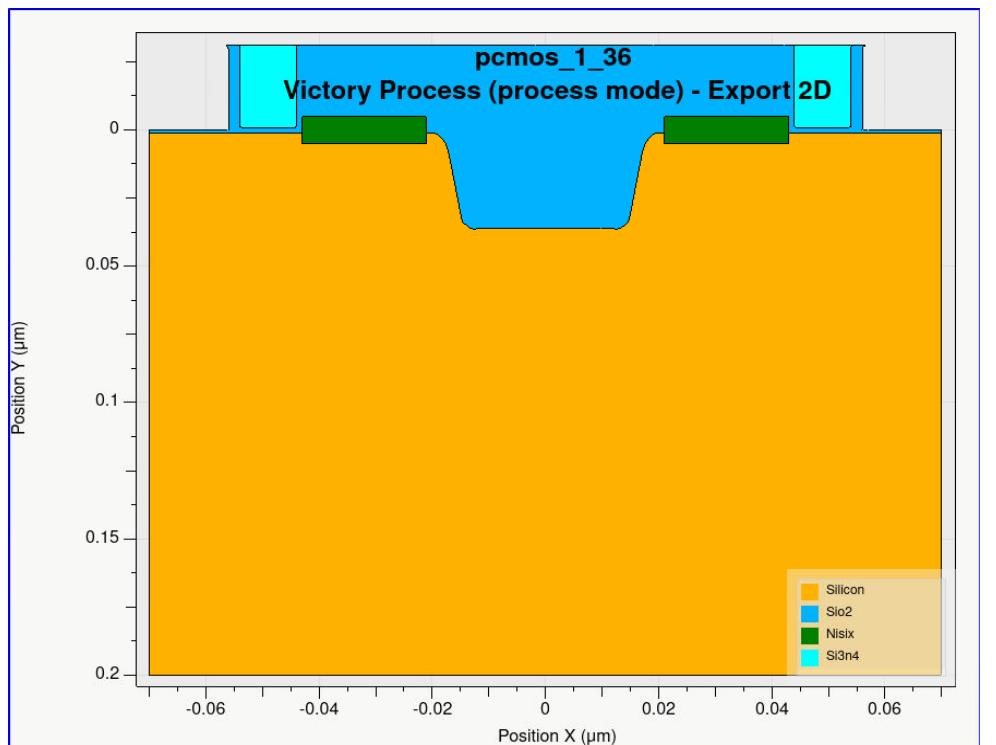


A conformal oxide layer is deposited in preparation for CMP to expose dummy gate poly.

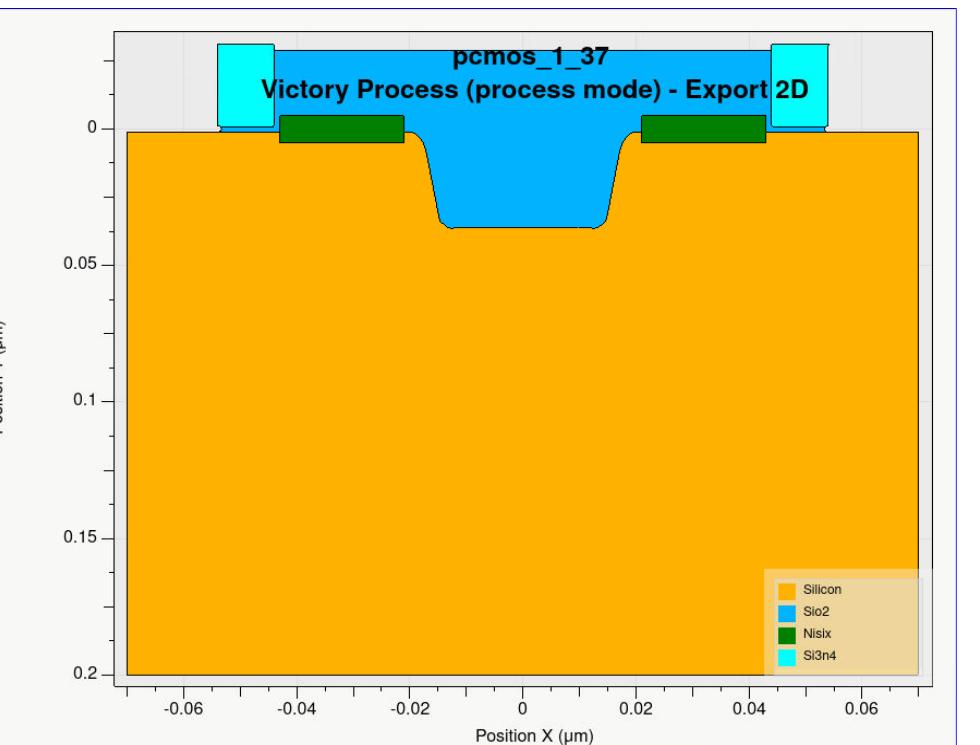


Oxide is polished back, removing hardmask oxide and stopping within the polysilicon of the dummy gates.

Planar HCKMG CMOS Flow: Dummy Gate "Pull" and Oxide Etch



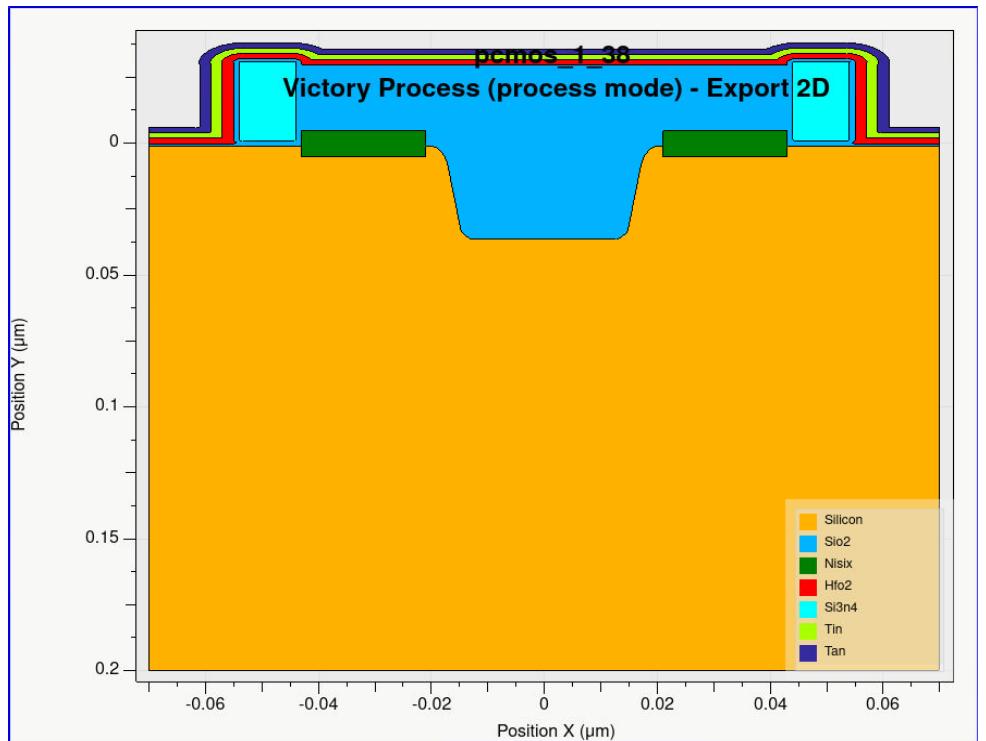
Polysilicon is removed by dry etch that is almost perfectly selective to oxide.



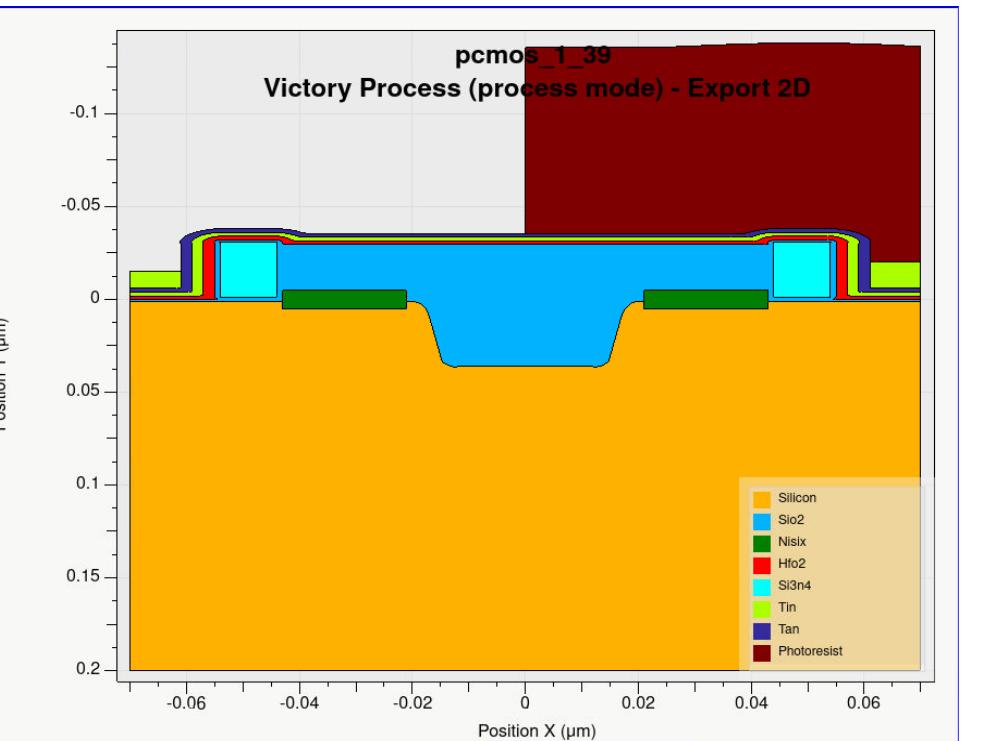
Original sacrificial gate oxide and poly sidewall oxide are etched back to reveal nitride spacer.



Planar HCKG CMOS Flow: High-K Gate Stack Deposition and WF Set



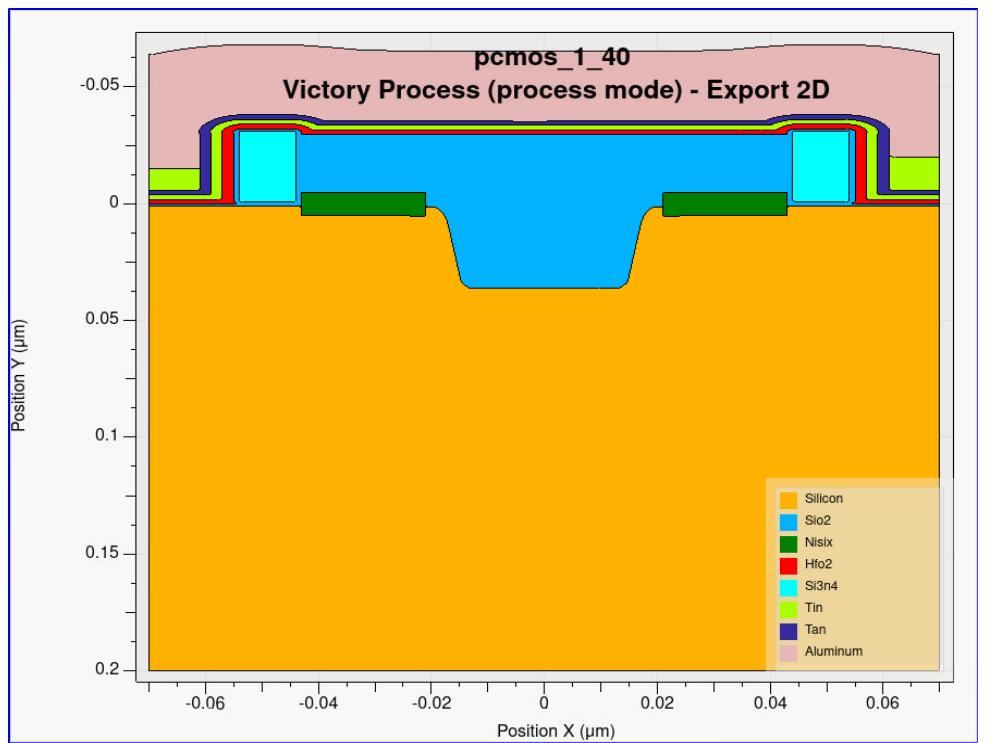
Polysilicon is removed by dry etch that is almost perfectly selective to oxide.



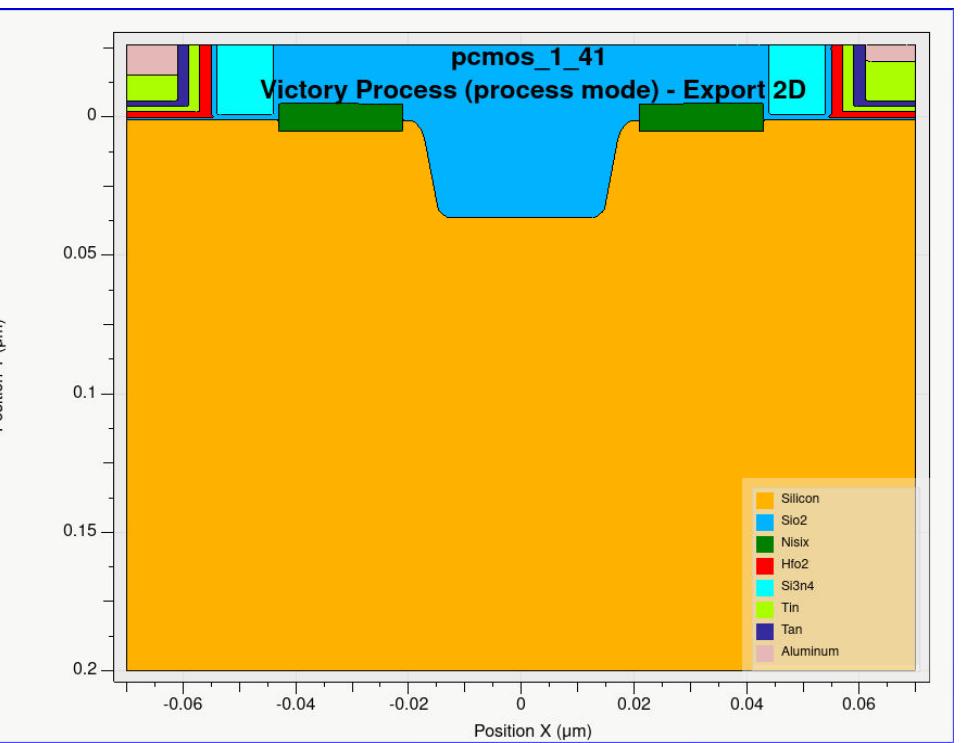
Masking and different metal and anneal conditions are applied to manipulate the workfunctions of the different devices.

The textbook example shows two different thicknesses of TiN (similar to the Sematech work on oxidation of TiN for workfunction control discussed in a prior lecture, but actual manufacturing processes will differ).

Planar HKMG CMOS Flow: Gate Metal Fill and Planarization



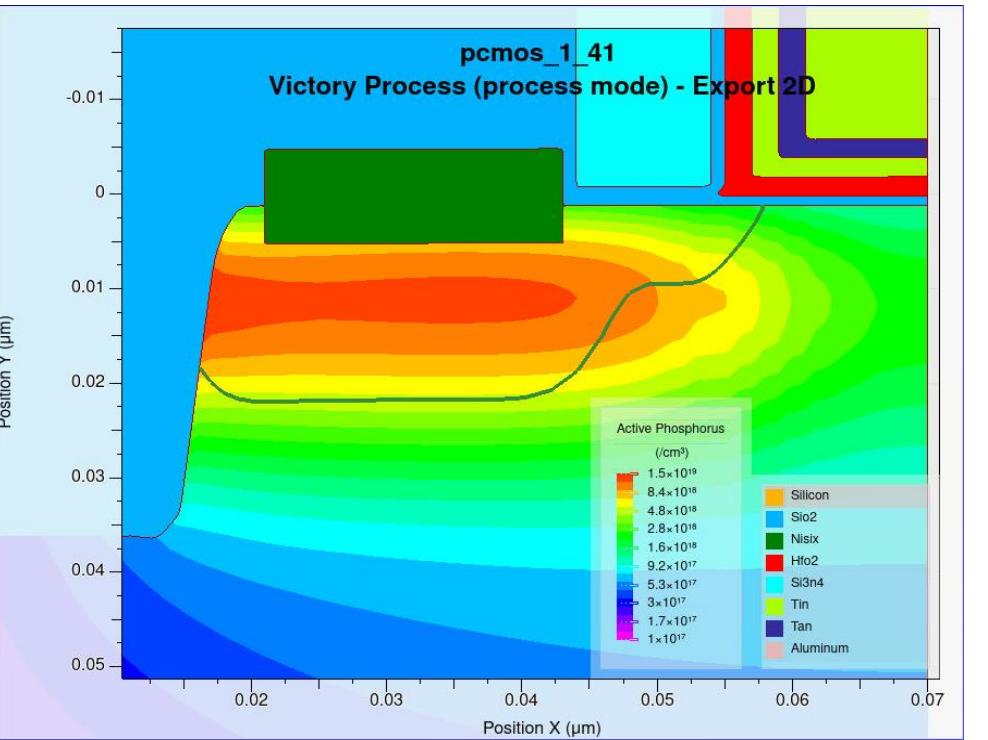
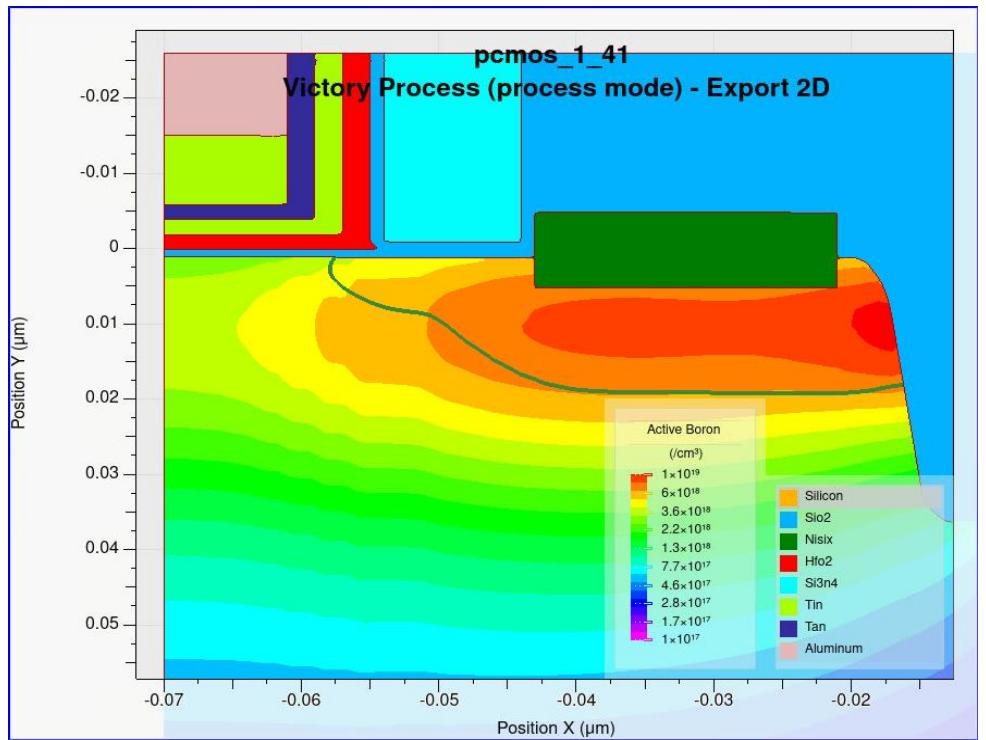
A highly-conductive metal is applied to fill any remaining volume (aluminum in this example).



CMP to remove the metal stack overburden completes the front-end process.



Planar HCKMG CMOS Flow: Final Halo and Junction Details



Victory Visual can be used to superimpose iso-surfaces (or in this case the junction outline) on a contoured image.

By overlaying the junction outline and selecting the doping range limits, the two-dimensional doping structure can be highlighted.



Planar HCKMG CMOS Flow: <output_root>_<index>_process.results file

```
output root: pcmos
index: 1
load point: 0
load file: NONE
mc_implant n.ions: N/A
```

*simulation
descriptors*

*process
input
parameters*

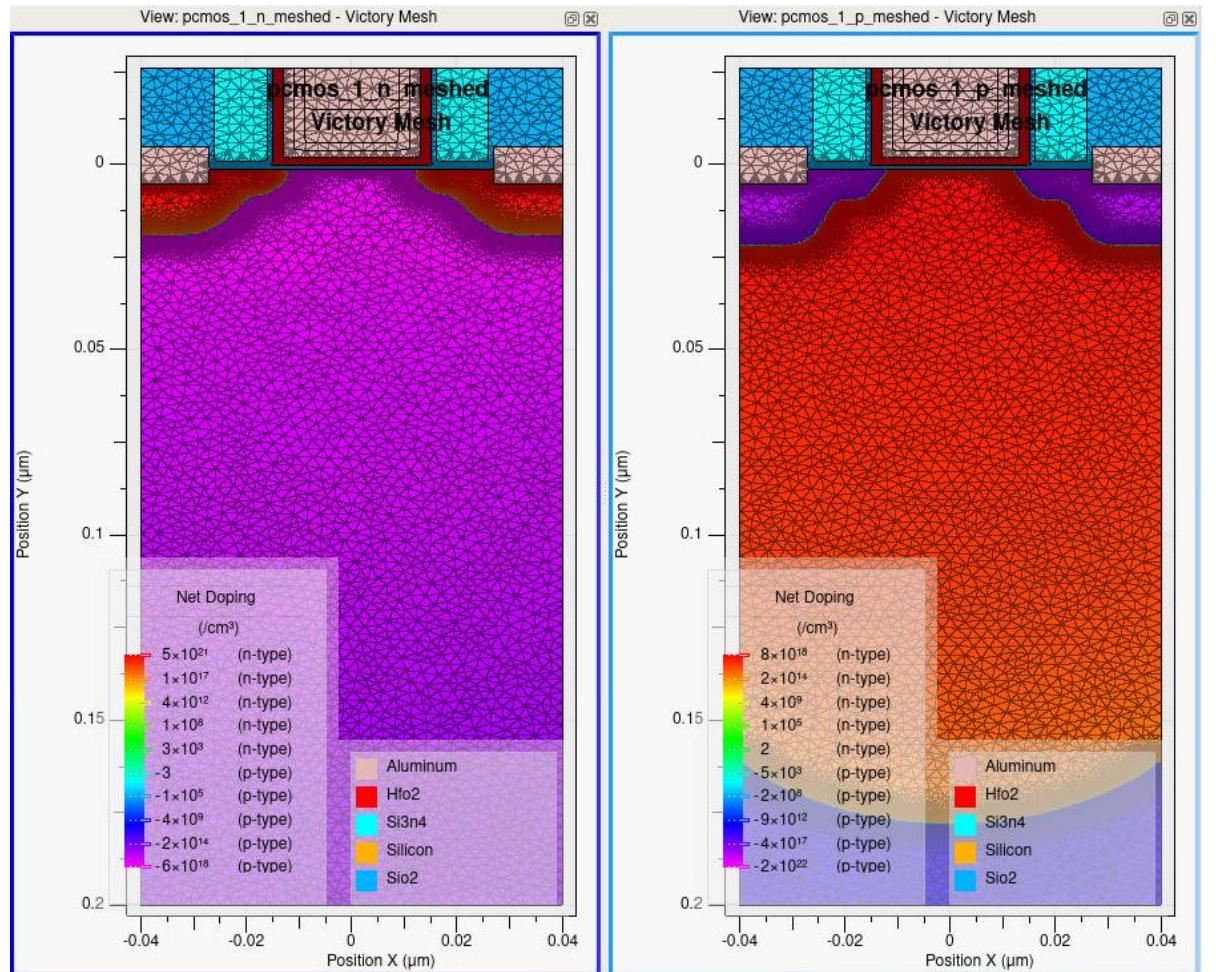
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z_height: 0.3
z_channel_offset: 0.0005
z_halo_depth: 0.012
poly_width: 0.028
iso_width: 0.03
iso_to_poly_width: 0.041
nisi_to_iso_width: 0.005
well_overlap: 0
sti_depth: 0.035
sti_angle: 85
t_oxImplant: 0.003
t_gox_sac: 0.001
t_ox_poly: 0.002
t_gox_sio2: 0.001
t_gox_hfo2: 0.002
t_tin: 0.002
t_nit_spacer: 0.01
t_nit_spacer_oet: 0.005
pwell_energy: 4
pwell_dose: 7e+12
nvt_energy: 4
nvt_dose: 6.9e+12
nwell_energy: 10
nwell_dose: 6.3e+12
pvt_energy: 10
pvt_dose: 2.4e+12
nhalo_energy: 3
nhalo_dose: 1.4e+13
phalo_energy: 8
phalo_dose: 1.8e+13
next_energy: 1.2
next_dose: 1e+15
pext_energy: 1.4
pext_dose: 2e+14
nsd_energy: 3
nsd_dose: 3e+15
psd_energy: 2
psd_dose: 7e+15
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well_diff_time: 14
ext_diff_temp: 1000
ext_diff_time: 0.02 (seconds)
sd_diff_temp: 1000
sd_diff_time: 0.02 (seconds)
```

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ext_depth_n: 0.00698898451
ext_depth_p: 0.00774702909
sd_depth_n: 0.0170415257
sd_depth_p: 0.019818278
leffj_n: 0.0245174904
lext_n: 0.0037412548
lmetal_n: 0.0259954244
overlap_n: 0.000738967
leffj_p: 0.0244574686
lext_p: 0.0037712657
lmetal_p: 0.02599542
overlap_p: 0.0007689757
end: Fri Sep 6 18:10:43 UTC 2024
```

*extracted
physical
dimensions*

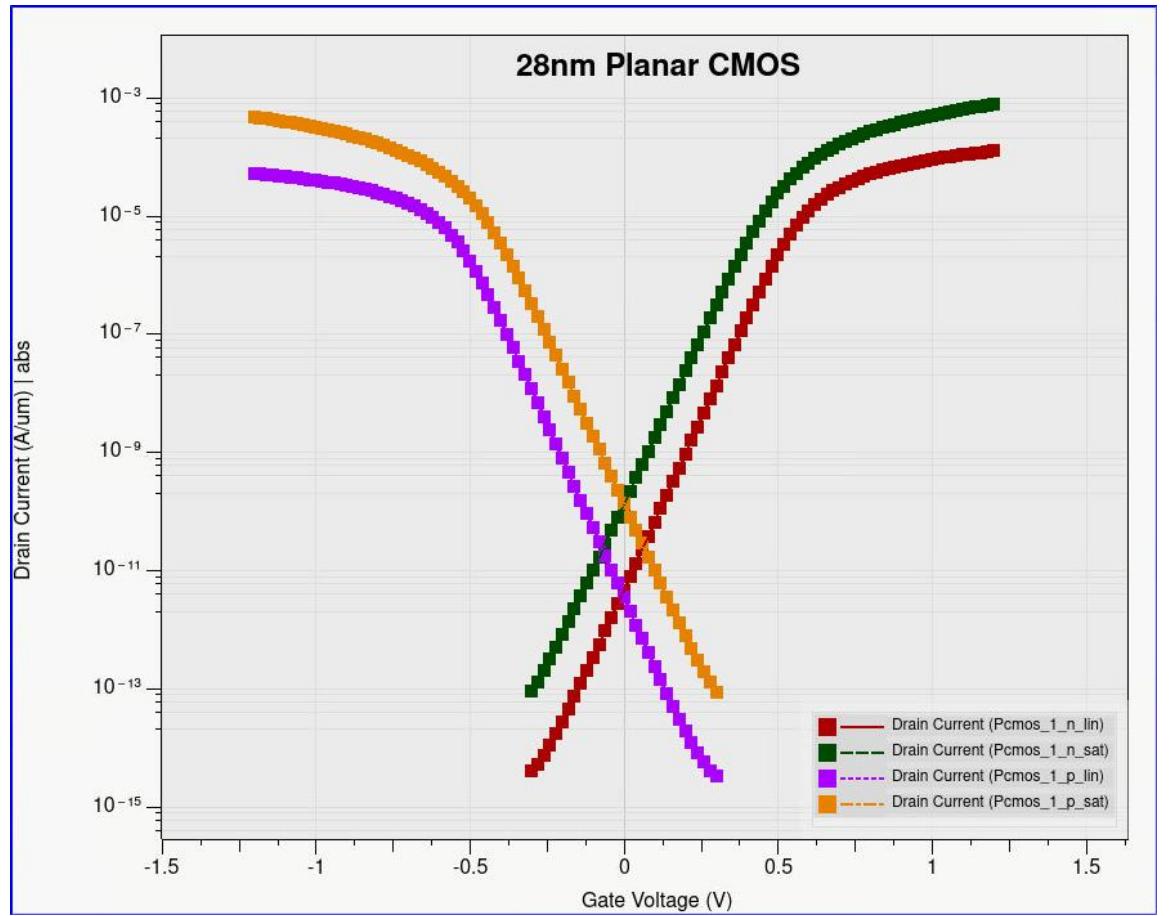
e.g. "cmos_1_process.results"

Planar HCKMG CMOS Flow: Cropping and Meshing for Electrical Simulation



To allow electrical simulation with Victory Device, the individual N and P transistors are cropped, mirrored, translated, and remeshed using Victory Mesh.

Planar HCKMG CMOS Flow: Electrical Simulation Output



	N	P
Linear Threshold Voltage (V_g for $I_d = 100\text{nA}/\mu\text{m}$, $I_d = 0.05$)	0.375	0.380
Saturation Threshold Voltage (V_g for $I_d = 100\text{nA}/\mu\text{m}$, $I_d = 0.05$)	0.255	0.252
I_{dlin} ($V_d = 1.2$, $V_g = 0.05$) $\mu\text{A}/\mu\text{m}$	123.6	51.78
I_{dsat} ($V_d = V_g = 1.2\text{V}$) $\mu\text{A}/\mu\text{m}$	759.3	468.9
Subthreshold Slope (mV/decade) linear ($V_d = 0.05$)	87.5	88.5
Subthreshold Slope (mV/decade) saturation ($V_d = 1.2$)	89.4	89.6
Off-State Leakage ($\text{nA}/\mu\text{m}$) linear ($V_d = 0.05$, $V_g = 0$)	0.00456	0.00348
Off-State Leakage ($\text{nA}/\mu\text{m}$) saturation ($V_d = 1.2$, $V_g = 0$)	0.131	0.136
Drain-Induced Barrier Lowering (mV)	120	128

The resulting device characteristics are well matched and well behaved.

Gate workfunctions set to 4.4eV and 5eV for n-channel and p-channel, respectively. Generation lifetimes of 100ps assumed for electrons and holes, with contact resistance of $10^{-10} \text{ ohm}\cdot\text{cm}^2$.

Planar HCKMG CMOS Flow: <output_root>_<index>_process.results file

cmos_1_n_lin.results:

```
index: 1
device: n
bias: lin

structure width: 0.08
workfunction: 4.4
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*1
drain bias: 0.05*1
minimum gate voltage: -0.3*1
maximum gate voltage: 1.2*1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep 6 18:13:48 UTC 2024
```

Vth_[V]=0.37532027

Id_[uA/um]=123.563068

Ileak_[nA/um]=0.00456331986

slope=11.4277097

ss_[mV/dec]=87.5065981

vtgmax=0.55259331

end: Fri Sep 6 18:15:41 UTC 2024

cmos_1_n_sat.results:

```
index: 1
device: n
bias: sat

structure width: 0.08
workfunction: 4.4
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*1
drain bias: 1.2*1
minimum gate voltage: -0.3*1
maximum gate voltage: 1.2*1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep 6 18:16:08 UTC 2024
```

Vth_[V]=0.255489571

Id_[uA/um]=759.241263

Ileak_[nA/um]=0.130946582

slope=11.1821198

ss_[mV/dec]=89.4284821

vtgmax=0.634296593

end: Fri Sep 6 18:18:09 UTC 2024

cmos_1_p_lin.results:

```
index: 1
device: p
bias: lin

structure width: 0.08
workfunction: 5
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*-1
drain bias: 0.05*-1
minimum gate voltage: -0.3*-1
maximum gate voltage: 1.2*-1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep 6 18:18:37 UTC 2024
```

Vth_[V]=-0.380041581

Id_[uA/um]=-52.3006066

Ileak_[nA/um]=-0.00348364983

slope=-11.3024544

ss_[mV/dec]=-88.4763578

vtgmax=-0.515151573

end: Fri Sep 6 18:21:57 UTC 2024

cmos_1_p_sat.results:

```
index: 1
device: p
bias: sat

structure width: 0.08
workfunction: 5
contact resistance: 1e-10
lifetime n0: 1e-10
lifetime p0: 1e-10
threshold current: 1e-07*-1
drain bias: 1.2*-1
minimum gate voltage: -0.3*-1
maximum gate voltage: 1.2*-1
drain bias step: 0.1
gate bias step: 0.1
gate ramp step: 0.02

start: Fri Sep 6 18:22:24 UTC 2024
```

Vth_[V]=-0.251754859

Id_[uA/um]=-469.747069

Ileak_[nA/um]=-0.136159708

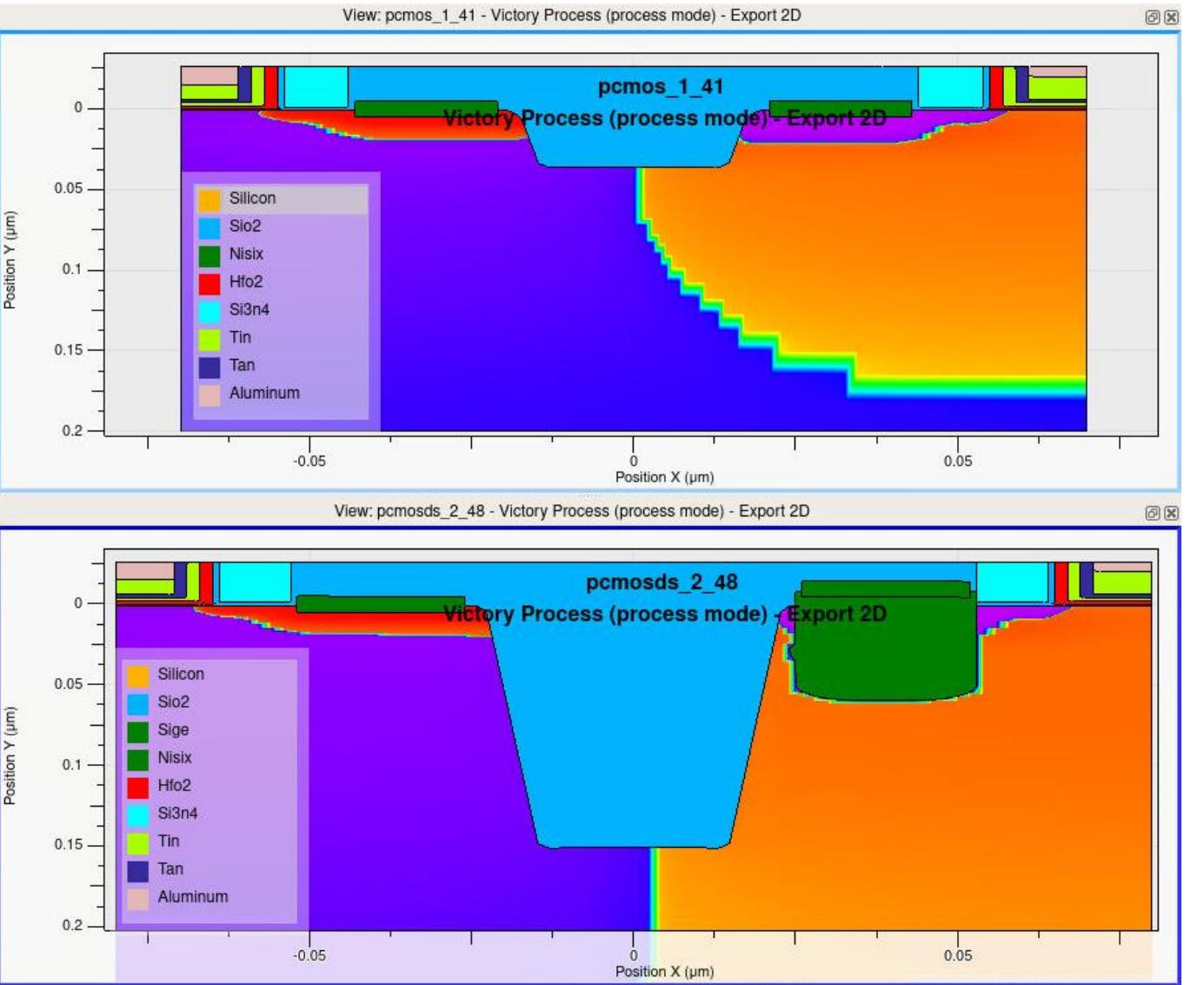
slope=-11.1564715

ss_[mV/dec]=-89.6340747

vtgmax=-0.622715814

end: Fri Sep 6 18:26:07 UTC 2024

Planar HCKMG CMOS Flow: Simulation Alterations



- Increase the trench isolation depth from 35nm to 150nm.
- Increase the isolation width from 30nm to 40nm.
- Introduce a 10nm overlap of nwell and pwell masks beyond the center of the isolation.
- Insert 60nm-deep SiGe into the p-channel source and drain.

N-channel to P-channel gate distance increased from 140nm to 160nm.
Gate length and gate insulator stack remain the same.



Planar HCKMG CMOS Flow: SiGe Insertion into PMOS S/D

mask, nhalo and ntip implants
mask, phalo and ptip implants
anneal
- sixth load point (flash)

spacer deposition

spacer etch

mask, N source/drain
mask, P source/drain
anneal

- seventh load point (sd)

silicide (silicon etch and NiSi deposition)

oxide deposition and CMP
poly pull
sacrificial gate etch

mask, nhalo and ntip implants
mask, phalo and ptip implants
anneal
- sixth load point (flash)

spacer deposition

**mask covering nmos (nwell mask)
pmos spacer etch**

mask, P source/drain
1st s/d anneal

- seventh load point (sd)
silicon recess etch in pmos s/d

SiGe selective epitaxy

**mask covering pmos (pwell mask)
nmos spacer etch**

mask, N source/drain
2nd anneal

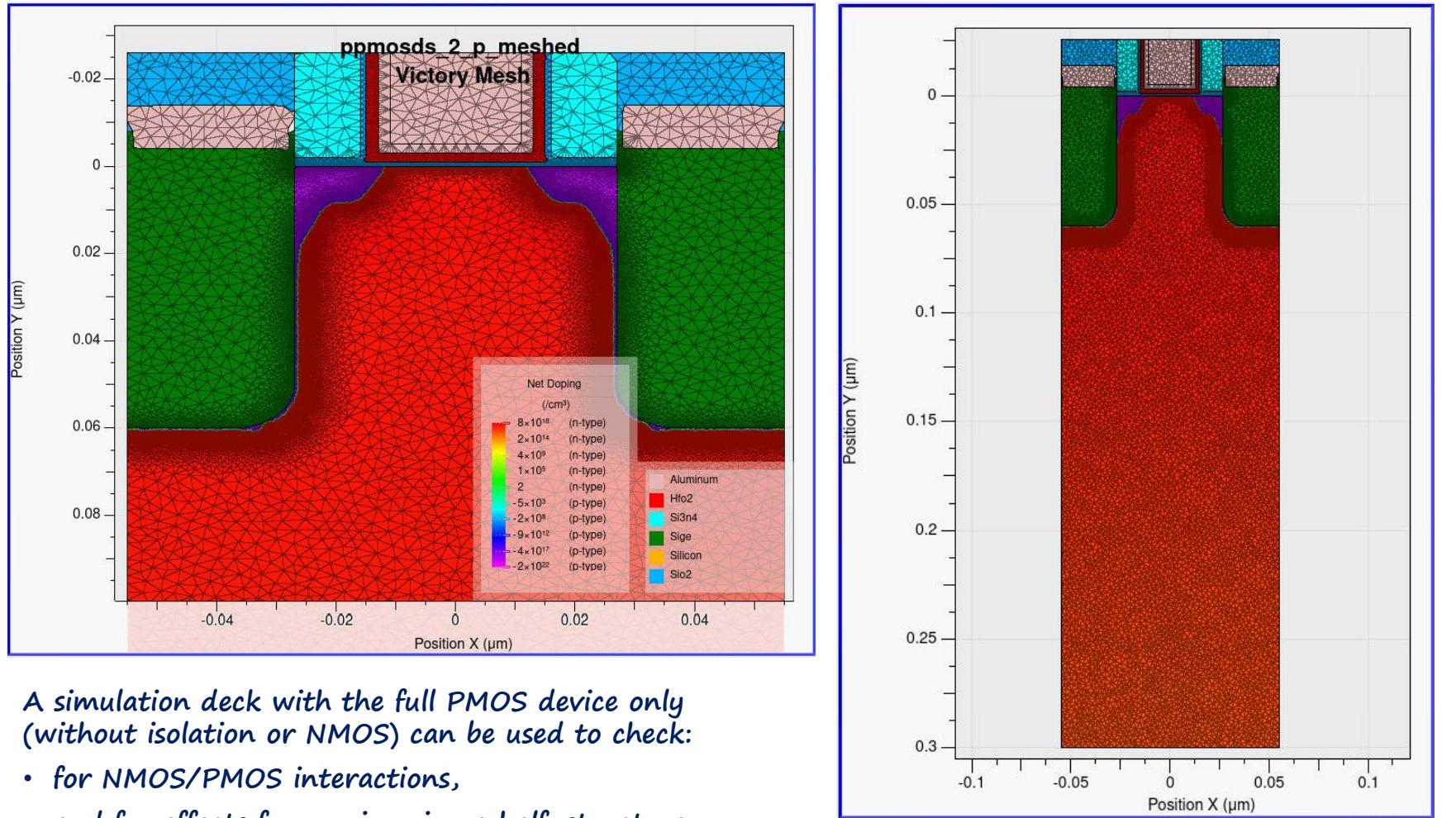
- eighth load point (sd2)

silicide (silicon and SiGe etch and NiSi deposition)

oxide deposition and CMP
poly pull
sacrificial gate etch



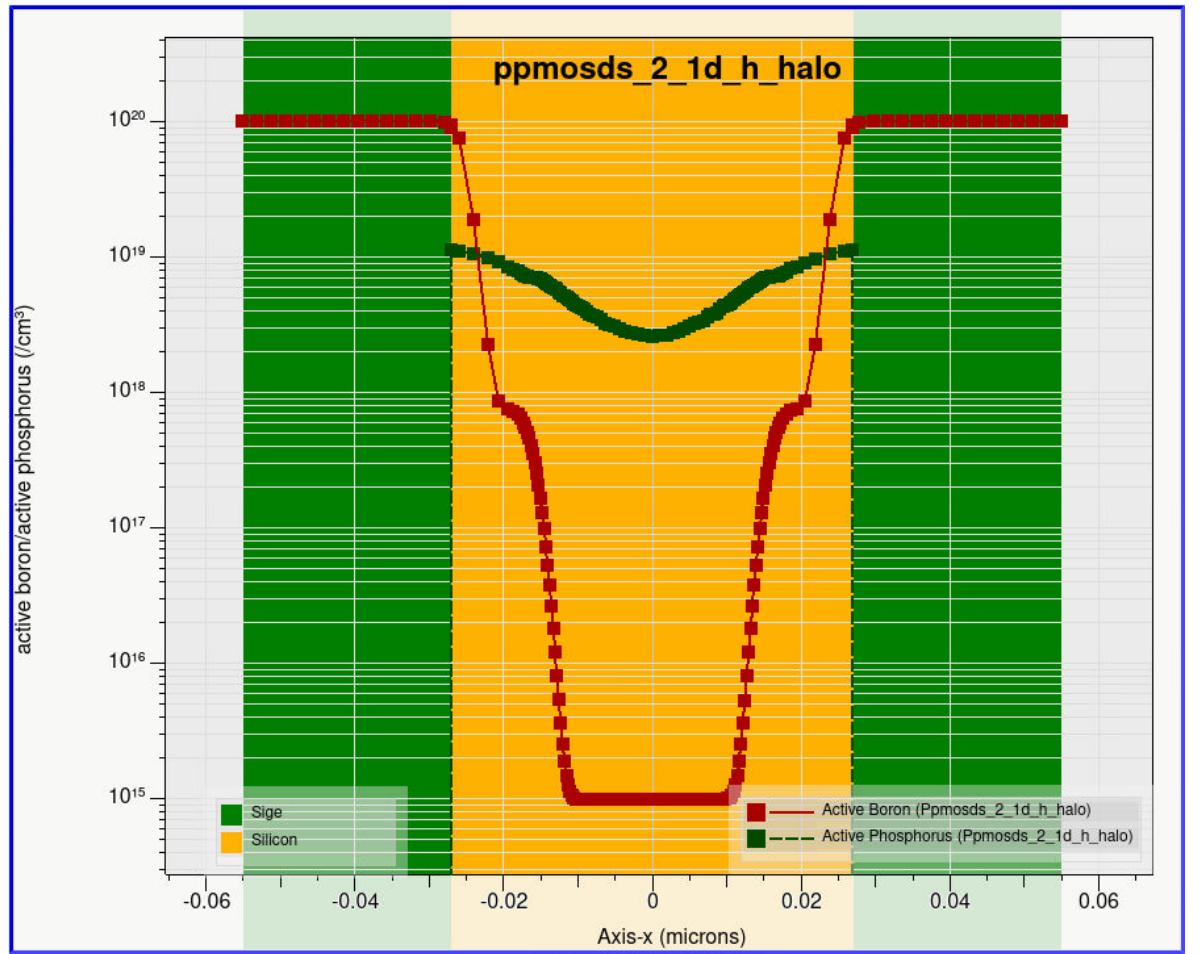
Planar HCKMG CMOS Flow: Full-Channel PMOS-Only Simulation with Stress



A simulation deck with the full PMOS device only (without isolation or NMOS) can be used to check:

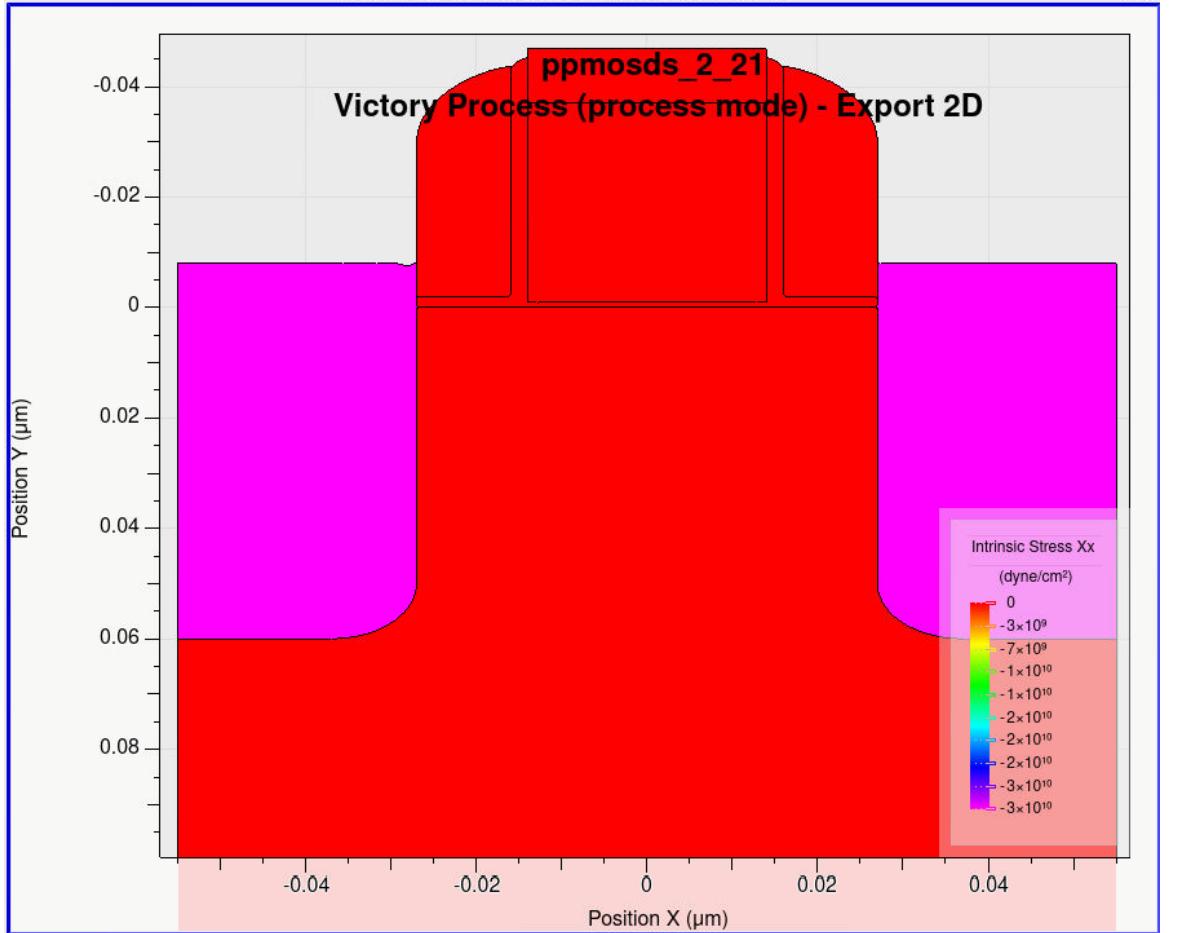
- for NMOS/PMOS interactions,
- and for effects from mirroring a half-structure,
- and for simulation of the effects of strain on the electrical characteristics.

Planar HCKMG CMOS Flow: Halo, Extension, and S/D Profiles



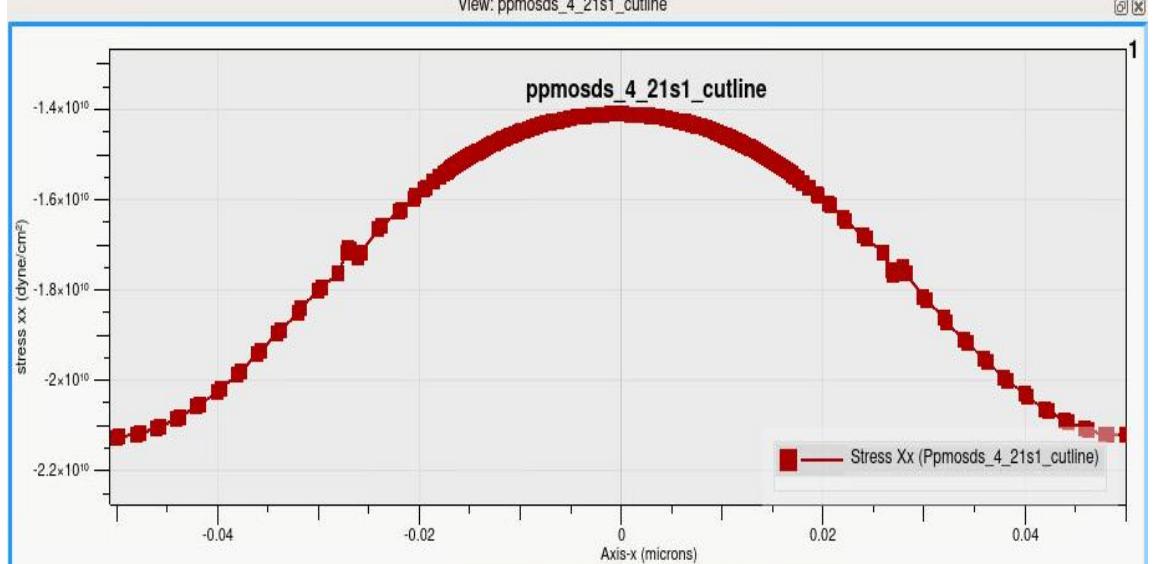
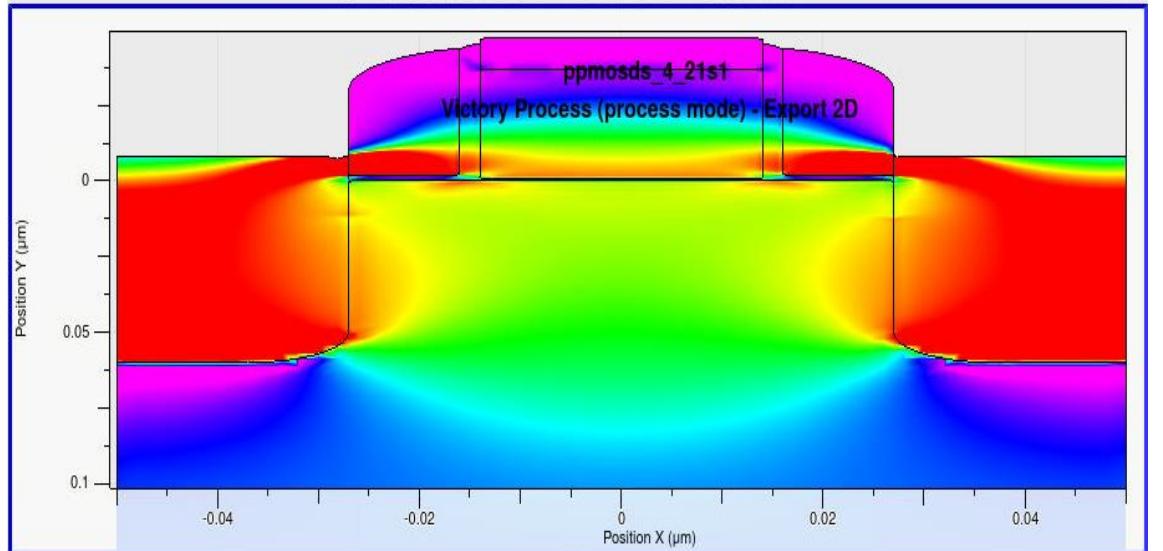
In the two-sided stand-alone P-channel device, the overlapping halo effects that lead to reverse short-channel effect are captured, and no boron migrates laterally from any adjacent nwell.

Planar HKMG CMOS Flow: Intrinsic Stress During SiGe Epitaxy



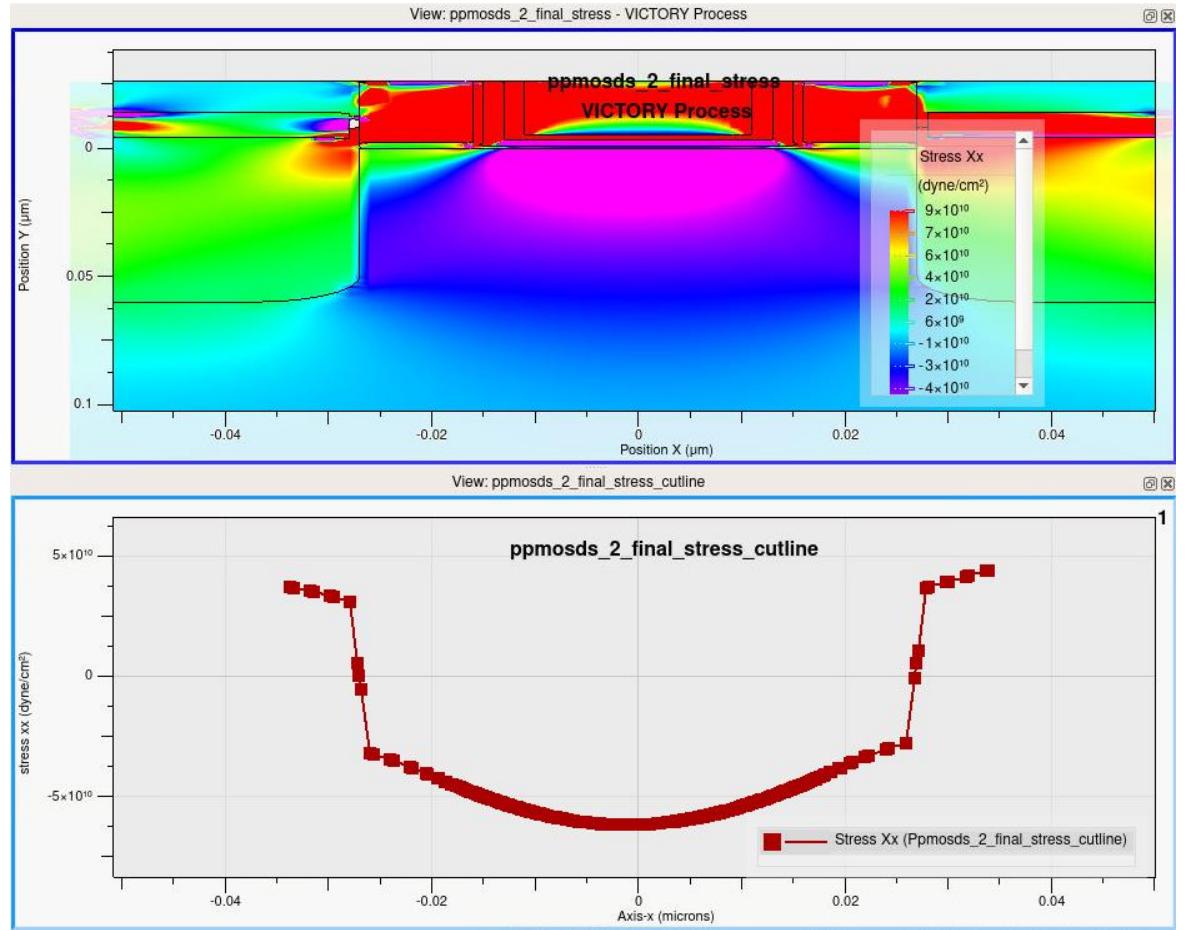
When the Victory Device method to capture stress from lattice mismatch is turned on during process simulation, the deposited SiGe shows intrinsic stress levels that are dependent on the germanium fraction.

Planar HKMG CMOS Flow: Stress Distribution After SiGe Addition



After the stress solution is calculated and transferred to the volume grid, the compressive lateral stress in the channel can be displayed.

Planar HKMG CMOS Flow: Final Results



The calculated stress changes significantly with further processing (particularly after the removal of the poly gate structure).

	P unstressed	P stressed
Linear Threshold Voltage (V_g for $I_d=100\text{nA}/\mu\text{m}$, $I_d=0.05$)	0.370	0.360
Saturation Threshold Voltage (V_g for $I_d=100\text{nA}/\mu\text{m}$, $I_d=0.05$)	0.202	0.186
I_{dlin} ($V_d=1.2$, $V_g=0.05$) $\mu\text{A}/\mu\text{m}$	54.53	69.68
I_{dsat} ($V_d=V_g=1.2\text{V}$) $\mu\text{A}/\mu\text{m}$	528.5	646.2
Subthreshold Slope (mV/decade) linear ($V_d=0.05$)	87.6	87.8
Subthreshold Slope (mV/decade) saturation ($V_d=1.2$)	92.6	93.1
Off-State Leakage ($\text{nA}/\mu\text{m}$) linear ($V_d=0.05$, $V_g=0$)	0.00424	0.00602
Off-State Leakage ($\text{nA}/\mu\text{m}$) saturation ($V_d=1.2$, $V_g=0$)	0.607	0.961
Drain-Induced Barrier Lowering (mV)	168	174

As shown in the table, final electrical characteristics show about 28% increase in P-channel linear current and about 22% increase in the saturation current over the unstressed simulation.

ECE 595 Semiconductor Device Integration Through Simulation