

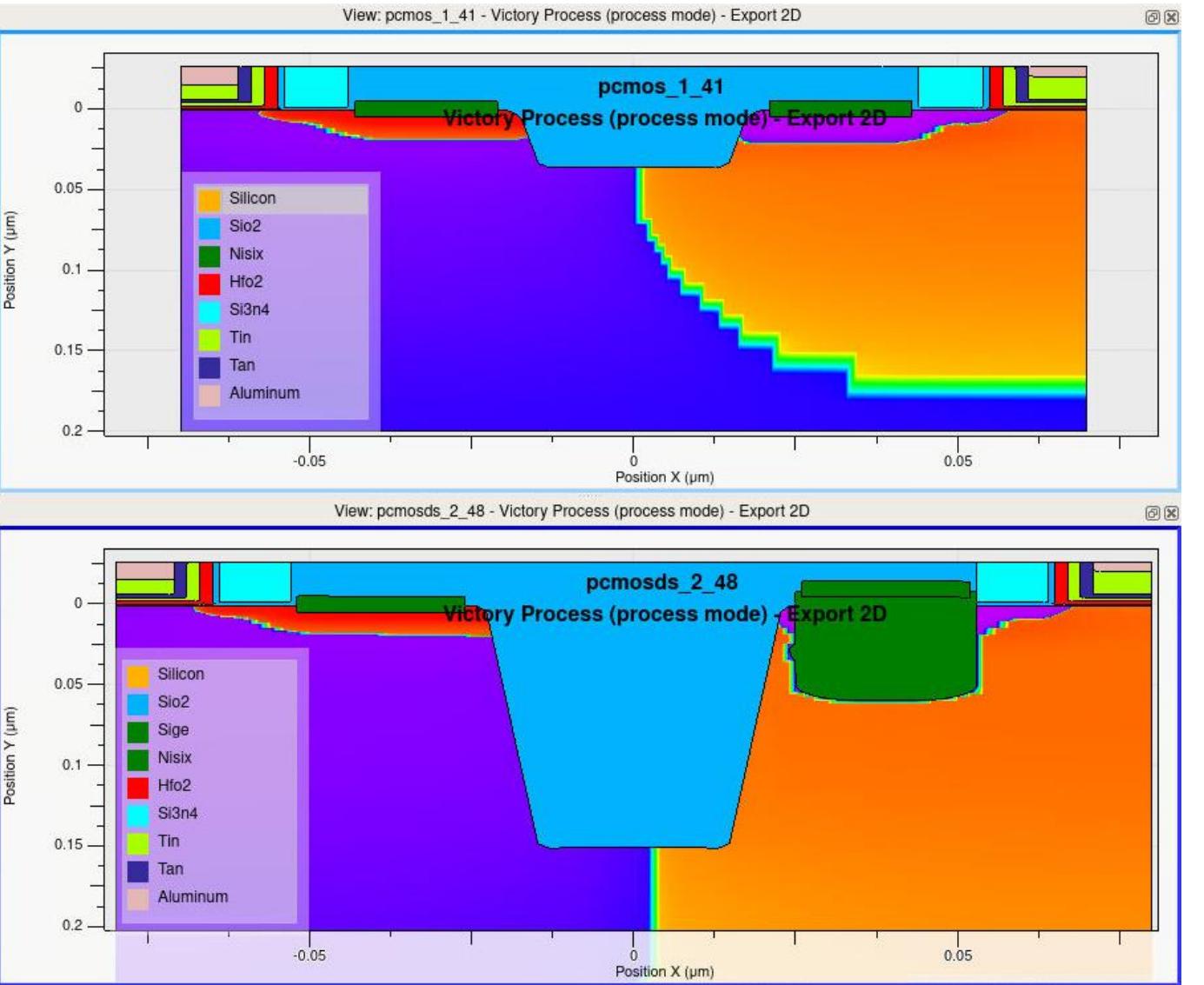
PLANAR HKMG CMOS

PART D: FLOW ALTERATION

ECE 595 Semiconductor Device
Integration Through Simulation

Tom Dungan

Planar HKMG CMOS Flow: Simulation Alterations



- Increase the trench isolation depth from 35nm to 150nm.
- Increase the isolation width from 30nm to 40nm.
- Introduce a 10nm overlap of nwell and pwell masks beyond the center of the isolation.
- Insert 60nm-deep SiGe into the p-channel source and drain.

N-channel to P-channel gate distance increased from 140nm to 160nm.
Gate length and gate insulator stack remain the same.

Planar HCKMG CMOS Flow: SiGe Insertion into PMOS S/D

mask, nhalo and ntip implants
mask, phalo and ptip implants
anneal
- sixth load point (flash)

spacer deposition

spacer etch

mask, N source/drain
mask, P source/drain
anneal

- seventh load point (sd)

silicide (silicon etch and NiSi deposition)

oxide deposition and CMP
poly pull
sacrificial gate etch

mask, nhalo and ntip implants
mask, phalo and ptip implants
anneal
- sixth load point (flash)

spacer deposition

**mask covering nmos (nwell mask)
pmos spacer etch**

mask, P source/drain
1st s/d anneal

- seventh load point (sd)
silicon recess etch in pmos s/d

SiGe selective epitaxy

**mask covering pmos (pwell mask)
nmos spacer etch**

mask, N source/drain
2nd anneal

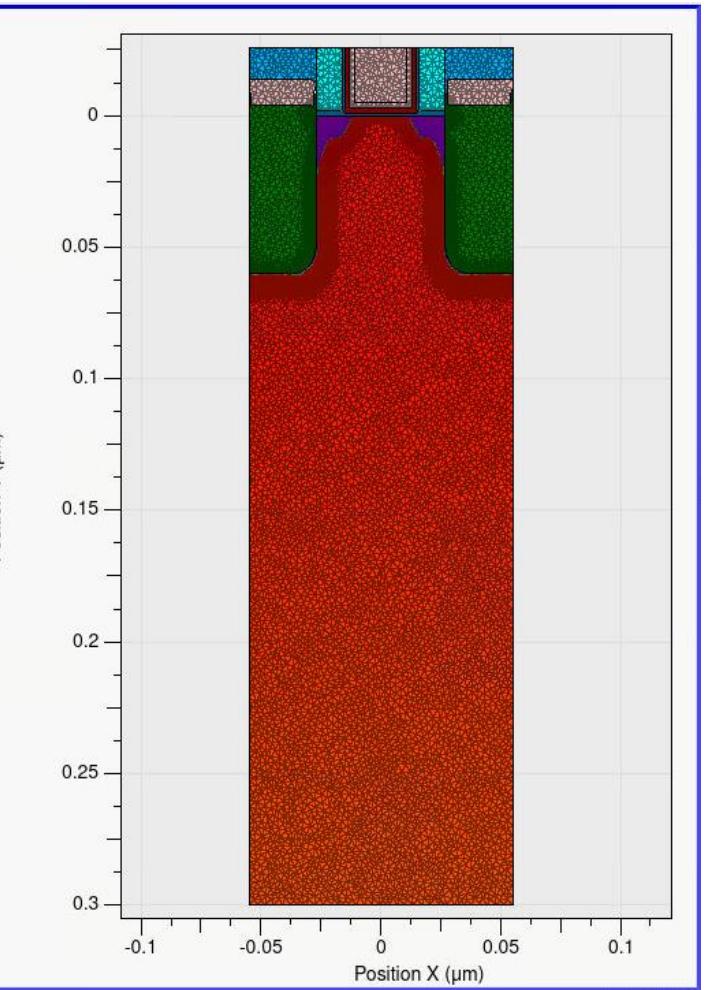
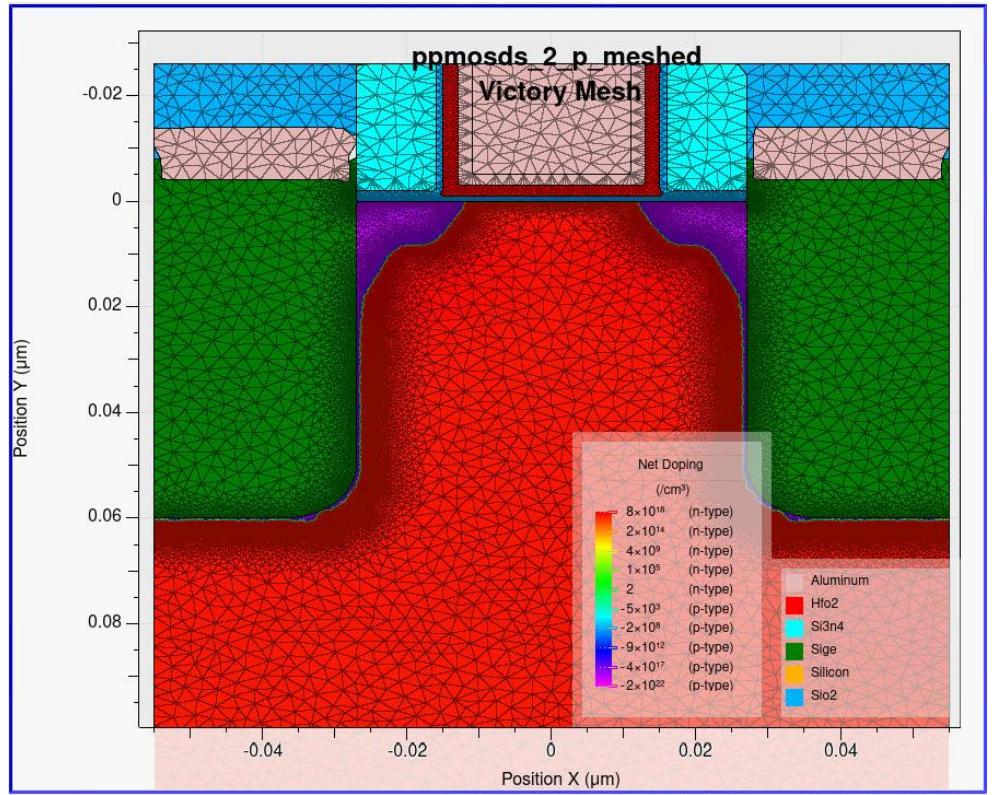
- eighth load point (sd2)

silicide (silicon and SiGe etch and NiSi deposition)

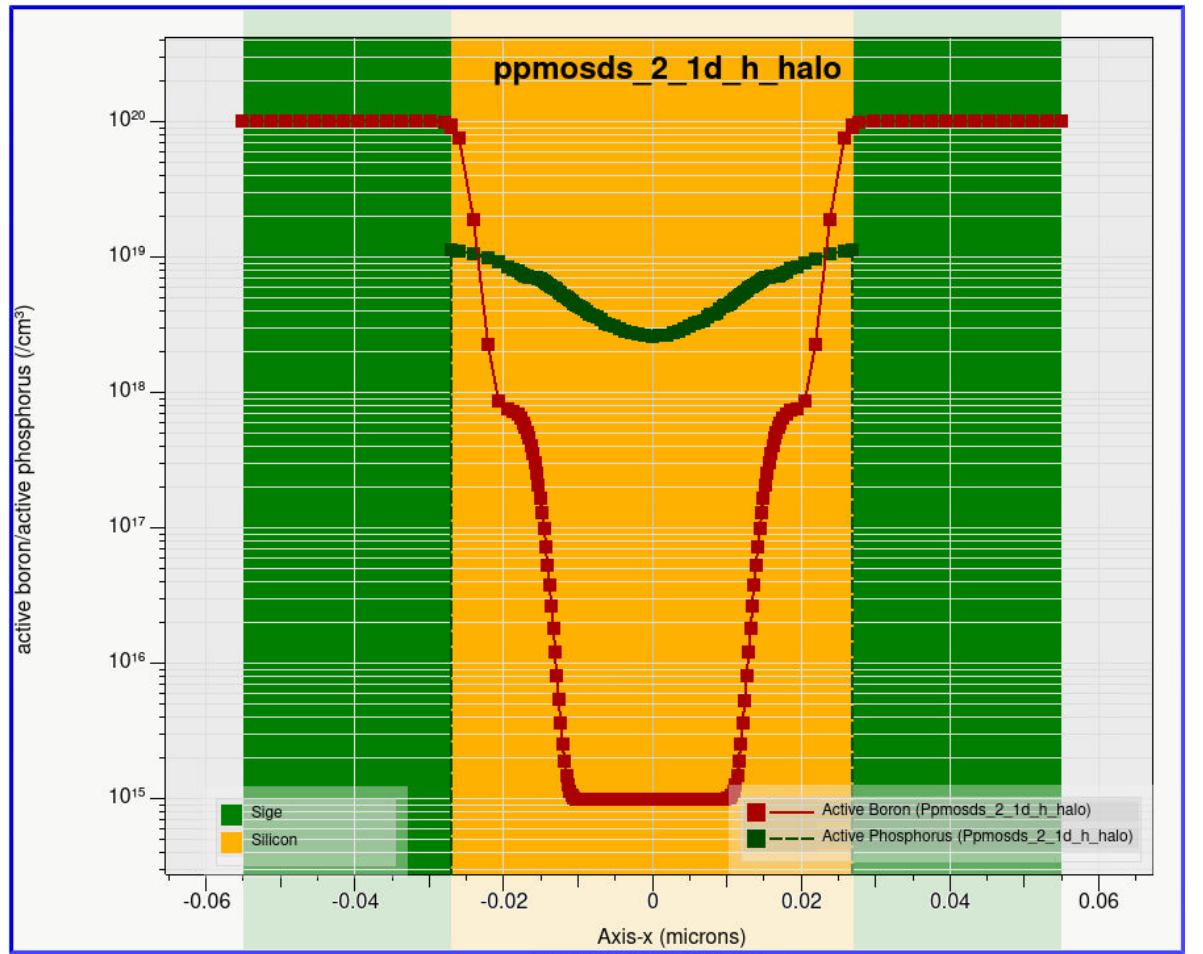
oxide deposition and CMP
poly pull
sacrificial gate etch



Planar HCKMG CMOS Flow: Full-Channel PMOS-Only Simulation with Stress

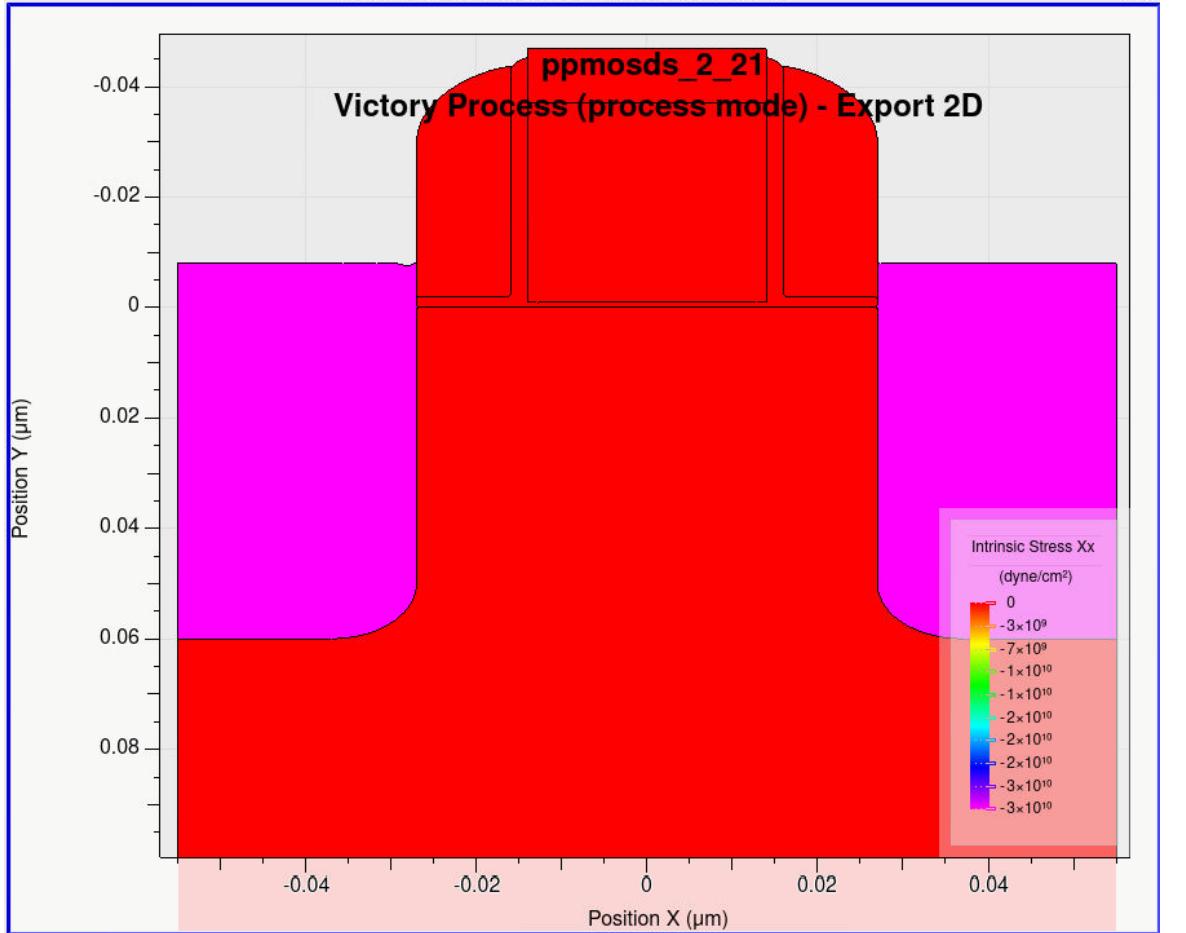


Planar HCKMG CMOS Flow: Halo, Extension, and S/D Profiles



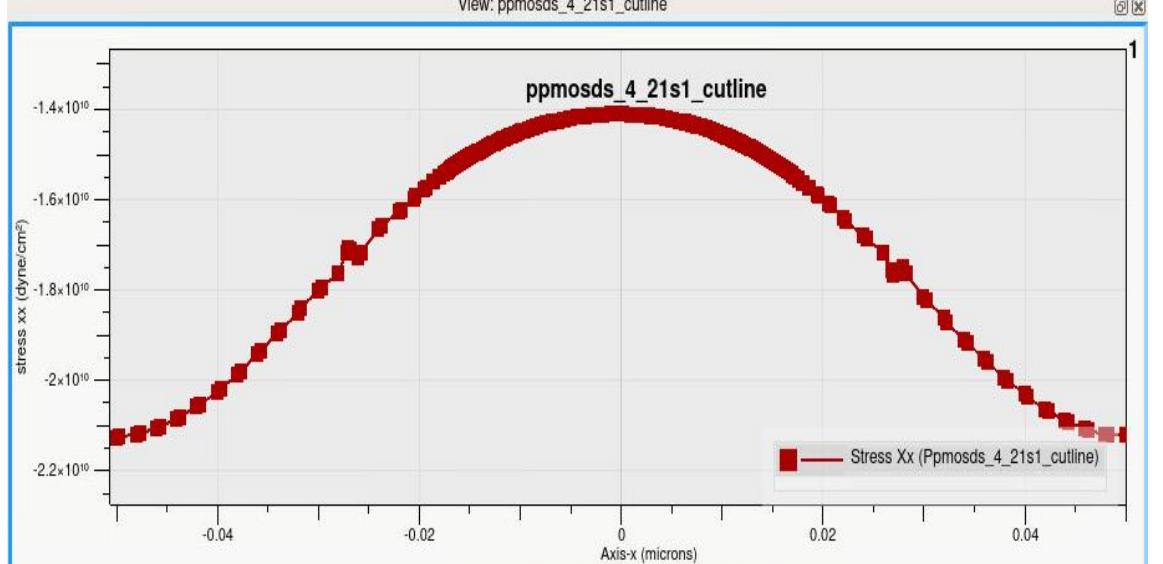
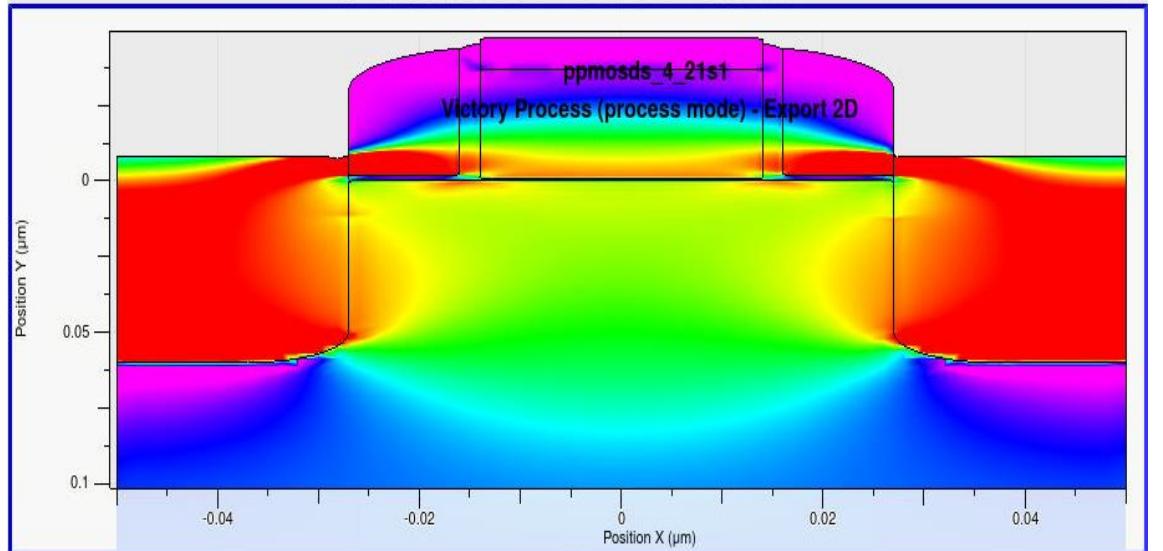
In the two-sided stand-alone P-channel device, the overlapping halo effects that lead to reverse short-channel effect are captured, and no boron migrates laterally from any adjacent nwell.

Planar HKMG CMOS Flow: Intrinsic Stress During SiGe Epitaxy



When the Victory Device method to capture stress from lattice mismatch is turned on during process simulation, the deposited SiGe shows intrinsic stress levels that are dependent on the germanium fraction.

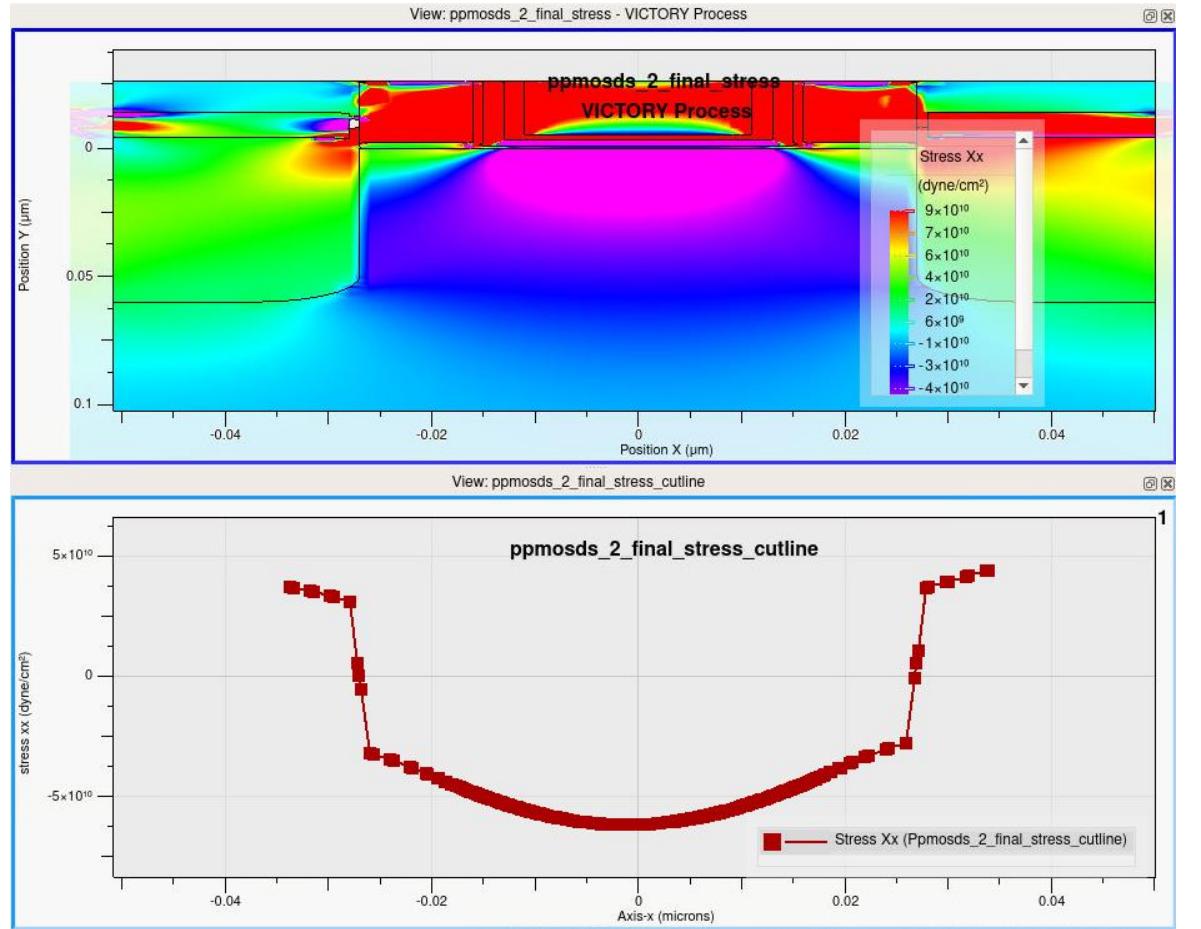
Planar HKMG CMOS Flow: Stress Distribution After SiGe Addition



After the stress solution is calculated and transferred to the volume grid, the compressive lateral stress in the channel can be displayed.



Planar HKMG CMOS Flow: Final Results



The calculated stress changes significantly with further processing (particularly after the removal of the poly gate structure).

	P unstressed	P stressed
Linear Threshold Voltage (Vg for Id=100nA/um, Id=0.05)	0.370	0.360
Saturation Threshold Voltage (Vg for Id=100nA/um, Id=0.05)	0.202	0.186
Idlin (Vd=1.2, Vg=0.05) uA/um	54.53	69.68
Idsat (Vd=Vg=1.2V) uA/um	528.5	646.2
Subthreshold Slope (mV/decade) linear (Vd=0.05)	87.6	87.8
Subthreshold Slope (mV/decade) saturation (Vd=1.2)	92.6	93.1
Off-State Leakage (nA/um) linear (Vd=0.05, Vg=0)	0.00424	0.00602
Off-State Leakage (nA/um) saturation (Vd=1.2, Vg=0)	0.607	0.961
Drain-Induced Barrier Lowering (mV)	168	174

As shown in the table, final electrical characteristics show about 28% increase in P-channel linear current and about 22% increase in the saturation current over the unstressed simulation.

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