Verilog Code

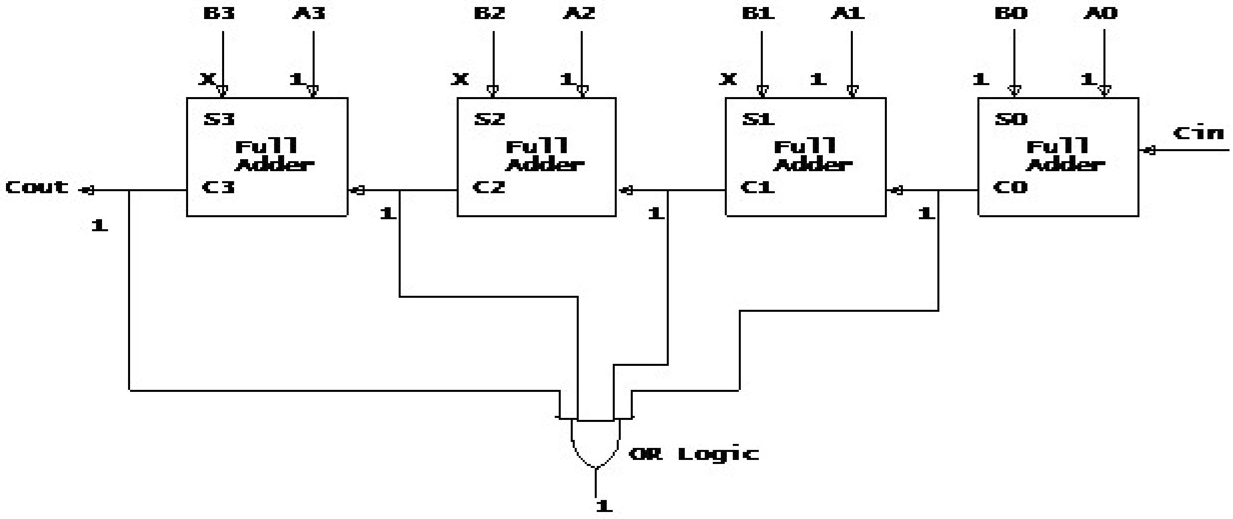
```
module rca_4bit(

   input  [3:0] A, B,   // 4-bit inputs

   input  Cin,          // Carry input

   output [3:0] Sum,     // 4-bit sum output

   output Cout          // Final carry output

);

   wire [2:0] carry;     // Internal carry wires


   full_adder fa0 (.A(A[0]), .B(B[0]), .Cin(Cin),      .Sum(Sum[0]), .Cout(carry[0]));

   full_adder fa1 (.A(A[1]), .B(B[1]), .Cin(carry[0]), .Sum(Sum[1]), .Cout(carry[1]));

   full_adder fa2 (.A(A[2]), .B(B[2]), .Cin(carry[1]), .Sum(Sum[2]), .Cout(carry[2]));

   full_adder fa3 (.A(A[3]), .B(B[3]), .Cin(carry[2]), .Sum(Sum[3]), .Cout(Cout));


endmodule
```

Test Bench Code

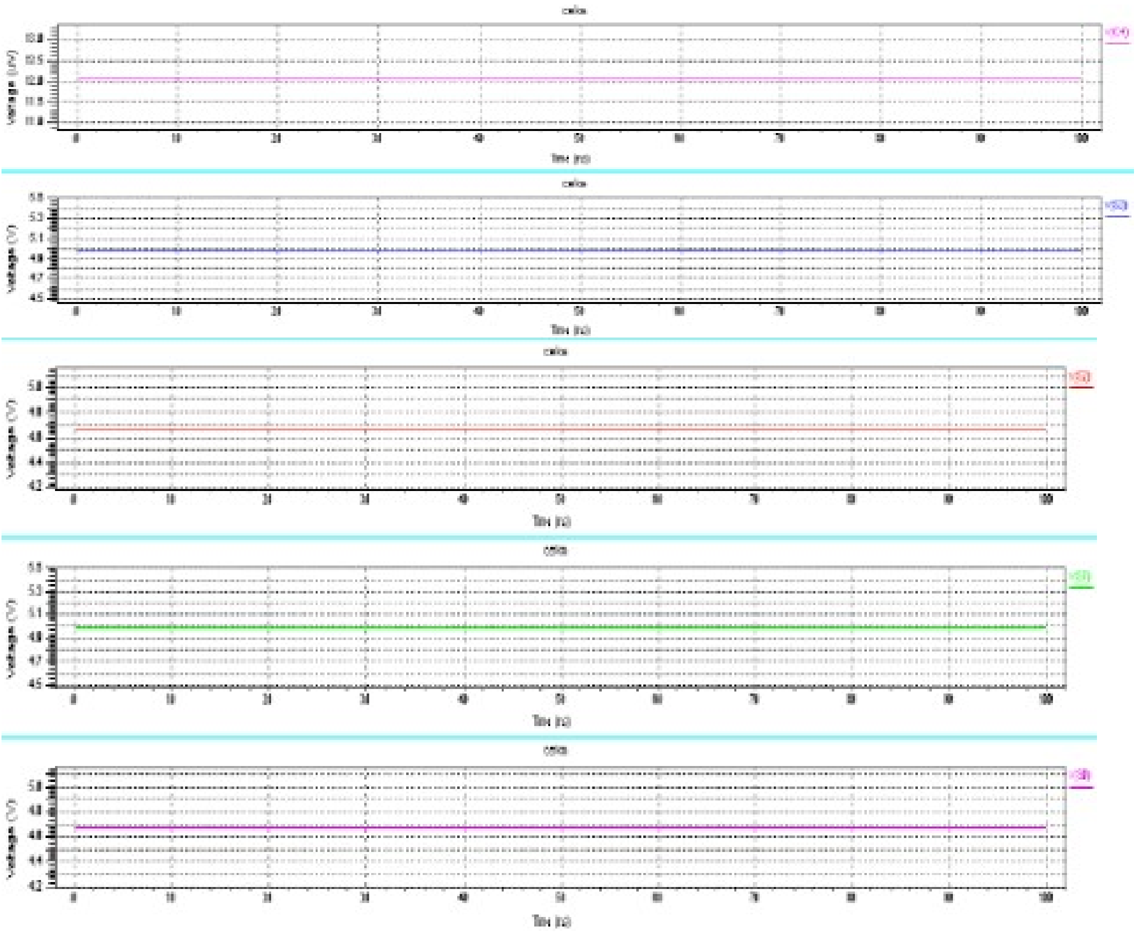
```
module tb_rca_4bit;

   reg  [3:0] A, B;

   reg  Cin;

   wire [3:0] Sum;

   wire Cout;


   rca_4bit dut (

      .A(A), .B(B), .Cin(Cin),

      .Sum(Sum), .Cout(Cout)

   );
```

```
  initial begin
    A = 4'b0101; B = 4'b0011; Cin = 0; #10;  // 5 + 3
    $display("A=%d B=%d Sum=%d Cout=%b", A, B, Sum, Cout);

    A = 4'b1001; B = 4'b0110; Cin = 0; #10;  // 9 + 6
    $display("A=%d B=%d Sum=%d Cout=%b", A, B, Sum, Cout);

    A = 4'b1111; B = 4'b0001; Cin = 0; #10;  // 15 + 1
    $display("A=%d B=%d Sum=%d Cout=%b", A, B, Sum, Cout);

    $finish;
  end
endmodule
```

Circuit



Output Wave Forms


Voltage (V)
Time (ns)