



Mo Tu We Th Fr Sa Su

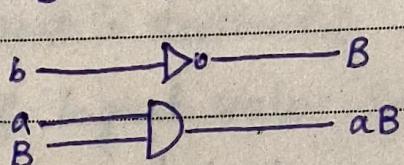
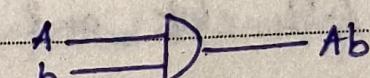
Memo No. _____

Date / /

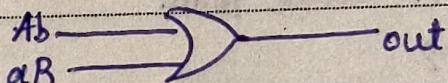
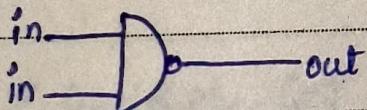
Project 1



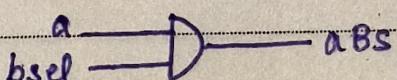
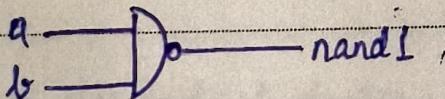
XOR:



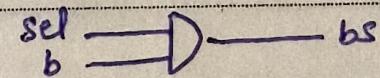
NOT:



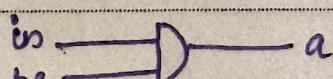
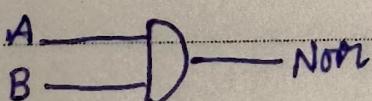
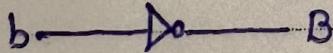
AND:



OR:



DMux:





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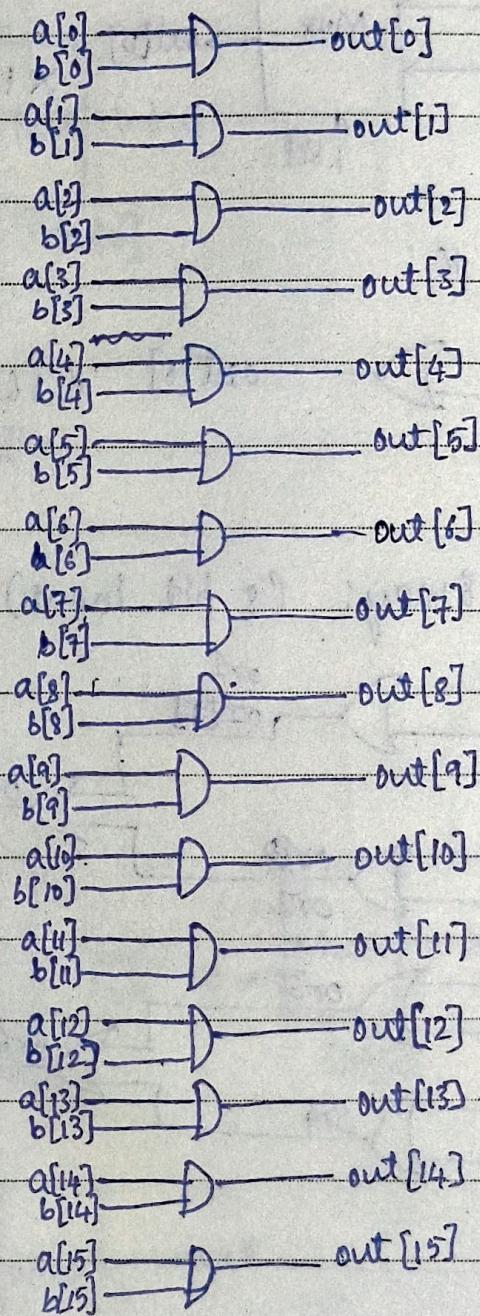
Memo No. _____

Date / /

Not 16

And 16

- in[0] → out[0]
- in[1] → out[1]
- in[2] → out[2]
- in[3] → out[3]
- in[4] → out[4]
- in[5] → out[5]
- in[6] → out[6]
- in[7] → out[7]
- in[8] → out[8]
- in[9] → out[9]
- in[10] → out[10]
- in[11] → out[11]
- in[12] → out[12]
- in[13] → out[13]
- in[14] → out[14]
- in[15] → out[15]



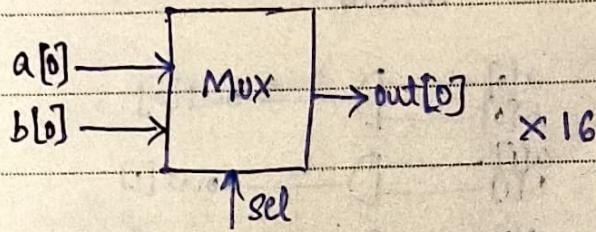


Mo Tu We Th Fr Sa Su

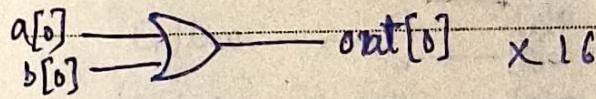
Memo No. _____

Date / /

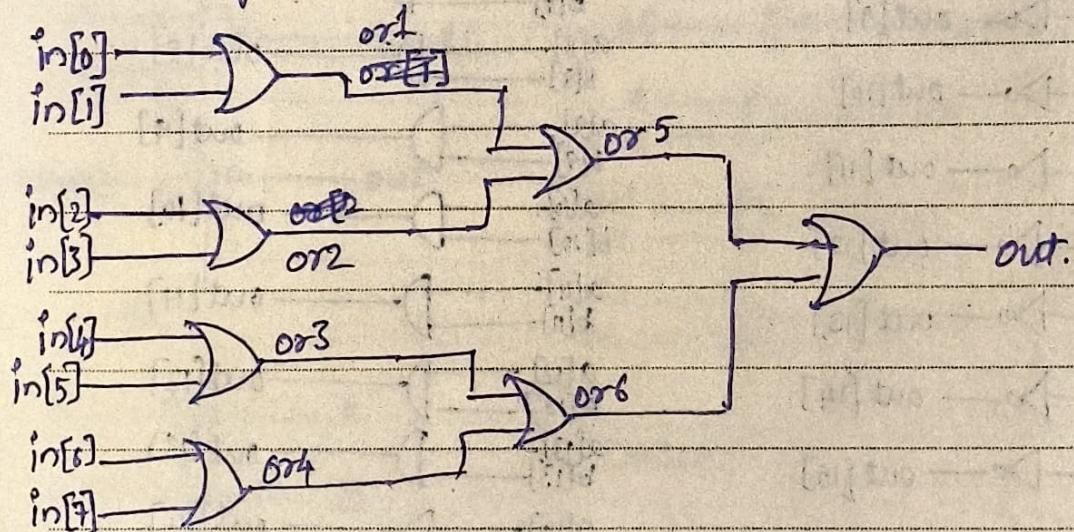
Mux 16:



Or 16:



Or 8 ways: (8 bit input)



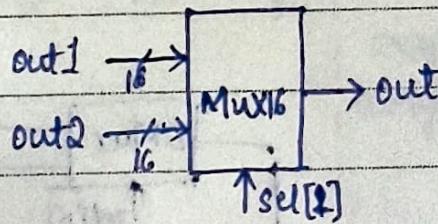
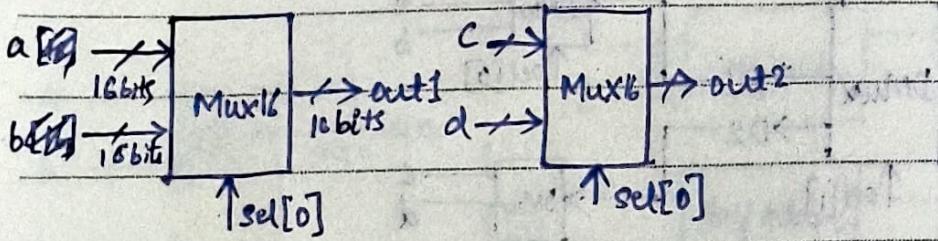


Mo Tu We Th Fr Sa Su

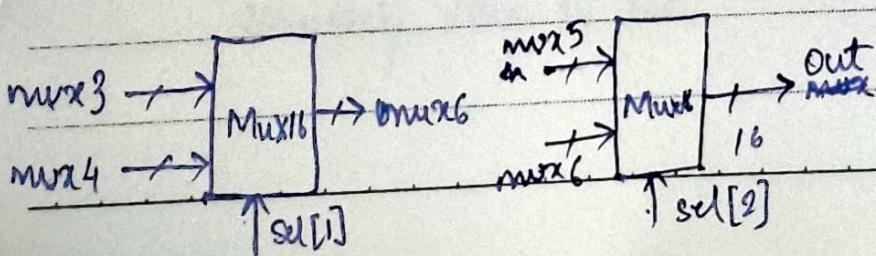
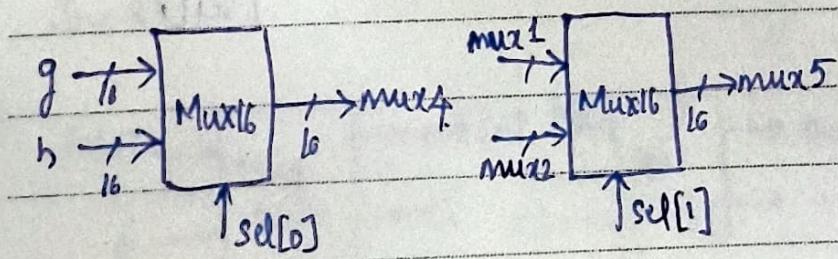
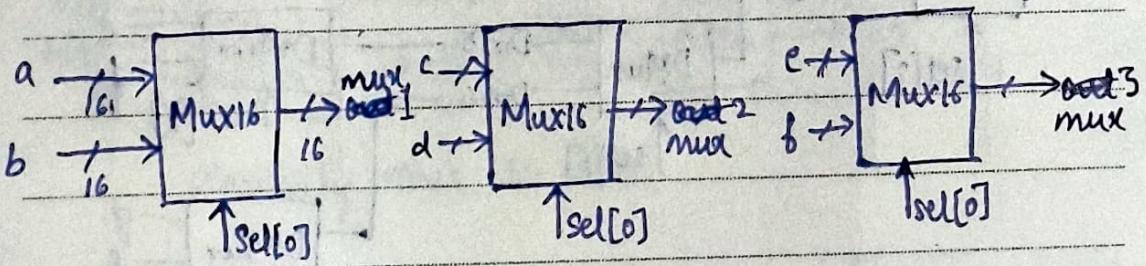
Memo No. _____

Date / /

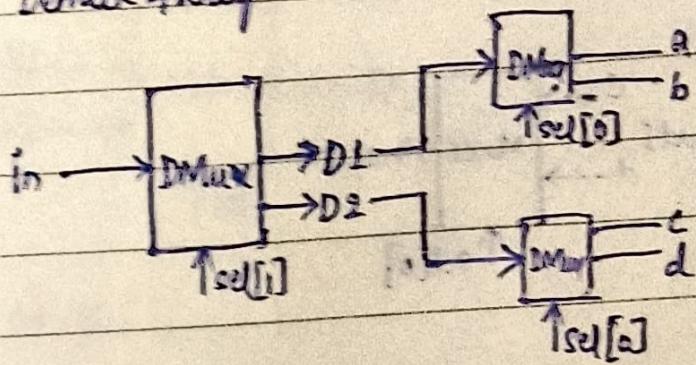
Mux4Way 16 :



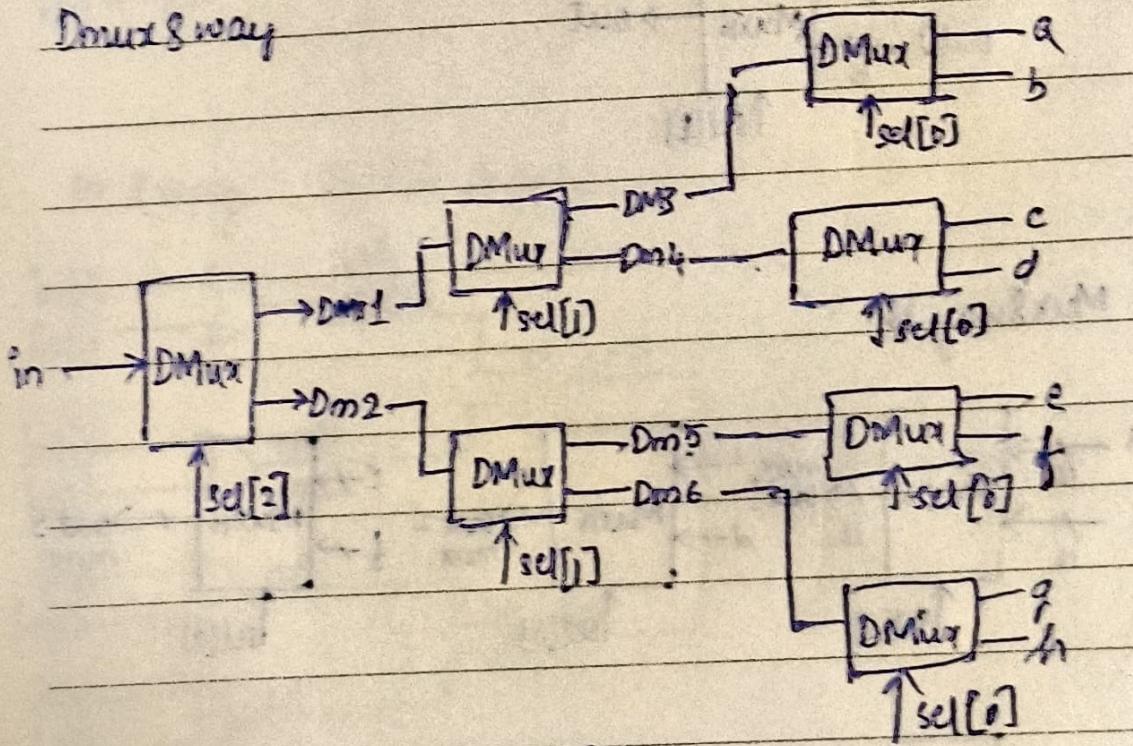
Mux8Way 16 :



Demand 4-way



Demand 8-way





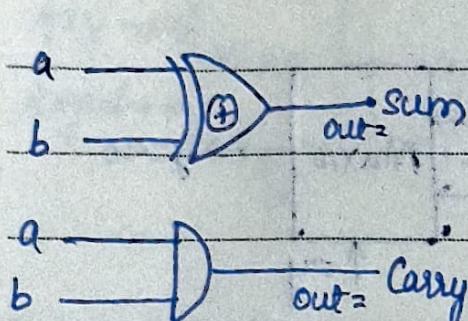
Mo Tu We Th Fr Sa Su

Memo No. _____

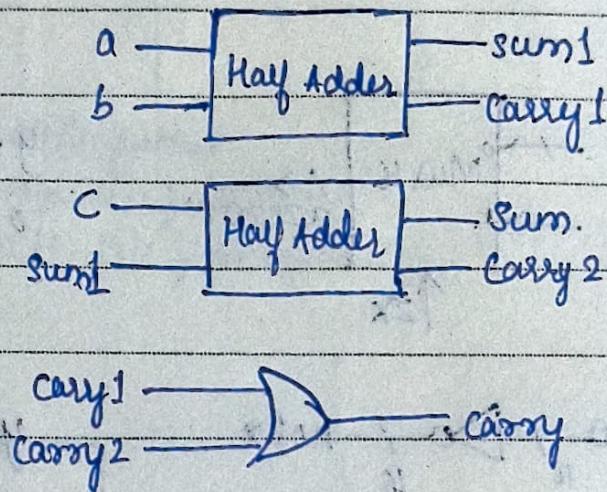
Date / /

Project 2

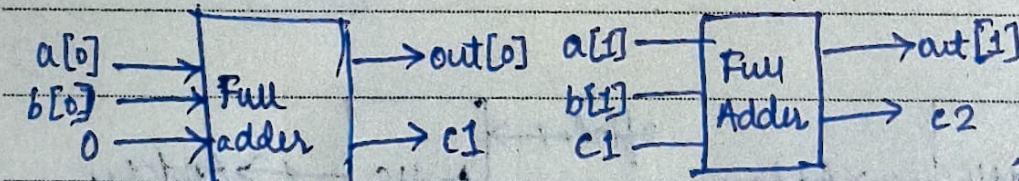
Half Adder:



Full Adder:

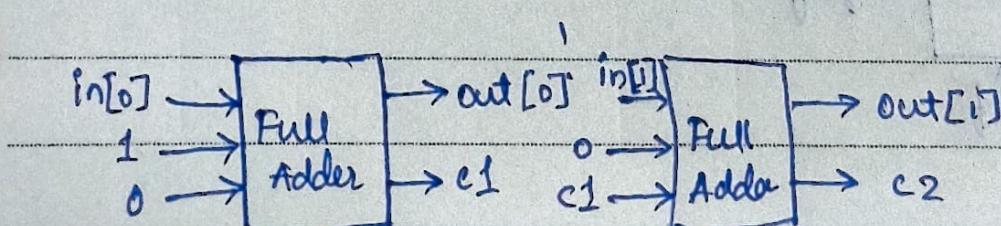


Add16



Similarly other 14 bits.

Inc16

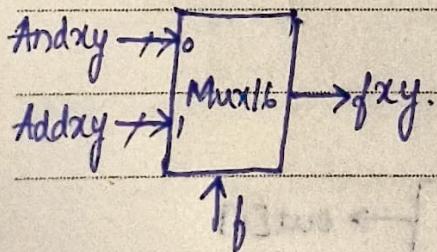
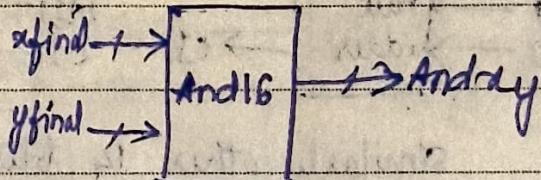
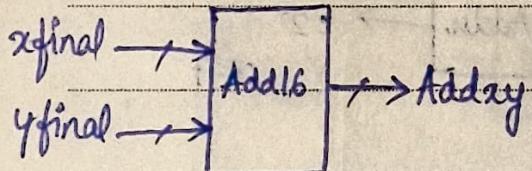
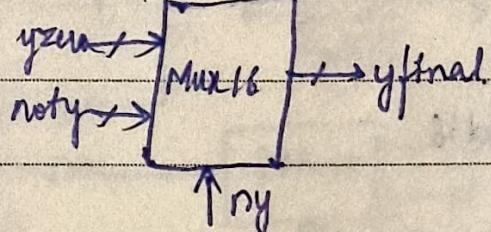
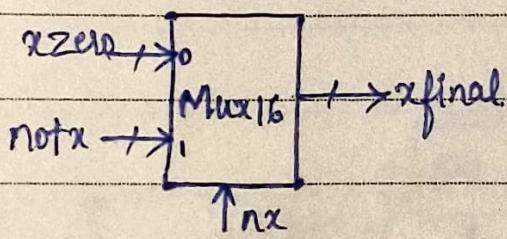
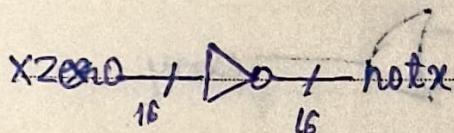
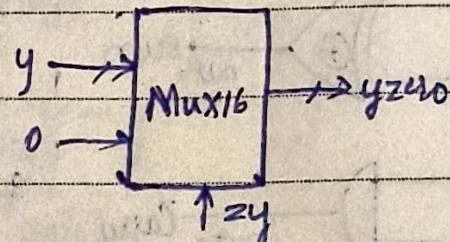
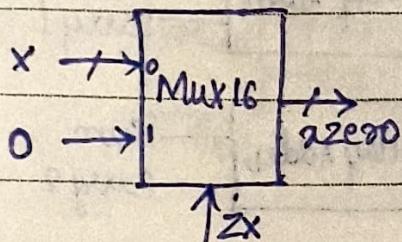


Similarly other 14 bits.

Mo	Tu	We	Th	Fr	Sa	Su

Memo No. _____

Date / /

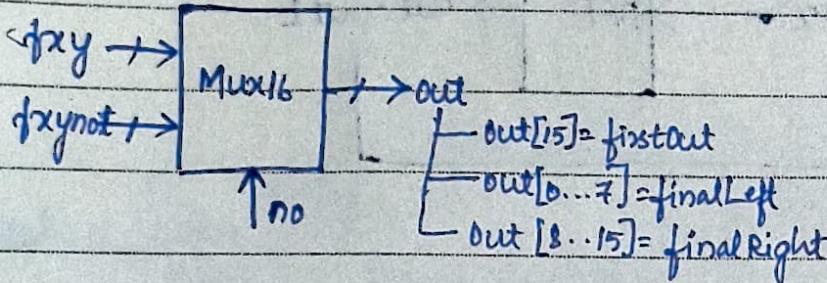
ALU



Mo Tu We Th Fr Sa Su

Memo No. _____
Date / /

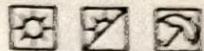
f_{xy} → Do → f_{xynot}



finalLeft → \oplus $\rightarrow z_{rl}$

final right → \oplus $\rightarrow z_{rr}$

firstout → \oplus $\rightarrow z_r$



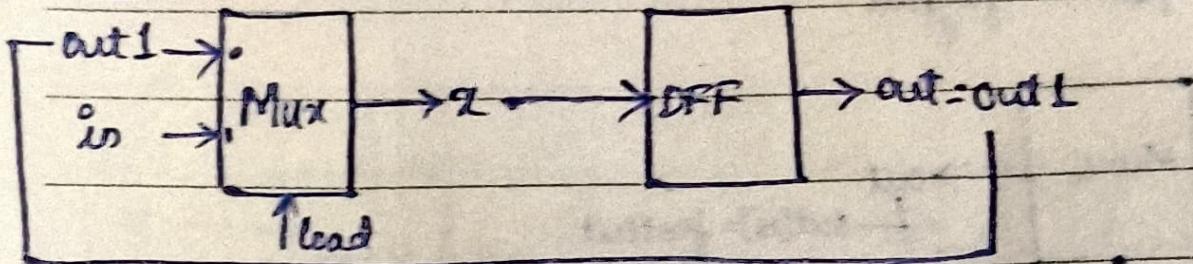
Mo Tu We Th Fr Sa Su

Memo No. _____

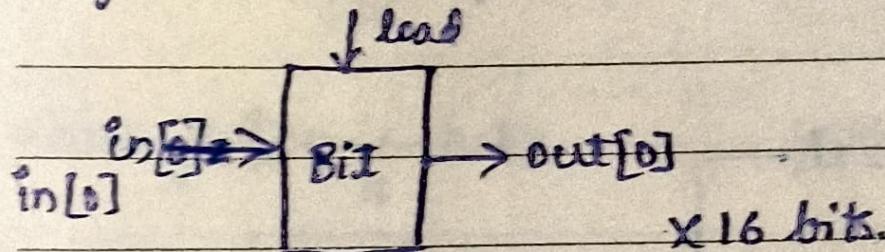
Date / /

Project 3

Bit:

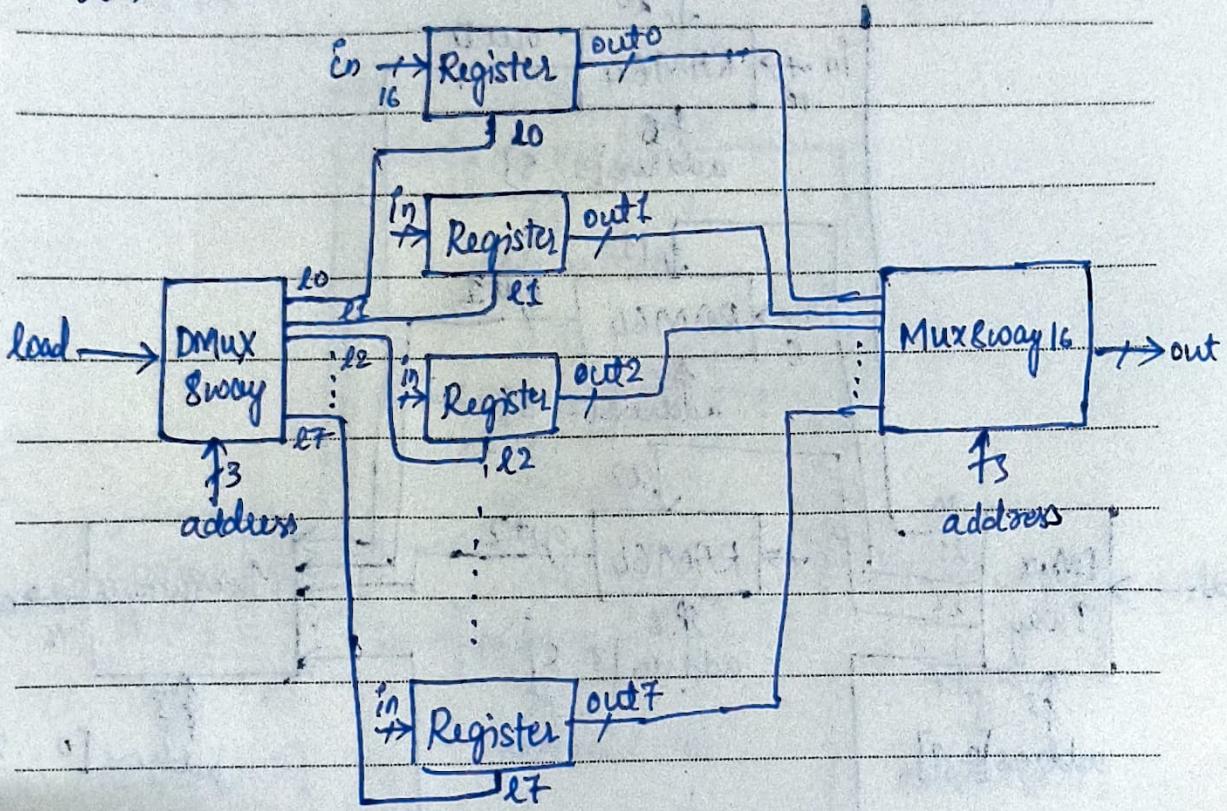


Registers 16 bit :

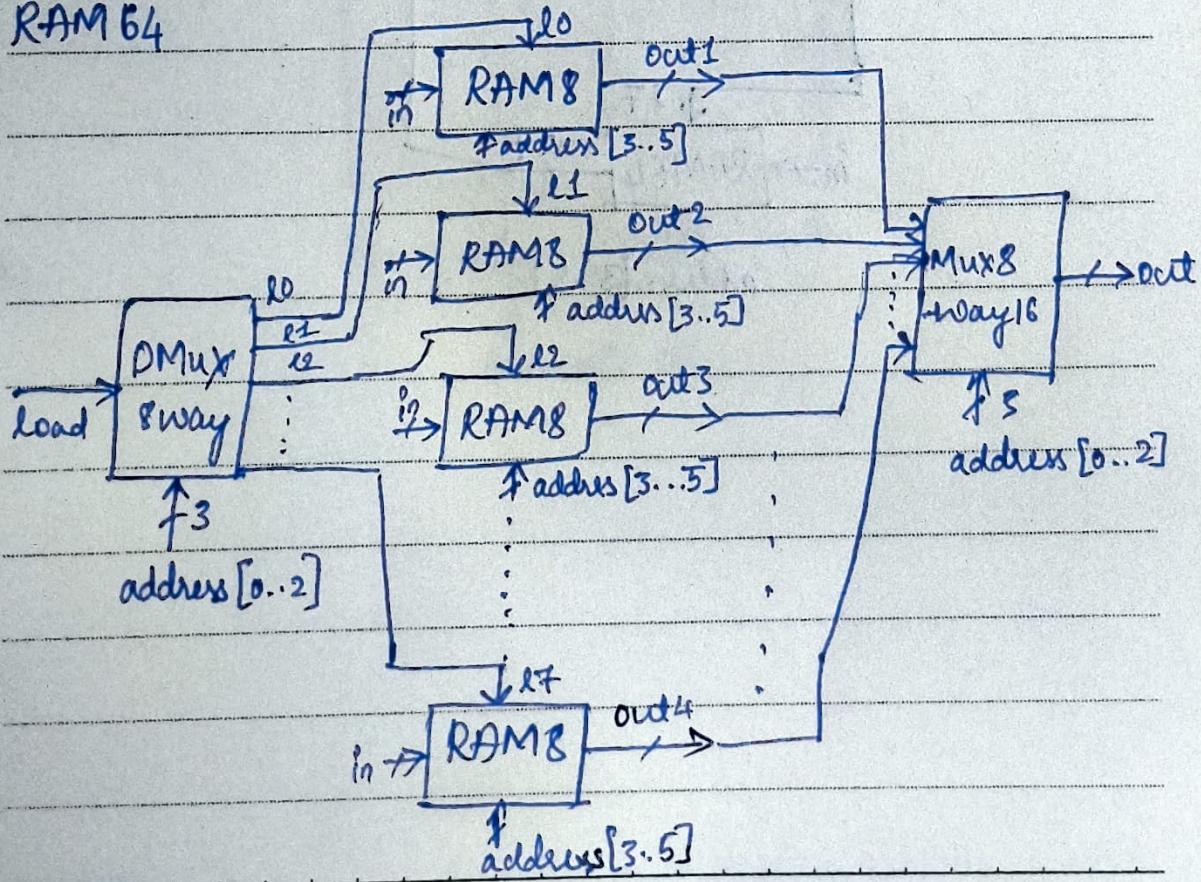


RAM8:

RAM8



RAM64



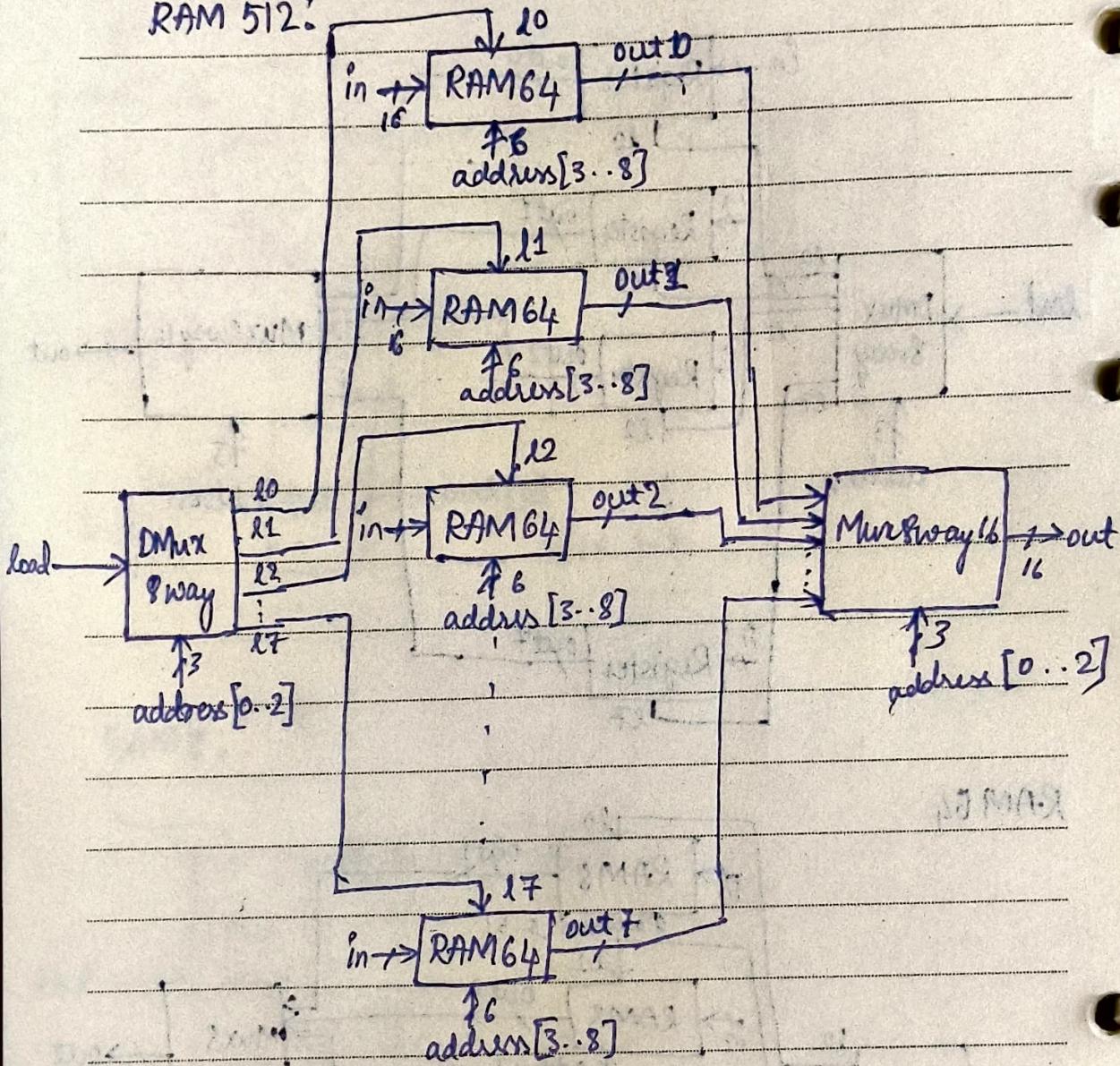


Mo Tu We Th Fr Sa Su

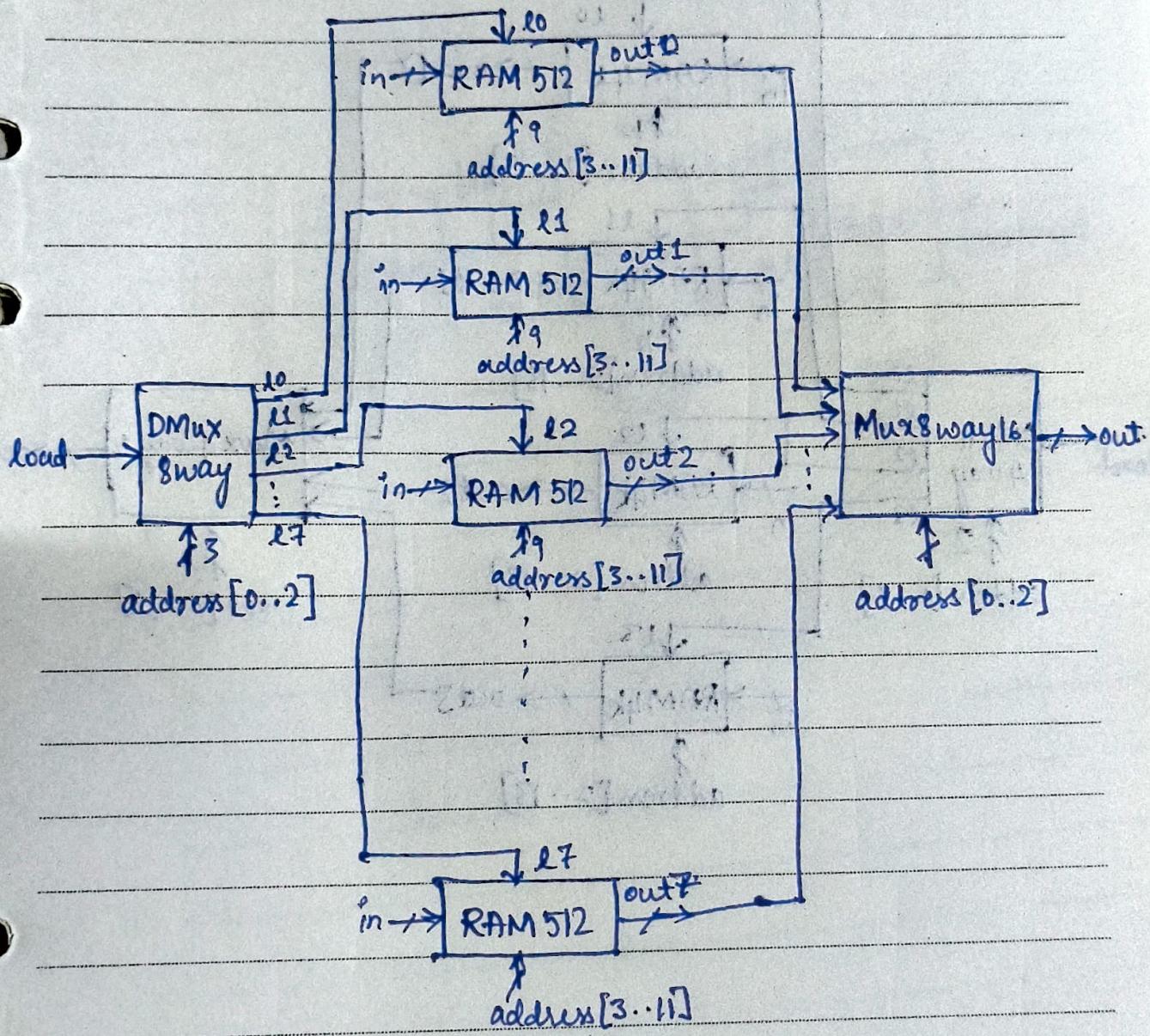
Memo No. _____

Date / /

RAM 512:



RAM 4K





Mo Tu We Th Fr Sa Su

Memo No. _____

Date / /

RAM16K

