Counters.

7A & 7B

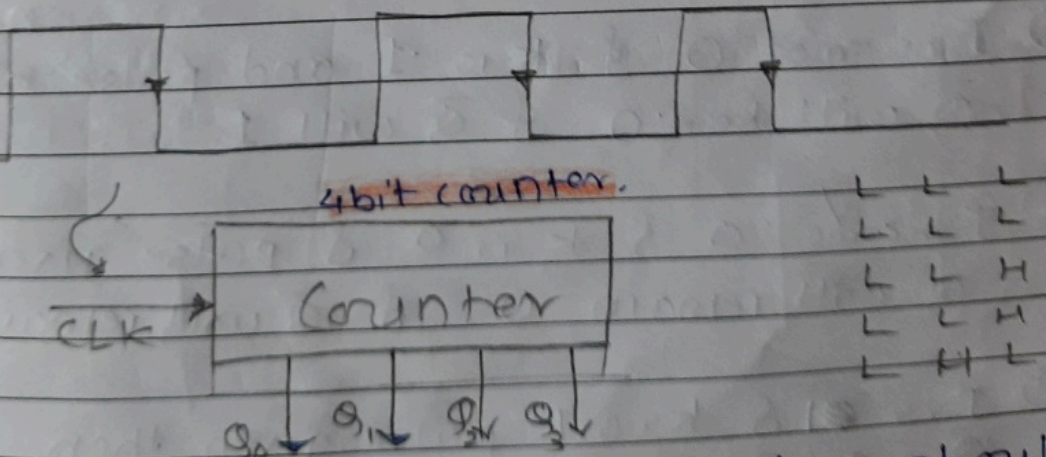
- For digital counting.
- Here, we have Binary numbering system, 0, 1
- In Binary, ~~up~~ sequence of upcounting & downcounting same.
- In given ~~eg~~.
  All zeroes advance to all ones in 2^n steps.

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
:	:	:	:
1	1	1	1

4 bits.

* Application.

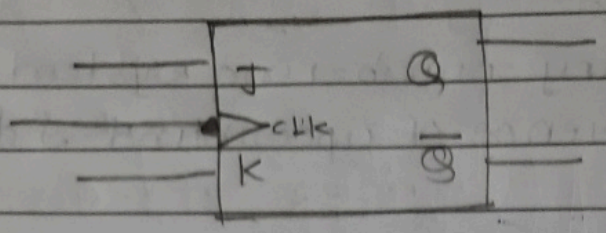
: At industry pens are moving on conveyor belt by using infrared sensors & LED displayed count



When one falling edge comes counter should move to next step.

initially output all is '0', (low) then ★

* M/slave.



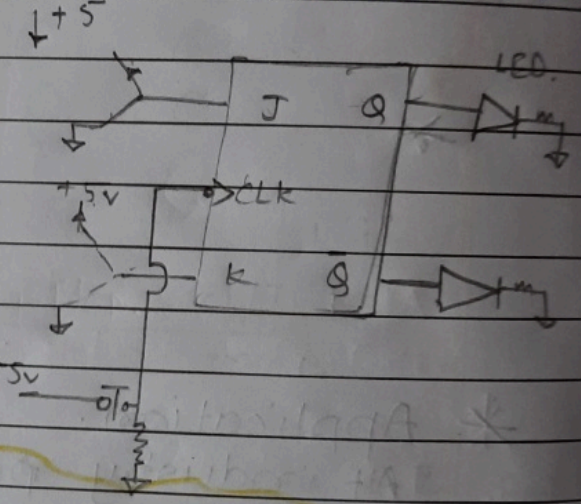
CLK	J	K	Q	$\overline{Q}$
0,1	X	X	LS	
↑↓	0	0	LS	
↑↓	0	1	0	1
↑↓	1	0	1	0
↑↓	1	1	Toggle	

- Whatever input at time of rising edge of JK Flipflop are consider master inside that is coppied by slave in falling edge.

For M/slave output (0,1) or (1,0) only

* For (1,1) input output is Toggle i.e $\overline{LS}$ (reverse of LS)

perfor exp.



IF

① J is 1 & K is 0 and pulse is given, then Q will 1 & $\overline{Q}$ will 0

② J is (become) 0 & K is 0 and Pulse is given, then Q will remain 1 & $\overline{Q}$ will remain 0.

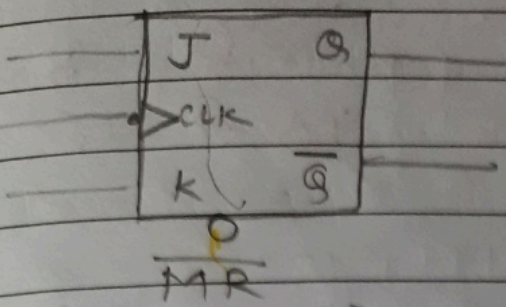
Output depends on previous state.

③ J become 0 & K is 1 and pulse given, then Q will become 0 & $\overline{Q}$ will 1

④ J become (is) 0 & K is 0 & pulse given then, Q will remain 0 & $\overline{Q}$ will remain 1

⑤ J is 1 & K is 1 pulse given then Q will invert to 1 & $\overline{Q}$ will invert to 0

⑥ J is 1 & K is 1 pulse given then, Q will invert again to 0 & $\overline{Q}$ to 1



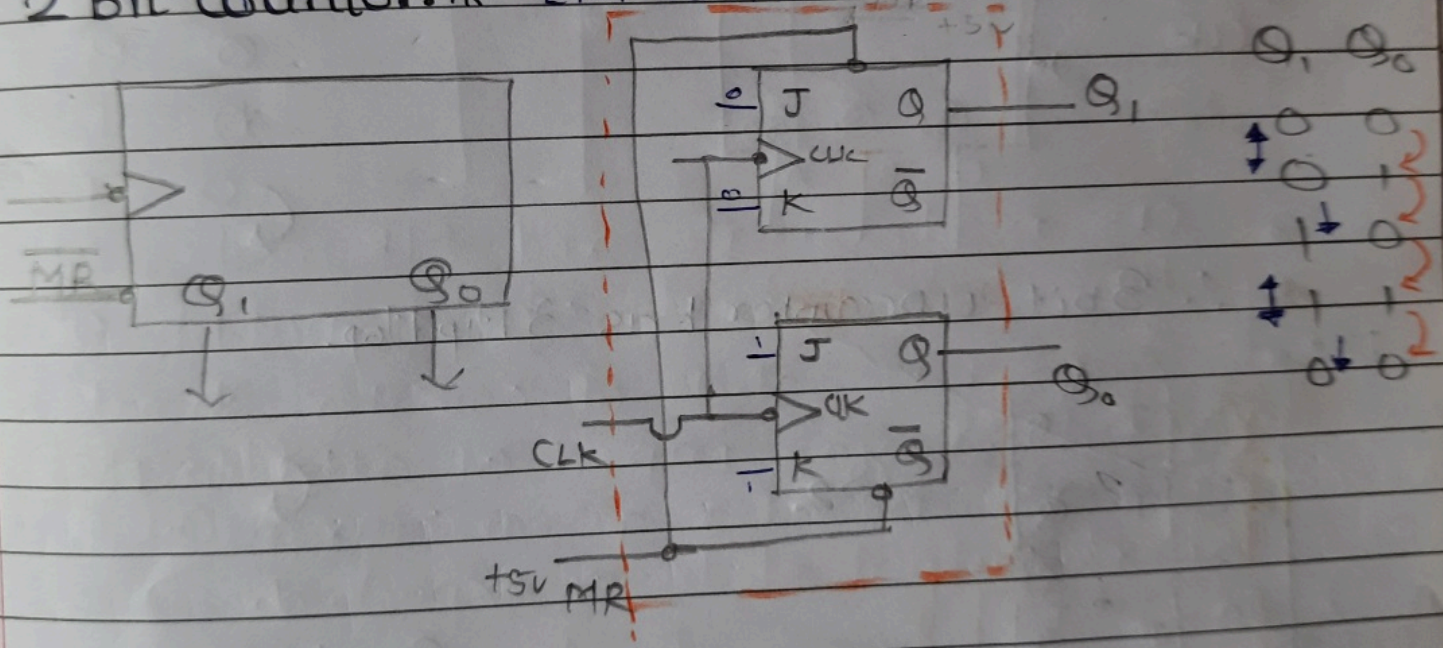
(Master reset)

is an overriding input over all combination.

It forces flip-flop to go to reset state.

$\overline{MR}$	CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$
0	X	X	X	0	1
1	0,1	X	X	LS	
1	↑↓	0	0	LS	
1	↑↓	0	1	0	1
1	↑↓	1	0	1	0
1	↑↓	1	1	$\bar{Q}_n$	Q_n
				Toggle	

* 2 bit Counter.* [For each bit - 1 Flip-Flop]



After each/every clock output must go on

Here Q_0 always toggle.

* ~~When Q_0 is changes to form 1 to 0~~.
* When Q_0 is 0 then next state of Q_1 is continuo
* When Q_0 is 0 then next state of Q_1 is toggling & If Q_0 is 1 then next state of Q_1 is

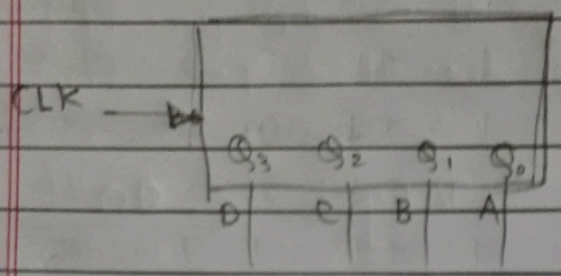
Input J, k, (0, 0) if want to conti.

(1, 1) ——— toggle.

8A & 8B

Design of Counters.

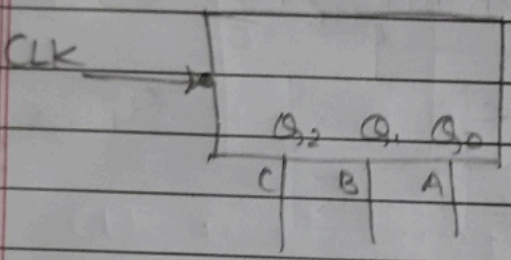
e.g 4 bit counter.



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
1	1	1	1

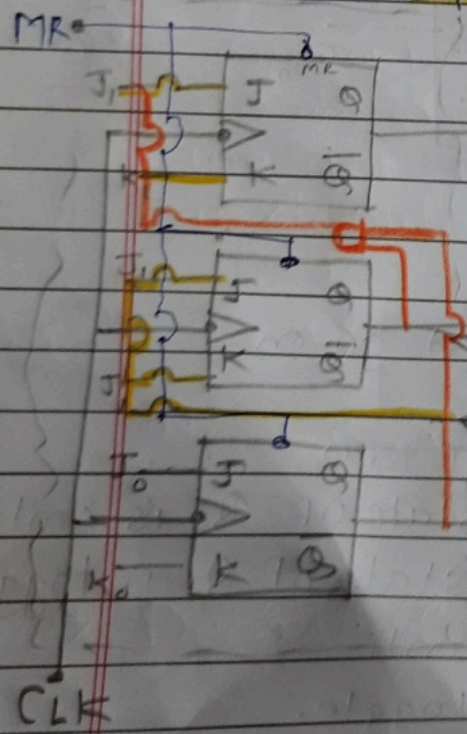
* In General.
n-bit Binary upcounter [UP-COUNTER.

* consider 3 bit counter



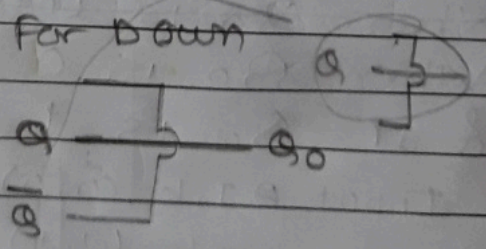
Q_2	Q_1	Q_0	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	
0	0	0	

∴ 3 bit upcounter has 3 Flip-flop.



Synchronous counter.
All Flip Flops in these driven by same CLK

For Down



- Here all clks are joined to make single CLK and Master resets of 3 flip-flops connected as one MR
- Design : Here we shall decide to give input J & K to these Flip-Flop such that required output is observed.

Now How $J_2, K_2, J_1 K_1, J_0 K_0$ is given to give output as given $Q_2, Q_1 Q_0$.

- In every next state output Q_0 is always toggles
Hence for toggline $J_0 = 1$ & $K_0 = 1$

Now,

- Next state of Q_1 depend on Q_0 (current state)
If Q_0 is 0 then next state of Q_1 is continuous
If ⎍ 1 then ⎍ Q_1 is toggle (change)
Q_0 direct connect to J_1, K_1
(output) ((common input of FF1)

Hence, $J_1 K_1$ / $Q_0 Q_0$

IF $Q_0 = 0$ $Q_1 = 0$
$Q_0 = 1$, continue $Q_1 = 0$
$Q_0 = 0$ toggle $Q_1 = 1$

- Deciding for FF 2 see output of Q_1 & Q_0 FF 2 toggles when output of Q_1 & Q_0 both 1
- Put ⇒ AND Gate betn Q_1, Q_0 & J_2, K_2 we can. ~~J_2 ~~K_2~~ K_2~~
$Q_1 Q_0$ $Q_1 Q_2$

J_0	K_0	J_1	K_1	J_2	K_2
1	1	Q_0	Q_0	$Q_1 Q_0$	$Q_0 Q_1$

* 3 Bit. [DOWN COUNTER]

What input.

J_0	K_0	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0	
1	1	$\bar{Q}$	$\bar{Q}$	$\bar{Q}_1 \bar{Q}_0$		1	1	1	2 DOWN
						1	1	0	
						1	0	1	
						1	0	0	
						0	1	1	
						0	1	0	
						0	0	1	
						0	0	0	

AS Reverse UP-counter.

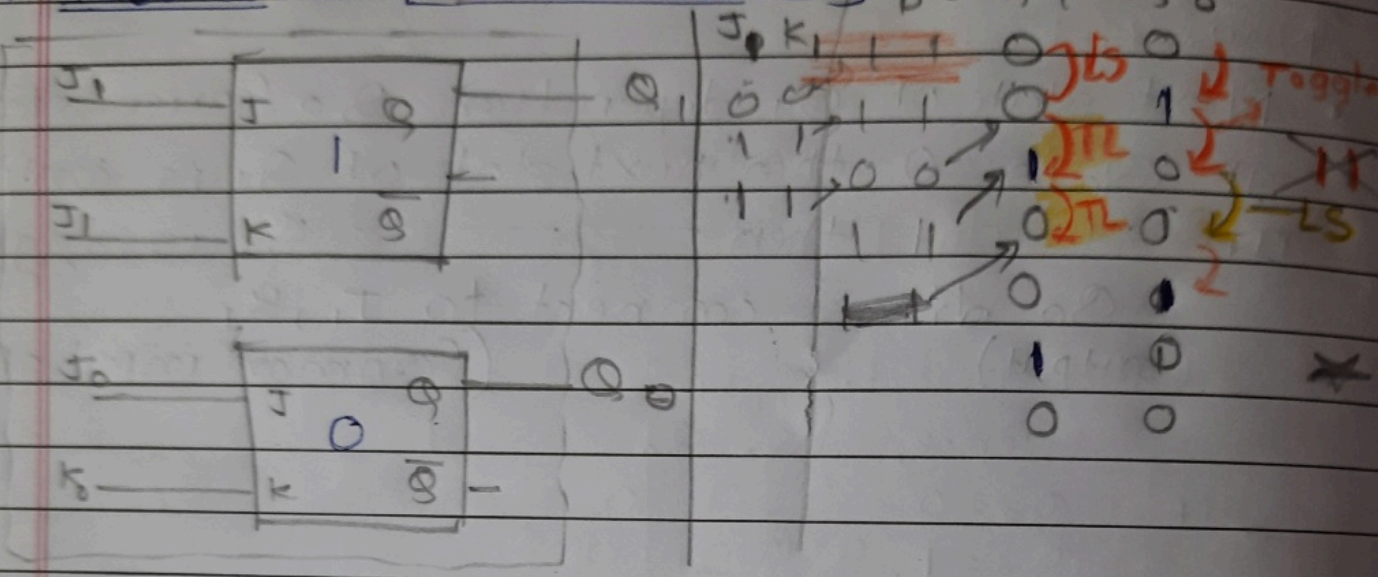
Conditions: If Q_0 0 then next state of Q_1 is toggle.
If Q_1, Q_0 is 0 then toggling for Q_2.

Design

* Decade counter — (has 10 states)

(2) n-bit Using 4 bits 16 states possible but not use of all uses only 10 states

* MOD-3 ~~coun~~ [UP COUNTER]



- CLK made single and MR make single of all.
- Here Output decide what input should be.
- Current ~~+~~ state of counter should be used to determine input of all flip flop hence we get ~~nex~~ for given current state we get next output state as expected.

J_0	K_0	J_1	K_1	Q_1	Q_0
$\overline{Q_1}$	$\overline{Q_0}$	$Q_1 \cdot \overline{Q_0}$	$\overline{Q_1} \cdot Q_0$		

Here ~~Q~~ when Q_1 is 0 then Q_0 toggle & ~~—~~ Q_1 is 1 ~~+~~ Q_0 continue.

* Decade Counter [10 state)

J_0	K_0	J_1	K_1	J_2	K_2	J_3	K_3
1	1	$Q_3(\overline{Q_3}\,\overline{Q_2}\,\overline{Q_1})$		$Q_1 Q_0$			

	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

$J_1 \; ? \; K_1 = Q_0$ $\quad Q_3 Q_2 Q_1$ should not be $1\,0\,0 \Implies$

$J_1 \& K_1 = 0$ when either

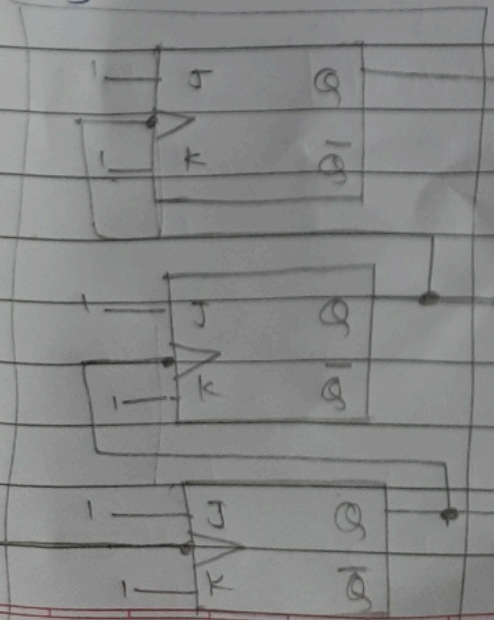
$Q_0 = 0$ or $Q_3 Q_2 Q_1 = 100$

$J_1 \& K_1 = Q_0 \cdot (\overline{Q_3 \cdot \overline{Q_2} \cdot \overline{Q_1}})$ → is 0 when $Q_3 Q_2 Q_1 = 100$

$J_3 \& K_3 = Q_2 Q_1 Q_0 + Q_3 \cdot Q_0$

$= Q_0 \cdot (Q_2 \cdot Q_1 + Q_3)$

* Asynchronous counter.



Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0