EXPERIMENT NO.5

Title of experiment: To design a encoder and decoder in Proteus.

Equipments required: Proteus 8

Theory

1)**Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

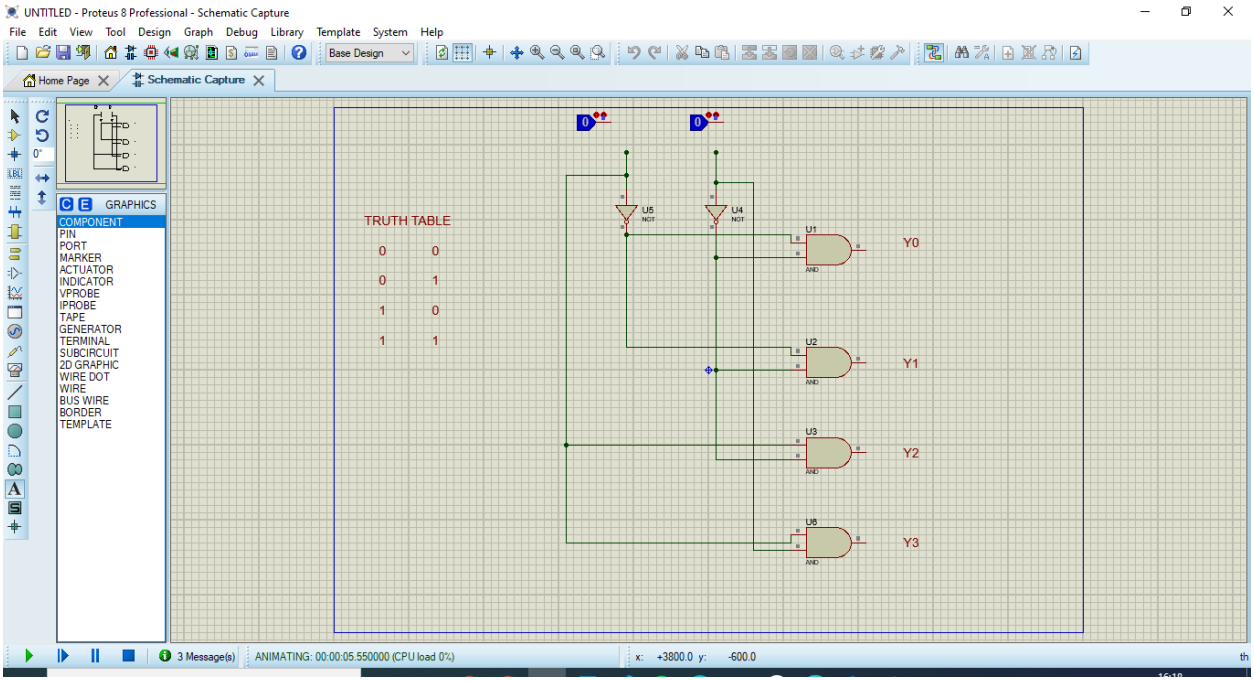
2) The **decoder** is an electronic device that is used to convert a digital signal to an analog signal. It allows a single input line and produces multiple output lines. The decoders are used in many communication projects that are used to communicate between two devices. The decoder allows N- inputs and generates 2 power N-numbers of outputs. For example, if we give 2 inputs that will produce 4 outputs by using 4 by 2 decoders.

Implementation:

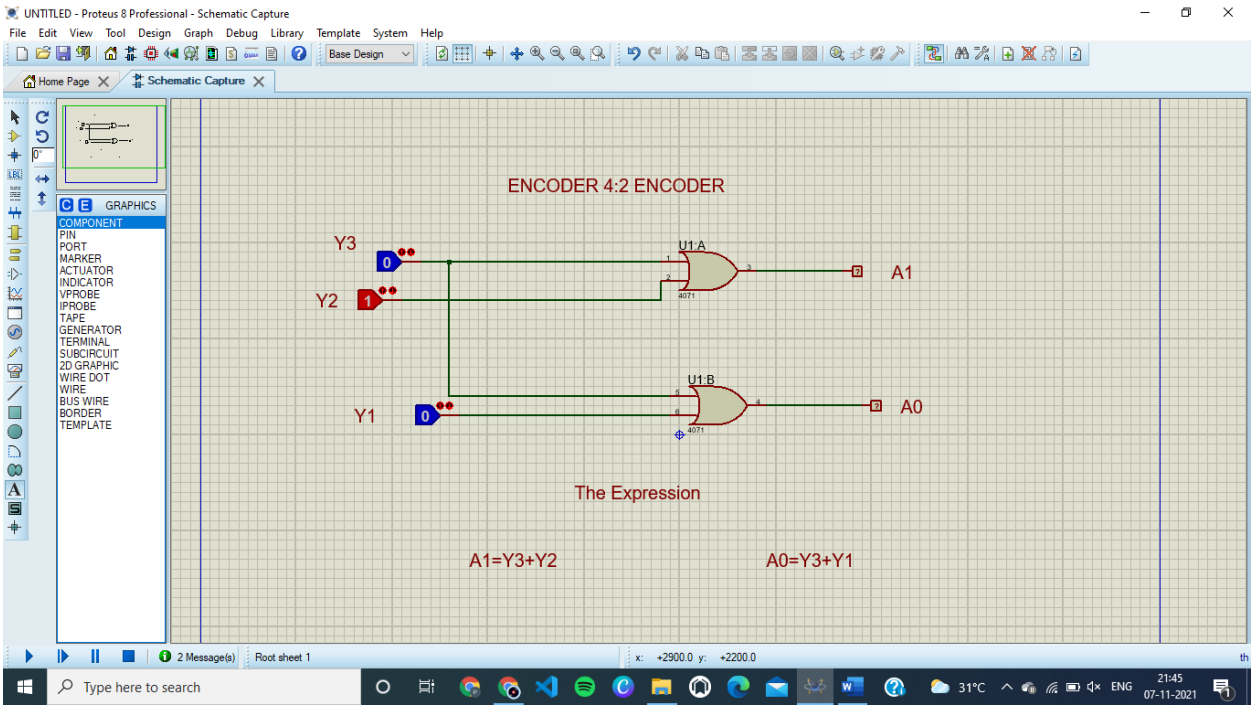
1)The AND gate(4081),OR gate(4071),NOR(74S02),XOR(4030), NOT gate,NAND(4011) are library devices used show the working of the data in Proteus 8 software
2)Logicstate,logicprobe devices are used to fetch output of logic gates.

Snapshots

Decoder



Encoder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GRAPHICS
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GENERATOR
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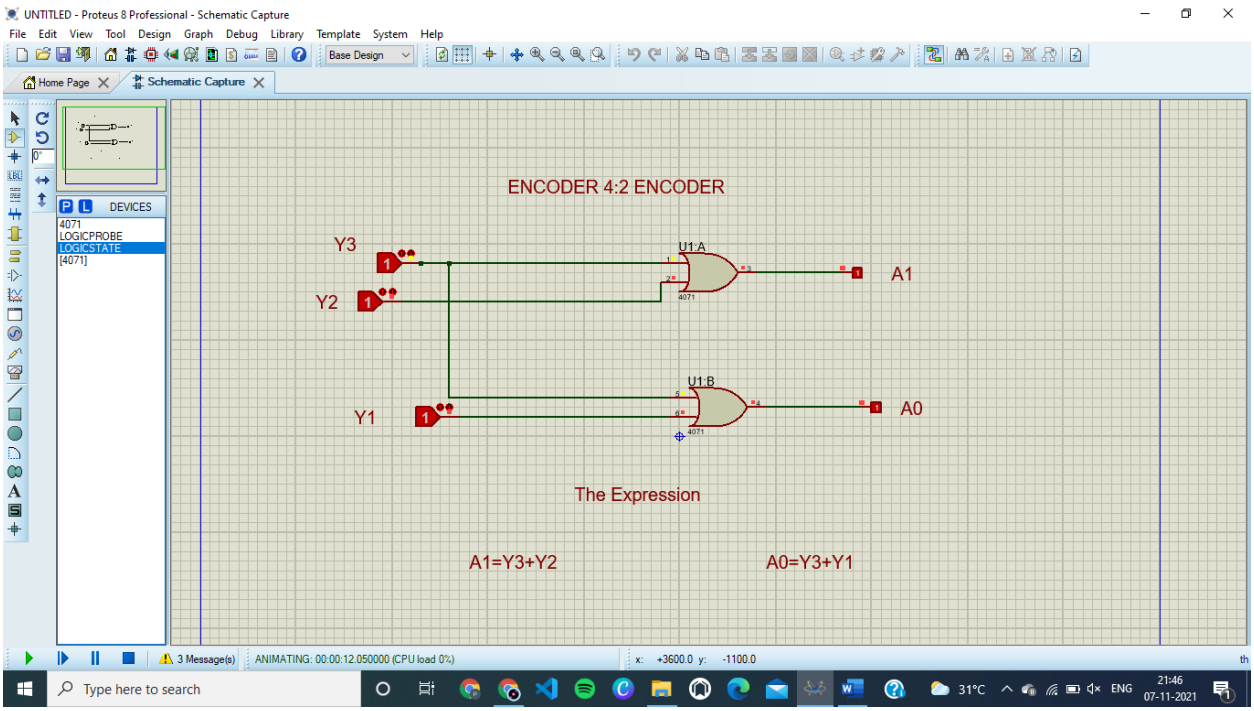
SUBCIRCUIT
2D GRAPHIC
WIRE DOT
WIRE
BUS WIRE
BORDER
TEMPLATE
ENCODER 4:2 ENCODER
Y3
Y2
Y1
U1:A
U1:B
A1
A0
The Expression
A1=Y3+Y2
A0=Y3+Y1
2 Message(s)
Root sheet 1
Type here to search
31°C
ENG
21:45
07-11-2021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Schematic Capture
DEVICES
4071
LOGICPROBE
LOGICSTATE
[4071]
ENCODER 4:2 ENCODER
Y3
Y2
Y1
U1:A
U1:B
A1
A0
The Expression
A1=Y3+Y2
A0=Y3+Y1
3 Message(s)
ANIMATING: 00:00:12.050000 (CPU load 0%)
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ENG
21:46
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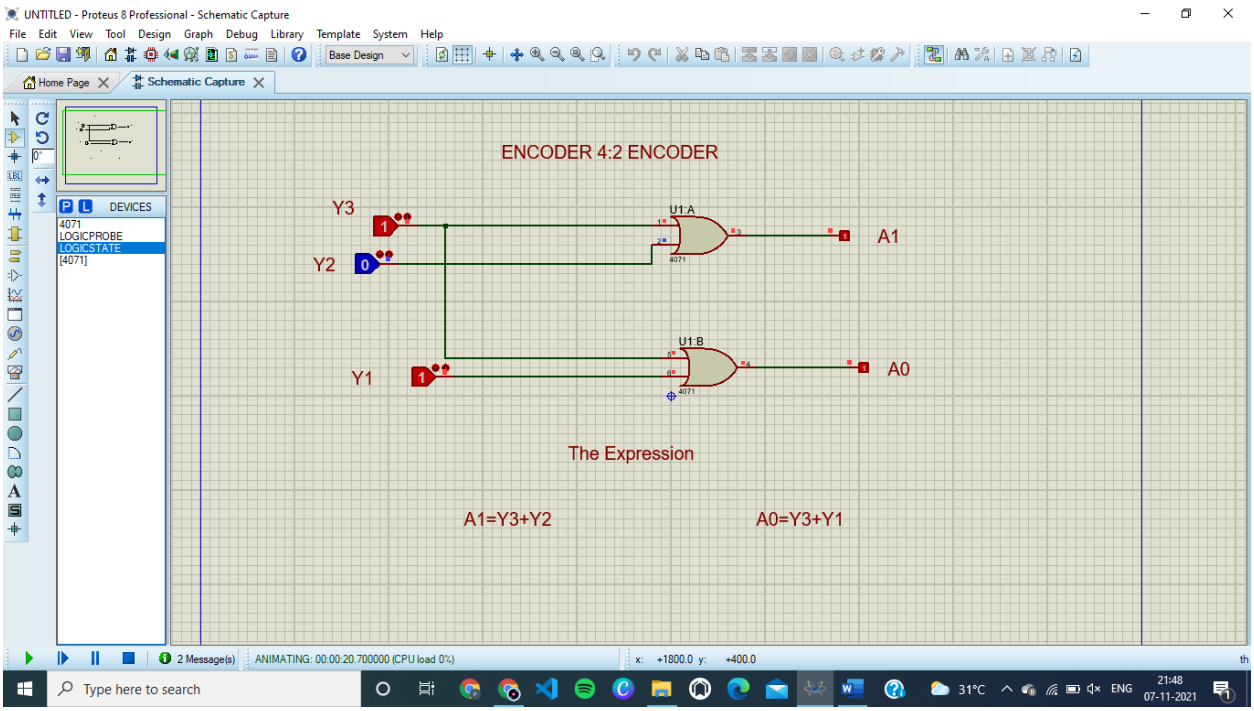

Conclusion

This is demonstration for encoder and decoder in digital circuits in Proteus.