4-bit Synchronous Up Counter:

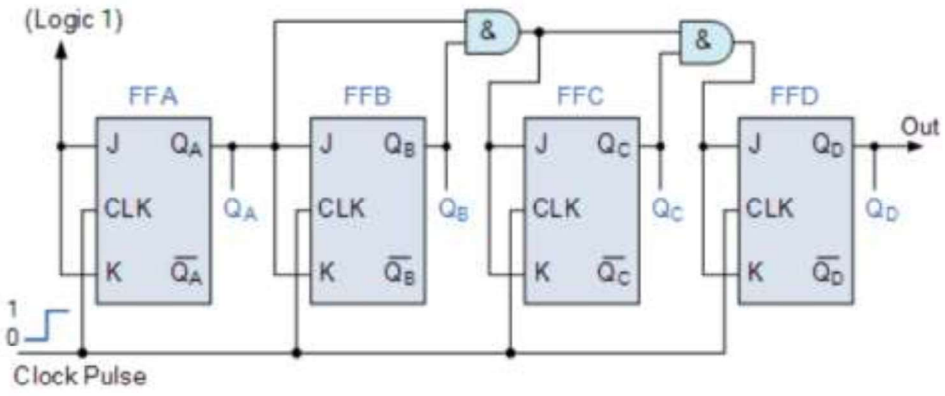
- A 4-bit Synchronous up counter start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then start new counting cycle by getting reset.
- Its operating frequency is much higher than same range Asynchronous counter.
- Also, there is no propagation delay in synchronous counter just because all flip-flops or counter stage is in parallel clock source and clk triggers all counters at the same time.
- The external clock signal is connected to clock input of every individual flip-flop within counter so that all of flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship.
- Changes in the output occur in "synchronisation" with the clock signal.
- Result of this synchronisation is that all individual output bits changing state at exactly same time in response to common clk signal with no ripple effect and hence no propagation delay.

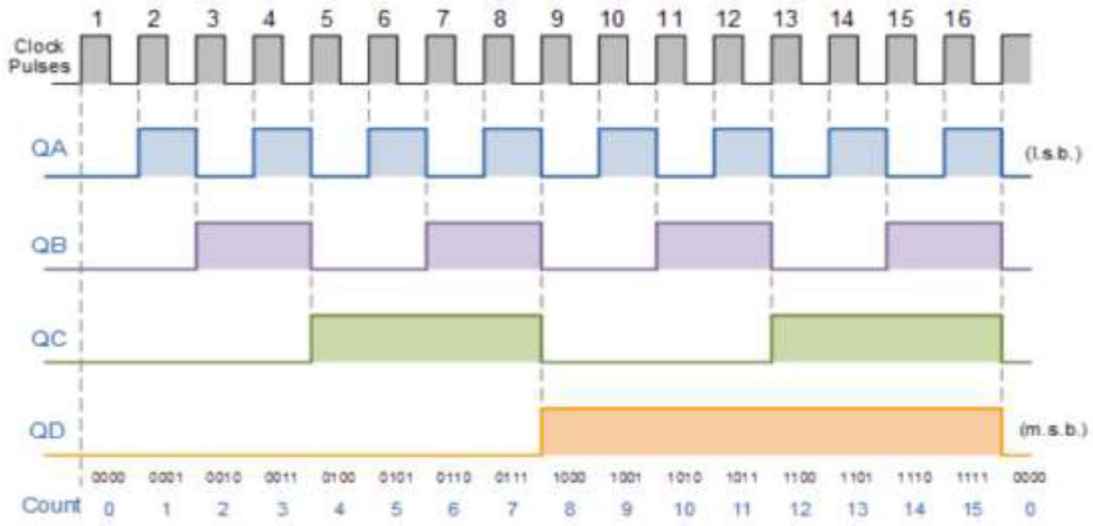
The external clock pulses are fed directly to each of the JK flipflop in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in first flip-flop, flip-flop FF-A (LSB) are they connected High, logic 1 allowing the flip-flop to toggle on every clock pulse. Then synchronous counter follows a predetermined sequence of states in response to common clock signal, advancing one state for each pulse.

The J, K inputs of flip-flop FF-B are connected directly to output Q_A of flip-flop FFA, but the J, K inputs of flip-flops FF-C and FF-D are driven from separate AND gates which are also supplied with signals from input-output of previous stage. These additional AND gates generate required logic for the JK inputs of the next stage.

If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are High we can obtain same counting sequence as with asynchronous circuit but without ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.

Then as there is no inherent propagation delay in synchronous counters, because all counter stages are triggered in parallel at the same time, maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.



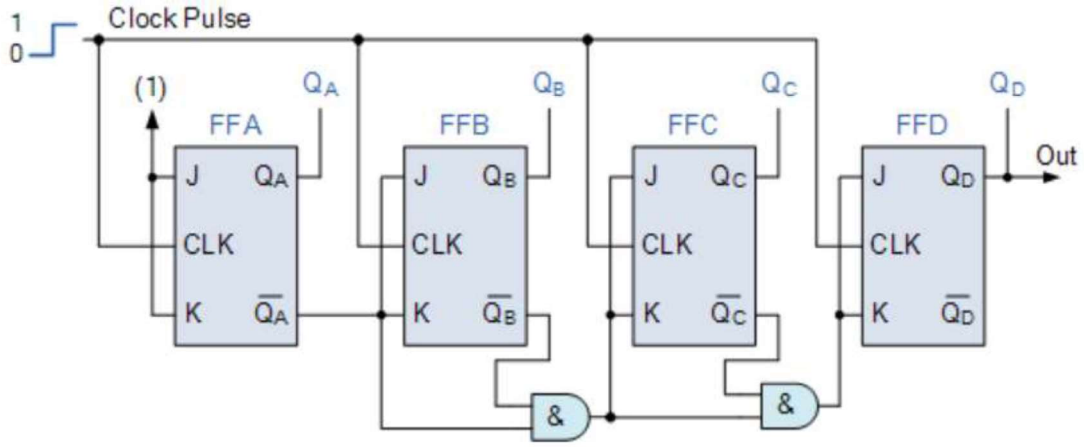


Because this 4-bit synchronous counter counts sequentially on every clock pulse resulting outputs count upwards from 0 (0000) to 15 (1111). Therefore, this type of counter is also known as a 4-bit Synchronous Up Counter.

However, we can easily construct a 4-bit Synchronous Down Counter by connecting AND gates to Q output of flip-flops as shown to produce a waveform timing diagram reverse of the above. Here counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again.

Synchronous Down Counter:

- It starts to count from 15 (1111 in binary) and decrement or count downwards to 0 or 0000 and after that it will start new counting cycle by getting reset.
- The AND Gate input is changed. First Flip-flop FFA input is same as we used in previous Synchronous up counter.
- Instead of directly feeding output of first flip-flop to next subsequent flip-flop, we are using inverted output pin which is used to give J and K input across next flip-flop FFB and also used as input pin across AND gate.
- Same as like previous circuit, two AND gates are providing necessary logic to next two Flip-flops FF-C and FF-D.



Modulus-N Counters

- Modulus Counters, or simply MOD counters, are defined based on number of states that counter will sequence through before returning back to its original value.
- For example,
  a 2-bit counter that counts from 00_2 to 11_2 in binary, that is 0 to 3 in decimal, has a modulus value of 4 ($00 \rightarrow 1 \rightarrow 10 \rightarrow 11$, and return back to 00) so would therefore be called a modulo-4, or mod-4, counter. Note that it has taken four clock pulses to get from 00 to 11.
- As in this example there are only two bits, (n = 2) then the maximum number of possible output states (maximum modulus) for the counter is: $2^n = 2^2$ or 4.
- Therefore, a Mod-N counter will require N number of flip-flops connected together to count a single data bit while providing 2^n different output states, (n is the number of bits).

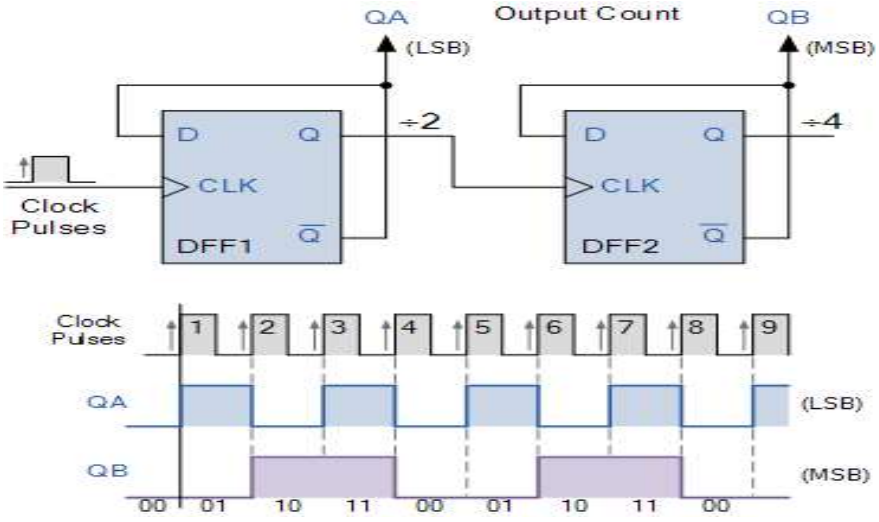
Types of Modulo-N Counter

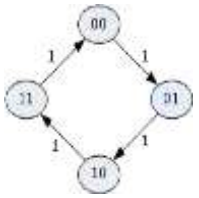
- **Modulo - 2 counter:**

Technically as well as being a 1-bit storage device, a single flip-flop on its own could be thought of as a MOD-2 counter, as it has a single output resulting in a count of two, either 0 or 1, on application of clock signal. But a single flip-flop on its own produces a limited counting sequence, so by connecting together more flip-flops to form a chain, we can increase the counting capacity and construct a MOD counter of any value.

- **Modulo - 4 Counter:**

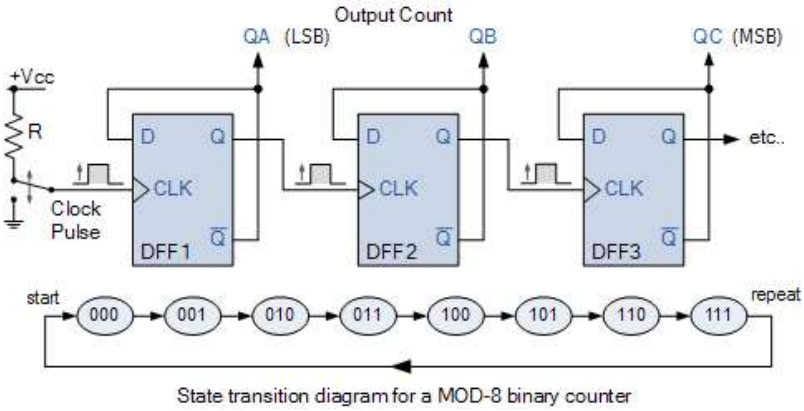
If a single flip-flop can be considered as MOD-2 counter, then adding a second flip-flop would give us a MOD-4 counter allowing it to count in four discrete steps. Overall effect would be to divide original clock input signal by four. Then binary sequence for this 2-bit MOD-4 counter would be: 00, 01, 10, and 11 as shown.



Lock pulse	Present state		Next state		State diagram
0 (start)	0	0	0	1	
1	0	1	1	0	
2	1	0	1	1	
3	1	1	0	0	
4 (repeat)	0	0	0	1	

- **Modulo – 8 Counter:**

By adding another flip-flop onto the end of a MOD-4 counter to produce a MOD-8 counter giving us a 2^3 binary sequence of counting from 000 up to 111, before resetting back to 000. A fourth flip-flop would make a MOD-16 counter and so on, in fact we could go on adding extra flip-flops for as long as we wanted



State transition diagram for a MOD-8 binary counter

- **Modulo - 5 counter:**

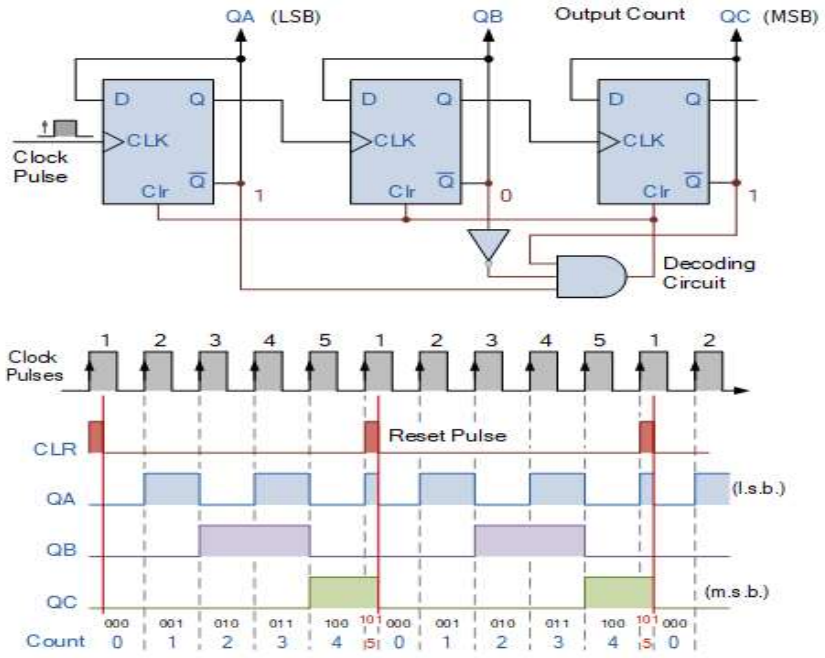
As we want to construct a MOD-5 counter, we need to modify the 3-bit (Mod-8) counter circuit so that it will reset itself back to zero after a count of 5. That is a count sequence of: 1→2→3→4→5→reset, and so on.

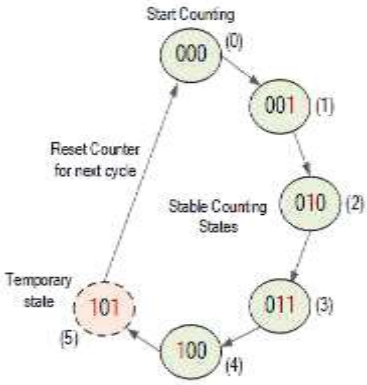
We can decode this output state of 101 (5) to give us a signal to clear (clr) the counter back to zero with the help of a 3-input AND gate and an inverter or NOT gate.

The output of the 3-input AND gate will therefore be at logic level 0 for any combinations of inputs, other than input sequence we want.

While it appears that counter counts up to 101 state, when asynchronous count sequence reaches next binary state of 101 (5), combinational logic decoding circuit will detect this 101 condition, so the AND gate will produce logic level 1 output resetting the counter back to its initial zero state. Thus, counter only remains in this 101 temporary state for only a few nanoseconds before it resets back to 000.

When the output from decoding circuit is LOW, it has no effect on the counting sequence.





- **Modulo – 10 Counter:**

  It is an example of a modulo-m counter circuit which uses external combinational circuits to produce a counter with a modulus of 10 is Decade Counter.

  Decade (divide-by-10) counters, have 10 states in its counting sequence making it suitable for human interfacing where a digital display is required.

  The decade counter has four outputs producing a 4-bit binary number and by using external AND and OR gates we can detect occurrence of 9th counting state to reset counter back to zero. As with other mod counters, it receives input clock pulse, one by one, and counts up from 0 to 9 repeatedly.

  Once it reaches the count 9 (1001 in binary), counter goes back to 0000 instead of continuing on to 1010. The basic circuit of a decade counter can be made from JK flip-flops that switch state on the negative trailing-edge of the clock signal