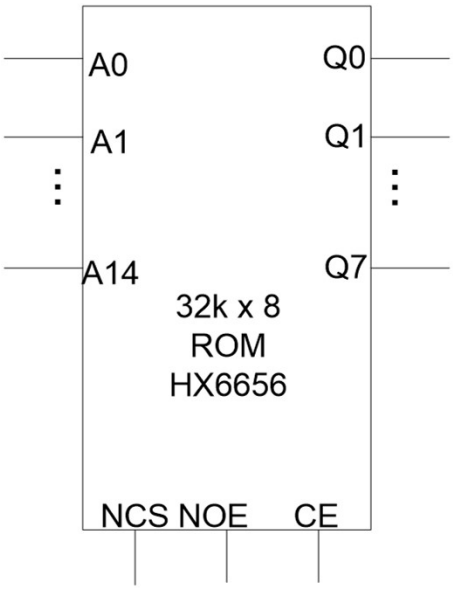
# Honeywell HX6656



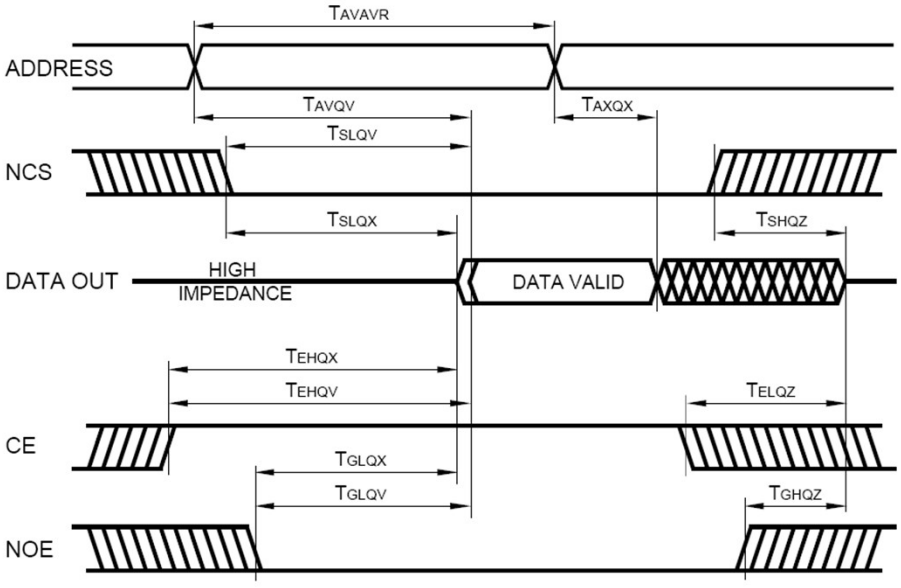

# Definicije signala

- **A: 0-14** Address input pins which select a particular eight-bit word within the memory array.
- **Q: 0-7** Data Output Pins.
- **NCS** Negative chip select, when at a low level allows normal read operation. When at a high level NCS forces the ROM to a precharge condition, holds the data output drivers in a high impedance state and disables all input buffers except CE. If this signal is not used it must be connected to VSS.
- **NOE** Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS and CE. If this signal is not used it must be connected to VSS.
- **CE** Chip enable, when at a high level allows normal operation. When at a low level CE forces the ROM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS input buffer. If this signal is not used it must be connected to VDD.

# Truth table

| NCS | CE | NOE | MODE | Q |
|---|---|---|---|---|
| L | H | L | Read | Data Out |
| H | X | XX | Deselected | High Z |
| X | L | XX | Disabled | High Z |

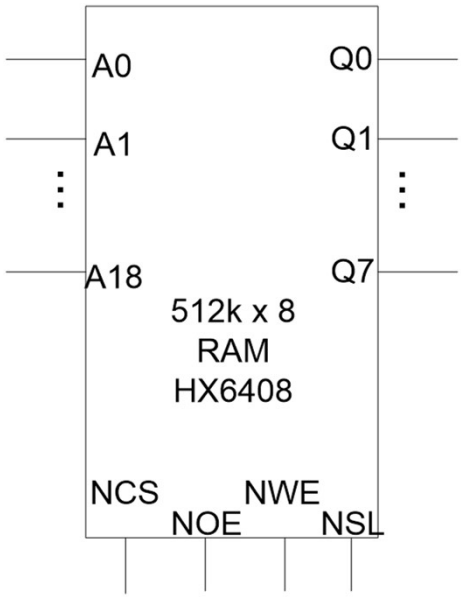
# Read cycle timing



# Timing characteristics

| Symbol | Parameter | Typical (2) | Worst Case (3) -55 to 125°C Min | Worst Case (3) -55 to 125°C Max | Units |
|---|---|---|---|---|---|
| TAVAVR | Address Read Cycle Time | | 25 | | ns |
| TAVQV | Address Access Time | | | 25 | ns |
| TAXQX | Address Change to Output Invalid Time | | 3 | | ns |
| TSLQV | Chip Select Access Time | | | 25 | ns |
| TSLQX | Chip Select Output Enable Time | | 5 | | ns |
| TSHQZ | Chip Select Output Disable Time | | | 10 | ns |
| TEHQV | Chip Enable Access Time (4) | | | 25 | ns |
| TEHQX | Chip Enable Output Enable Time (4) | | 5 | | ns |
| TELQZ | Chip Enable Output Disable Time (4) | | | 10 | ns |
| TGLQV | Output Enable Access Time | | | 9 | ns |
| TGLQX | Output Enable Output Enable Time | | 0 | | ns |
| TGHQZ | Output Enable Output Disable Time | | | 9 | ns |

# Honeywell HX6408



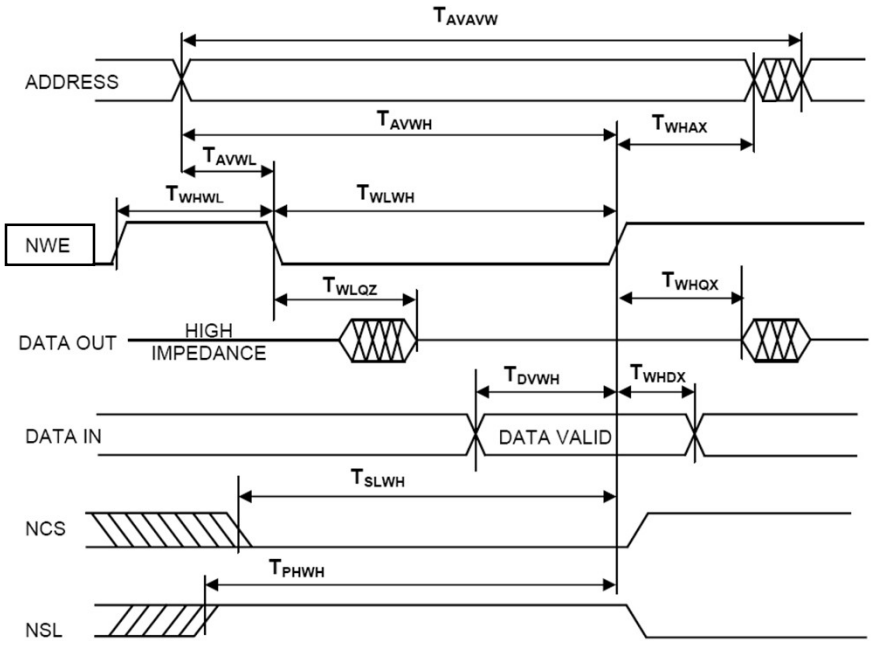
# Definicije signala

- **A: 0-18** Address input pins, which select a particular eight-bit word within the memory array.
- **DQ: 0-7** Bidirectional data pins, which serve as data outputs during a read operation and as data inputs during a write operation.
- **NCS** Negative chip select, when at a low level allows normal read or write operation. When at a high level NCS forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state. If this signal is not used it must be connected to VSS.
- **NWE** Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level NWE allows normal read operation.
- **NOE** Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and NSL. This signal is asynchronous.
- **NSL** Not sleep, when at a high level allows normal operation. When at a low level NSL forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS and NOE input buffers. If this signal is not used it must be connected to VDD. This signal is asynchronous. The HX6408 may be ordered without the sleep mode option and pin 36 is then a NC.

# Truth table

| NCS | NSL | NWE | NOE | MODE | DQ |
|---|---|---|---|---|---|
| L | H | H | L | Read | Data Out |
| L | H | L | X | Write | Data In |
| H | X | X | X | Deselected | Nigh Z |
| X | L | X | X | Sleep | High Z |

# Write cycle timing




# Timing characteristics

| Symbol | Parameter | | Typical (2) | Worst Case (3) -55 to 125°C Min | Worst Case (3) -55 to 125°C Max | Units |
|---|---|---|---|---|---|---|
| TAVAVW | Write Cycle Time (4) | 300KRad | | 20 | | ns |
| | | 1MRad | | 25 | | |
| TWLWH | Write Enable Write Pulse Width | 300KRad | | 15 | | ns |
| | | 1MRad | | 20 | | |
| TSLWH | Chip Select to End of Write Time | 300KRad | | 16 | | ns |
| | | 1MRad | | 20 | | |
| TDVWH | Data Valid to End of Write Time | 300KRad | | 12 | | ns |
| | | 1MRad | | 15 | | |
| TAVWH | Address Valid to End of Write Time | 300KRad | | 20 | | ns |
| | | 1MRad | | 25 | | |
| TWHDX | Data Hold after End of Write Time | | | 0 | | ns |
| TAVWL | Address Valid Setup to Start of Write Time | | | 0 | | ns |
| TWHAX | Address Valid Hold after End of Write Time | | | 0 | | ns |
| TWLQZ | Write Enable to Output Disable Time | | | | 7 | ns |
| TWHQX | Write Disable to Output Enable Time | | | 4 | | ns |
| TWHWL | Write Disable to Write Enable Pulse Width (5) | | | 5 | | ns |

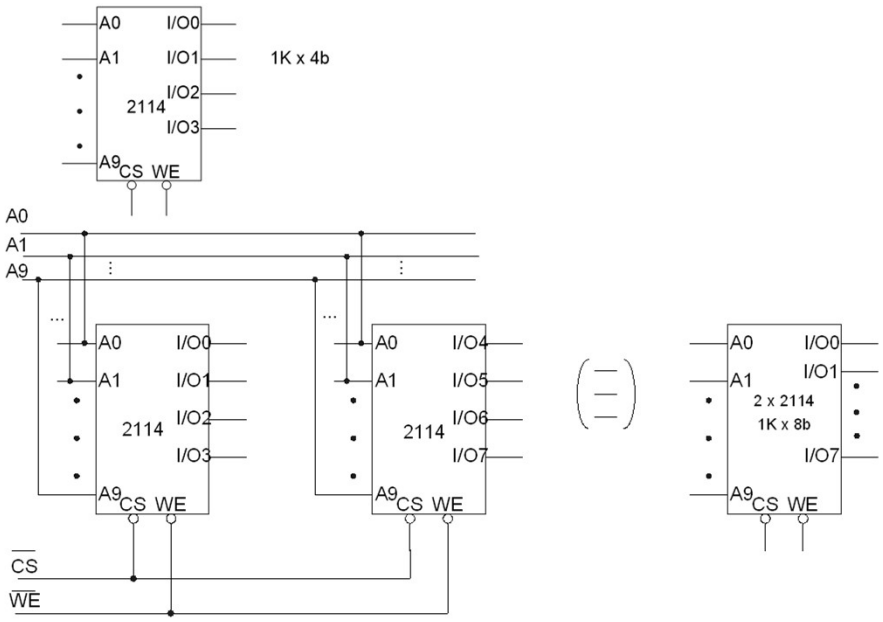
- Zadatak

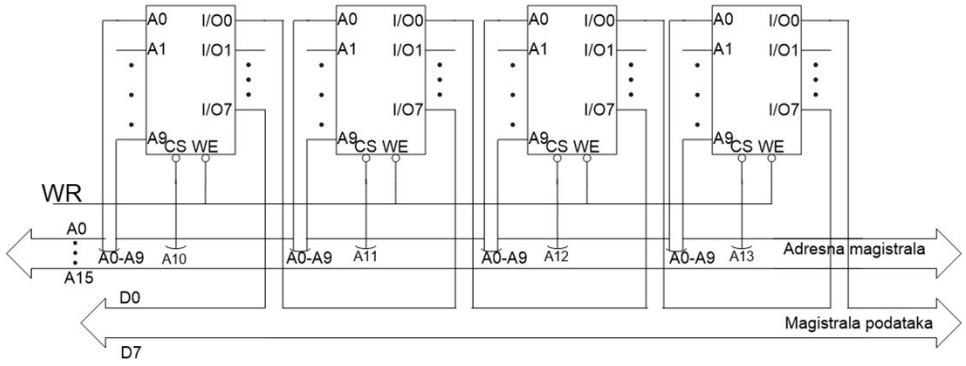
  Na 8-bitni mikroprocesor sa 16-bitnom adresnom magistralom treba priključiti RAM

  a) Kapaciteta 4KB

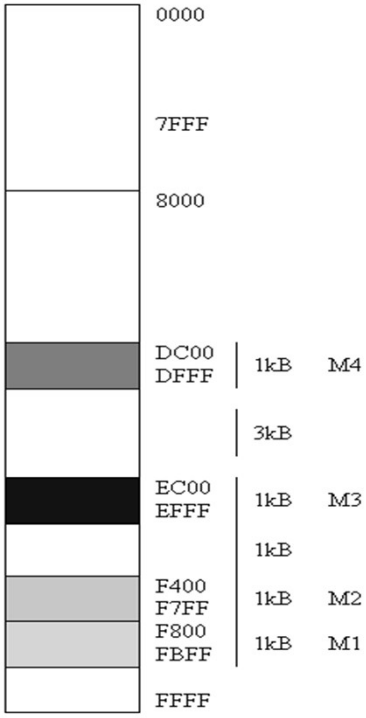
  b) Kapaciteta 24KB.

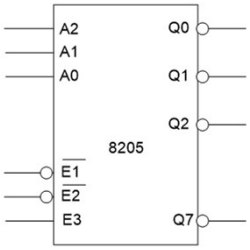
  Na raspolaganju su RAM čipovi 2114. Razmotriti linearni izbor čipova i izbor dekodiranjem adrese. Koje su gornje granice kapaciteta memorije sa zadatim čipovima pri korišćenju linearnog izbora čipa odnosno primenom dekodiranja adrese?



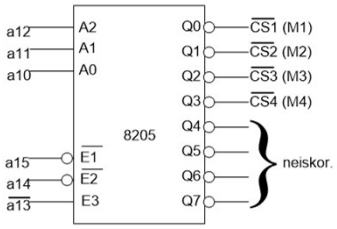



| M1 | | M2 | | M3 | M4 |
|---|---|---|---|---|---|
| A15 A14 A13 A12 A11 A10<br>1 1 1 1 1 0 | 0…0<br>1…1 | A15 A14 A13 A12 A11 A10<br>1 1 1 1 0 1 | 0…0<br>1…1 | 111011 | 110111 |
| F800-FBFF | | F400-F7FF | | EC00-EFFF | DC00-DFFF |






| A2 | A1 | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

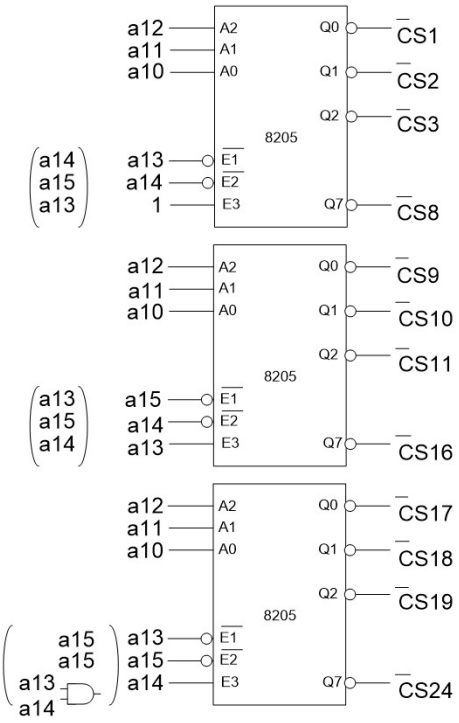



| A15 | A14 | A13 | A12 | A11 | A10 | A9 | | … | A0 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | … | 0 | } | M1 | 0000 |
| | | | | | | 1 | 1 | … | 1 | } | | 03FF |
| . | | | . | 0 | 1 | 0 | 0 | … | 0 | } | M2 | 0400 |
| . | | | . | | | 1 | 1 | | 1 | } | | 07FF |
| . | | | . | 1 | 0 | 0 | 0 | … | 0 | } | M3 | 0800 |
| | | | | | | 1 | 1 | | 1 | } | | 0BFF |
| | | | | 1 | 1 | 0 | 0 | … | 0 | } | M4 | 0C00 |
| | | | | | | 1 | 1 | | 1 | } | | 0FFF |

b) 24 x (1K x 8)

| A15 | A14 | A13 | A12 | A11 | A10 | A9 | … | A0 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 0 | … | 0 | M1 | DEK1 |
| | | | | | | 1 1 | … | 1 | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| | | | 1 | 1 | 1 | 0 0 | … | 0 | M8 | |
| | | | | | | 1 1 | | 1 | | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 0 | … | 0 | M9 | DEK2 |
| | | | | | | 1 1 | … | 1 | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| | | | 1 | 1 | 1 | 0 0 | … | 0 | M16 | |
| | | | | | | 1 1 | | 1 | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 0 | … | 0 | M17 | DEK3 |
| | | | | | | 1 1 | … | 1 | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| | | | 1 | 1 | 1 | 0 0 | … | 0 | M24 | |
| | | | | | | 1 1 | | 1 | | |

| | DEK1 | DEK2 | DEK3 |
|---|---|---|---|
| A13 | 0 | 1 | 0 |
| A14 | 0 | 0 | 1 |
| $\overline{E1}$ | A13 | A15 | A13 |
| $\overline{E2}$ | A14 | A14 | A15 |
| E3 | 1 | A13 | A14 |




24 čipa po 1K smestiti od 2000 do 7FFF

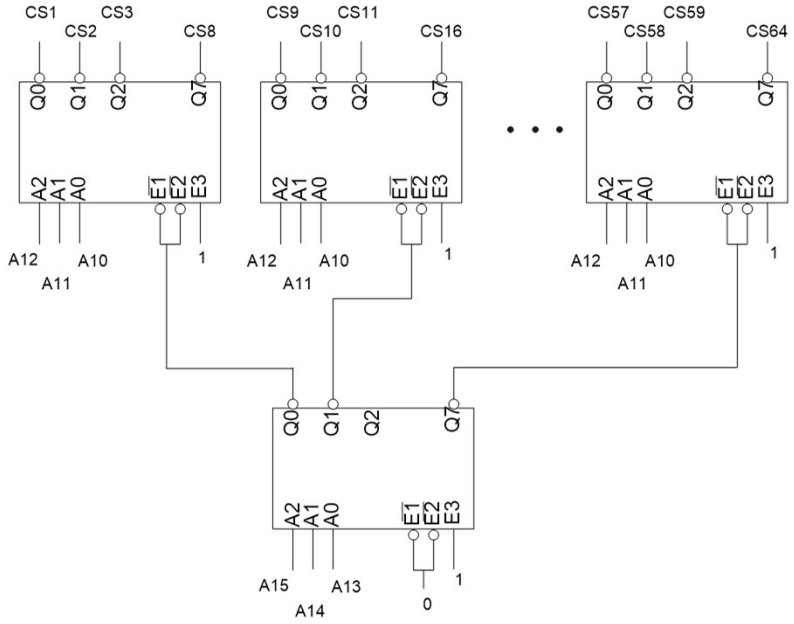
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | … | A0 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 0 | … | 0 | M1 | DEK1 |
| | | | | | | 1 1 | … | 1 | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| | | | 1 | 1 | 1 | 0 0 | … | 0 | M8 | |
| | | | | | | 1 1 | | 1 | | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 0 | … | 0 | M9 | DEK2 |
| | | | | | | 1 1 | … | 1 | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| | | | 1 | 1 | 1 | 0 0 | … | 0 | M16 | |
| | | | | | | 1 1 | | 1 | | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 0 | … | 0 | M17 | DEK3 |
| | | | | | | 1 1 | … | 1 | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| . | | | . | | . | | . | | | |
| | | | 1 | 1 | 1 | 0 0 | … | 0 | M24 | |
| | | | | | | 1 1 | | 1 | | |

24 čipa po 1K smestiti od 2000 do 7FFF

| | DEK1 | DEK2 | DEK3 |
|---|---|---|---|
| A13 | 1 | 0 | 1 |
| A14 | 0 | 1 | 1 |
| $\overline{E1}$ | A14 | A13 | A15 |
| $\overline{E2}$ | A15 | A15 | A15 |
| E3 | A13 | A14 | A14 * A13 |

64 čipa po 1K izbor u dva nivoa dekodiranja

64 x 1K



7xRAM 4Kx8b od 0000 do 6FFFF H
3xEPROM 8Kx8bn od 7000 do CFFF H

| | | A15 | A14 | A13 | A12 |
|---|---|---|---|---|---|
| **RAM1** | H'0000 – 0FFF | 0 | 0 | 0 | 0 |
| **RAM2** | H'1000 – 1FFF | 0 | 0 | 0 | 1 |
| **RAM3** | H'2000 – 2FFF | 0 | 0 | 1 | 0 |
| **RAM4** | H'3000 – 3FFF | 0 | 0 | 1 | 1 |
| **RAM5** | H'4000 – 4FFF | 0 | 1 | 0 | 0 |
| **RAM6** | H'5000 – 5FFF | 0 | 1 | 0 | 1 |
| **RAM7** | H'6000 – 6FFF | 0 | 1 | 1 | 0 |
| **EPROM1** | H'7000 – 8FFF | 0<br>1 | 1<br>0 | 1<br>0 | 1<br>0 |
| **EPROM2** | H'9000 – AFFF | 1<br>1 | 0<br>0 | 0<br>1 | 1<br>0 |
| **EPROM3** | H'b000 – CFFF | 1<br>1 | 0<br>1 | 1<br>0 | 1<br>0 |