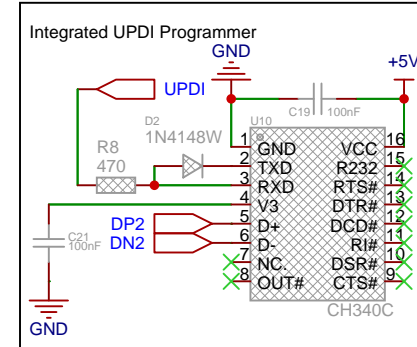
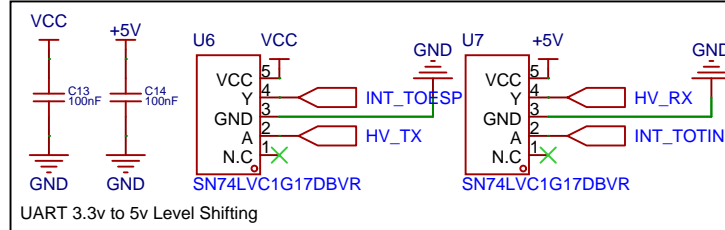
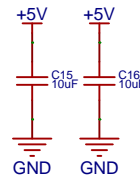
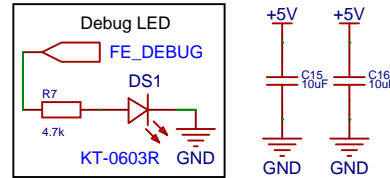
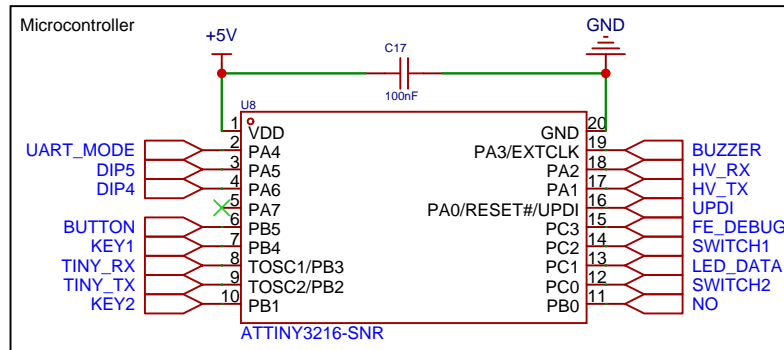


Schematic	V2.3.2 Schematic		Update Date	2024-10-21
			Create Date	2024-07-26
Page	Front End		Part Number	JLCPCB-002
Drawn	Jim Heaney	Access Control Core		
Reviewed	Jim Heaney			
		VER	SIZE	PAGE 1 OF 6
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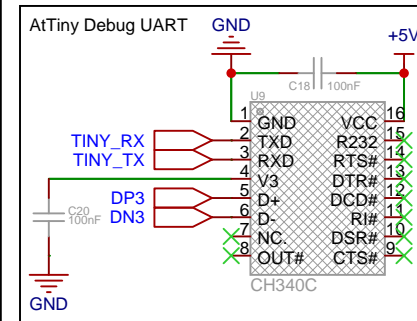
RIT



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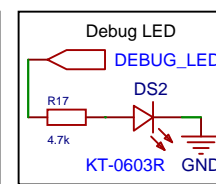
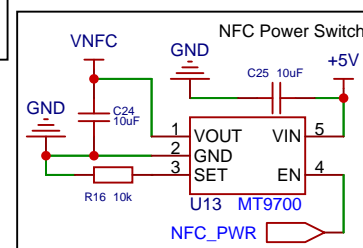
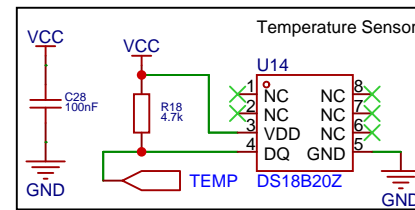
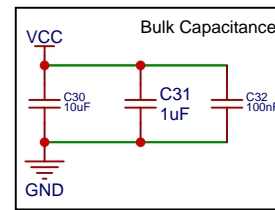
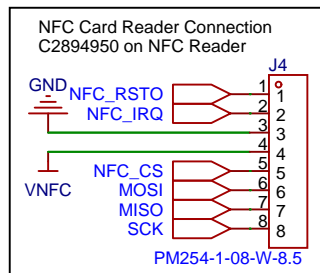
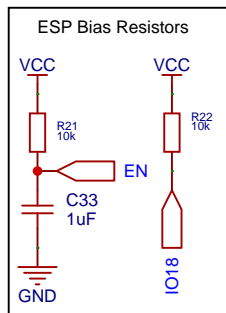
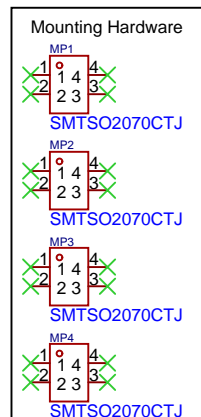
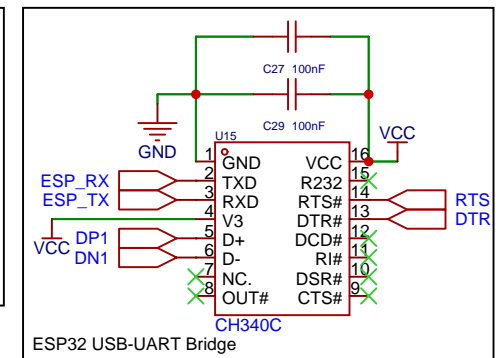
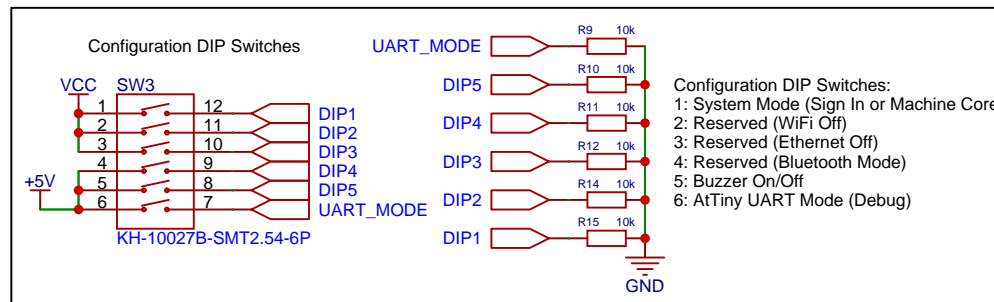
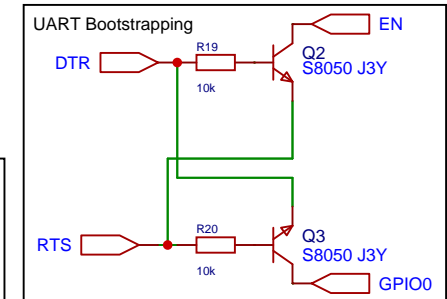
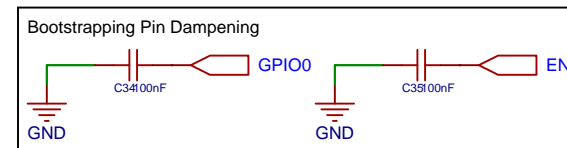
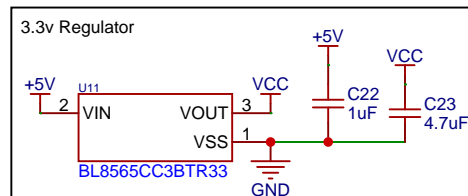
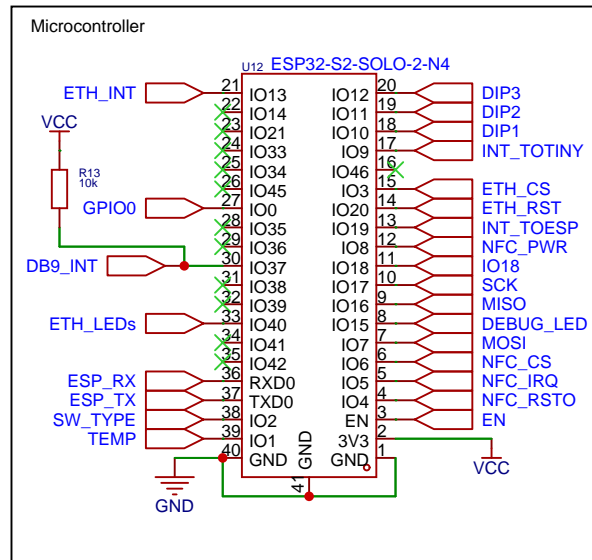


If UART_MODE is high, AtTiny re-assigns location of RX/TX to communicate with ESP32. By default and/or with no special code running, UART goes to USB

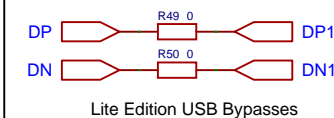
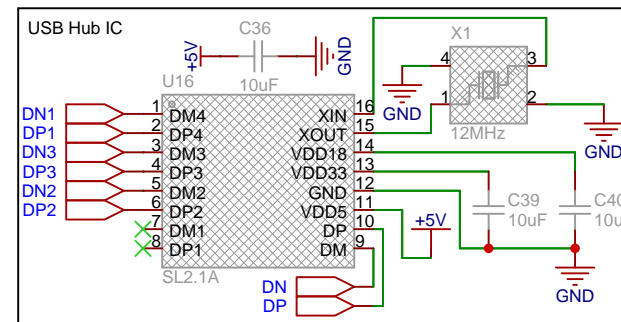
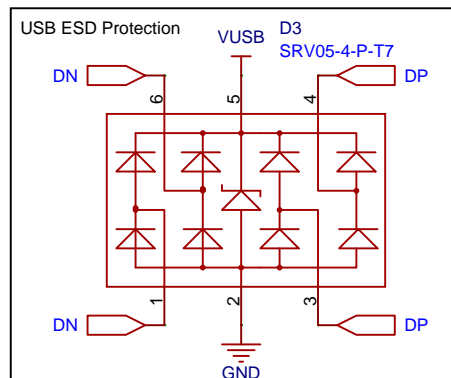
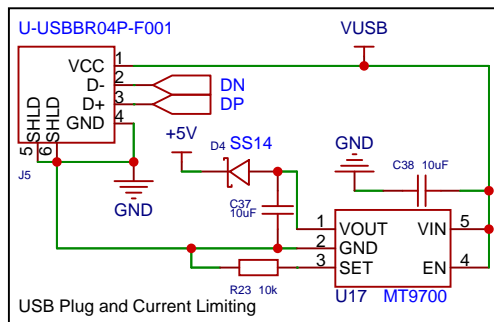


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Schematic	V2.3.2 Schematic		Update Date	2024-10-21
			Create Date	2024-07-26
Page	Front End MCU		Part Number	JLPCB-002
Drawn	Jim Heaney	Access Control Core		
Reviewed	Jim Heaney			
RIT		VER	SIZE	PAGE 2 OF 6
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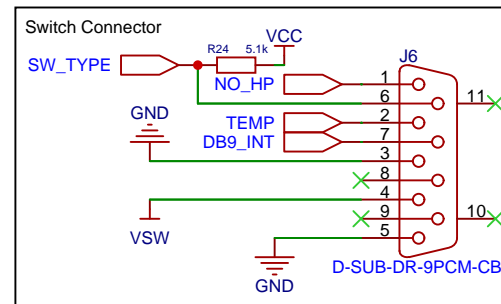
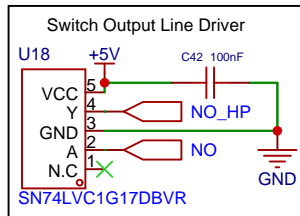
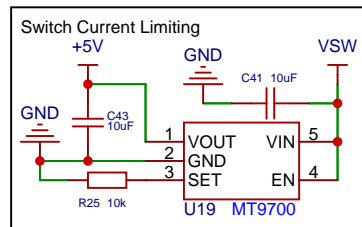
Schematic	V2.3.2 Schematic			Update Date	2024-10-21
Page	Network MCU			Create Date	2024-07-26
Drawn	Jim Heaney	Access Control Core			
Reviewed	Jim Heaney				
		VER	SIZE	PAGE	3 OF 6
RIT		V0.1	A4	RIT SHED MAKERSPACE	



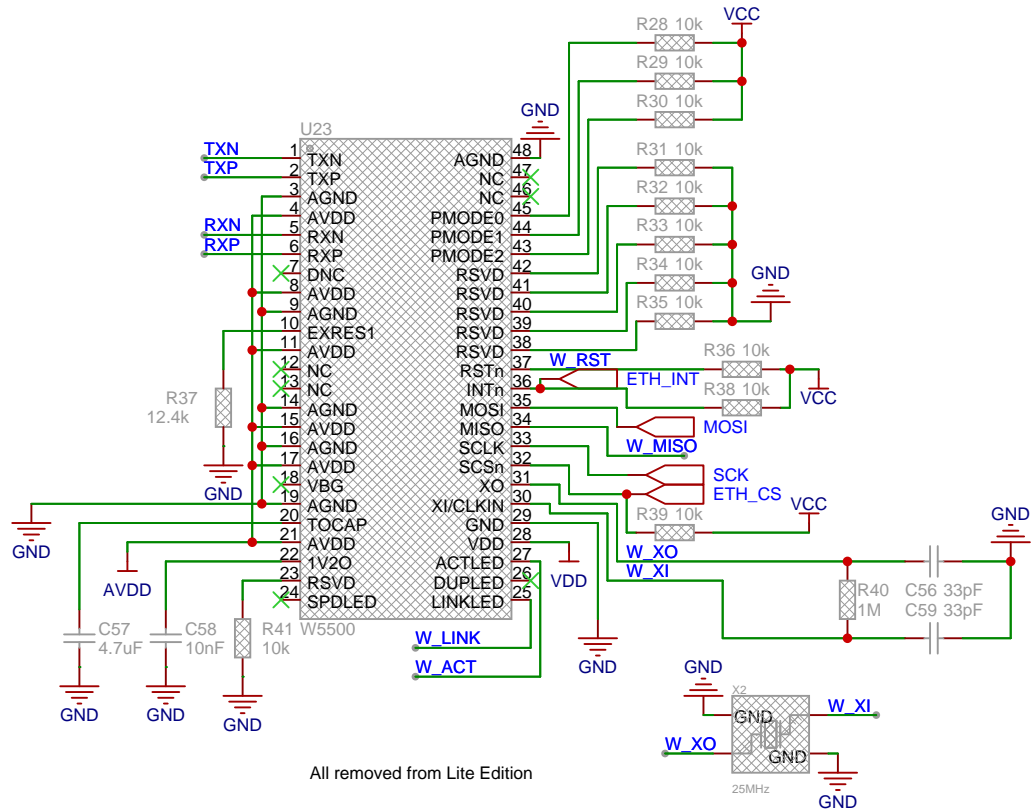
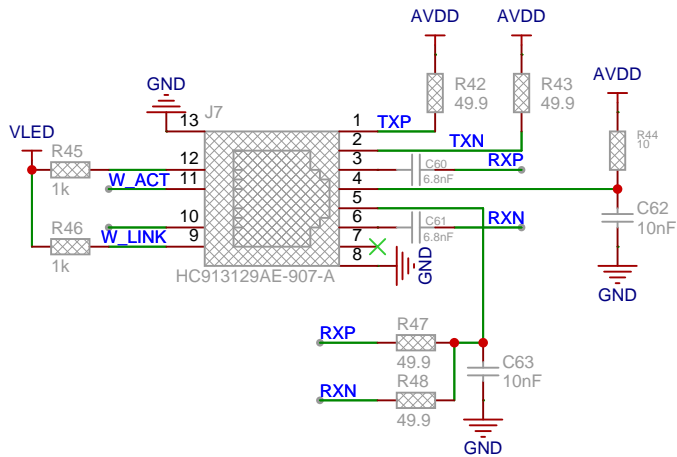
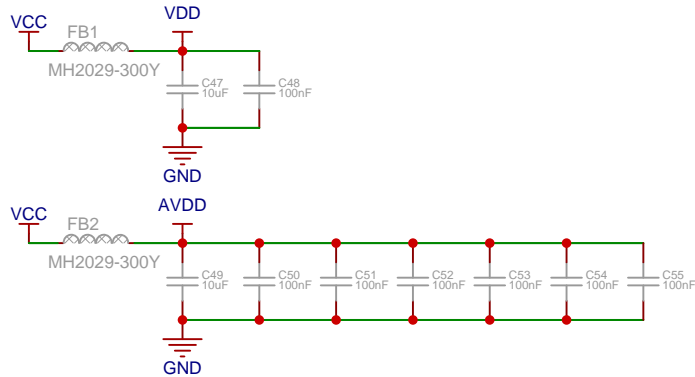
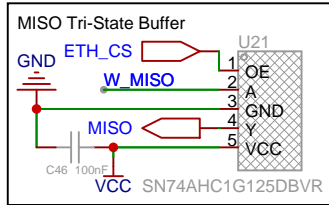
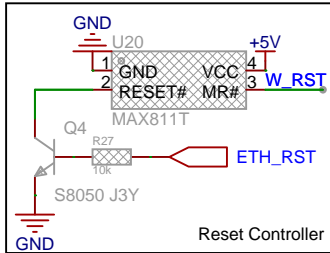
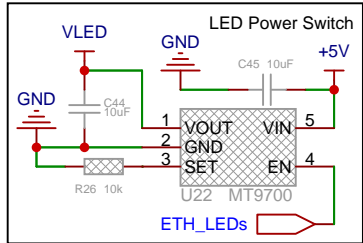
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Schematic	V2.3.2 Schematic			Update Date	2024-10-21
Page	USB			Create Date	2024-07-26
Drawn	Jim Heaney	Access Control Core			
Reviewed	Jim Heaney				
		VER	SIZE	PAGE	4 OF 6
		V0.1	A4	RIT SHED MAKERSPACE	

RIT



Schematic	V2.3.2 Schematic			Update Date	2024-10-21
				Create Date	2024-07-26
Page	Switch Interface			Part Number	JLCPCB-002
Drawn	Jim Heaney	Access Control Core			
Reviewed	Jim Heaney				
RIT		VER	SIZE	PAGE	5 OF 6
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Schematic	V2.3.2 Schematic			Update Date	2024-10-21
Page	Ethernet			Create Date	2024-07-26
Drawn	Jim Heaney	Access Control Core			
Reviewed	Jim Heaney				
		VER	SIZE	PAGE	6 OF 6
		V0.1	A4	RIT SHED MAKERSPACE	