

EE533 Lab3

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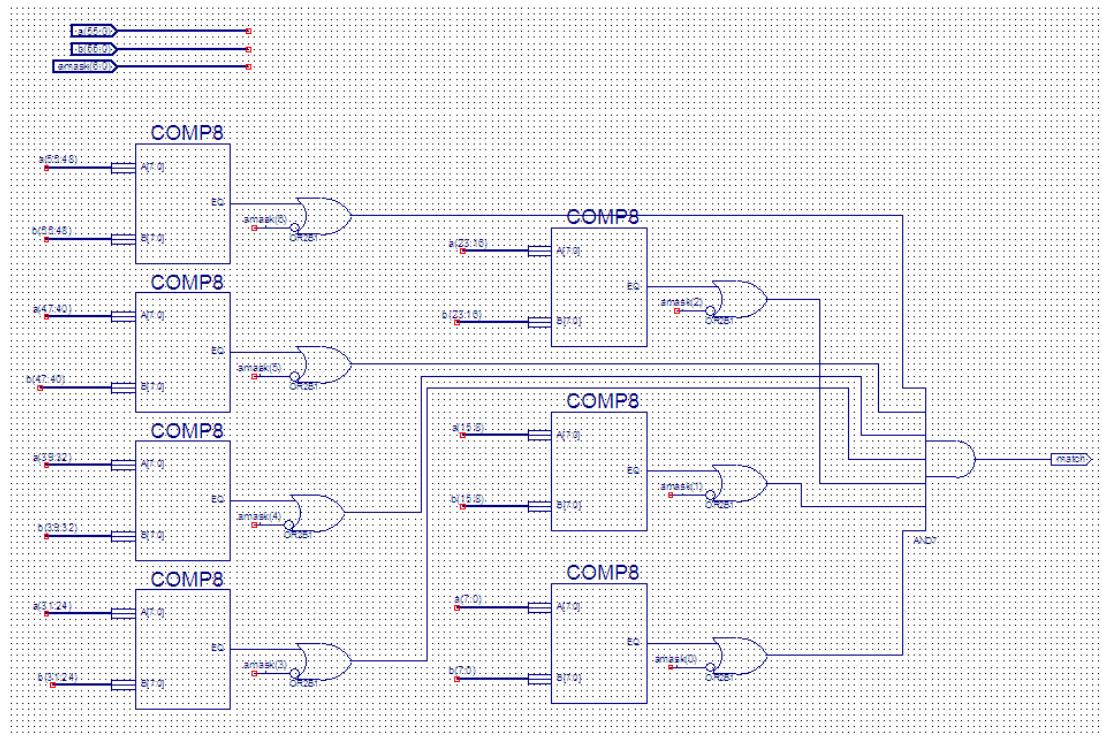
1. Schematic Capture

Verilog code in github: https://github.com/rita0128/EE533_lab3

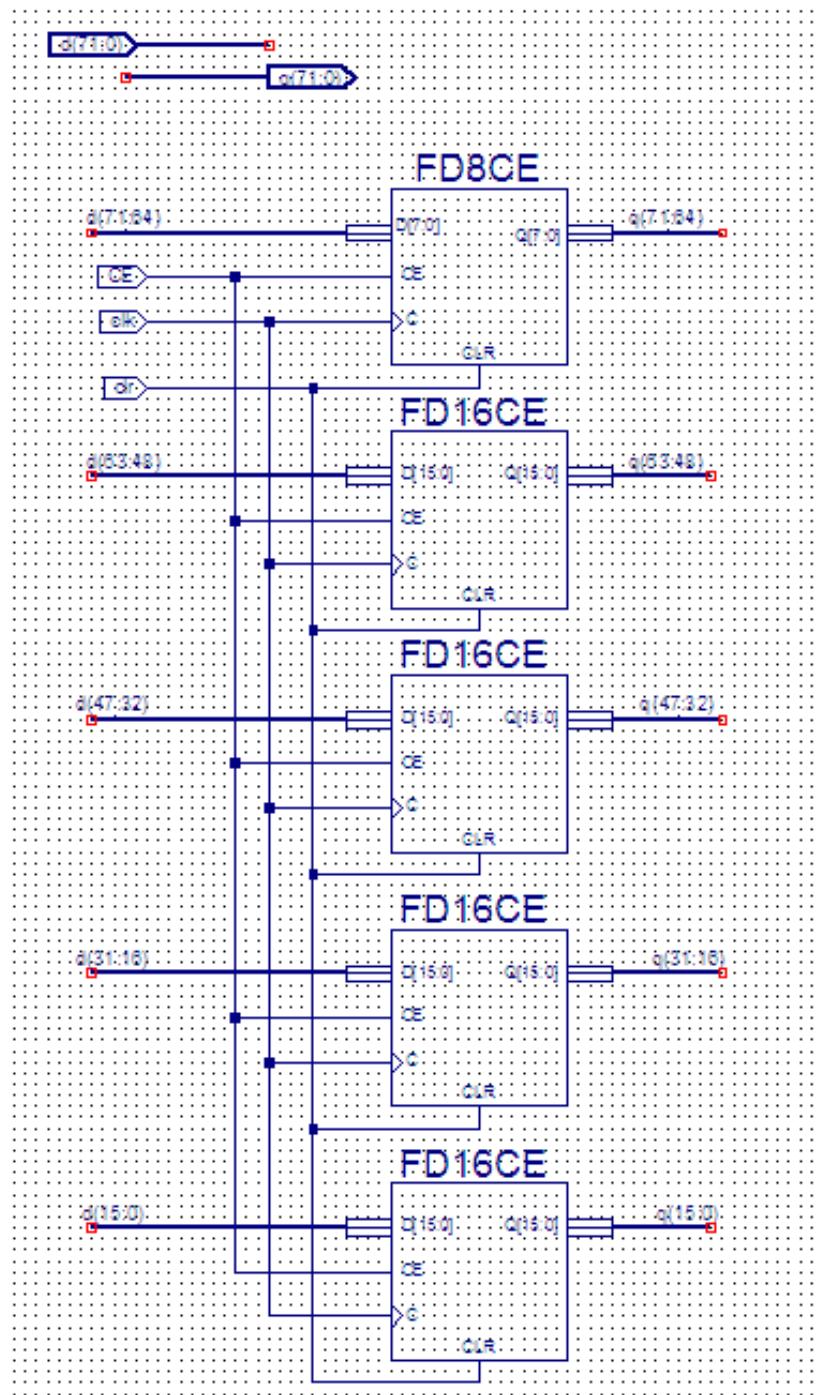
- Busmerge.v

```
21 module busmerge(da, db, q);
22     input [47:0] da;
23     input [63:0] db;
24     output [111:0] q;
25     assign q = (da, db);
26 endmodule
27
```

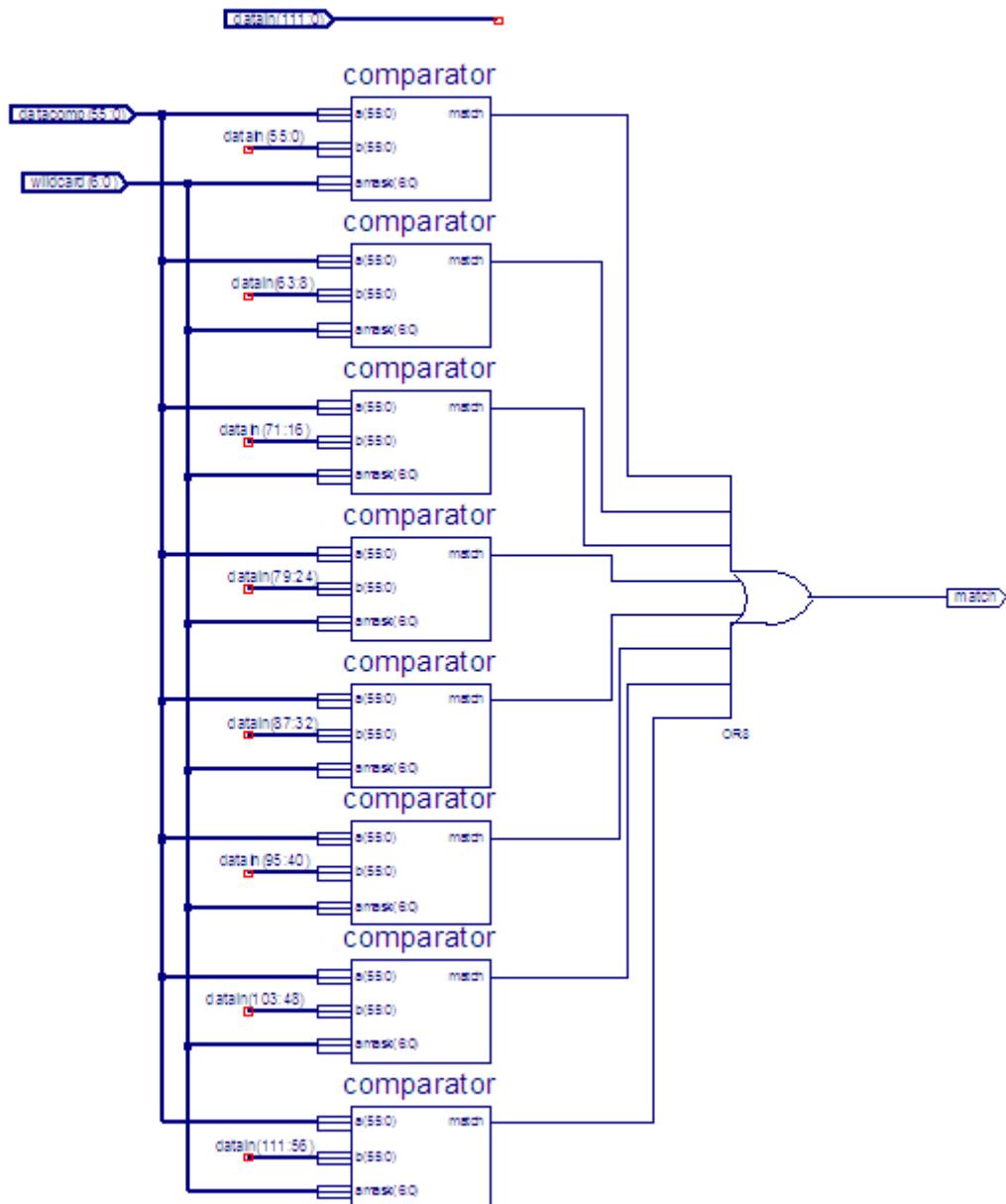
- Comparator schematic



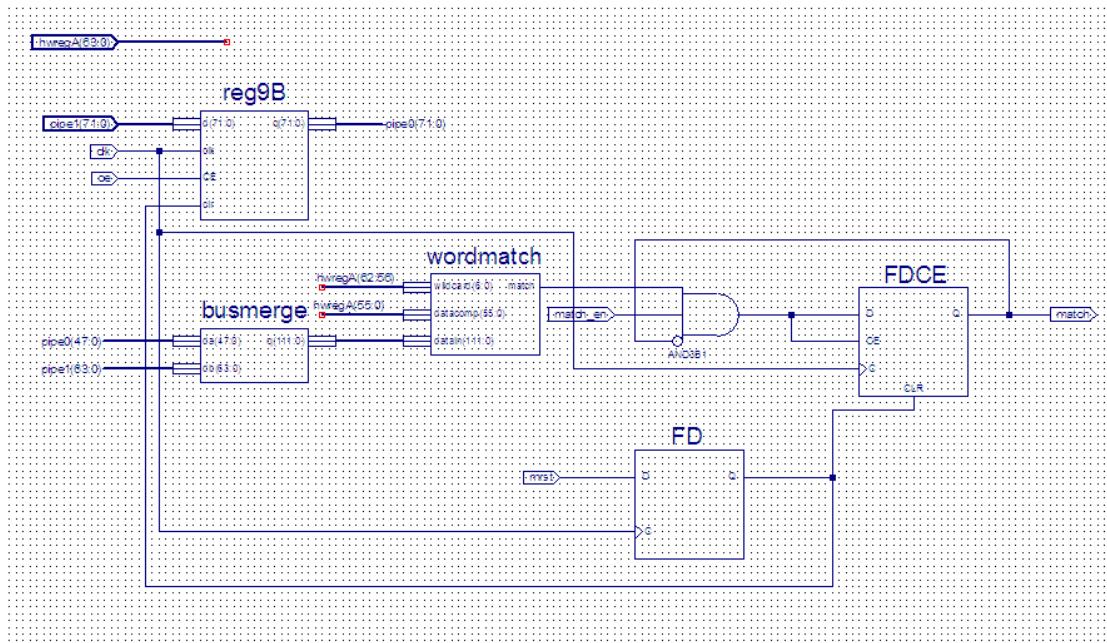
- Reg9B schematic



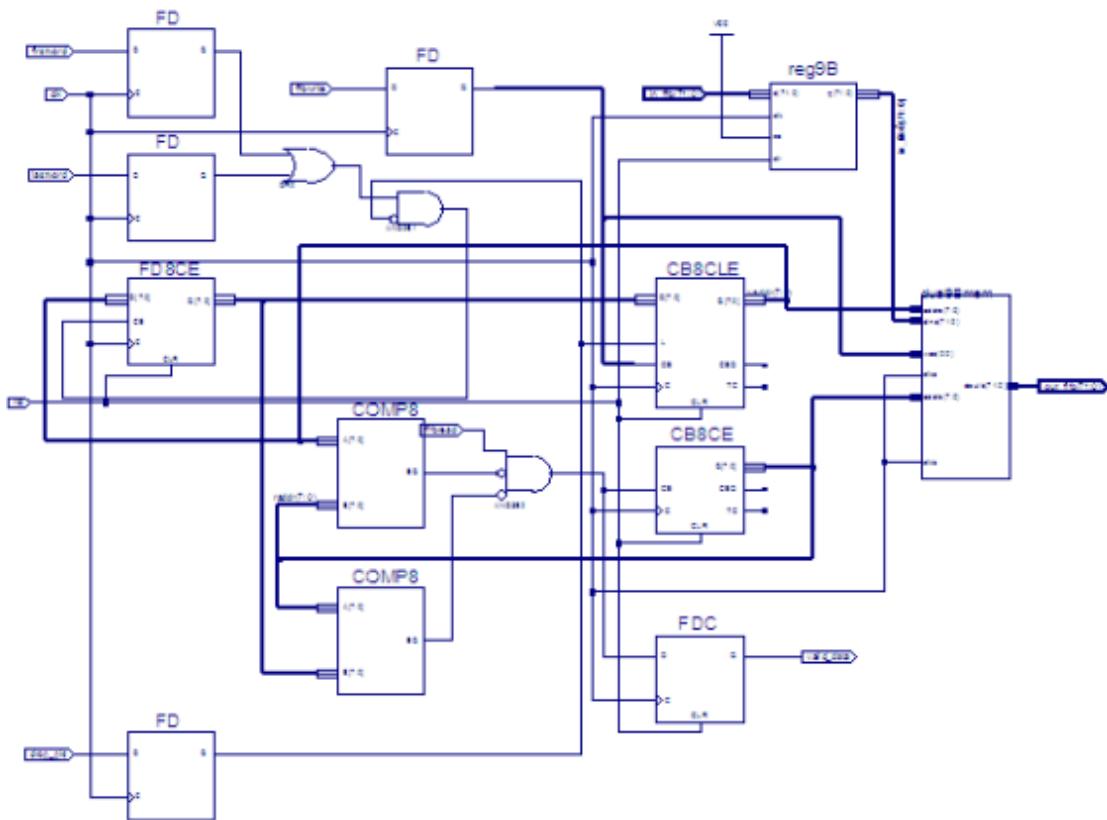
- wordmatch schematic



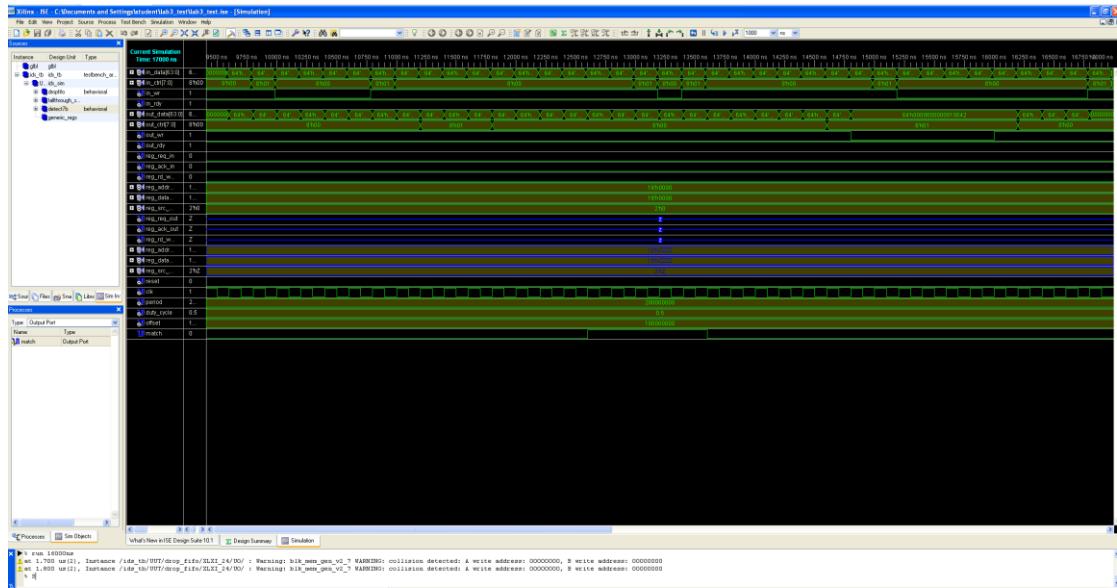
- detect9B schematic



- dropfifo



- Final simulation



2. Submission and Demonstration

a) Explain the pattern matching algorithm in the report

Before the pattern comes in, there are headers. We don't check the headers, but check the payload behind them. The pattern might be cut into different cycles, so we use busmerge to combine the data from the last and the new cycle. After merging the data, we use comparators to check different starting points and see if they match.

b) What is the purpose of AMASK[6:0]?

The purpose of AMASK is to tell the comparator which bytes are important and which ones are not, because real packets have changing fields, so we need to ignore them to match the attack pattern correctly.

- If AMASK =0 → the inverter makes it into 1 and the output will be 1 → this means the system ignores this byte.
- If AMASK =1 → the inverter makes it into 0 → the system will have to check the data

c) What exactly does busmerge.v do?

It combines 48 bits from the last clock cycle with 64 bits from the new clock cycle. There might be some pattern cut into two parts across different cycles, so we need to combine them to check if it matches or not.

d) What do the comp8 modules do in this schematic?

It is an 8-bit comparator. It compares the data and pattern to check if they are the same or not. If they match, the output will be 1.

e) What is the purpose of dual9Bmem in dropfifo.sch?

The purpose of dual9Bmem is to store data and wait for the IDS to check it. It also allows the system to read previously stored data while new data is written. If the data matches the pattern, the FIFO will drop. If it isn't a match, the FIFO will read and send to the next module.