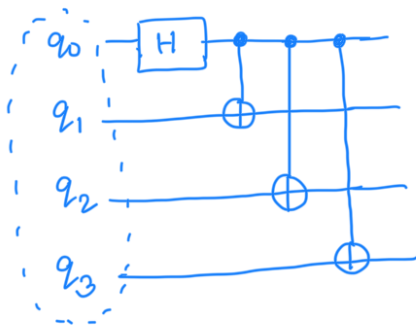


QUBIT SELECTION

Refer to Measurement error mitigation demo where we pre-selected some qubits.

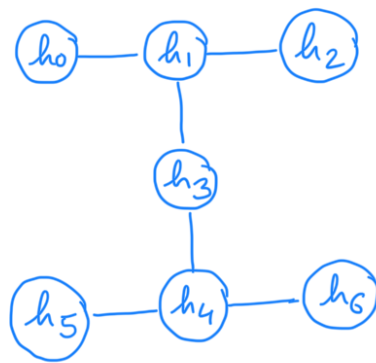
Q> were those the best qubits to select?

Circuit



virtual/circuit
qubit

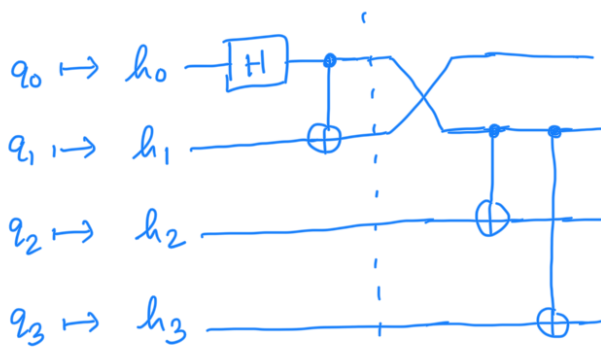
Hardware



physical qubits

Q> which virtual qubit should be placed on which physical qubit?

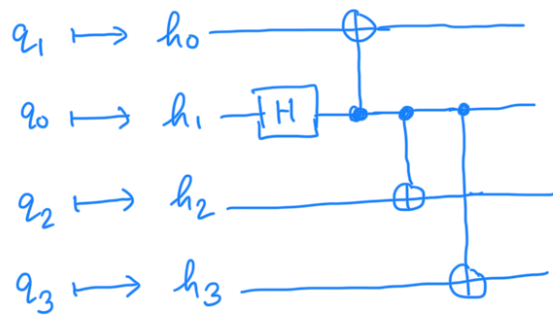
attempt 1: $q_0 \rightarrow h_0$, $q_1 \rightarrow h_1$, \dots , $q_3 \rightarrow h_3$



h_0 has no more
neighbours

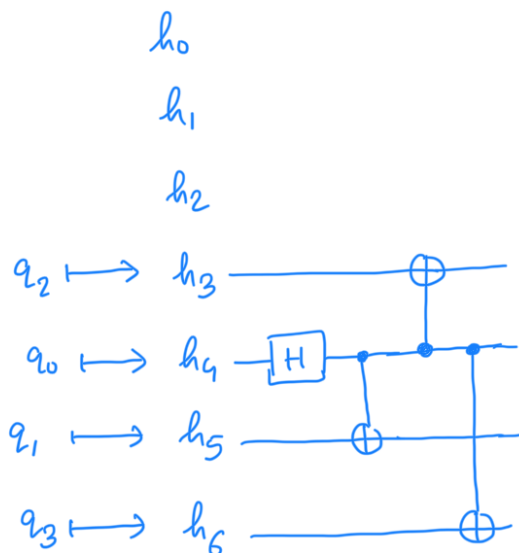
\Rightarrow 1 swap gate

attempt 2 : $q_0 \rightarrow h_1$, $q_1 \rightarrow h_0$, $q_2 \rightarrow h_2$, $q_3 \rightarrow h_3$



\Rightarrow 0 swap gate
this transpilation is better

attempt 3 : $q_0 \rightarrow h_4$, $q_1 \rightarrow h_5$, $q_2 \rightarrow h_3$, $q_3 \rightarrow h_6$



\Rightarrow 0 swap gate

which one of the last two should we select ?

\Rightarrow NOT ALL QUBITS & INTERACTIONS HAVE THE SAME ERROR PROBABILITY

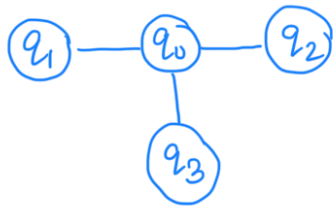
- Joint optimization is hard

Idea of mapomatic

... ..

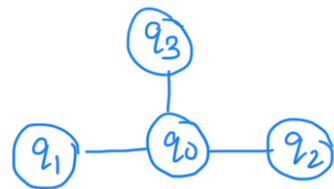
- 1) Find an optimal placement without considering the error probability of the qubits / interaction.
- any one of the last 2 placements is good.

- 2) Create a graph from the transpiled circuit.



- 3) Find subgraph isomorphisms of the transpiled graph on the hardware graph.

- how many different ways can we place the transpiled graph on the hardware graph without losing the orientation?



\Rightarrow correspond to the 3rd transpilation

- 4) Calculate the error probability of each isomorphism.

- one method is to check the error probability of all qubits (correspond to 1 qubit gates), readout errors, and interactions (correspond to 2 qubit gates)

- 5) Select the isomorphism with the lowest error probability