8254 AND 8279 PPI

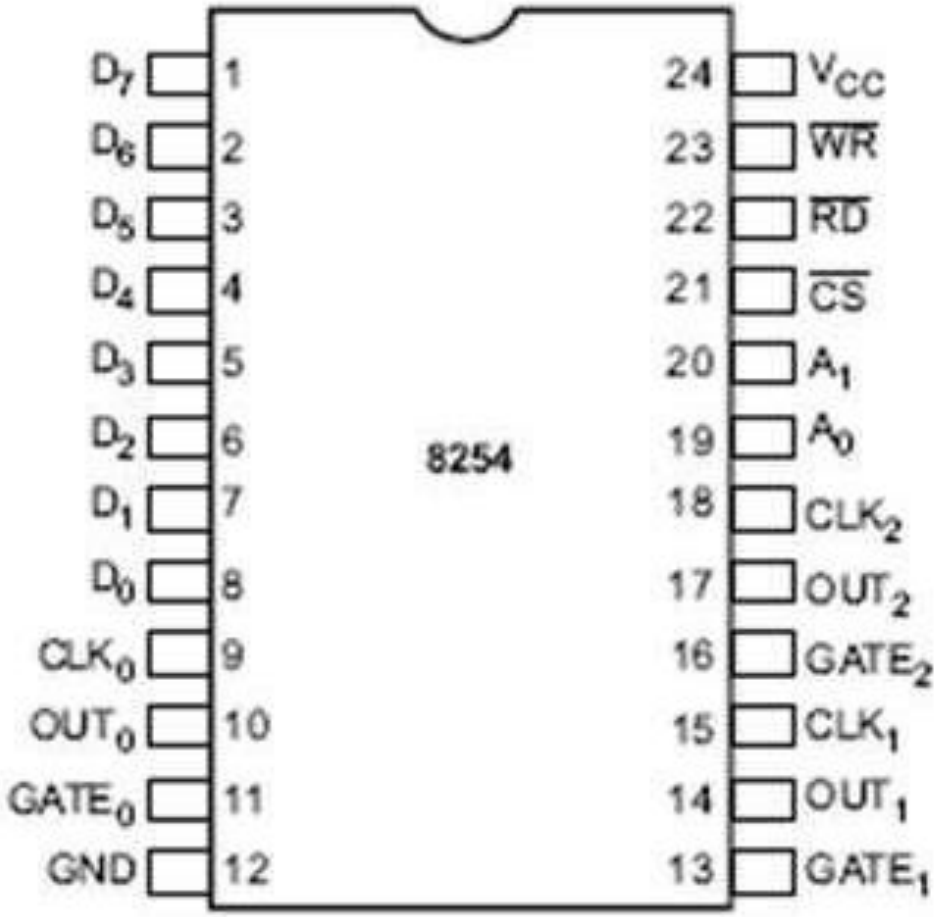
8254

8254 is Programmable Interval Timer designed for microprocessors to perform timing and counting functions using three 16-bit counters.

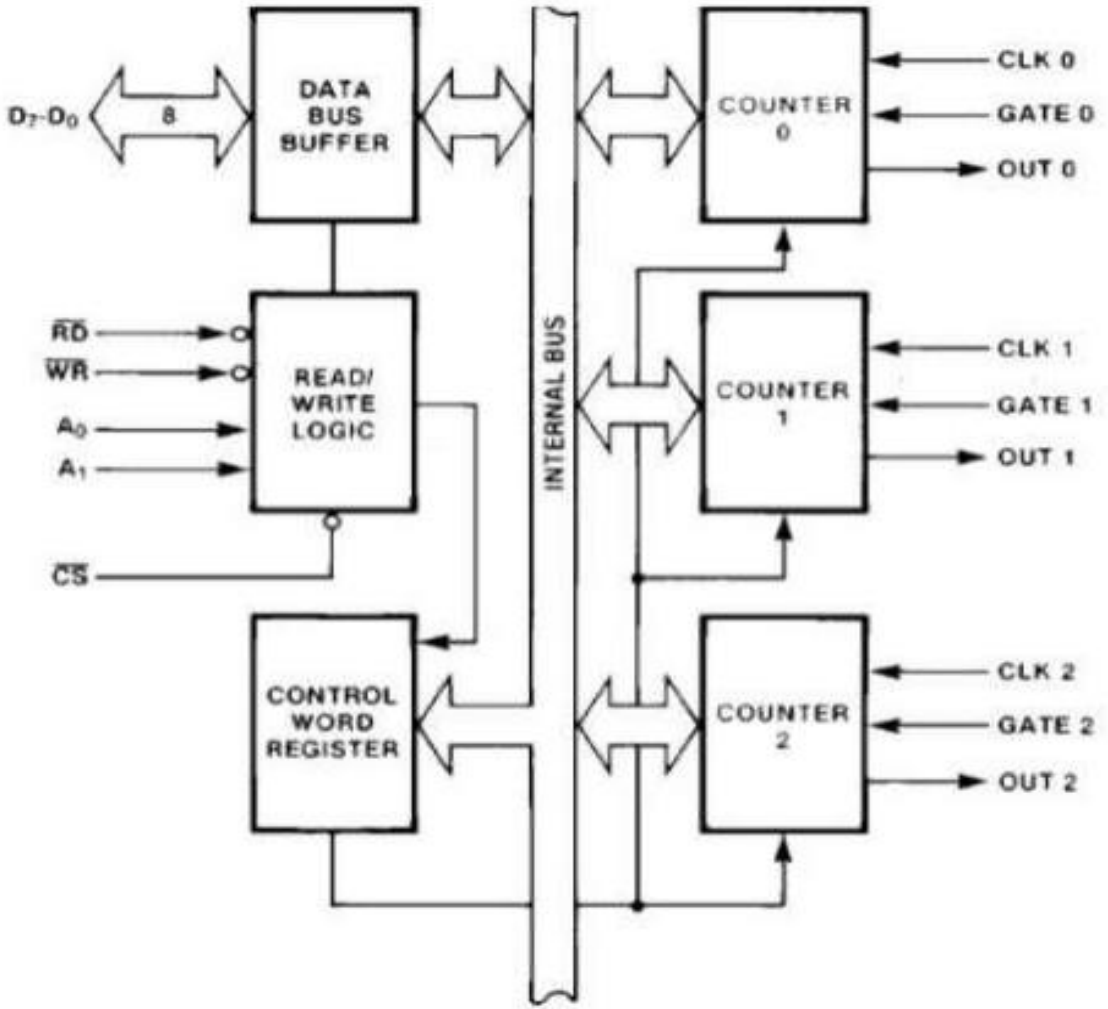
FEATURES OF 8254

- **It has three independent 16-bit down counters.**
- **It can handle inputs from DC to 10 MHz.**
- **These three counters can be programmed for either binary or BCD count.**
- **It is compatible with almost all microprocessors.**
- **8254 has a powerful command called *Status Read Back* command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.**

PIN DIAGRAM


D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
CLK0 9
OUT0 10
GATE0 11
GND 12
24 VCC
23 WR
22 RD
21 CS
20 A1
19 A0
18 CLK2
17 OUT2
16 GATE2
15 CLK1
14 OUT1
13 GATE1
8254

8254 BLOCK DIAGRAM



In the above figure, there are three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals - CLOCK & GATE, and one output signal - OUT.

Data Bus Buffer: It is a tri-state, bi-directional, 8-bit buffer, which is used to interface 8254 to the system data bus. It has three basic functions –

- Programming the modes of 8254.
- Loading the count registers.
- Reading the count values.

Read/Write Logic: It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW. Address lines A0 & A1 of the MPU are connected to lines A0 and A1 of the 8254, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

A_1	A_0	Result
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register
X	X	No Selection

8254 CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

M—MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

BCD:

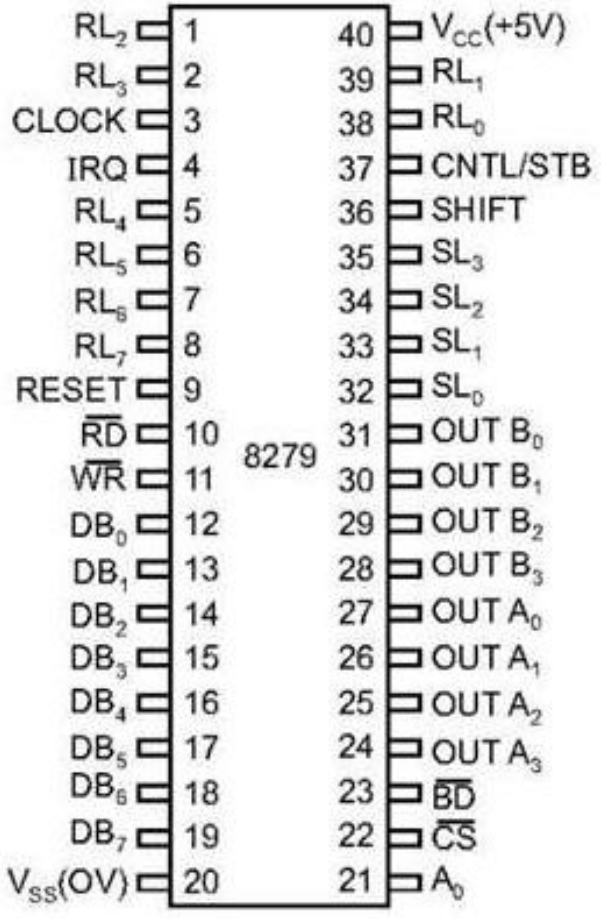
0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Note: Don't Care Bits (X) Should Be 0 to Ensure Compatability with Future Intel Products.

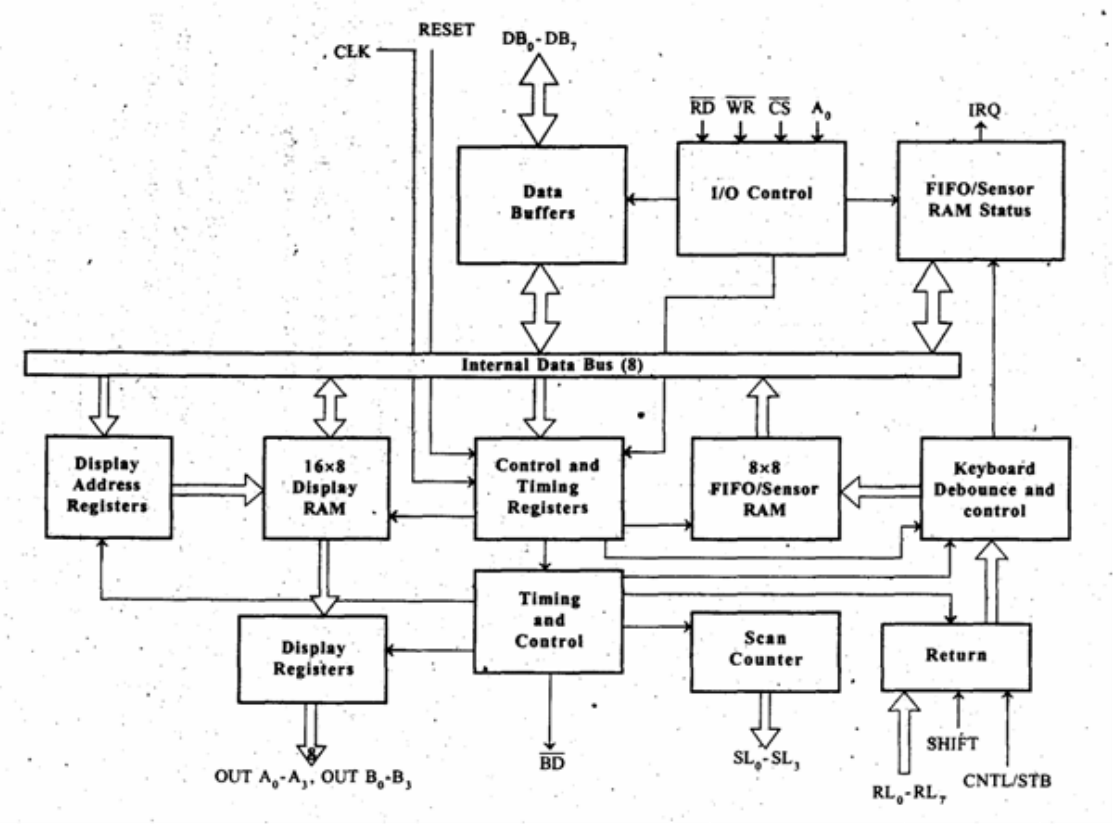
8279

8279 is a programmable keyboard and display controller, designed by Intel that interfaces a keyboard and a multiplexed display with the MPU. The keyboard first scans the keyboard and identifies if any key has been pressed. It then sends their relative response of the pressed key to the MPU and vice-a-versa.

8279 PIN DIAGRAM



BLOCK DIAGRAM OF 8279



SECTIONS

- **Keyboard**
- **Scan**
- **Display**
- **MPU interface**

KEYBOARD SECTION

- The keyboard section consists of eight return lines RL0 - RL7 that can be used to form the columns of a keyboard matrix.
- It has two additional input : shift and control/strobe. The keys are automatically debounced.
- The two operating modes of keyboard section are 2-key lockout and N-key rollover.
- In the 2-key lockout mode, if two keys are pressed simultaneously, only the first key is recognized.
- In the N-key rollover mode simultaneous keys are recognized and their codes are stored in FIFO.
- The keyboard section also have an 8 x 8 FIFO (First In First Out) RAM.
- The FIFO can store eight key codes in the scan keyboard mode. The status of the shift key and control key are also stored along with key code.
- The 8279 generate an interrupt signal when there is an entry in FIFO.

SCAN SECTION

- **The scan section has a scan counter and four scan lines, SL0 to SL3.**
- **These four scan lines can be decoded using a 4-to-16 decoder to generate 16 lines for scanning.**
- **These scan lines can be connected to the rows of a matrix keyboard and digit drivers of a multiplexed display, to turn ON/OFF.**

DISPLAY SECTION

- **The display section has eight output lines divided into two groups A0-A3 and B0-B3.**
- **The output lines can be used either as a single group of eight lines or as two groups of four lines, in conjunction with the scan lines for a multiplexed display.**
- **The output lines are connected to the anodes through driver transistor in case of common cathode 7-segment LEDs.**
- **The cathodes are connected to scan lines through driver transistors.**
- **The display can be blanked by BD (low) line.**
- **The display section consists of 16 x 8 display RAM. The MPU can read from or write into any location of the display RAM.**

MPU INTERFACE SECTION

- **The MPU interface section takes care of data transfer between 8279 and the processor.**
- **This section has eight bidirectional data lines DB0 to DB7 for data transfer between 8279 and MPU.**
- **It requires two internal address A =0 for selecting data buffer and A = 1 for selecting control register of 8279.**
- **The control signals WR (low), RD (low), CS (low) and A0 are used for read/write to 8279.**
- **It has an interrupt request line IRQ, for interrupt driven data transfer with processor.**
- **The 8279 require an internal clock frequency of 100 kHz. This can be obtained by dividing the input clock by an internal prescaler.**
- **The RESET signal sets the 8279 in 16-character display with two - key lockout keyboard modes.**

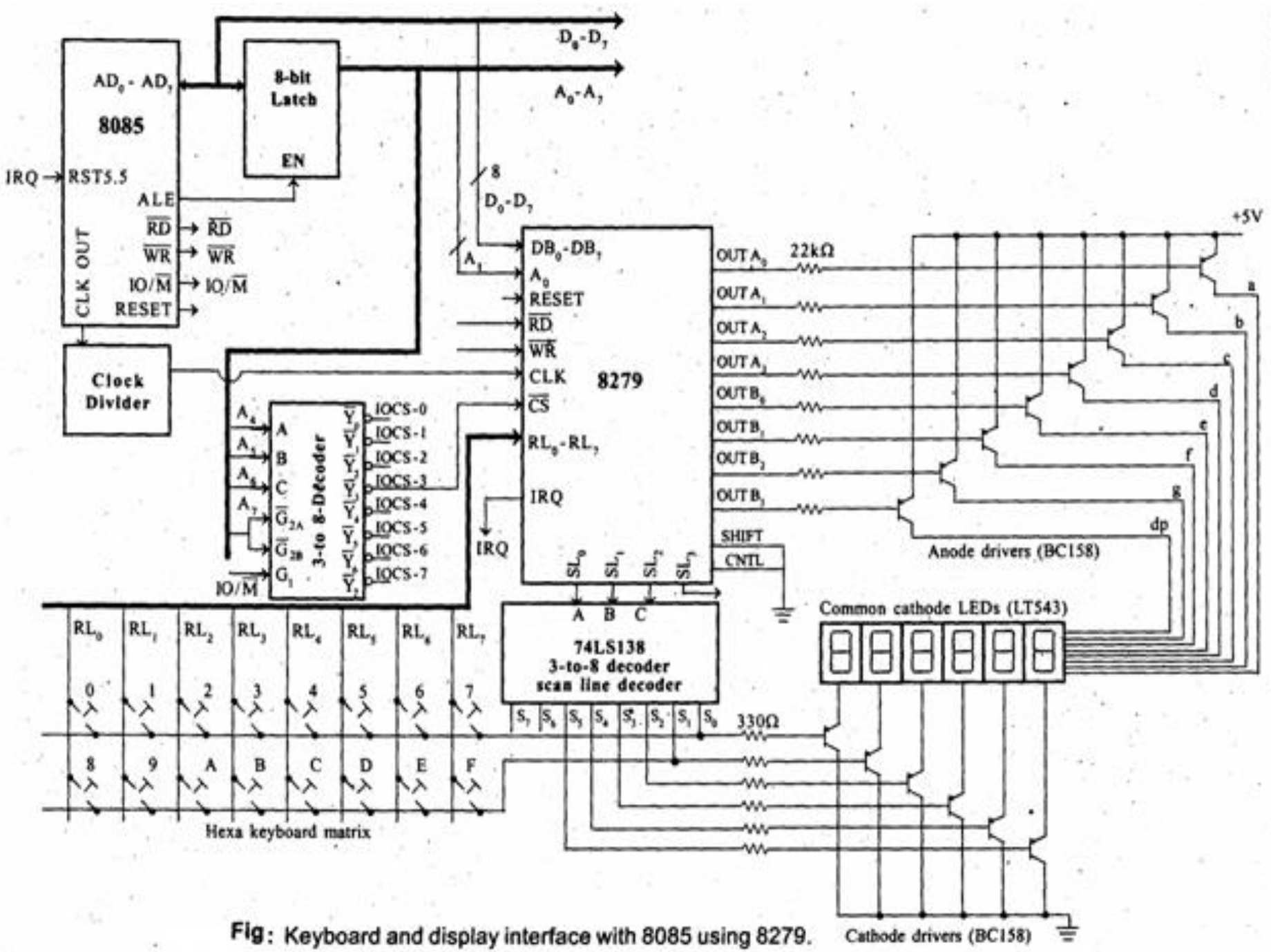


Fig: Keyboard and display interface with 8085 using 8279.