BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

# MACHINE CYCLES AND TIMING DIAGRAMS

**Instruction Cycle:**
This is the time required by the µP to fetch and execute one complete instruction.
The instruction cycle is in two parts:
1. Fetch Cycle
2. Execute Cycle

**Fetch Cycle:**
This is the time required by the µP to fetch all bytes of an instruction
The length of the fetch cycle is thus determined by the no of bytes in an instruction.

**Execution Cycle:**
This is the time required by the µP to execute a fetched instruction.

**T-State:**
A T-State is one clock cycle of the µP.
∴T = Clock Period = 1/Clock Frequency

**Machine Cycle:**
It is the time required by the µP doing one operation and accessing one byte from the external module (Memory or I/O)

## Machine Cycles of 8085

The Machine cycles of 8085 are given below:

| Name | IO/M | RD | WR | S1 | S0 | INTA | T-States |
|---|---|---|---|---|---|---|---|
| Opcode Fetch | 0 | 0 | 1 | 1 | 1 | 1 | **4/6** |
| Mem Read | 0 | 0 | 1 | 1 | 0 | 1 | 3 |
| Mem Write | 0 | 1 | 0 | 0 | 1 | 1 | 3 |
| IO Read | 1 | 0 | 1 | 1 | 0 | 1 | 3 |
| IO Write | 1 | 1 | 0 | 0 | 1 | 1 | 3 |
| Int. Acknowledge | 1 | 1 | 1 | 1 | 1 | 0 | **3 or 6** |
| Bus Idle | 0 | 1 | 1 | 0 | 0 | 1 | 3 |

BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

## Opcode Fetch

- This cycle is used to **fetch** the **Opcode from** the **memory**.
- This is the **First** Machine Cycle of every instruction.
- It is a **compulsory** Machine Cycle
- It is **generally** of **4 T**-States but **some** instructions require a **6 T**-State Opcode Fetch.

**During T1**

- **A15-A8** contains the higher byte of the address (**PCH**)
- As **ALE** is **high AD7-AD0** contains the lower byte of the address(**PCL**).
- Since it is an Opcode fetch cycle, **S1** and **S0** go **high**.
- Since it is a memory operation, **IO/M** goes **low**.

**During T2**

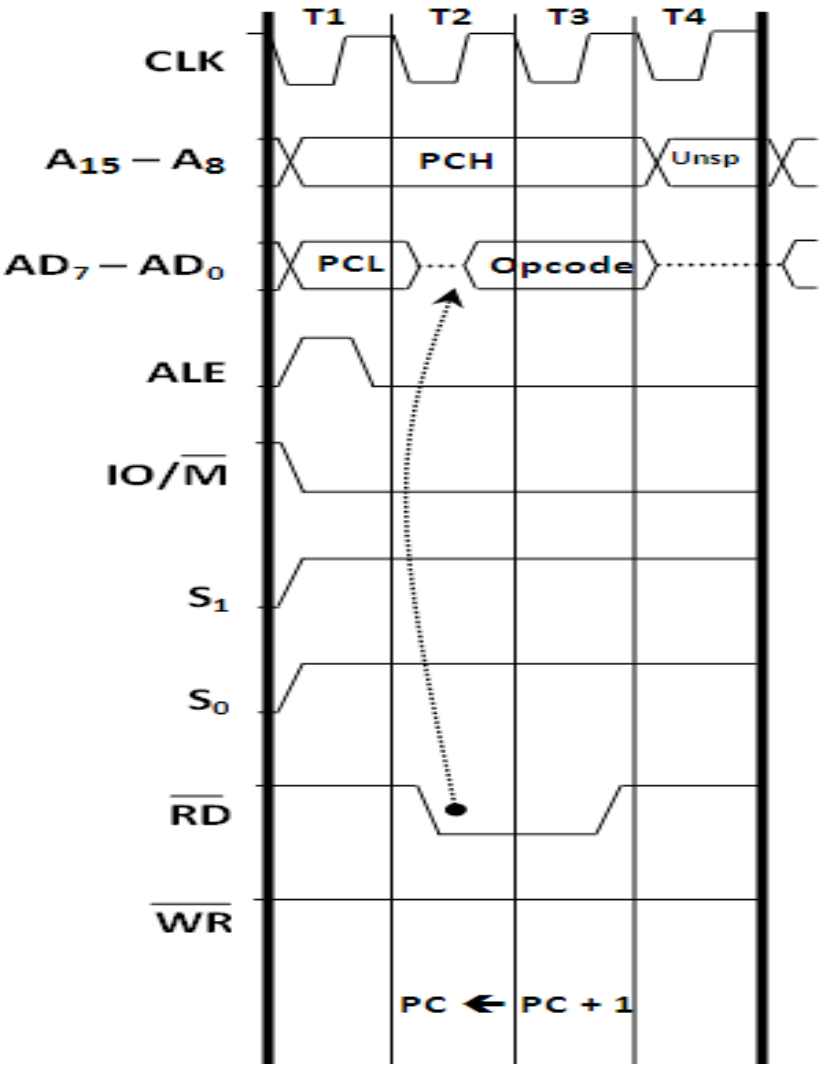
- As **ALE** goes **low** address is removed from AD7-AD0.
- As **RD** goes **low**, **data** appears **on AD7-AD0**. ☺ In case of doubts, contact Bharat Sir: - 98204 08217.
- The µP examines the state of the READY pin. If it is low then the µP enters wait-state by executing wait cycles and remains in the wait-state until READY goes high.

**During T3**

- Data remains on AD7-AD0 till RD is low.

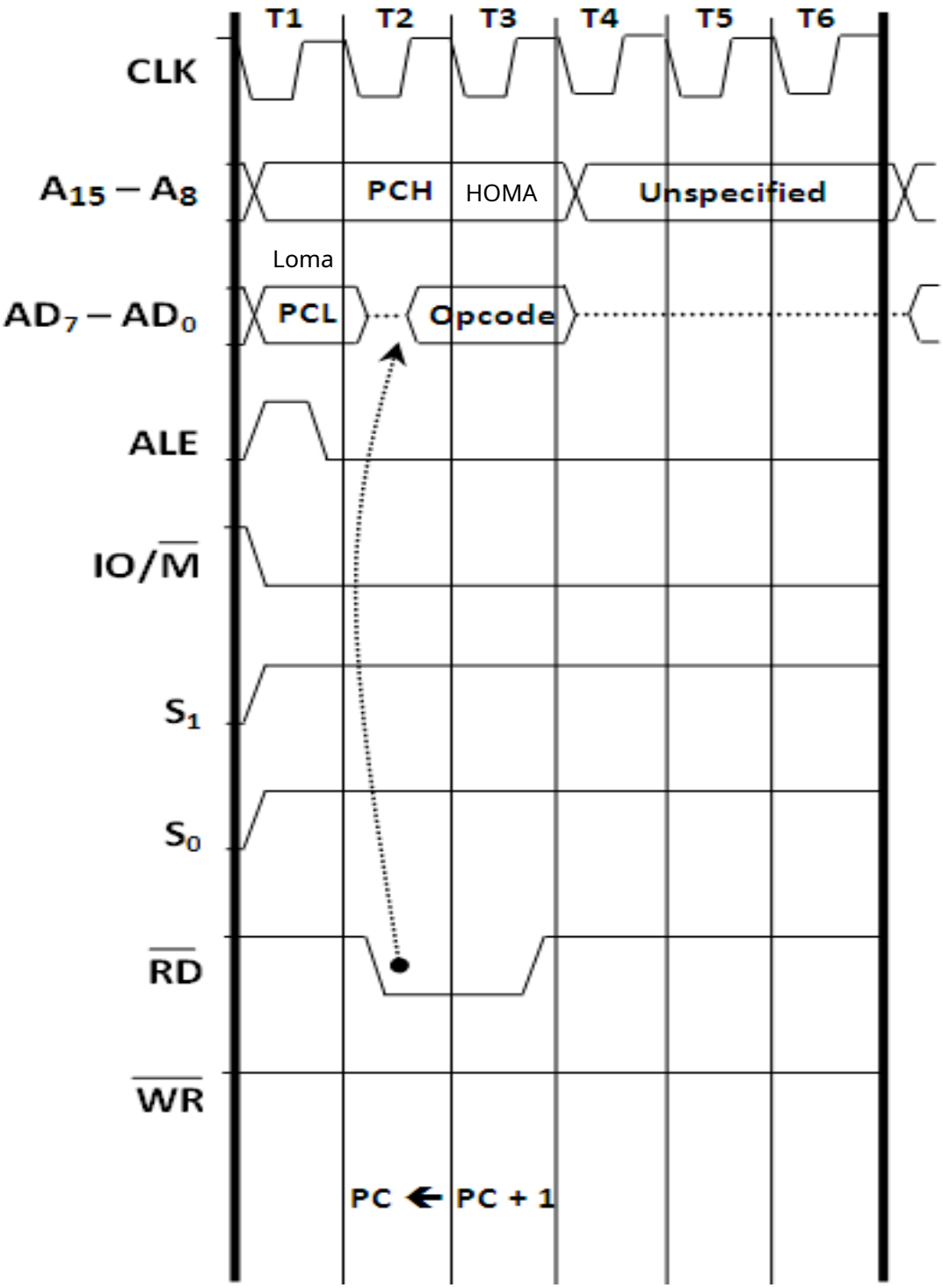
**During T4**

- T4 state is used by the µP to decode the Opcode.



BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

# Opcode Fetch of 6 T-States



BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

## Memory Read

- This cycle is used to **fetch one byte from** the **memory**.
- This cycle can be used to fetch the operand bytes of an instruction or any data from the memory.
- It is a not compulsory Machine Cycle
- It requires **3 T-States**.

**During T1**

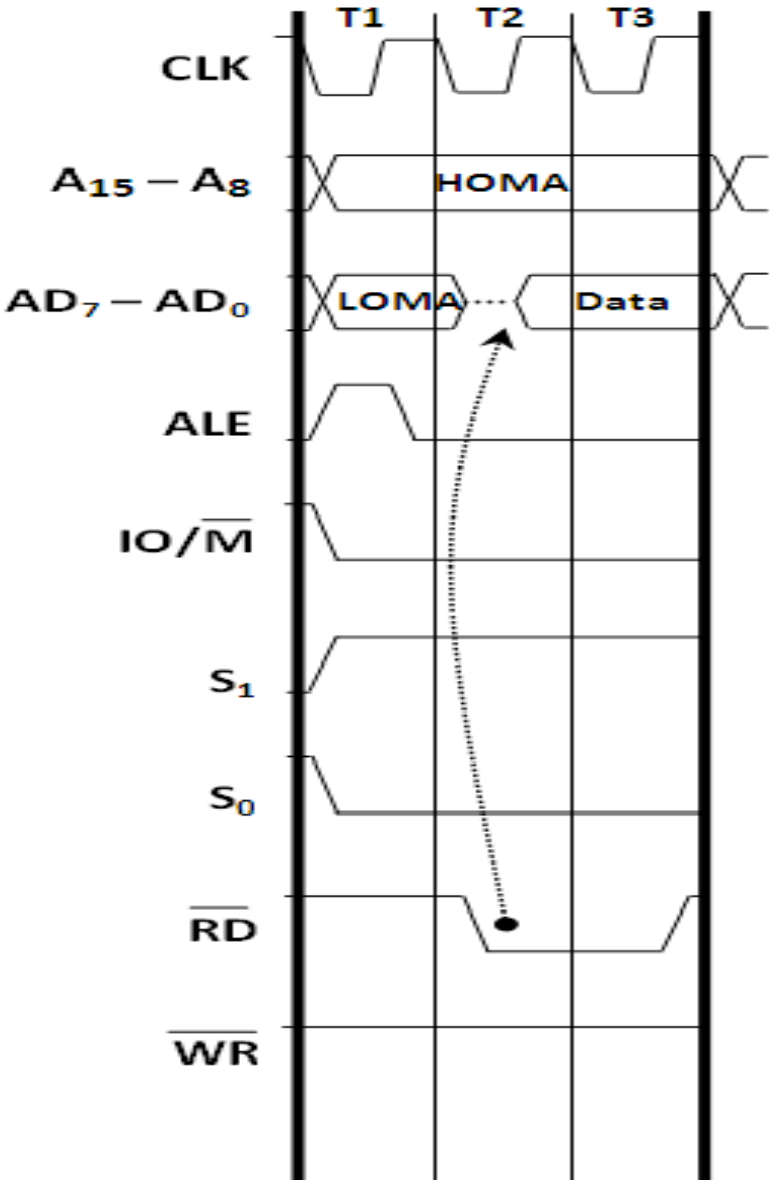
- **A15-A8** contains the higher byte of the address (**PCH**)
- As **ALE** is **high**, **AD7-AD0** contains the lower byte of the address (**PCL**).
- Since it is a Memory Read cycle, **S1** goes **high**.
- Since it is a memory operation, **IO/M** goes **low**.

**During T2**

- **ALE** goes **low**.
- Address is removed from AD7-AD0.
- As **RD** goes **low, data** appears **on AD7-AD0**.

**During T3**

- Data remains on AD7-AD0 till RD is low.



BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

## Memory Write

- This cycle is used to **send** (write) **one byte into** the **memory**.
- It is a not compulsory Machine Cycle
- It requires **3 T-States**.

**During T1**

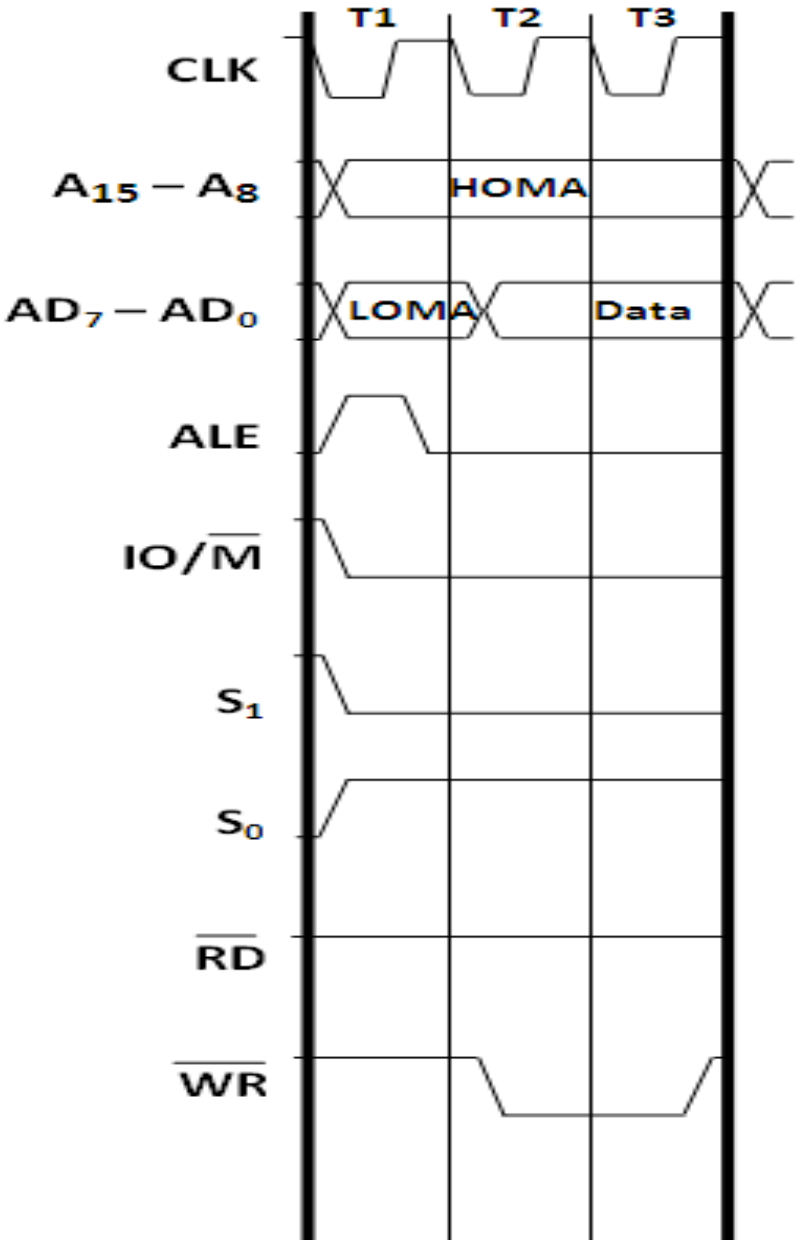
- **A15-A8** contains the higher byte of the address (**PCH**)
- As **ALE** is **high**, **AD7-AD0** contains the lower byte of the address (**PCL**).
- Since it is a Memory Write cycle, **S0** goes **high**.
- Since it is a memory operation, **IO/M** goes **low**.

**During T2**

- **ALE** goes **low**.
- Address is removed from AD7-AD0.
- **Data** appears **on AD7-AD0** and **WR** goes **low**.

**During T3**

- Data remains on AD7-AD0 till WR is low.



BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

## IO Read

- This cycle is used to **fetch one byte from** an **IO Port**.
- It is a not compulsory Machine Cycle
- It requires **3 T-States**.

**During T1**

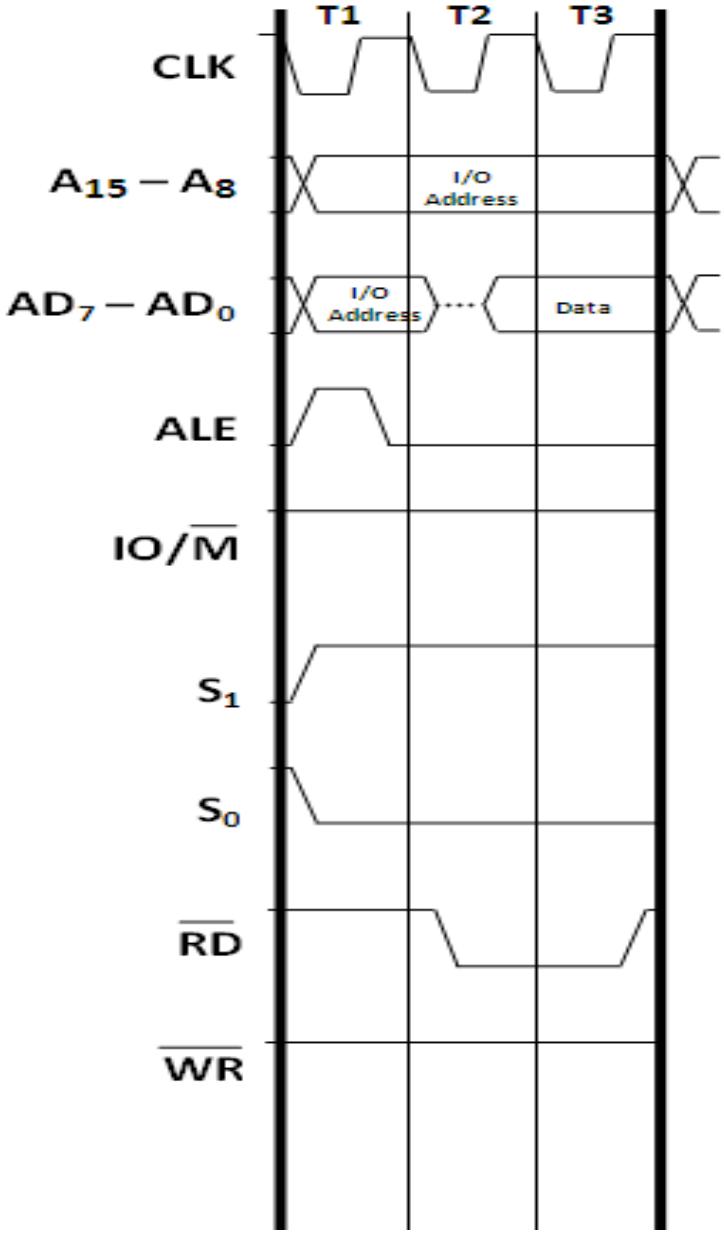
- The **lower 8 bits of the IO Port Address** are **duplicated into** the higher order address bus **A15-A8**.
- As **ALE** is **high AD7-AD0 contains** the **lower byte of** the **address**
- Since it is an IO **Read** cycle **S1** goes **high**.
- Since it is an **IO** operation **IO/M** goes **high**.

**During T2**

- **ALE** goes **low.**
- Address is removed from AD7-AD0.
- As **RD** goes **low**, **data** appears on **AD7-AD0**.

**During T3**

- Data remains on AD7-AD0 till RD is low.



BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

## IO Write

- This cycle is used to **send** (write) **one byte into** an **IO Port**.
- It is a not compulsory Machine Cycle
- It requires **3 T-States.**

**During T1**

- The **lower 8 bits of the IO Port Address** are **duplicated into** the higher order address bus **A15-A8**.
- As **ALE** is **high AD7-AD0 contains** the **lower byte of** the **address**
- Since it is an IO **Write** cycle, **S0** goes **high**.
- Since it is an **IO** operation, **IO/M** goes **high**.

**During T2**

- **ALE** goes **low.**
- Address is removed from AD7-AD0.
- **Data** appears **on AD7-AD0** and **WR** goes **low**.

**During T3**

- Data remains on AD7-AD0 till RD is low.