Lecture Notes
for
Semiconductor Devices and Circuits : JFET and MOSFET

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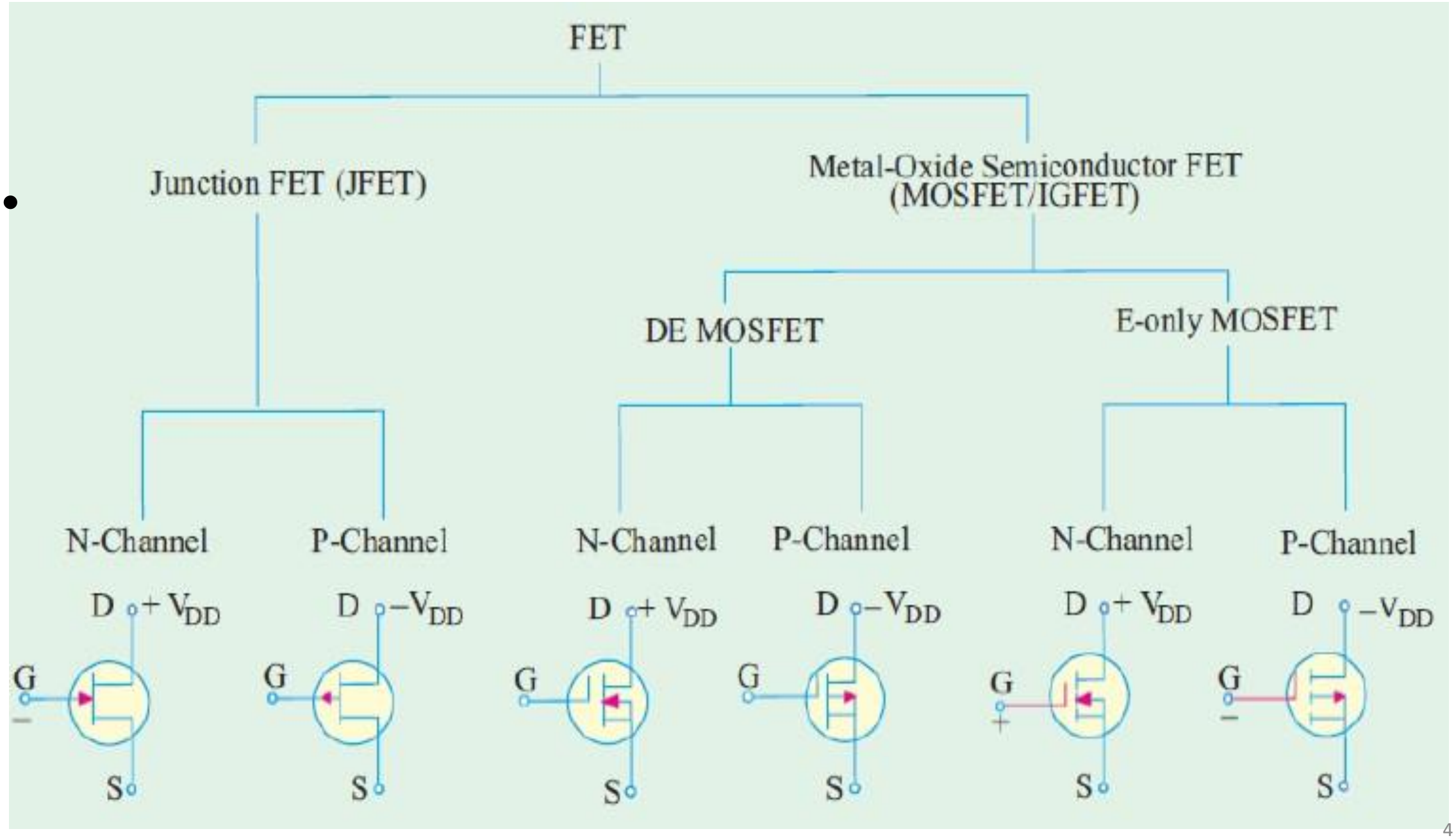
Contents

1. FIELD EFFECT TRANSISTOR (FET)

- FET is a three terminal semiconductor device. It is unipolar transistor i.e. depends only on one type of charge carrier, either electron or hole.
- The current is controlled by the applied electric field hence, it is a voltage controlled device.
- FET is simple to fabricate and occupies less space on a chip than a BJT. About 100000 FETs can be fabricated in a single chip. This makes them useful in VLSI (very large scale integrate) system.
- It have high input Impedances and Low output Impedance so they are used as buffers at the front end of voltage and other measuring devices.
- It has small coupling capacitances, as a result, they are used in hearing aids.
- There are two types of FET – the JFET (Junction Field Effect Transistor) and MOSFET (Metal Oxide Semiconductor Field Effect Transistor)


FET
Junction FET (JFET)
Metal-Oxide Semiconductor FET
(MOSFET/IGFET)
DE MOSFET
E-only MOSFET
N-Channel
P-Channel
N-Channel
P-Channel
N-Channel
P-Channel
D
+ VDD
G
S
D
−VDD
G
S
D
+ VDD
G
S
D
−VDD
G
S
D
+ VDD
G
S
D
−VDD
G
S

2. Junction Field Effect Transistor (JFET)

- It is of two types

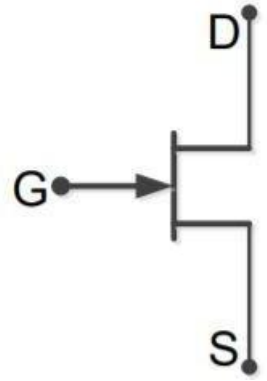
❑ P-channel JFET

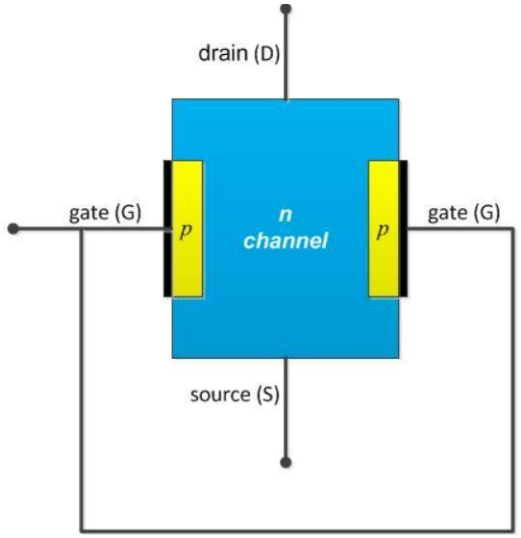
❑ n-channel JFET

- The n- channel JFET consists of a bar of n-type semiconductor with two islands of p- type material embedded in the sides. The drain and source terminals are made by ohmic contacts at the end of p-type of semiconductor bar . Majority charge carrier i.e. electrons can be cause to flow along length of bar by means of a voltage applied between the source and drain .The electrons leave from drain the third terminal, known as the gate is formed by electrically connecting the two p-type regions

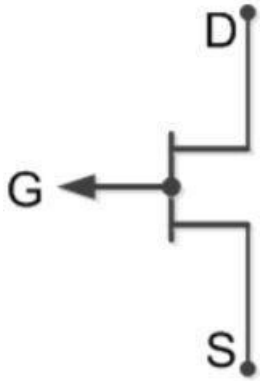
- The circuit symbol of p- channel JFET is similar to that of an n-channel JFET except that the gate arrow points outward as shown in below.

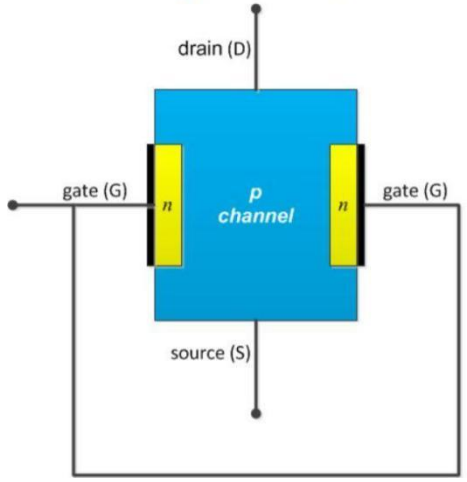
- **Symbol & Structure of n-channel JFET**





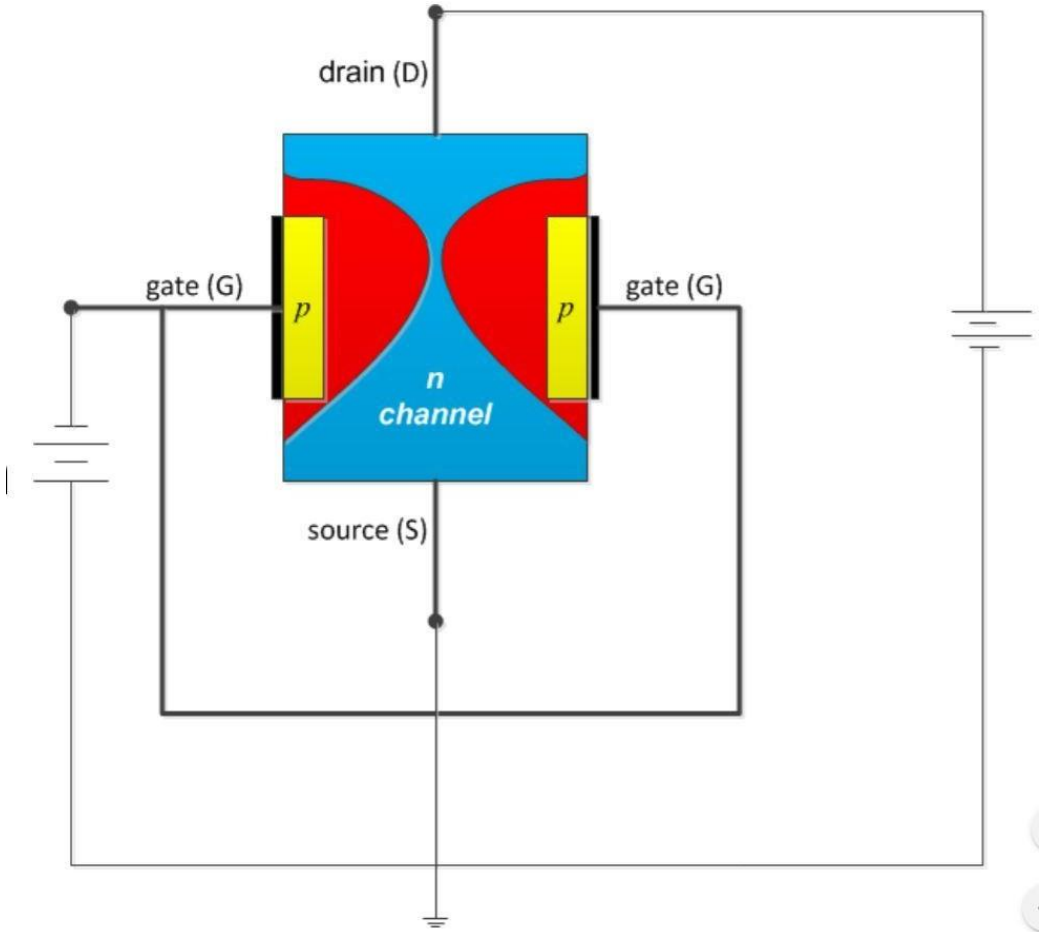
- **Symbol & Structure of p-channel JFET**

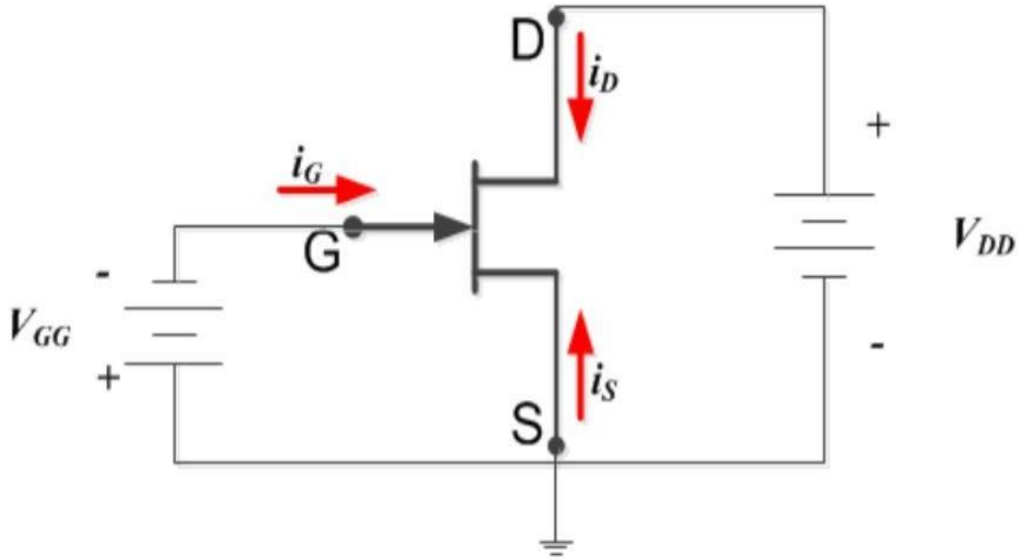




2.1 JFET Operation and Circuit analysis

- **Figure shows an n-channel JFET in the common source configuration showing the depletion region**





2.1 JFET Operation

- The Gate and channel constitute a PN junction diode which is reverse biased by the gate to the source voltage.
- A depletion layer is developed in the channel as reverse bias increases the width of depletion layer increases.
- For a fixed drain to source voltage, the drain current will be a function of reverse bias voltage across the gate junction.
- At a gate-to-source voltage $V_{GS}=V_p$ known as the “Pinch- off” voltage which eliminates the channel, the channel width is reduces to zero.
- The term Field Effect is used to describe this device because of mechanism to control current using reverse bias voltage $V_{GS.}$

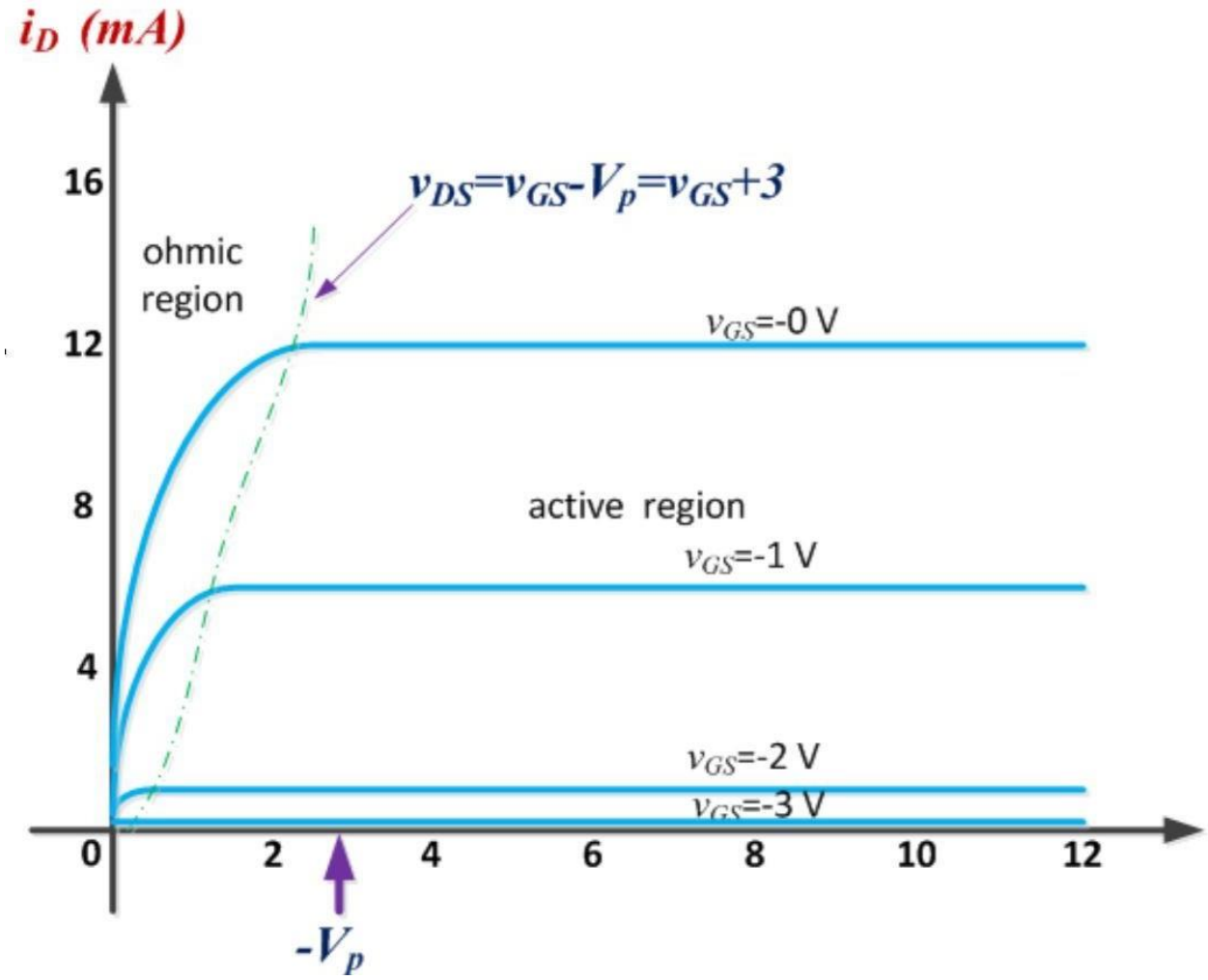
2.2 Drain characteristics

I_{DSS}= 12mA and pinch off voltage is Vp= -3V.

If v_{GS}=0 V, channel pinch off when v_{DS}= - V_p=3V

If v_{GS} =-1V, channel pinch off at v_{DS} = v_{GS} - V_p = -1+3=2V

The dashed curve is corresponding to v_{DS} = v_{GS} - V_p To the right of this curve , (v_{DS} > v_{GS} - V_p), The channel is pinched off and this region is called as pinch off region or **saturation region**.
(active region). To the left of this curve, (v_{DS} < v_{GS} - V_p), the channel is not pinched off and the region is called as **ohmic region**.
When the gate is sufficiently reverse biased , channel will be totally eliminated for v_{GS} < V_p, under this circumstances increasing v_{DS}, will not be sufficient to produce a drain current. i_D=0 and JFET is said to be in cutoff.



Important Parameters of JFET

- Transconductance (g_m) :It is given by $g_m = (I_d/V_{GS})\Big|_{V_{DS}}$

i.e. It is the ratio of change in drain current to the change in gate source voltage at constant drain source voltage.

- Output resistance (r_d):It is given by $r_d = (V_{DS}/I_d)\Big|_{V_{GS}}$

i.e. It is the ratio of change in AC drain source voltage to the change in AC drain current at constant gate source voltage

- Amplification factor(❍):It is defined as ❍ = $(-V_{DS}/V_{GS})\Big|_{I_D}$

i.e. It is the change in the AC drain-voltage

2.3 Comparison Between FET and BJT

FET	BJT
i) Carriers of only one type i.e either electron or hole (majority carrier) are responsible for the conduction.	i) Carriers- electron and hole (majority and minority carrier)-involved in current conduction
ii) It is the drift mechanism that helps the movement of carriers	ii) The carriers are transported by the process of diffusion.
iii) More stable than BJT.	iii) Less stable than FET
iv) The FET is voltage controlled device or voltage amplifier.	iv) It is current controlled device or current amplifier
v) Input impedance offered much higher than BJT	v) Input impedance offered is Less
vi) Easy to fabricate and required less space and hence all the ICs use as their basic technology and preferred VLSI design.	vi) Not easy as compared to FET.
vii) Less noisy compared to BJT thats way extensively used in communication devices.	vii) Required more space than FET.
viii) Offers high power gain compared to BJT	vii) More noisy than FET.

3. MOSFET

- A FET is made by growing a very thin layer of SiO_2 (0.1μm) over a semiconductor material . Metal such as aluminium is deposited over dielectric layer of SiO_2 is known as MOSFET/metal oxide semiconductor field effect

Similar to JFET , It has n-channel as well as p-channel .Construction wise we can categorise the device into four types

i. P-channel Enhancement MOSFET
ii. n-channel Enhancement MOSFET
iii. n-channel Depletion MOSFET
iv. p-channel Depletion MOSFET

3.1 The ideal MOS Structure have the following explicit properties

i. The metallic gate is sufficiently thick so that it can be considered to be an equipotential region under both AC and DC biasing.

ii. The oxide is perfect insulator with zero current flowing through the oxide layer under all static biasing condition.

iii. There are no charge centers located in the oxide or in oxide semiconductor interface .

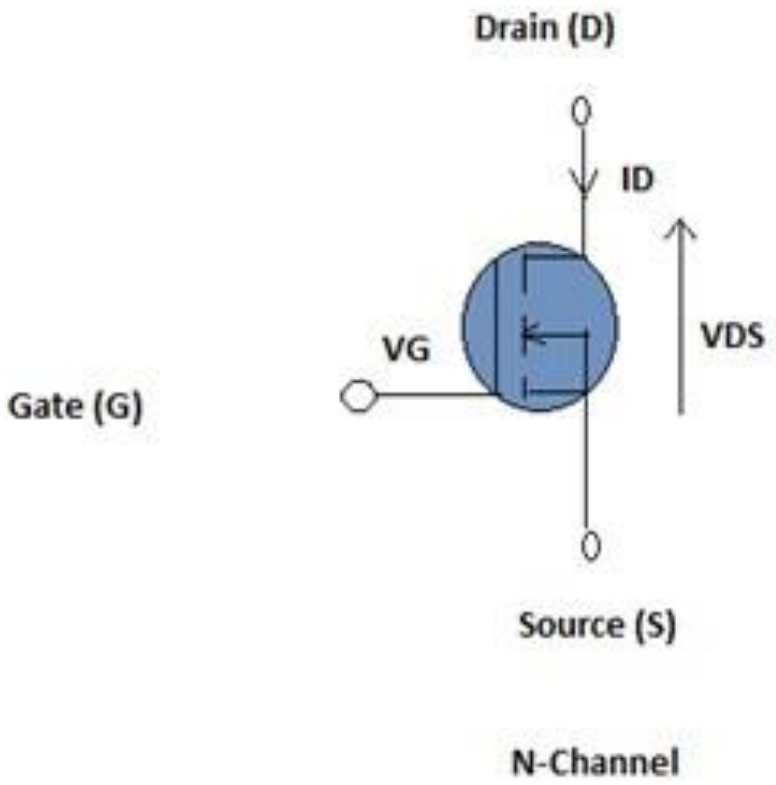
iv. The semiconductor is sufficiently thick to ensure that regardless of the applied gate potential, a field-free region is encountered before reaching the black contact.

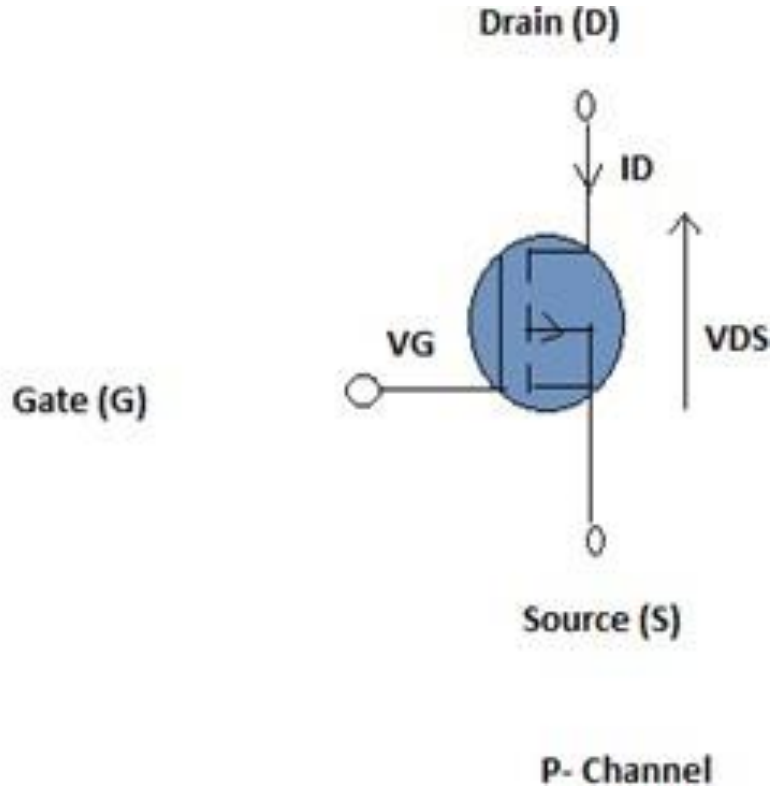
v. The semiconductor is uniformly doped.

vi. An ohmic contact has been established between the semiconductor and the metal on the black side of the device.

3.2 Enhancement mode

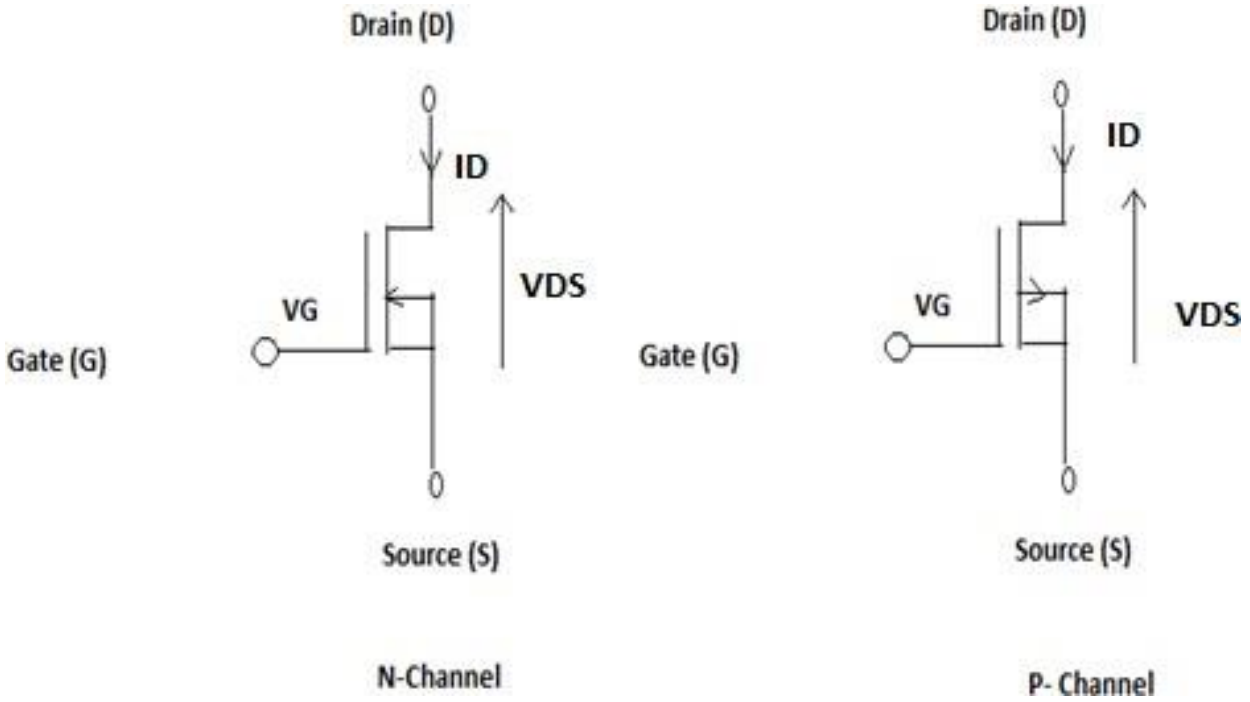
When there is no voltage on the gate, the device doesn't conduct. More voltage on the gate, the better the device can conduct.





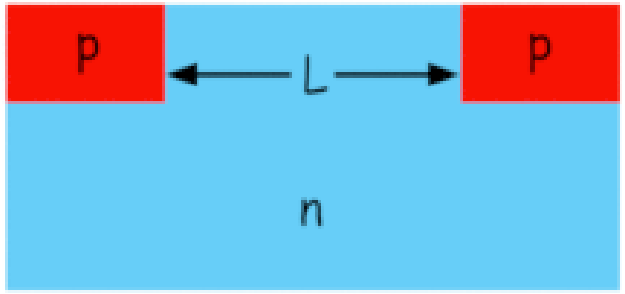
3.3 Depletion mode

When No Voltage On The Gate, The Channel Shows Its Maximum Conductance. As The Voltage On The Gate Is Either Positive Or Negative, The Channel Conductivity Decreases.

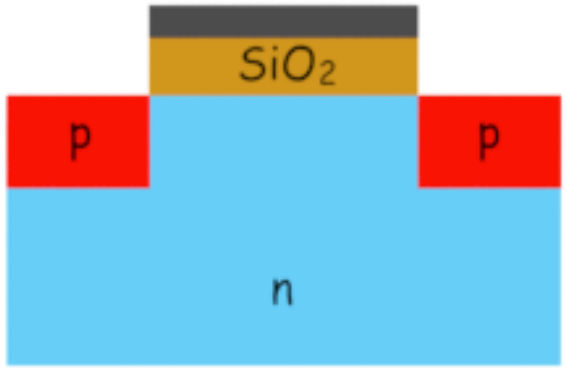


i) P – Channel Enhancement MOSFET

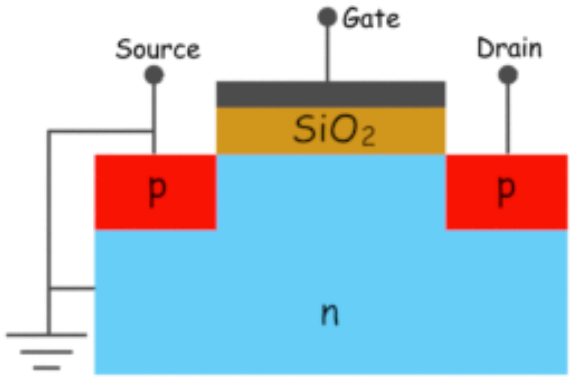
- We also call the **p channel MOSFET** as **PMOS**. Here, a substrate of lightly doped n-type semiconductor forms the main body of the device. We usually use silicon or gallium arsenide semiconductor material for this purpose. Two heavily doped p-type regions are there in the body separated by a certain distance L. We refer this distance L as **channel length** and it is in order of 1 µm.



- Now there is a thin layer of silicon dioxide (SiO_2) on the top of the substrate. We may also use Al_2O_3 for the purpose but SiO_2 is most common. This layer on the substrate behaves as a dielectric. There is an aluminum plate fitted on the top of this SiO_2 dielectric layer. Now the aluminum plate, dielectric and semiconductor substrate form a capacitor on the device.



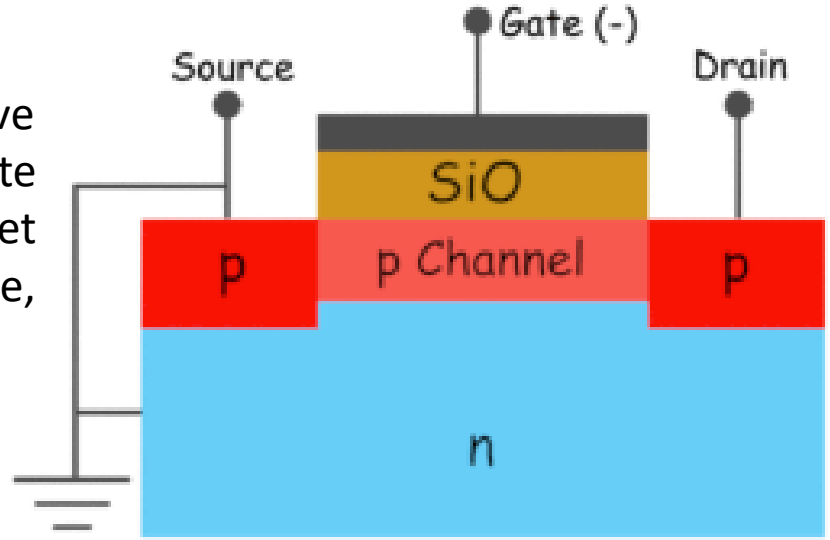
- The terminals connected to two p-type regions are the source (S) and drain (D) of the device respectively. The terminal projected from the aluminum plate of the capacitor is gate (G) of the device. We also connect the source and body of the MOSFET to earth to facilitate the supply and withdrawal of free electrons as per requirement during operation of the MOSFET



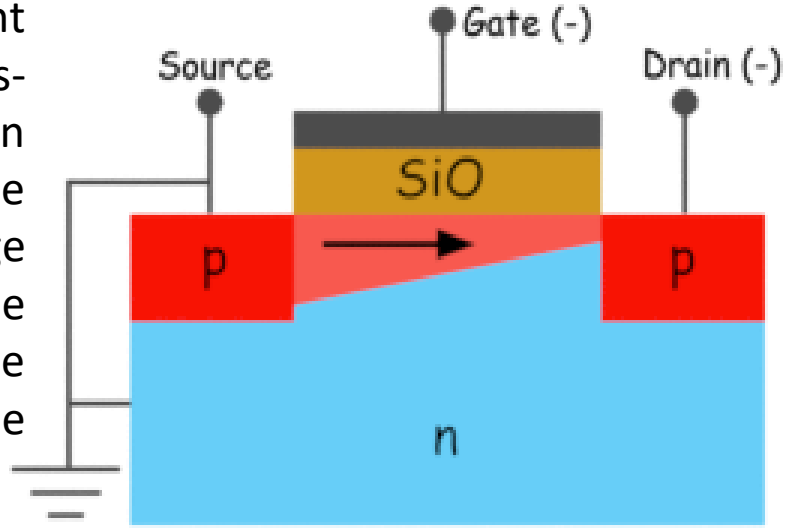
- Now let us apply a negative voltage at gate (G). This will create negative static potential at the aluminum plate of the capacitor. Due to capacitive action, positive charge gets accumulated just below the dielectric layer.

Basically, the free electrons of that portion of the n-type substrate get shifted away due to the repulsion of negative gate plate and consequently layers of uncovered positive ions appear here. Now if we further increase the negative voltage at the gate terminal, after a certain voltage called threshold voltage, due to the electrostatic force, covalent bonds of the crystal just below the SiO_2 layer start breaking. Consequently, electron-hole pairs get generated there. The holes get attracted and free electrons get repealed due to the negativity of the gate. In this way, the concentration of holes increases there and create a channel of holes from source to drain region. Holes also come from both heavily doped p-type source and drain region. Due to the concentration of holes in that channel the channel becomes conductive in nature through which electric current can pass

- Now, let us apply a negative voltage at drain terminal. The negative voltage in the drain region reduces the voltage difference between gate and drain reduces, as a result, the width of the conductive channel get reduced toward the drain region as shown below. At the same time, current flows from source to drain shown by arrowhead.



- The channel created in the MOSFET offers a resistance to the current from source to drain. The resistance of the channel depends on the cross-section of the channel and the cross section of the channel again depends on the applied negative gate voltage. So we can control the current from the source to drain with the help of an applied gate voltage hence MOSFET is a voltage controlled electronic device. As the concentration of holes forms the channel, and the current through the channel gets enhanced due to increase in negative gate voltage, we name the MOSFET as P – Channel Enhancement MOSFET.



3.4 I-V Characteristics

- The transfer characteristics of **p-type enhancement MOSFETs** from which it is evident that I_{DS} remains zero (cutoff state) until V_{GS} becomes equal to $-V_T$. This is because, only then the channel will be formed to connect the drain terminal of the device with its source terminal.

- After this, the I_{DS} is seen to increase in reverse direction (meaning an increase in I_{SD}, signifying an increase in the device current which will flow from source to drain) with the decrease in the value of V_{DS}.

- This means that the device is functioning in its ohmic region wherein the current through the device increases with an increase in the applied voltage (which will be V_{SD}).

- However as V_{DS} becomes equal to $-V_P$, the device enters into saturation during which a saturated amount of current (I_{DSS}) flows through the device, as decided by the value of V_{GS} .

- Further it is to be noted that the value of saturation current flowing through the device is seen to increase as the V_{GS} becomes more and more negative i.e. saturation current for V_{GS3} is greater than that for V_{GS2} and that in the case of V_{GS4} is much greater than both of them as V_{GS3} is more negative than V_{GS2} while V_{GS4} is much more negative when compared to either of them (Figure 2b)

- **In addition, from the locus of the pinch-off voltage it is also clear that as V_{GS} becomes more and more negative, even the negativity of V_P also increases.**

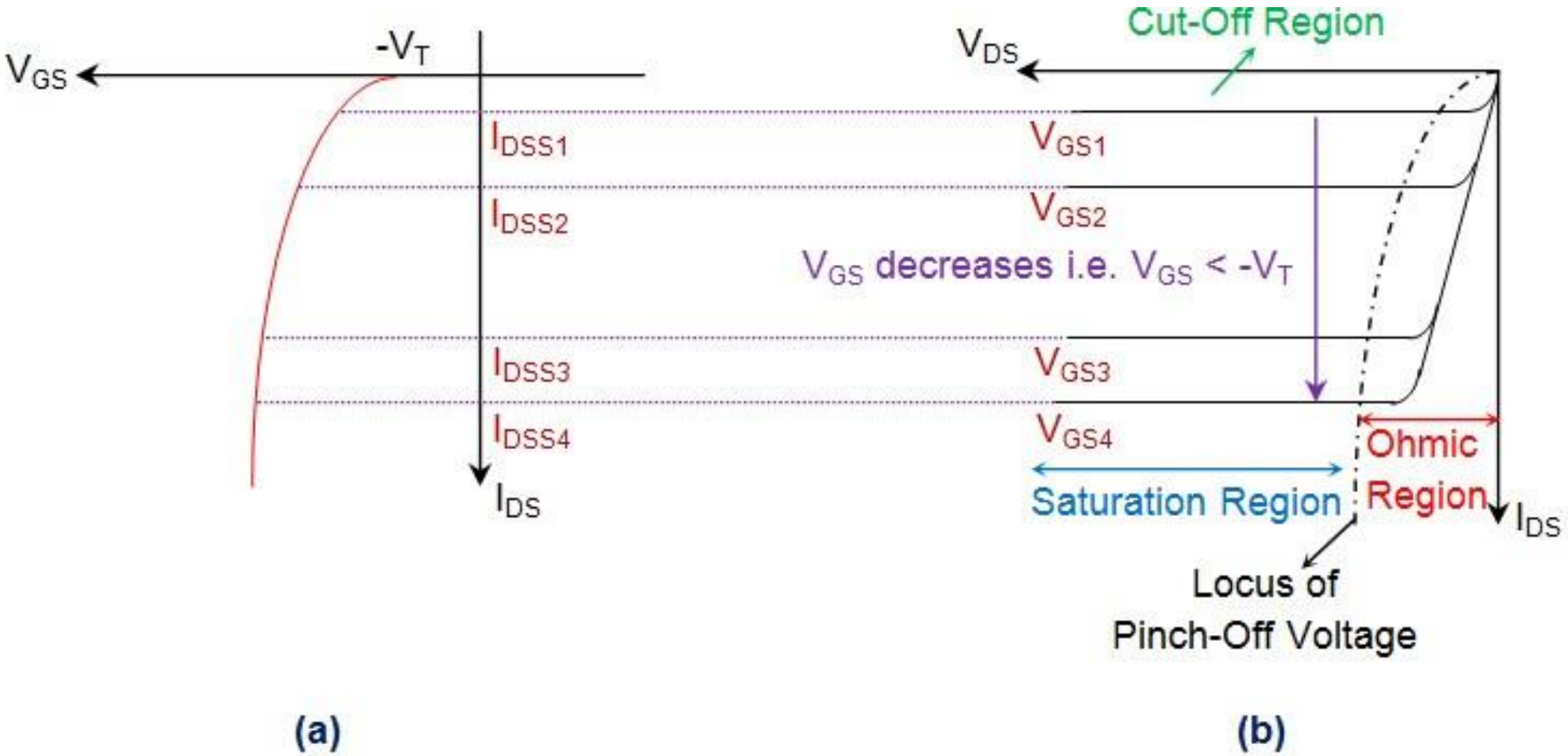
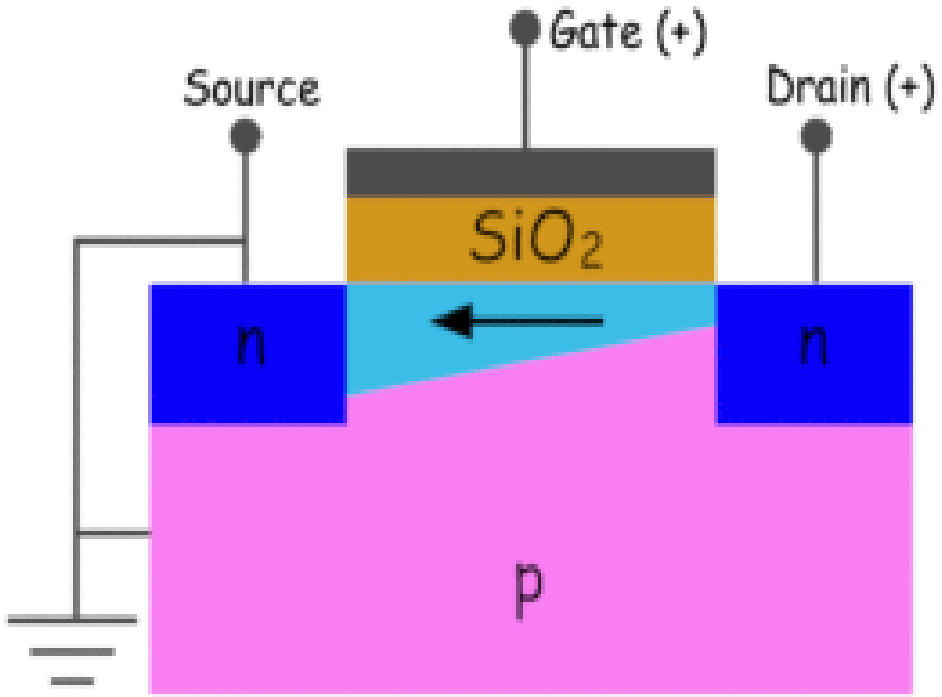


Figure 2 *p*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

ii) n – Channel Enhancement MOSFET

- **Its working is similar to that of p-channel enhancement MOSFET but only operationally and constructionally there are different from each other.**

- **The Characteristics is shown in figure**



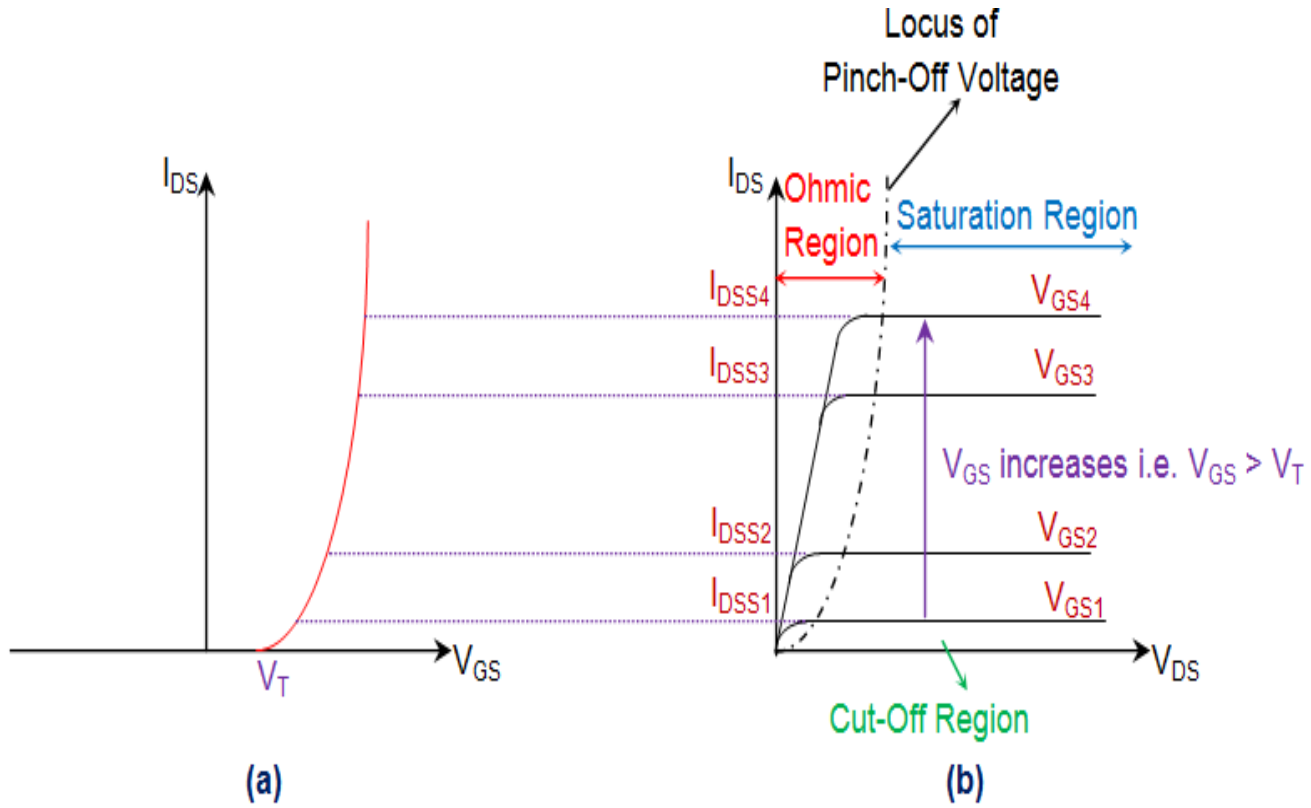


Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

iii) n-channel Depletion-type MOSFET

➢ **The construction and the characteristics regions are shown below**

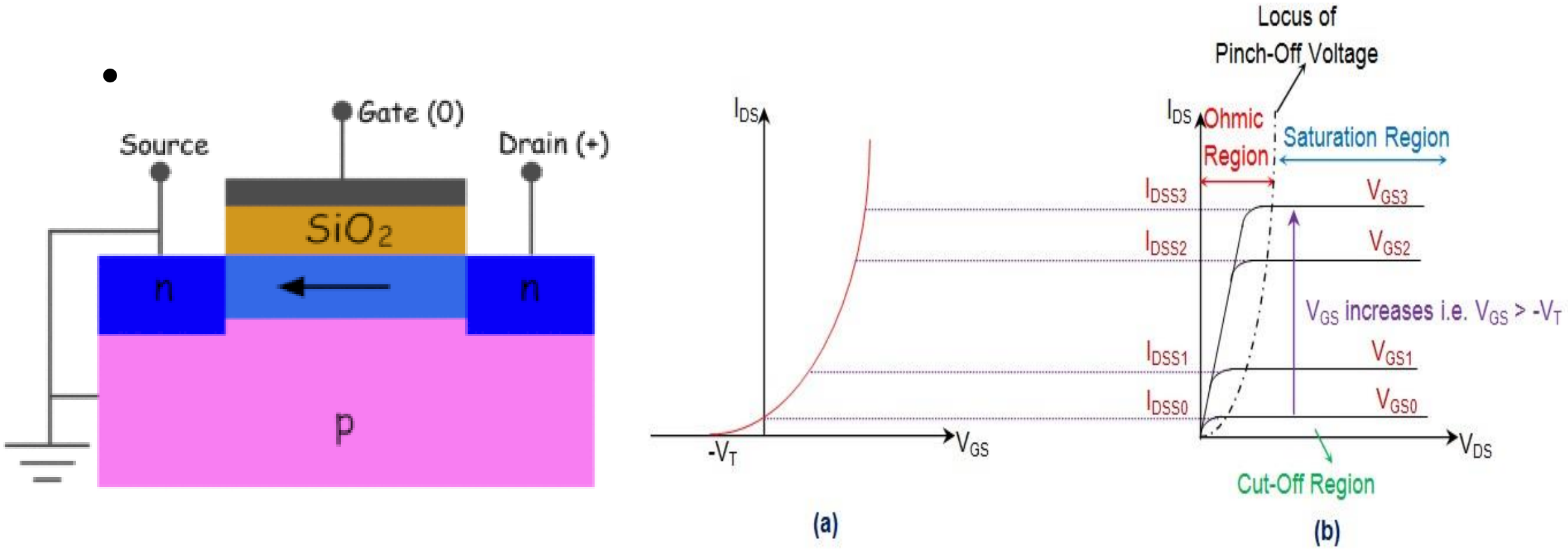
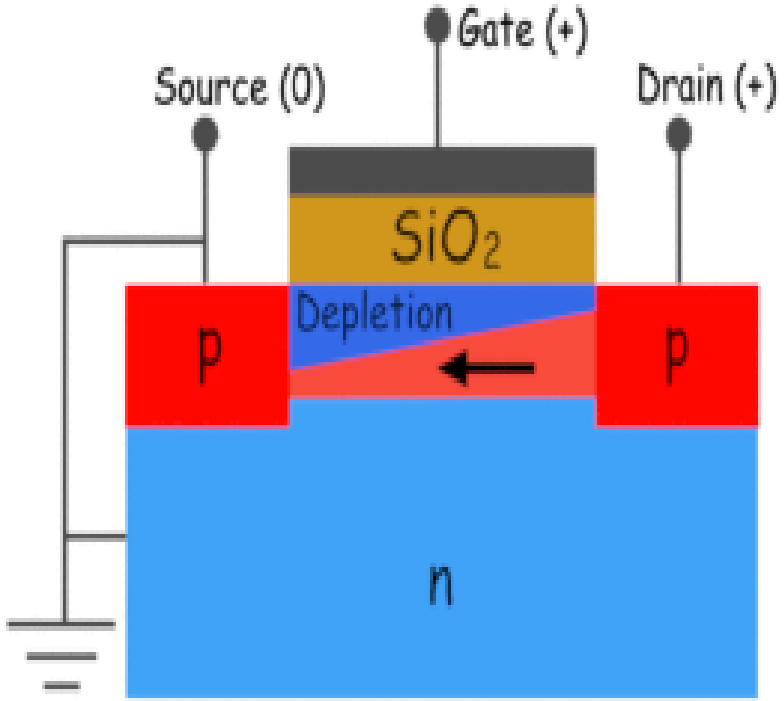


Figure 3 *n*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics

iv) p-channel Depletion-type MOSFET

- **Construction wise p-channel DE-MOSFET is just reverse of the n channel depletion MOSFET**



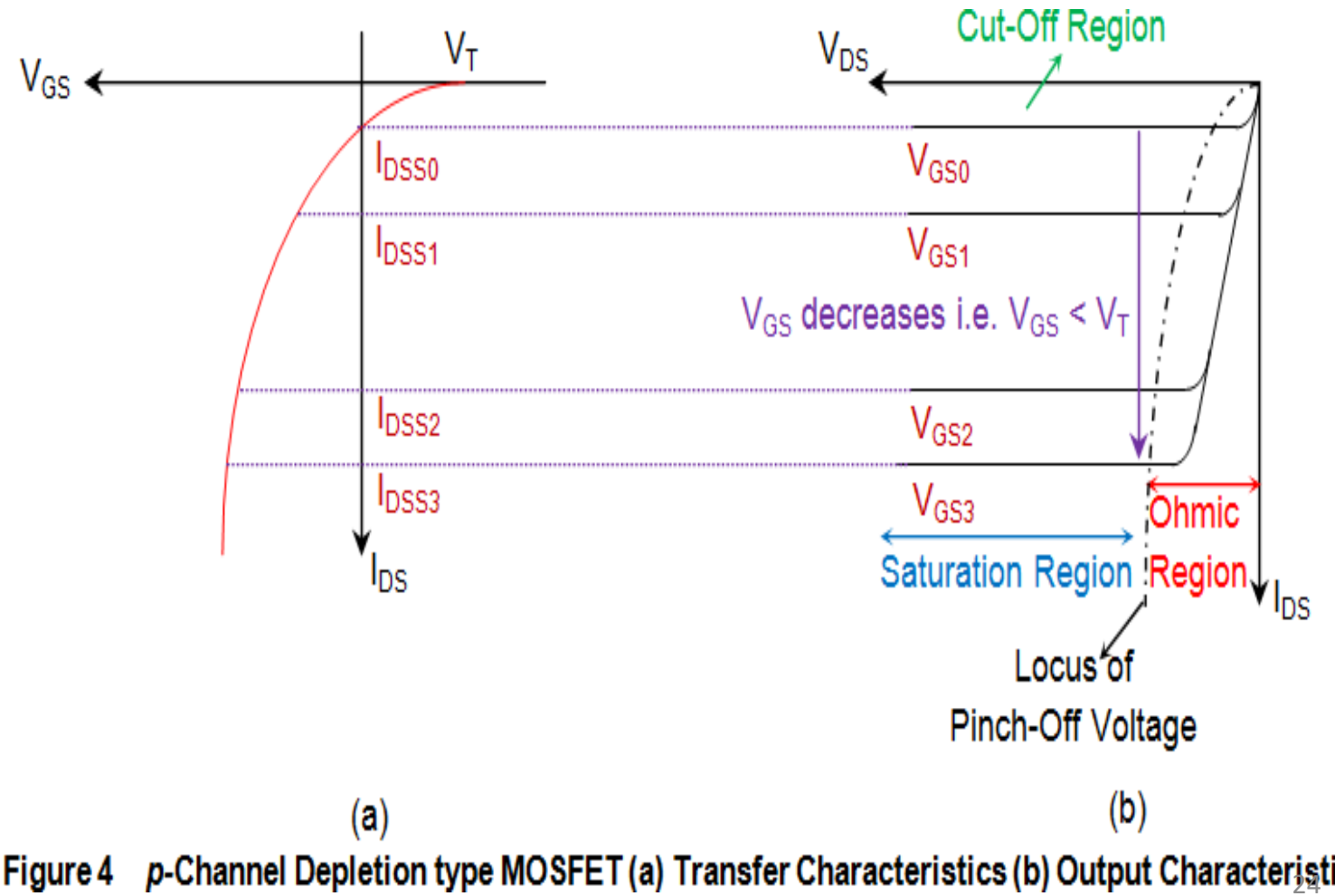


Figure 4 *p*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics

References

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