Biased *pn* Junction

Semiconductor Devices and Circuits

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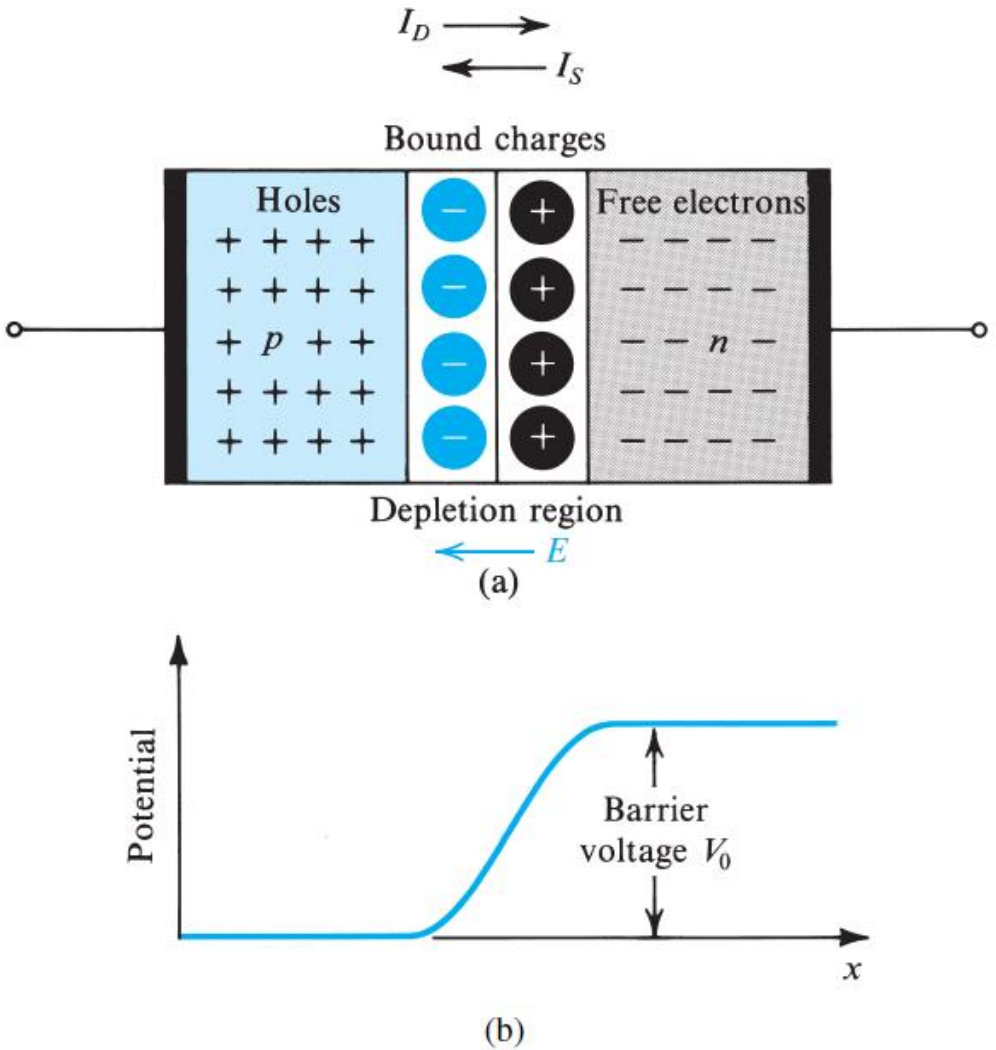
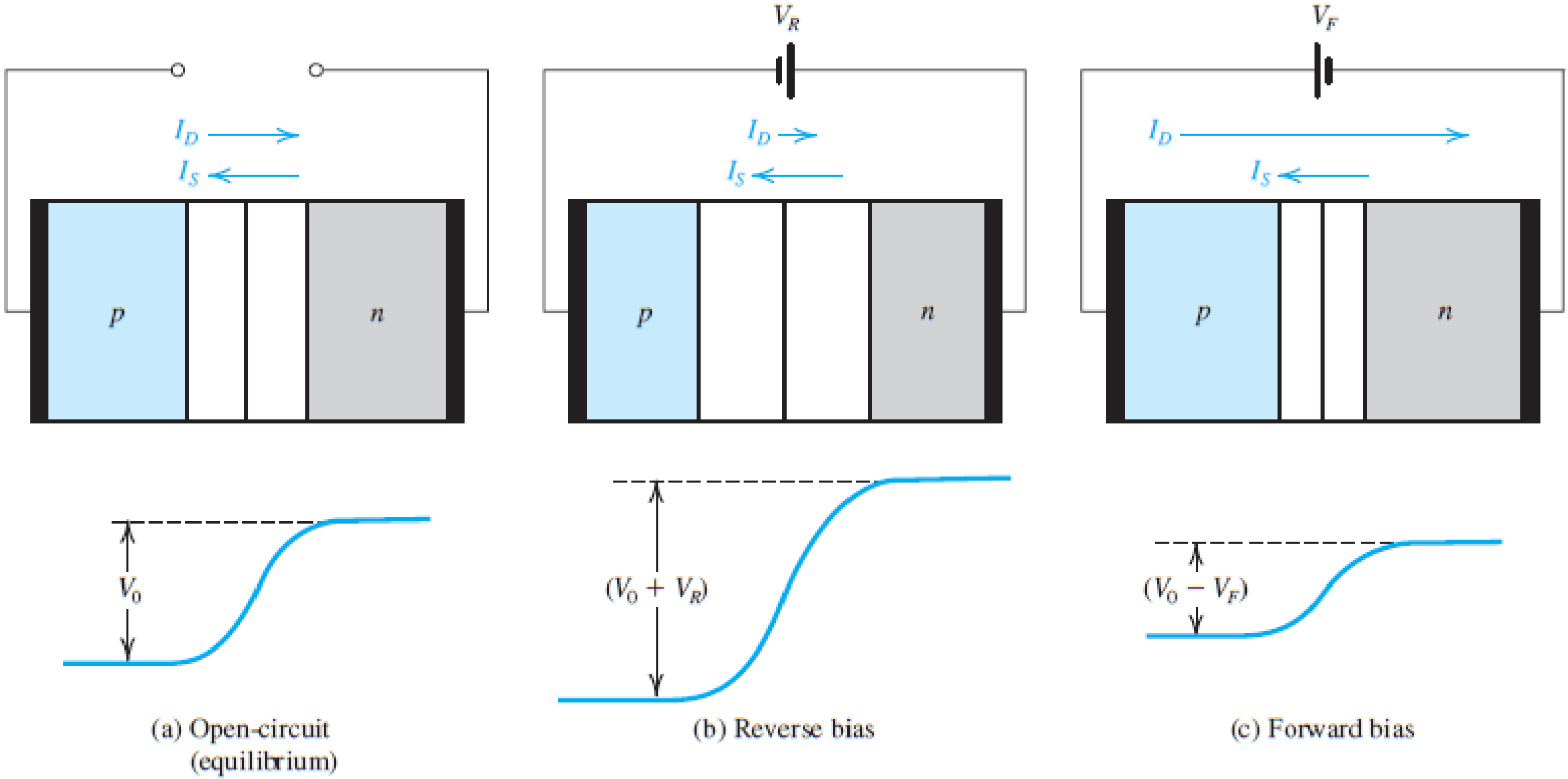
The *pn* Junction





(a) Open-circuit (equilibrium)

(b) Reverse bias

(c) Forward bias

Reversed Biased *pn* Junction

- The externally applied voltage V_R is in the direction to add to the barrier voltage, thus increasing the effective barrier voltage to $V_0 + V_R$.
- Reduces the number of holes that diffuse into the *n* region and the number of electrons that diffuse into the *p* region.
- The diffusion current I_D is dramatically reduced.
- A reverse-bias voltage of a volt or so is sufficient to cause $I_D = 0$.
- The current across the junction and through the external circuit = I_S (the current due to the drift of the thermally generated minority carriers across the depletion region).
- In the reverse direction, the *pn* junction conducts a very small and almost-constant current equal to I_S.

- The increase in barrier voltage will be accompanied by a corresponding increase in the stored uncovered charge on both sides of the depletion region.
- It means a wider/ extended depletion region needed to uncover the additional charge required to support the larger barrier voltage $V_0 + V_R$.
- The width of the depletion region can be obtained by replacing V_0 by $V_0 + V_R$ in

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

- The magnitude of the charge stored on either side of the depletion region can be determined by replacing V_0 in $V_0 + V_R$ in

$$Q_J = A\sqrt{2\epsilon_s q\left(\frac{N_A N_D}{N_A + N_D}\right)V_0}$$

Forward Biased *pn* Junction

- The applied external voltage V_F is in the direction that subtracts from the built-in voltage V_0, resulting in a reduced barrier voltage $V_0 - V_F$ across the depletion region.
- Reduced barrier voltage is accompanied by reduced depletion-region charge and correspondingly a narrower depletion-region width W.
- Lowering of the barrier voltage enables more holes to diffuse from *p* to *n* and more electrons to diffuse from *n* to *p*.
- Diffusion current I_D increases substantially and can become many orders of magnitude larger than the drift current I_S.
- The current I in the external circuit is the difference between I_D and I_S, and it flows in the forward direction of the junction, from *p* to *n*.

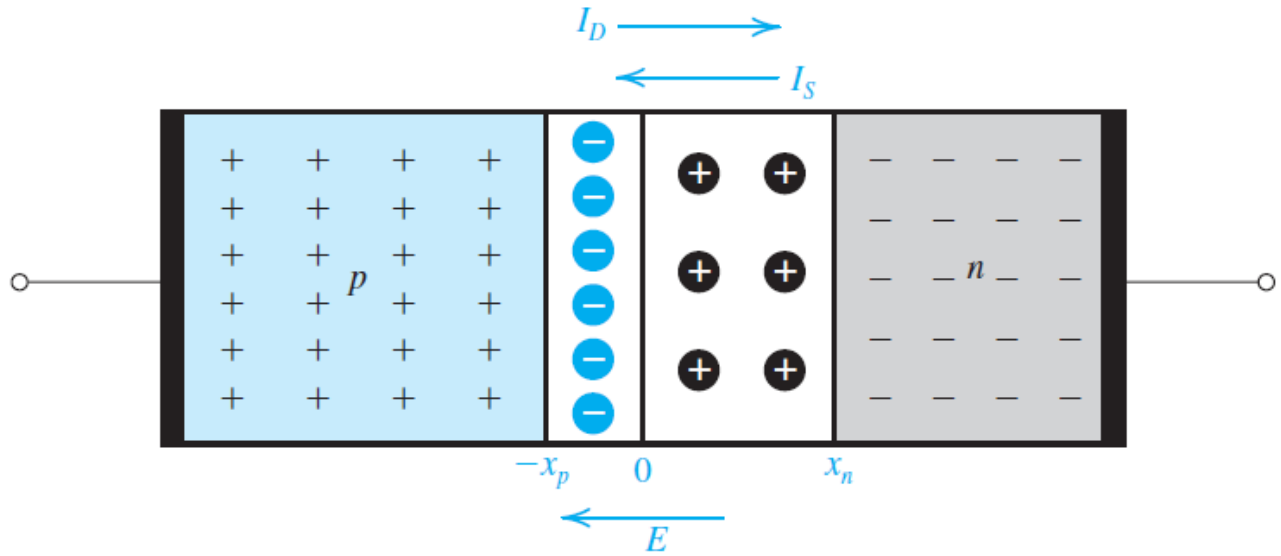
$$I = I_D - I_S$$

- The *pn* junction can conduct a substantial current in the forward-bias region and that current is mostly a diffusion current whose value is determined by the forward-bias voltage V_F.

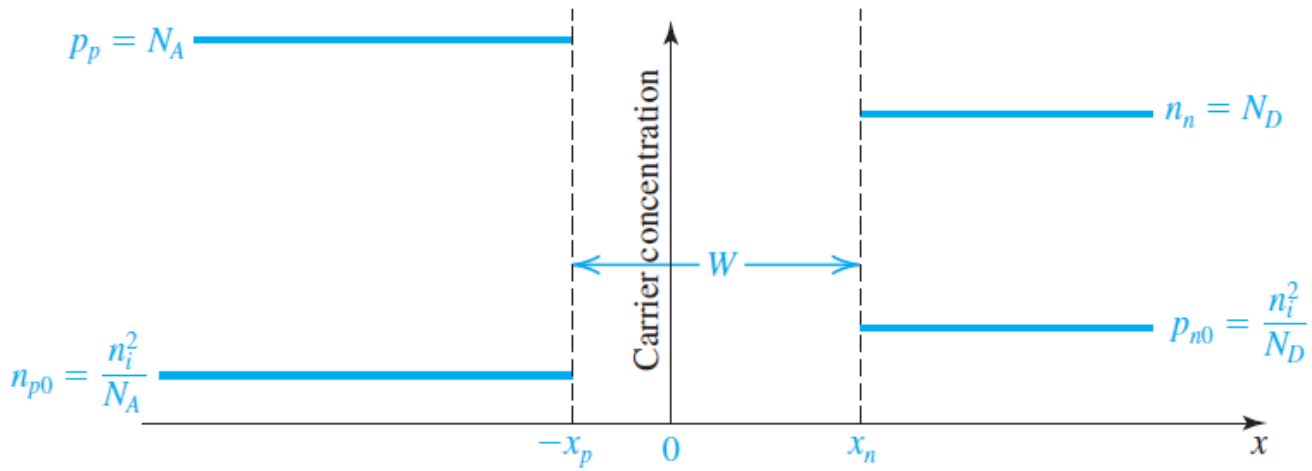
Current–Voltage (I-V) Relationship of the Forward Biased Junction

- The forward-bias voltage subtracts from the built-in voltage, lowering the barrier voltage making it possible for a greater number of holes to overcome the barrier and diffuse into the *n* region and electrons from the *n* region diffusing into the *p* region.
- The concentration of holes injected into the *n* region at the edge of the depletion region increases considerably.
- That is, the concentration of the minority holes increases from the equilibrium value of p_{n0} to a much larger value determined by the value of *V*, and it is given by:

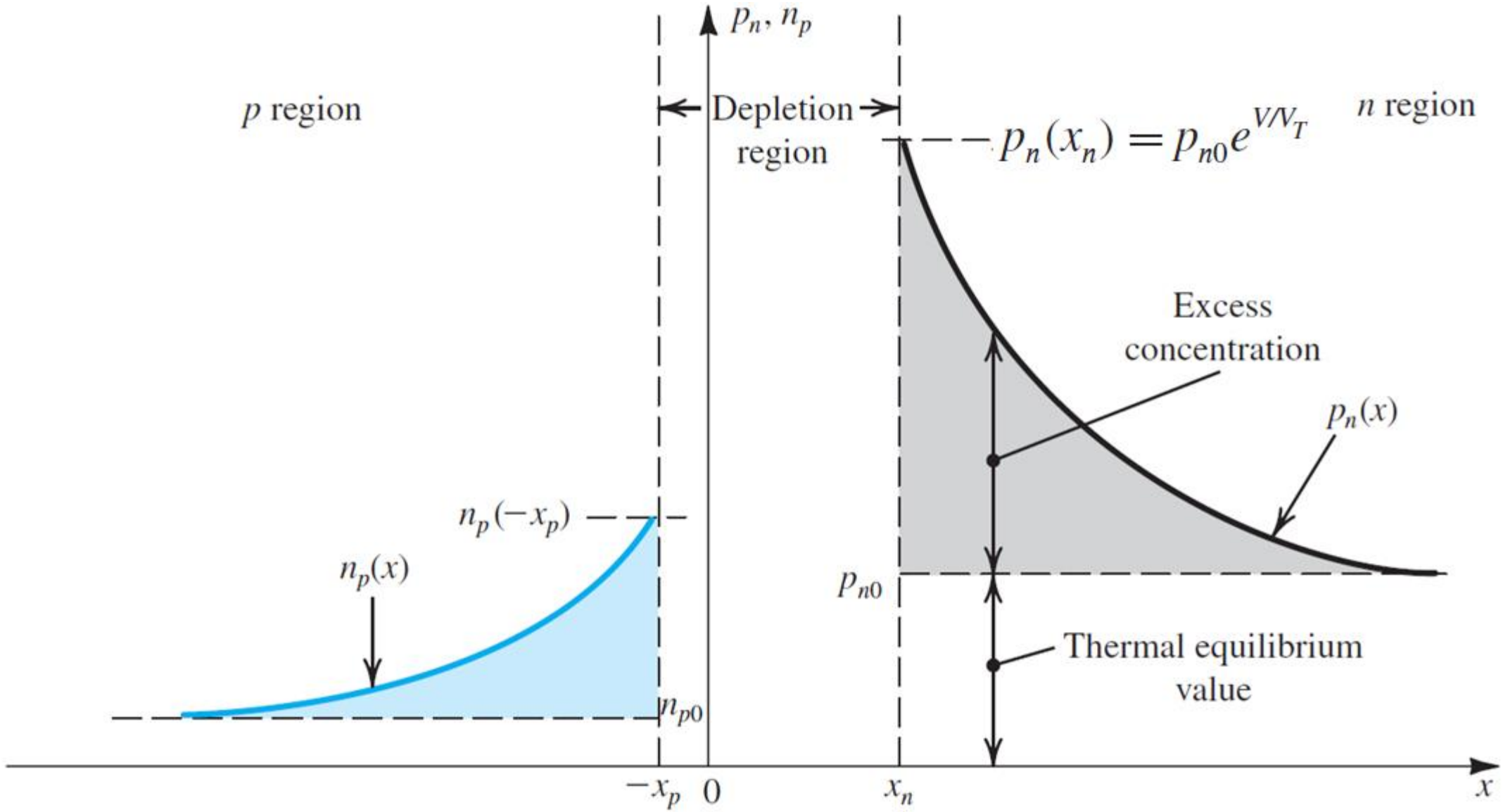
$$p_n(x_n) = p_{n0} e^{V/V_T}$$


I_D
I_S
p
n
$-x_p$
0
x_n
E

(a)


$p_p = N_A$
$n_n = N_D$
Carrier concentration
W
$n_{p0} = \frac{n_i^2}{N_A}$
$p_{n0} = \frac{n_i^2}{N_D}$
$-x_p$
0
x_n
x

(b)


p_n, n_p
p region
Depletion region
n region
$p_n(x_n) = p_{n0}e^{V/V_T}$
Excess concentration
$p_n(x)$
$n_p(-x_p)$
$n_p(x)$
p_{n0}
Thermal equilibrium value
n_{p0}
$-x_p$
0
x_n
x

- The forward-bias voltage *V* results in an **excess concentration** of minority holes at $x = x_n$, which is given by;

$$\text{Excess concentration} = p_{n0}e^{V/V_T} - p_{n0}$$
$$= p_{n0}\left(e^{V/V_T} - 1\right)$$

- As the injected holes diffuse into the *n* material, some will recombine with the majority electrons and disappear. The excess hole concentration will decay exponentially with distance and as a result.
- The total hole concentration in the *n* material becomes:

$$p_n(x) = p_{n0} + (\text{Excess concentration})e^{-(x-x_n)/L_p}$$
$$p_n(x) = p_{n0} + p_{n0}\left(e^{V/V_T} - 1\right)e^{-(x-x_n)/L_p}$$

- The exponential decay is characterized by the constant *Lp*, which is called the **diffusion length** of holes in the *n* material.

Hole–Diffusion Current Density

- Applying the diffusion current equation due to the concentration gradient of holes in the *n* region;

$$J_p(x) = -qD_p \frac{dp_n(x)}{dx} = q\left(\frac{D_p}{L_p}\right) p_{n0}\left(e^{V/V_T} - 1\right) e^{-(x-x_n)/L_p}$$

- $J_{p(x)}$ is highest at $X = X_n$ and decays exponentially for $X > X_n$, as the minority holes recombine with the majority electrons.

$$J_p(x_n) = q\left(\frac{D_p}{L_p}\right) p_{n0}\left(e^{V/V_T} - 1\right)$$

- Recombination, however, means that the majority electrons will have to be replenished by a current that injects electrons from the external circuit into the *n* region of the junction. This latter current component has the same direction as the hole current (because electrons moving from right to left give rise to current in the direction from left to right).
- Similarly for electrons injected from the *n* to the *p* region, results in an electron diffusion current given by

$$J_n(-x_p) = q\left(\frac{D_n}{L_n}\right) n_{p0}\left(e^{V/V_T} - 1\right)$$

pn Junction Current Equation

- The two current densities due to diffusion of holes and electrons add and when they are multiplied by the junction area *A* give the total current *I* as

$$I = A(J_p + J_n)$$

$$I = Aq\left(\frac{D_p}{L_p}p_{n0} + \frac{D_n}{L_n}n_{p0}\right)\left(e^{V/V_T} - 1\right)$$

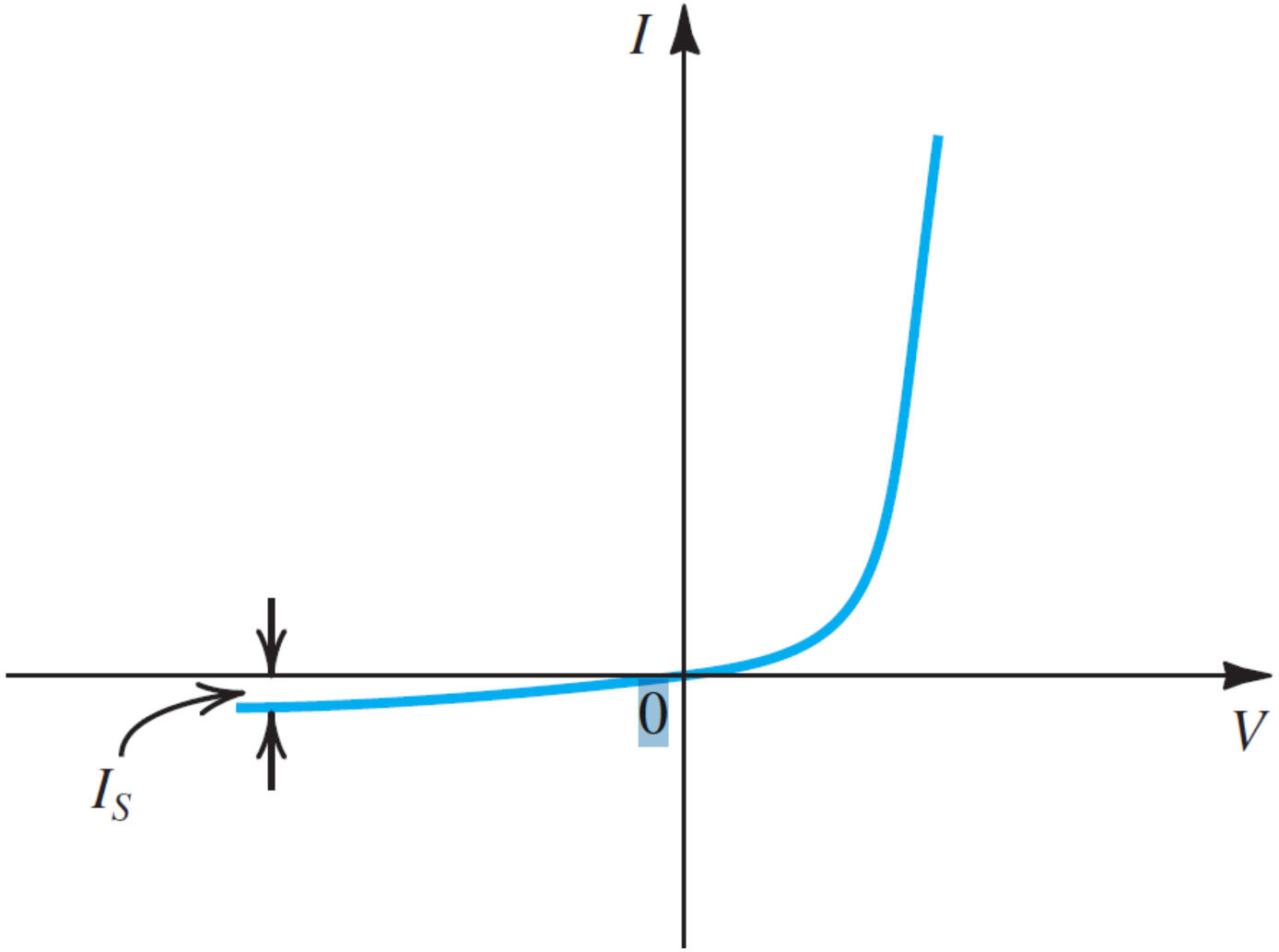
- Substituting for $p_{n0} = n_i^2/N_D$ and for $n_{p0} = n_i^2/N_A$ gives

$$I = Aqn_i^2\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)\left(e^{V/V_T} - 1\right)$$

- For a negative *V* (reverse bias) with a magnitude of a few times V_T (25.9 mV), the exponential term becomes essentially zero, and the current across the junction becomes negative and constant.

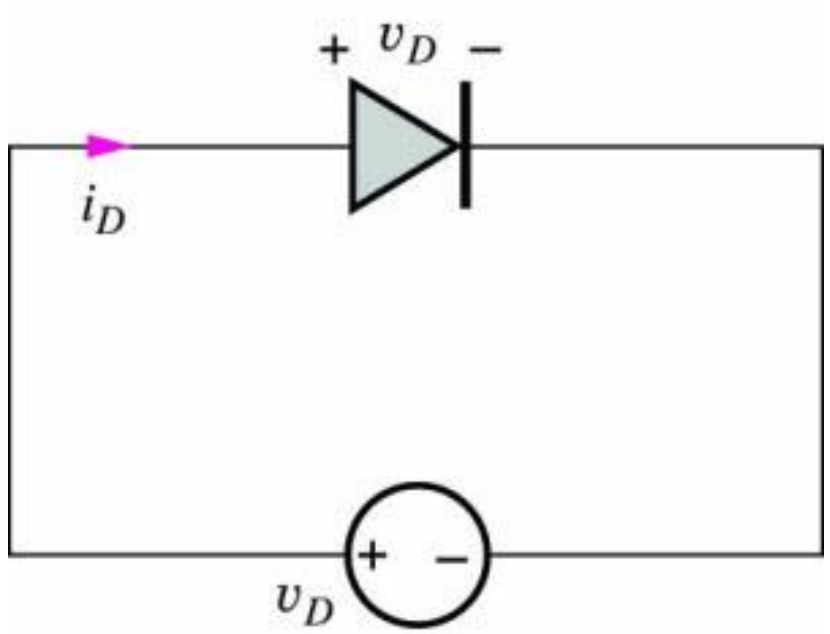
$$I = I_S\left(e^{V/V_T} - 1\right) \quad \text{and} \quad I_S = Aqn_i^2\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)$$

pn Junction *I–V* Characteristic



Diode Equation

$$i_D = I_S\left[\exp\left(\frac{qv_D}{nkT}\right)-1\right] = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right]$$



where
- I_S = reverse saturation current (A)
- v_D = voltage applied to diode (V)
- q = electronic charge (1.60 x 10-19 C)
- k = Boltzmann's constant (1.38 x 10^{-23} J/K)
- T = absolute temperature
- n = nonideality factor (dimensionless)
- V_T = kT/q = thermal voltage (V) (25 mV at room temp.)

I_S is typically between 10^{-18} and 10^{-9} A, and is strongly temperature dependent due to its dependence on n_i^2. The nonideality factor is typically close to 1, but approaches 2 for devices with high current densities. It is generally taken as 1.

Diode Current for Reverse, Zero, and Forward Bias

- Reverse bias:

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right] \approx I_S\left[0-1\right] \approx -I_S$$

- Zero bias:

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right] \approx I_S\left[1-1\right] \approx 0$$

- Forward bias:

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right] \approx I_S \exp\left(\frac{v_D}{nV_T}\right)$$

Diode Voltage and Current Calculations (Example)

Problem: Find diode voltage for diode with given specifications

Given data: I_S=0.1 fA I_D= 300 μA

Assumptions: Room-temperature dc operation with V_T=0.025 V

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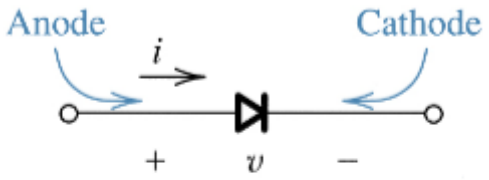
Analysis:

With I_S=0.1 fA $V_D = nV_T \ln\left(1+\frac{I_D}{I_S}\right) = 1(0.0025\text{V})\ln\left(1+\frac{3\times10^{-4}\text{A}}{10^{-16}\text{A}}\right) = 0.718\text{V}$

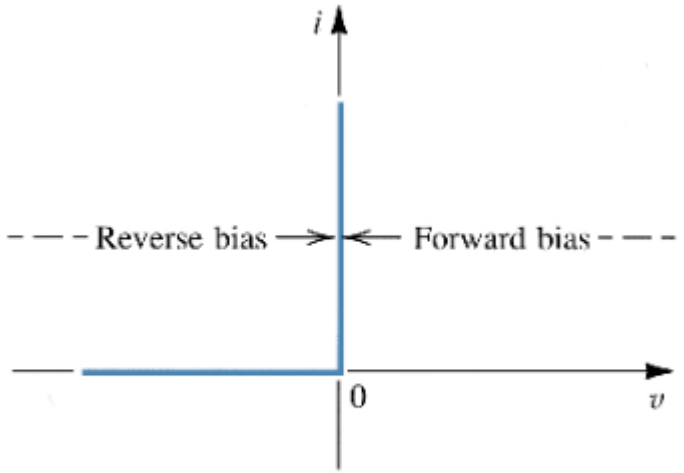
With I_S=10 fA $V_D = 0.603\text{V}$

With I_S=0.1 fA , I_D= 1 mA $V_D = 0.748\text{V}$

The Ideal Diode



(a)



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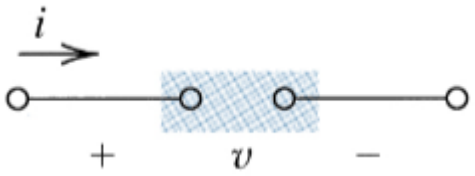
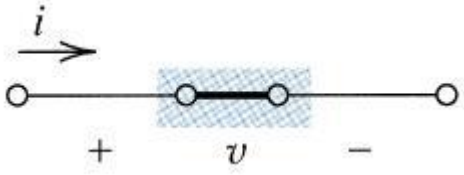


$v < 0 \Rightarrow i = 0$

(c)



$i > 0 \Rightarrow v = 0$

(d)

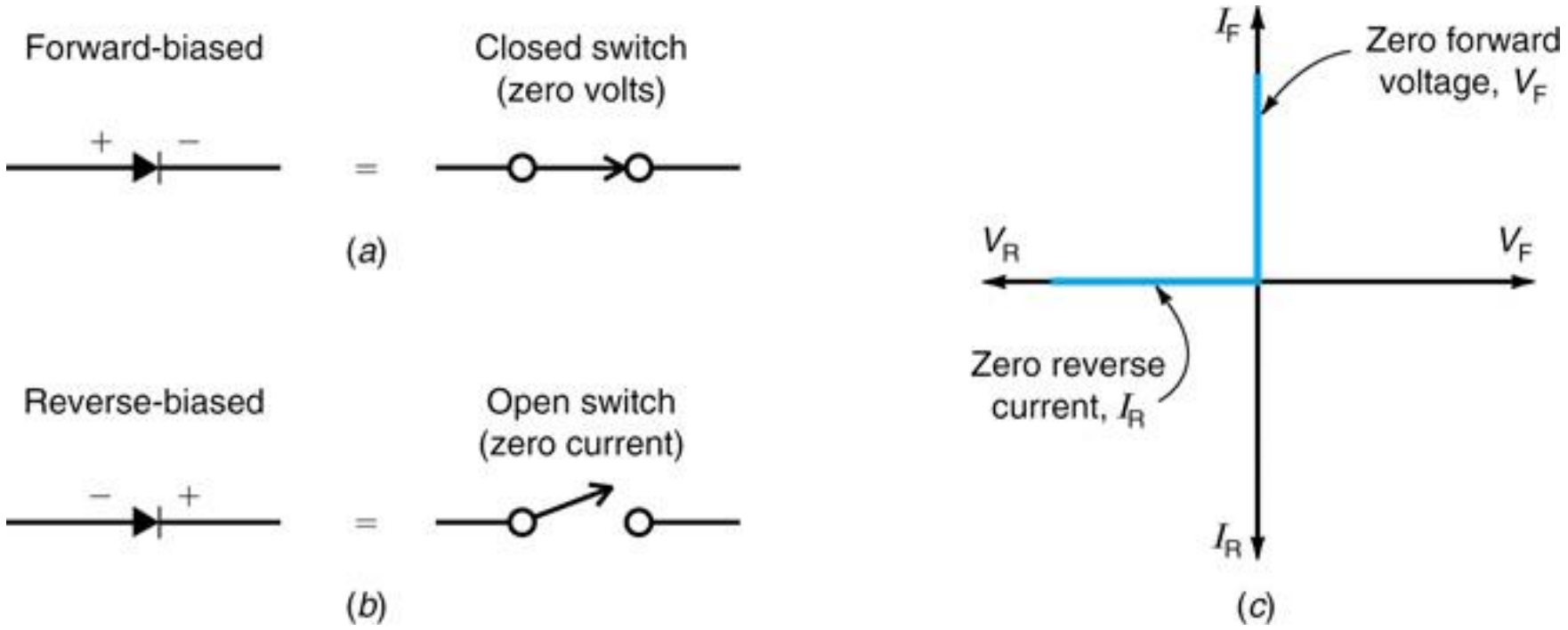
The ideal diode: **(a)** diode circuit symbol; **(b)** *i-v* characteristic; **(c)** equivalent circuit in the reverse direction; **(d)** equivalent circuit in the forward direction.

Diode Equivalent Circuits

- Three different approximations can be used when analyzing diode circuits.
- The one used depends on the desired accuracy of your circuit calculations.
- These approximations are referred to as
  - The first approximation
  - The second approximation
  - The third approximation

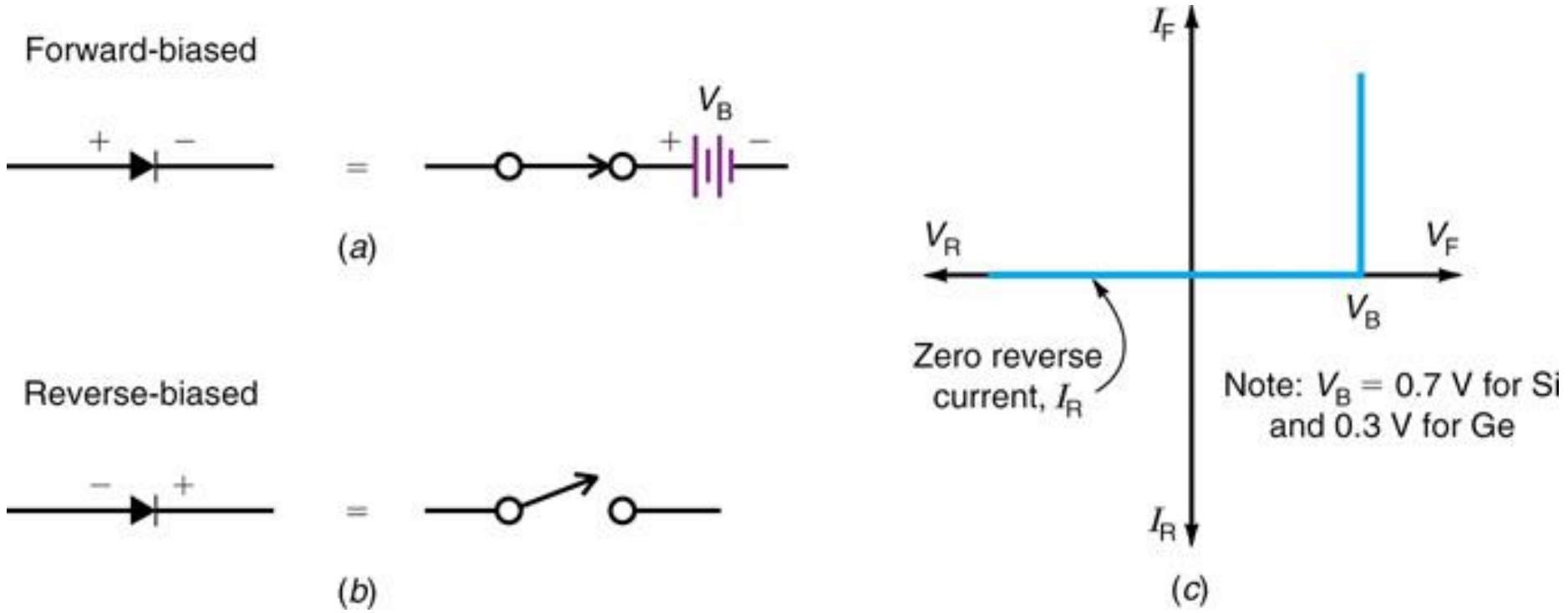
The First Approximation

The first approximation treats a forward-biased diode like a closed switch with a voltage drop of zero volts, as shown in Fig.



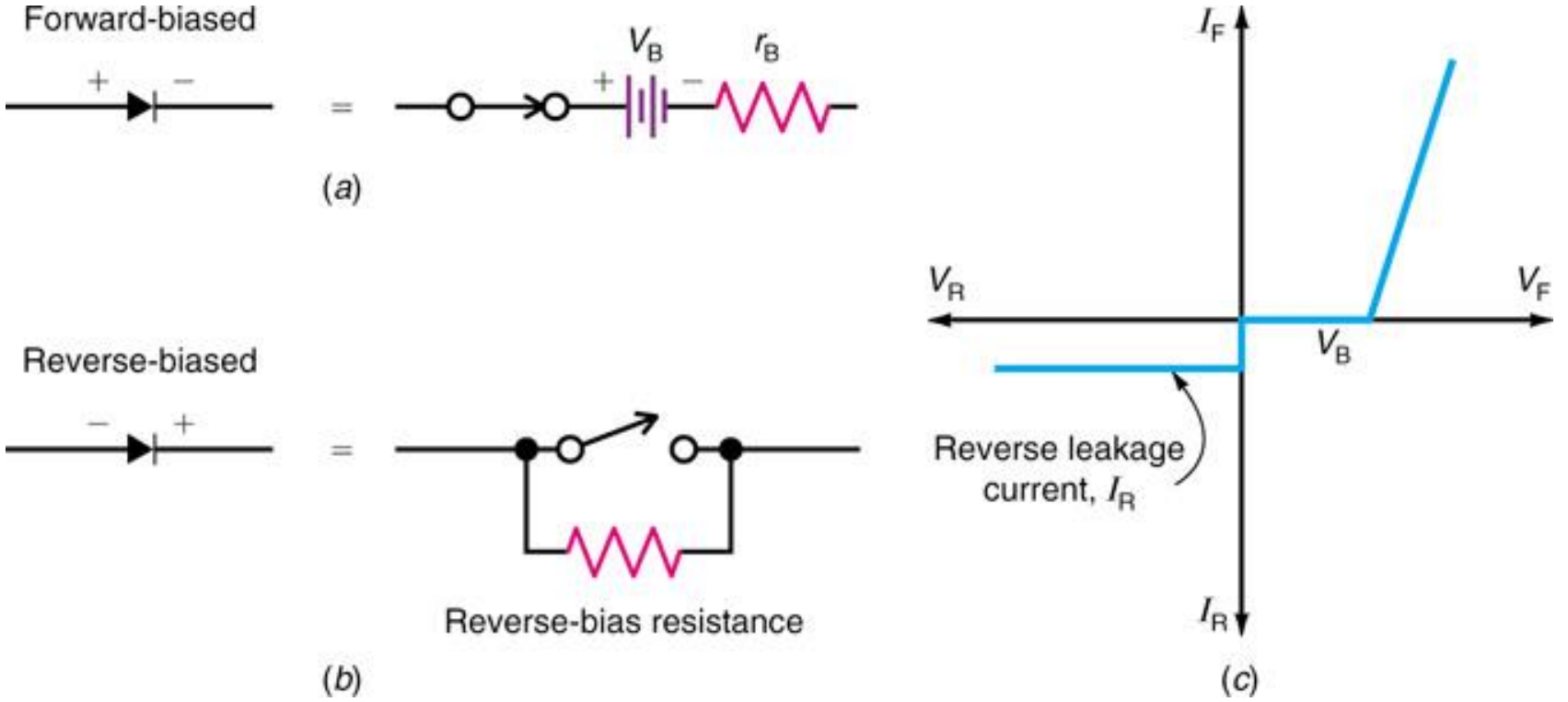
The Second Approximation

The second approximation treats a forward-biased diode like an ideal diode in series with a battery, as shown in Fig.

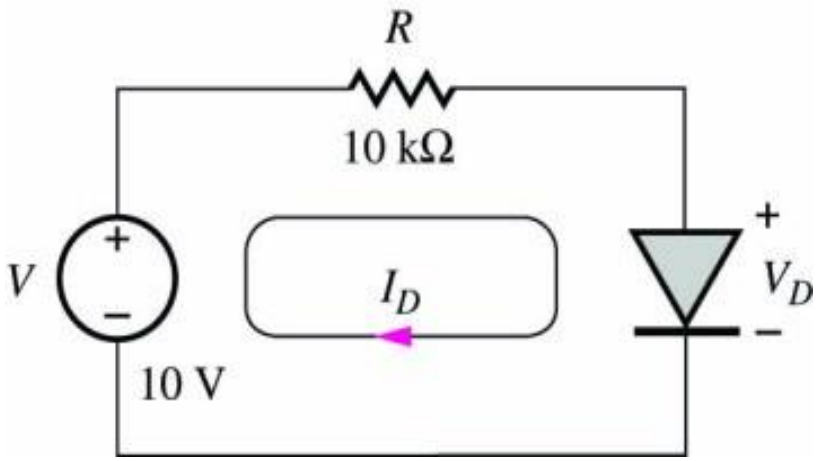


The Third Approximation

- The third approximation of a diode includes the bulk resistance, r_B.
- The bulk resistance, r_B is the resistance of the p and n materials.
- The third approximation of a forward-biased diode is shown in Fig.



Diode Circuit Analysis: Basics



Objective of diode circuit analysis is to find **quiescent operating point** for diode, consisting of dc current and voltage that define diode's *i*-*v* characteristic.

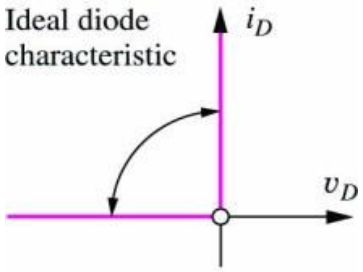
Loop equation for given circuit is:

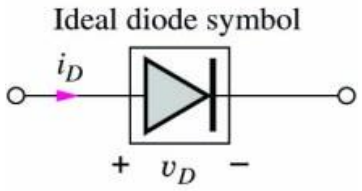
$$V = I_D R + V_D$$

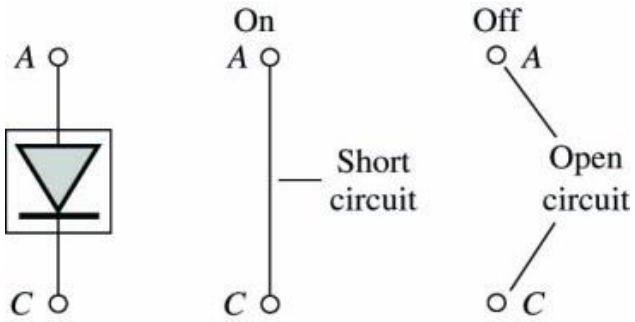
This is also called the **load line** for the diode. Solution to this equation can be found by:

1. Simplified analysis with ideal diode model.
2. Simplified analysis using constant voltage drop model.
3. Graphical analysis using load-line method.
4. Analysis with diode's mathematical model.

Analysis using Ideal Model for Diode







If diode is forward-biased, voltage across diode is zero. If diode is reverse-biased, current through diode is zero.

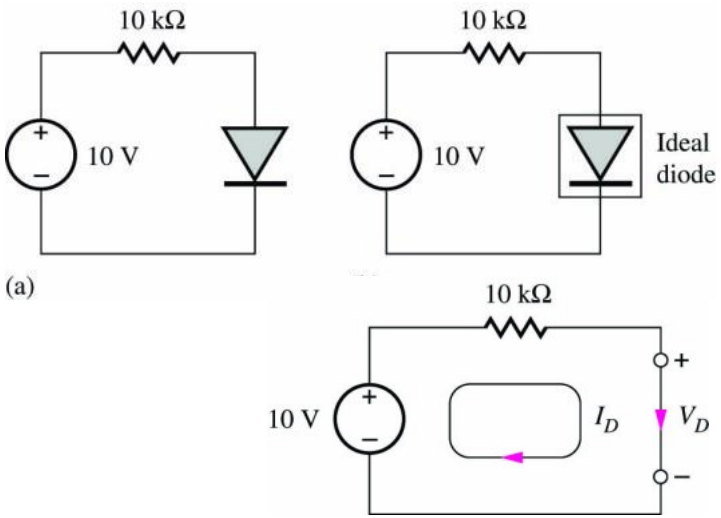
$v_D = 0$ for $i_D > 0$ and $v_D = 0$ for $v_D < 0$

Thus diode is assumed to be either on or off.

Analysis is conducted in following steps:

1. Select diode model.
2. Identify anode and cathode of diode and label v_D and i_D.
3. Guess diode's region of operation from circuit.
4. Analyze circuit using diode model appropriate for assumed operation region.
5. Check results to check consistency with assumptions.

Analysis using Ideal Model for Diode: Example

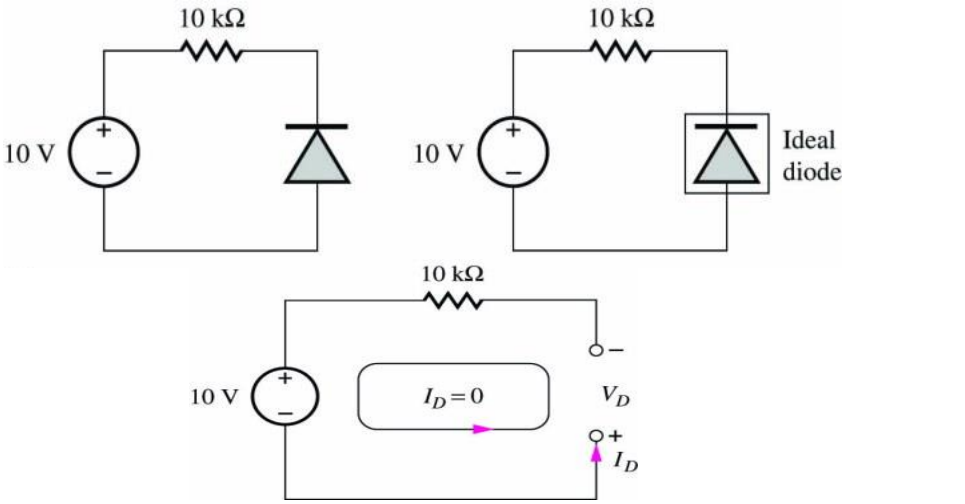


Since source is forcing positive current through diode assume diode is on.

$$I_D = \frac{(10-0)\text{V}}{10\text{k}\Omega} = 1\text{m}A$$

$\because I_D \geq 0$

Q-point is(1 mA, 0V)



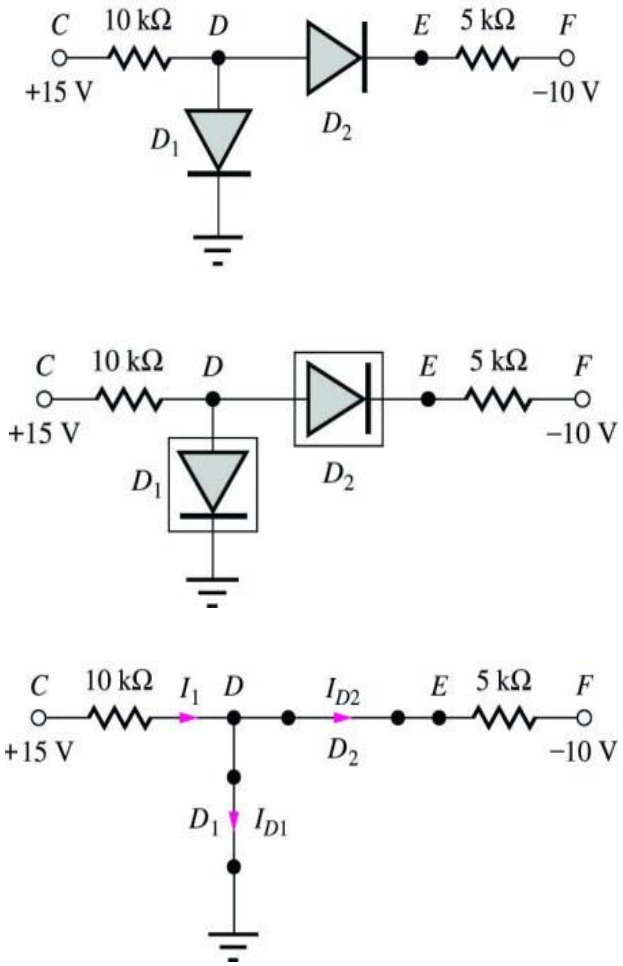
Since source is forcing current backward through diode assume diode is off. Hence I_D =0 . Loop equation is:

$$10 + V_D + 10^4 I_D = 0$$

$$\therefore V_D = -10\text{V}$$

Q-point is (0, -10 V)

Two-Diode Circuit Analysis



Analysis: Ideal diode model is chosen.
Since 15V source is forcing positive current through D_1 and D_2 and -10V source is forcing positive current through D_2, assume both diodes are on.

Since voltage at node D is zero due to short circuit of ideal diode D_1,

$$I_1 = \frac{(15-0)\text{V}}{10\text{k}\Omega} = 1.50\text{mA} \qquad I_{D2} = \frac{0-(-10)\text{V}}{5\text{k}\Omega} = 2.00\text{mA}$$

$$I_1 = I_{D1} + I_{D2} \qquad \therefore I_{D1} = 1.5-2 = -0.50\text{mA}$$

Q-points are (-0.5 mA, 0 V) and (2.0 mA, 0 V)

But, $I_{D1} < 0$ is not allowed by diode, so ?.

References:

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- http://www.ecse.rpi.edu/~schubert/Course-ECSE-2210-Microelectronics-Technology-2010/