Field Effect Transistor (FET)

Semiconductor Devices and Circuits

(ECE 181302)

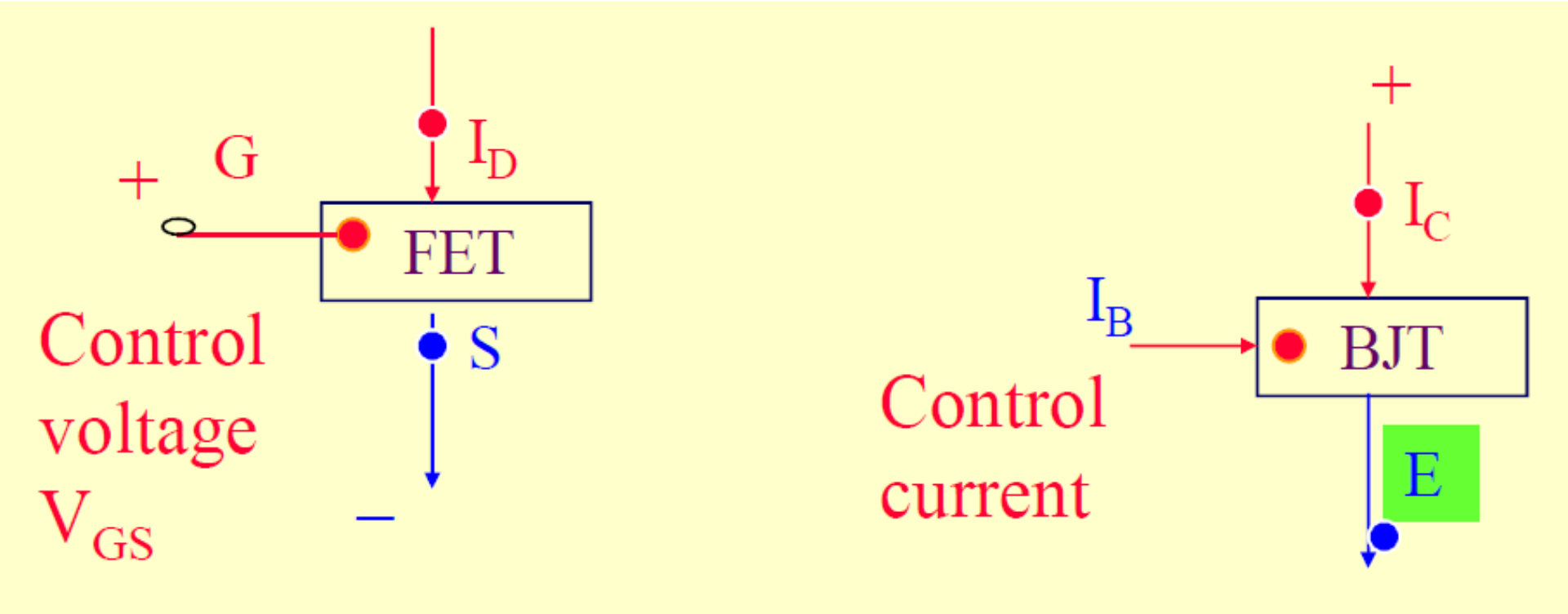
7th January 2022

Transistor

- *Transferred-resistance or transistor* is a multi-junction device that is capable of;
  - Current gain
  - Voltage gain
  - Signal-power gain

Types of Transistors

- **Bipolar Junction Transistor (BJT) is an active device.**
  - *It is a current controlled valve. The base current (I_B) controls the collector current (I_C).*
- **Field Effect Transistor (FET) is an active device.**
  - *It is a voltage controlled valve. The gate-source voltage (V_{GS}) controls the drain current (I_D).*
- The conventional bipolar transistor has two type of current carriers of both polarities (majority and minority) and FET has only one type of current carriers, p or n (holes or electrons)
- The BJT is current controlled and FET is voltage controlled current between two other terminals
- FET is characterized by practically zero gate current, and a very high impedance at input whereas the base current of the BJT is always some value greater than zero.


+
G
I_D
FET
Control
voltage
V_{GS}
S
–
+
I_C
I_B
BJT
Control
current
E

BJTs

- Three different currents in the device: I_C, I_B and I_E
- Consume a lot of power
- Large size device

FETs

- Mostly widely used today
- Low power
- Very small device (nm)
- Simple manufacturing process
- Only 1 current, I_D

Comparison between BJT and FET

BJT	*FET*
1. Two types of carriers (electrons and holes) are required.	1. Only one type of carrier (electron or hole) is required.
2. Carriers move through the base by diffusion process.	2. Carriers move through the channel by drift process.
3. The BJT has a comparatively lower switching speed due to the diffusion process.	3. The FET has a higher switching speed due to the drift process; the drift of the carrier is faster than diffusion.
4. The BJT is not a thermally stable device.	4. The FET has a negative temperature coefficient at high-current operations, i.e., the current decreases as temperature increases Due to this particular feature, a uniform temperature distribution and protection against breakdown can be achieved.
5. In case of IC fabrication, the BJT requires more space than the FET.	5. In case of IC fabrication the FET requires lesser space than the BJT.
6. At audio frequencies the BJT offers less power gain.	6. At audio frequencies the FET offers greater power gain.
7. The BJT is a current-controlled device.	7. The FET is a voltage-controlled device.
8. The BJT offers low input impedance.	8. The FET offers high input impedance, therefore, it can be used as a buffer.
9. BJT is much noisier than FET.	9. FET is less noisy.
10. The BJT has offset voltage.	10. The FET has no offset voltage.
11. The BJT can also be used as a switch; it is taken to be in the OFF state when operating in the cut off region, and in the ON state when it is operating in the saturation region.	11. The FET is particularly useful for its operation as a controlled switch, operating in both the conducting and the non-conducting zones.

Field Effect Transistor (FET)

- The field-effect transistor (FET) is a generic term for a device that controls current through a circuit via an applied voltage, i.e. it is a voltage-controlled resistor.
- A FET has three terminals:
  - Gate: as in the “gate” keeper of the current
  - Source: the source of the current
  - Drain: the destination of the current
- The FET operation is by:
  - apply a voltage to the gate
  - this voltage sets up an electric field in the “body” of the device
  - electric field inhibits/supports the flow of charge from source to drain

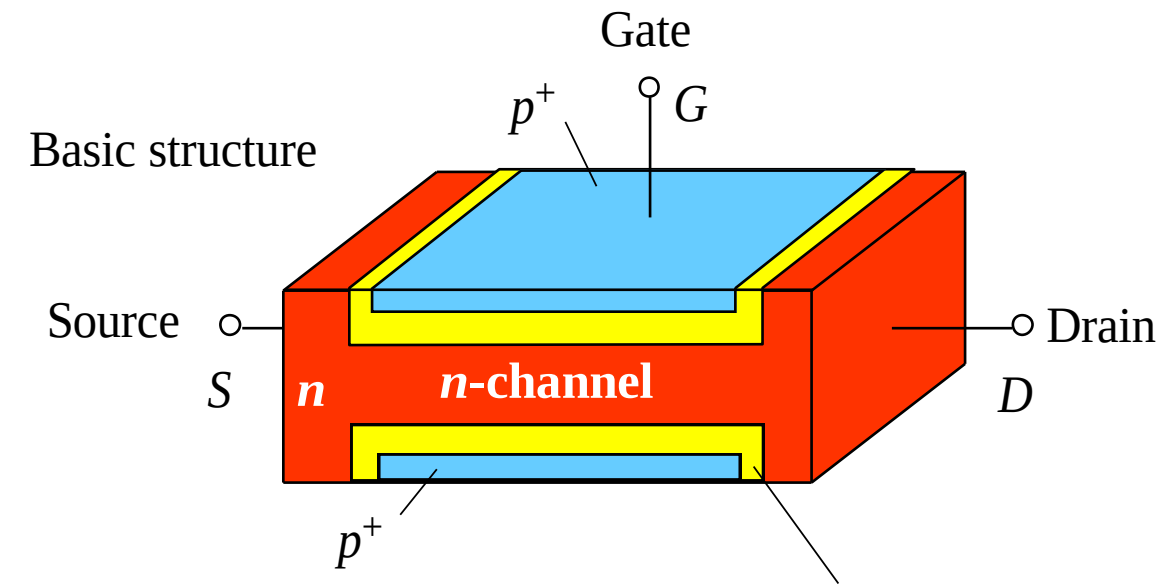
Types of FET

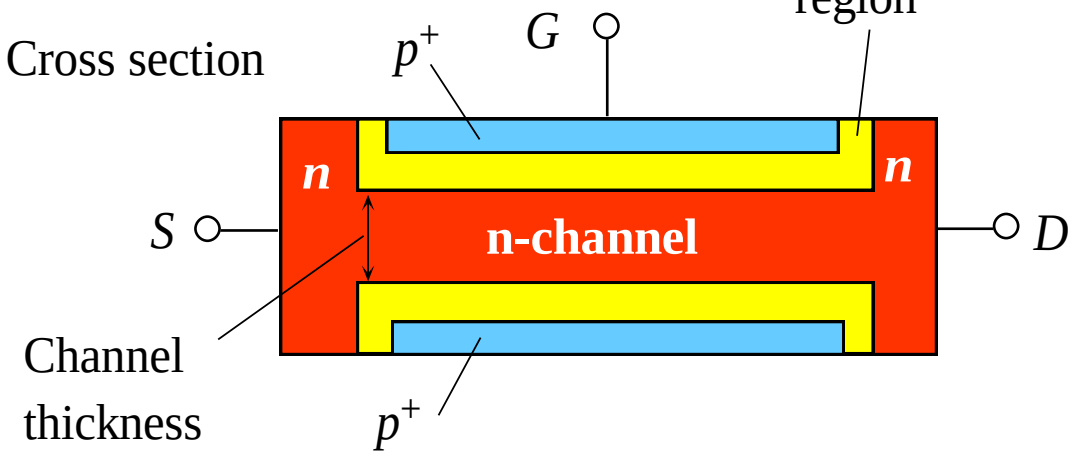
- According to the type of the channel, FETs can be classified as:
  - JFET: **junction field-effect transistor**
    - P channel
    - N channel
  - MOSFET: **metal-oxide-semiconductor field-effect transistor**
    - N channel
      - **Enhancement type**
      - **Depletion type**
    - P channel
      - **Enhancement type**
      - **Depletion type**

JFET vs MOSFET

- Differ in the way the gate contact is made on the source drain channel.
- In the JFET the gate-channel contact is a reverse biased PN *junction. The gate-channel* junction of the JFET must always be reverse biased otherwise it may behave as a diode.
- All JFETs are depletion mode devices: they are *"on" when the gate bias is zero* ($V_{GS} = 0$).
- In the MOSFET the gate-channel contact is a metal electrode separated from the channel by a thin layer of insulating oxide.
- MOSFETs are made in both depletion mode (*"on" with zero* biased gate, $V_{GS} = 0$) *and in enhancement mode ("off" with zero biased gate,* $V_{GS} = 0$).

Basic Structure of JFET

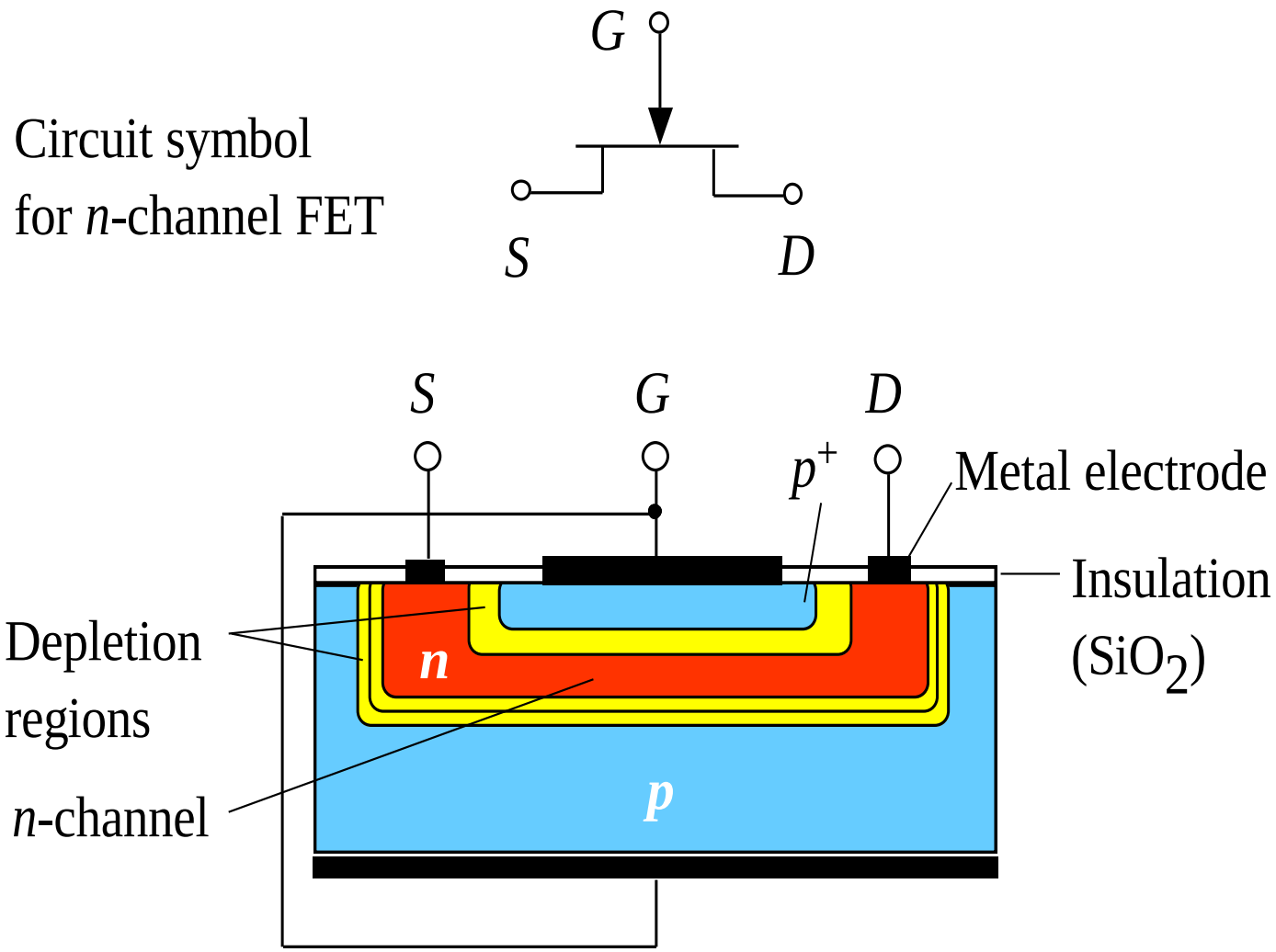




(a)

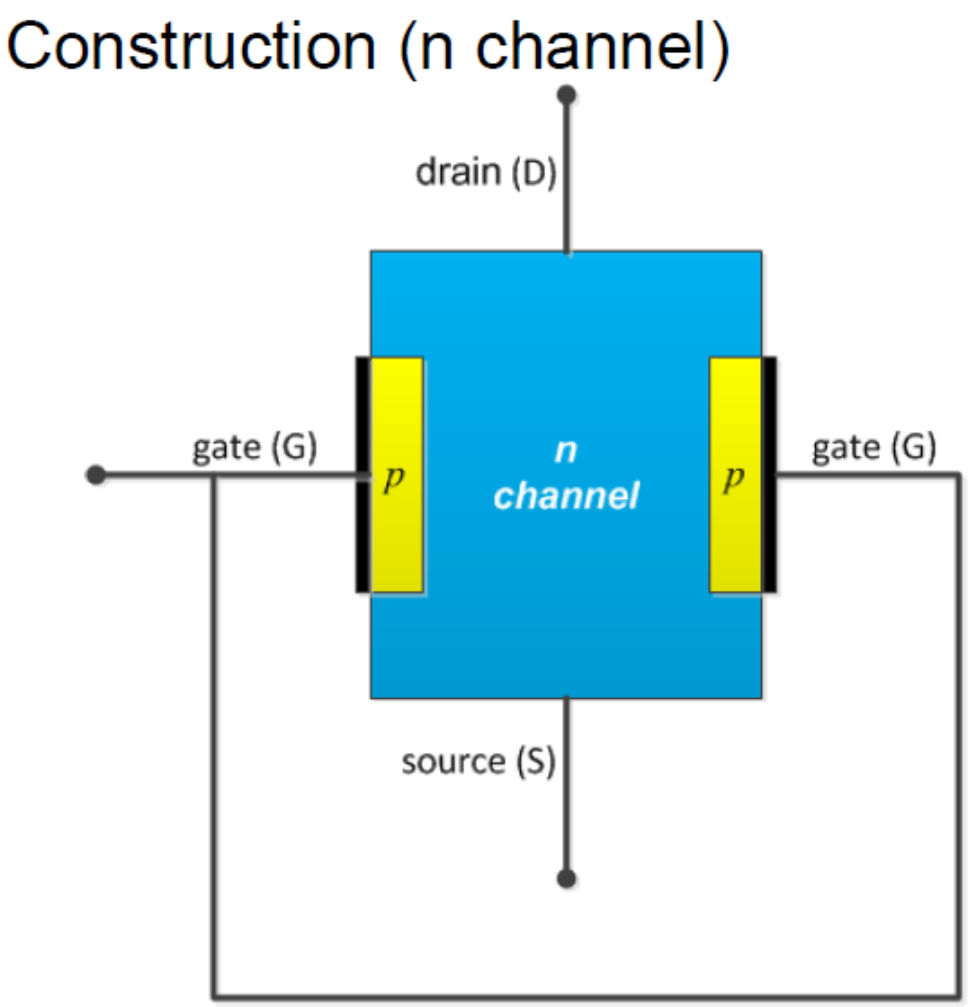
The two P+ regions are electrically connected and form the gate.

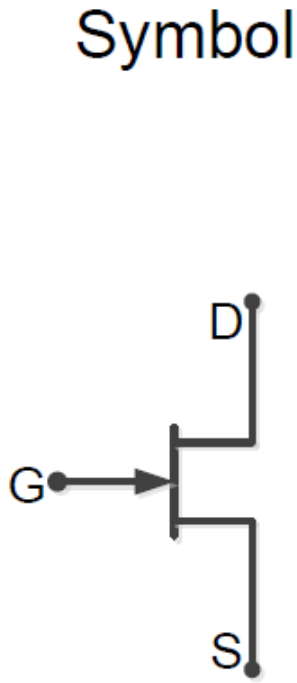
Practical n-channel JFET



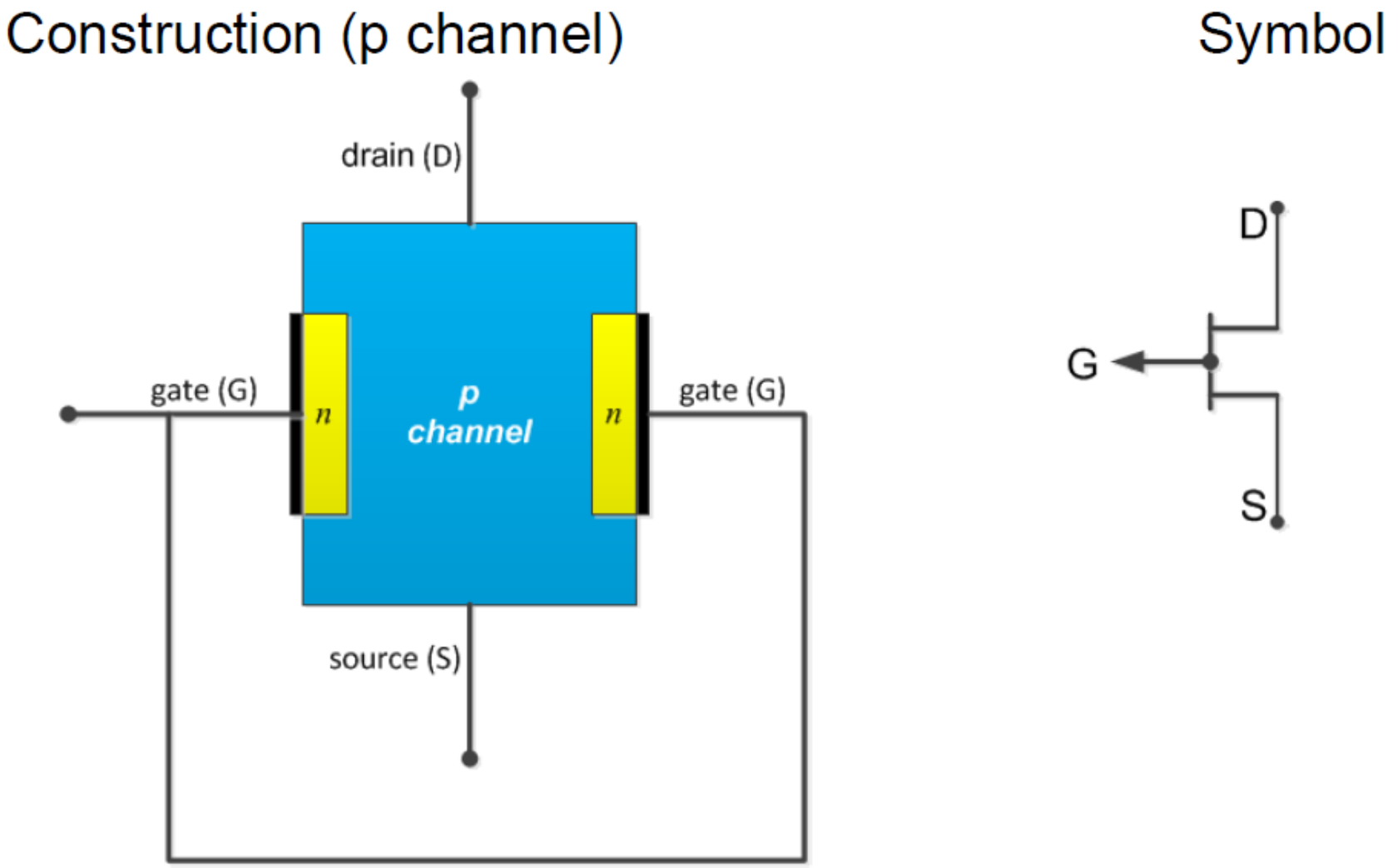
(b)

n-Channel JFET

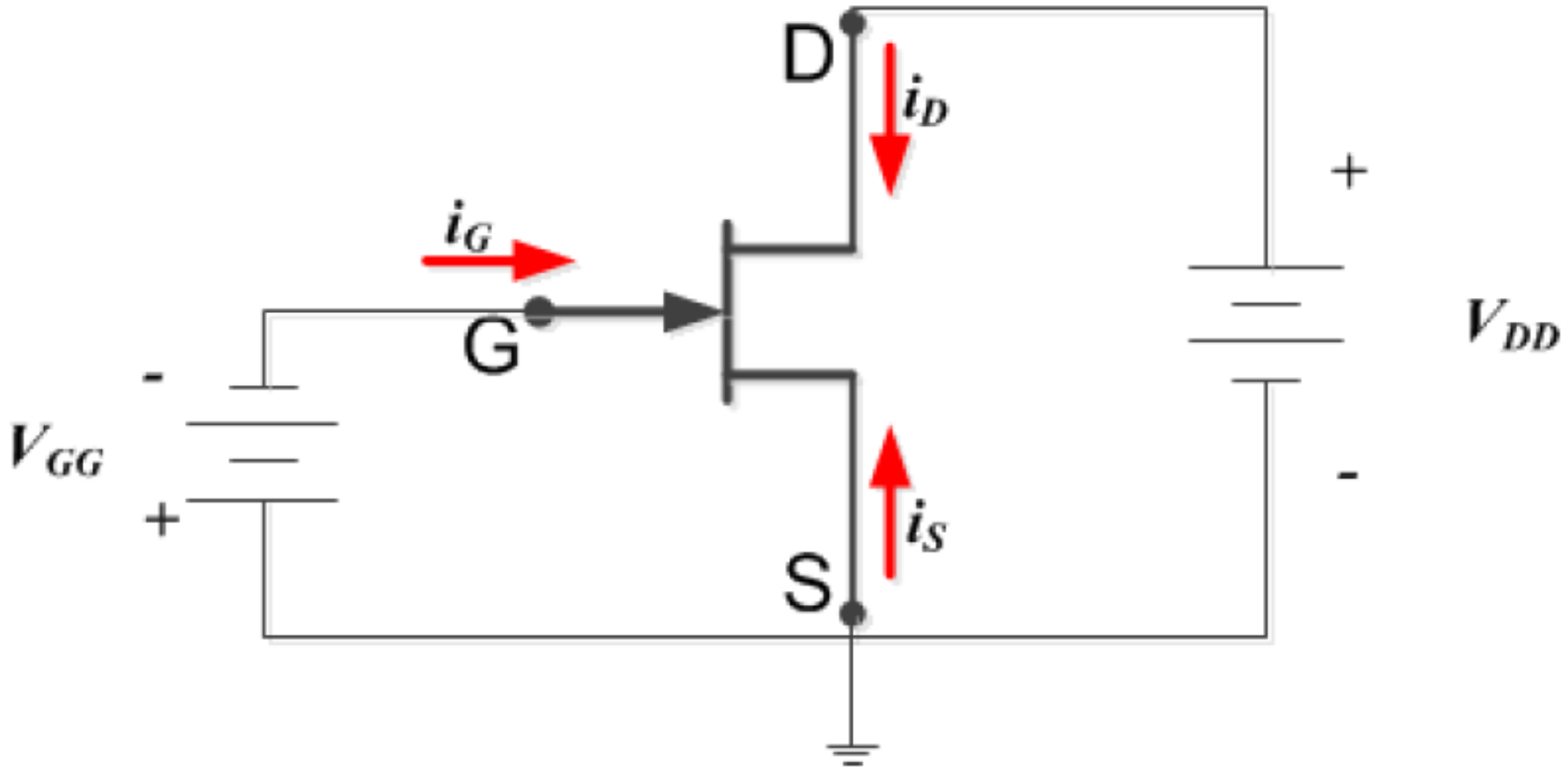




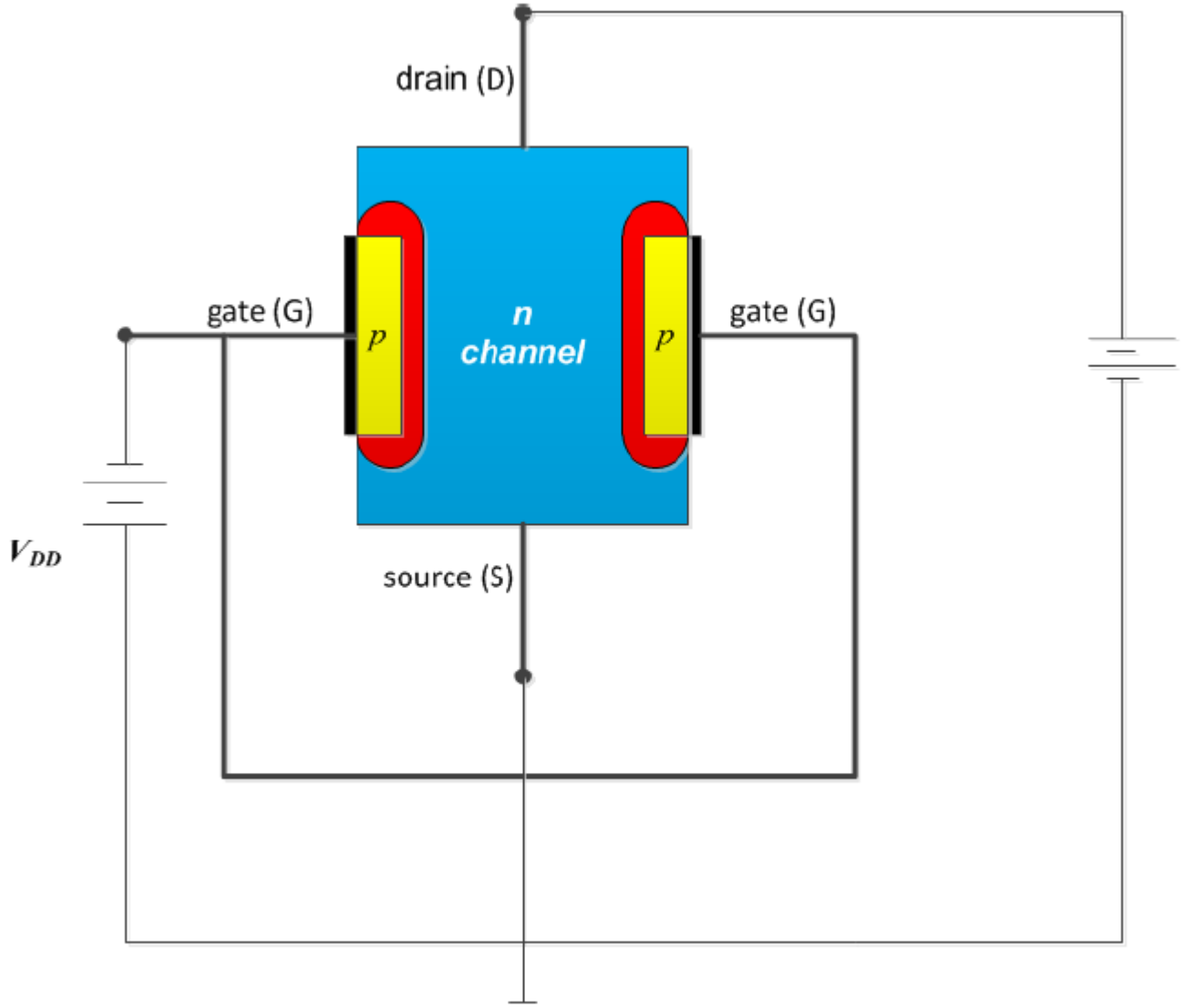
p-Channel JFET



Circuit Analysis

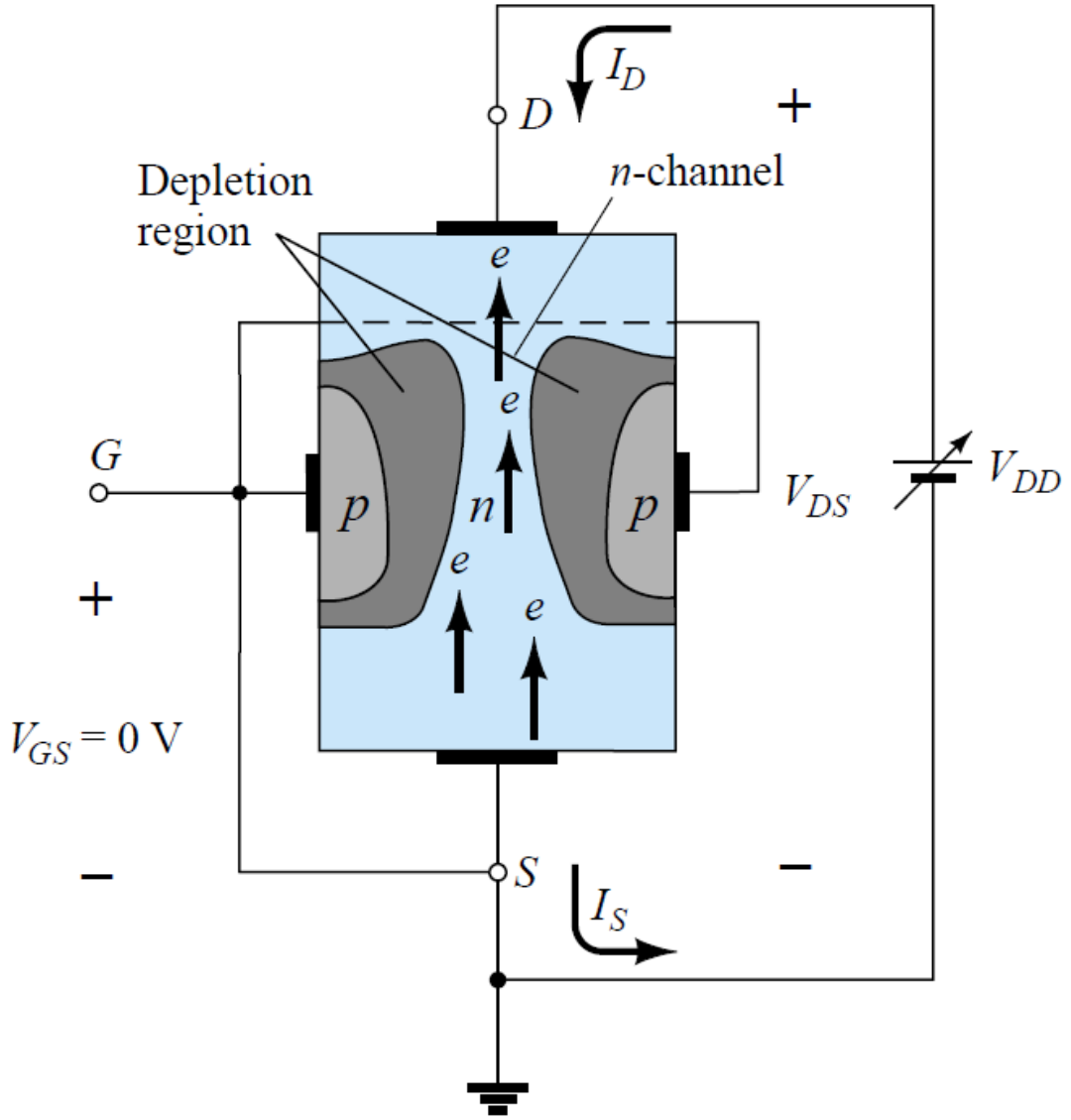


- $V_{DD} = V_{GG}=0$
- The two PN junctions are associated with a depletion region



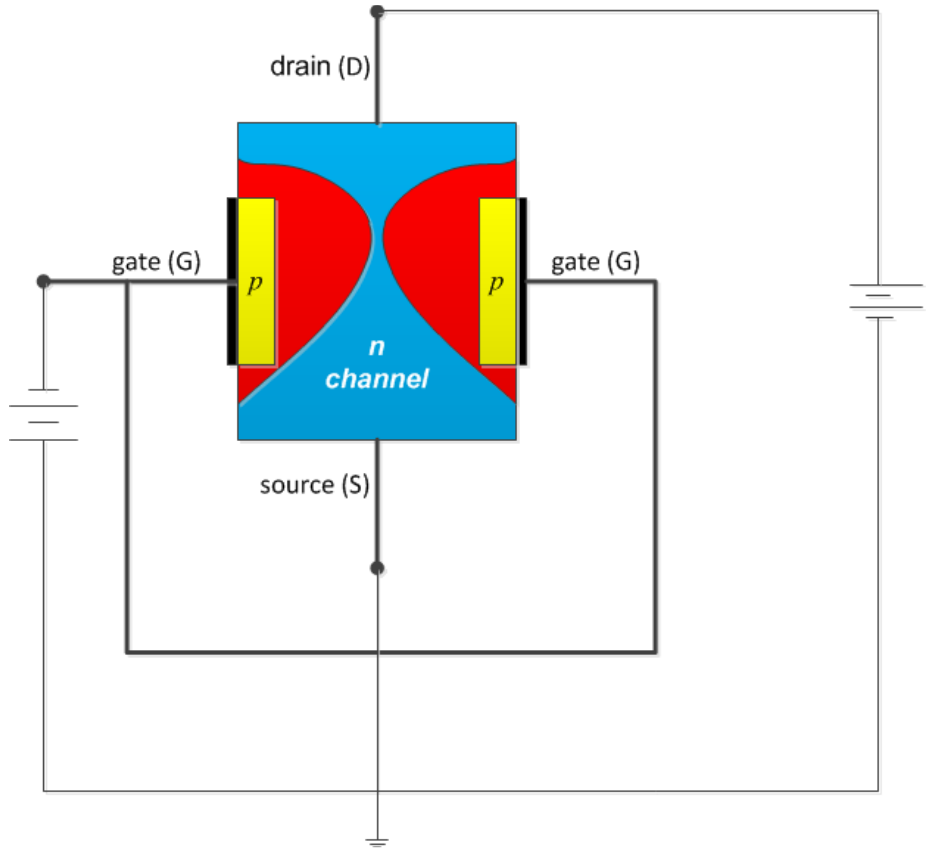
V_{GS} = 0 V and V_{DS} is some Positive Value

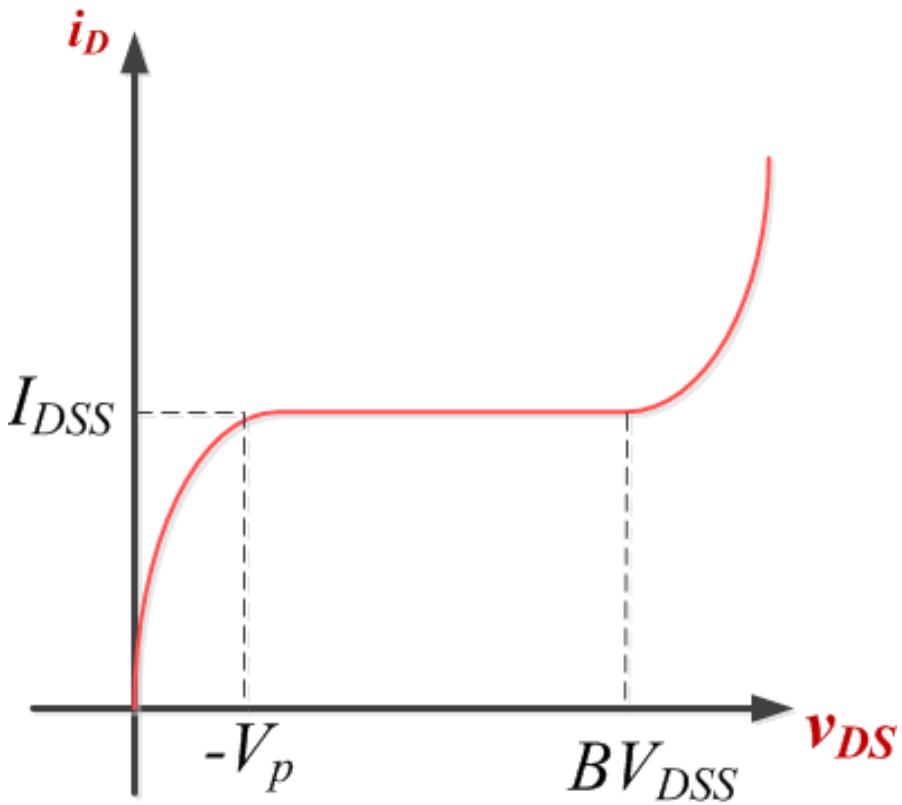
- Gate is connected directly to the source to establish the condition V_{GS} = 0 V.
- Depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions
- When voltage V_{DD} (V_{DS}) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current I_D
- $I_D = I_S$



Note:

- Since gate drain voltage is negative and gate source voltage is zero, portion of the PN junction between the gate and drain is more reverse biased than portion between gate and source.
- The channel is narrower at the drain end than source end.
- Depletion region is wider near the top of both *p*-type materials.
- Assuming a uniform resistance in the *n*-channel, the resistance of the channel can be broken down to the divisions.
- Current I_D will establish the voltage levels through the channel.
- The upper region of the *p*-type material will be reverse biased compared to the lower region.
- The fact that the *p*-*n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes; $I_G = 0$ A.


drain (D)
gate (G)
p
p
gate (G)
n
channel
source (S)


i_D
I_{DSS}
$-V_p$
BV_{DSS}
v_{DS}

- As the voltage V_{DS} is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plots a linear I_D versus V_{DS}
- As V_{DS} increases and approaches a level referred to as V_P , the depletion regions widen, causing a noticeable reduction in the channel width.
- The reduced path of conduction causes the resistance to increase and the curve in the graph flattens.
- The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region.
- If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" , a condition referred to as *pinch-off* will result.
- The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P .
- In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A.
- This is hardly the case— I_D maintains a saturation level defined as I_{DSS}.

• As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of I_D remains essentially the same.
• Once $V_{DS} > V_P$ the JFET has the characteristics of a current source.
• The current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels > V_P) is determined by the applied load.

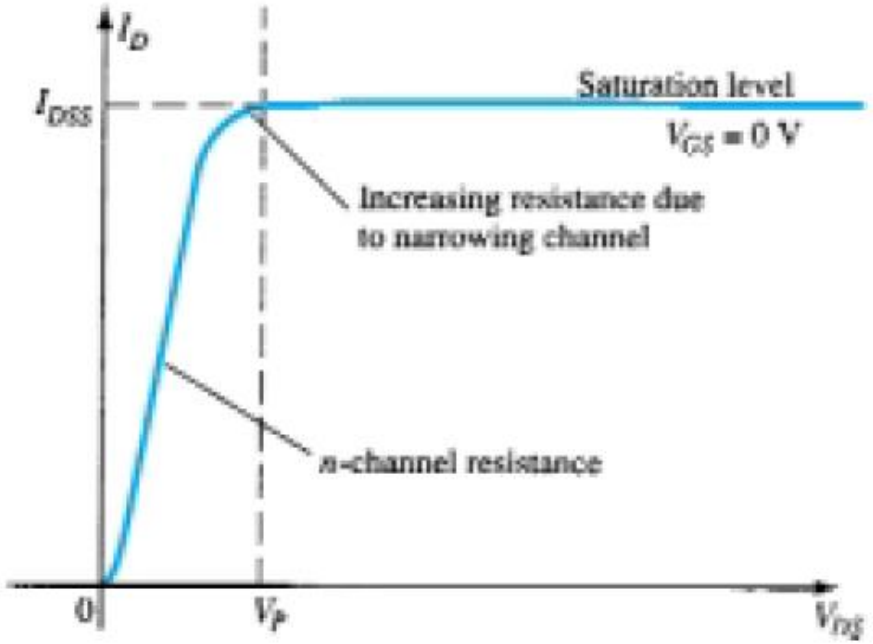


Figure 5.6 I_D versus V_{DS} for $V_{GS} = 0$ V.

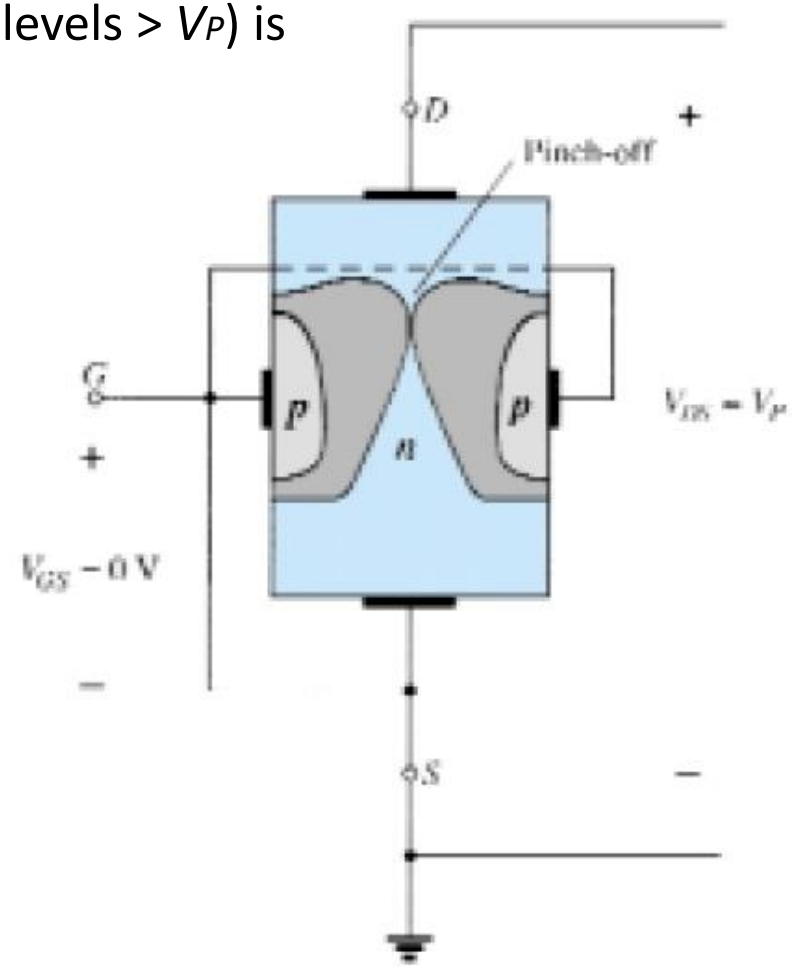
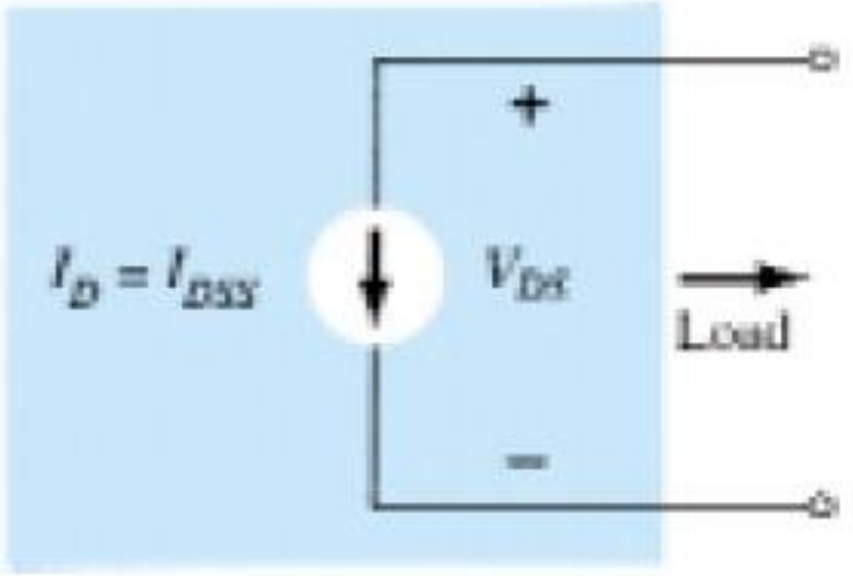
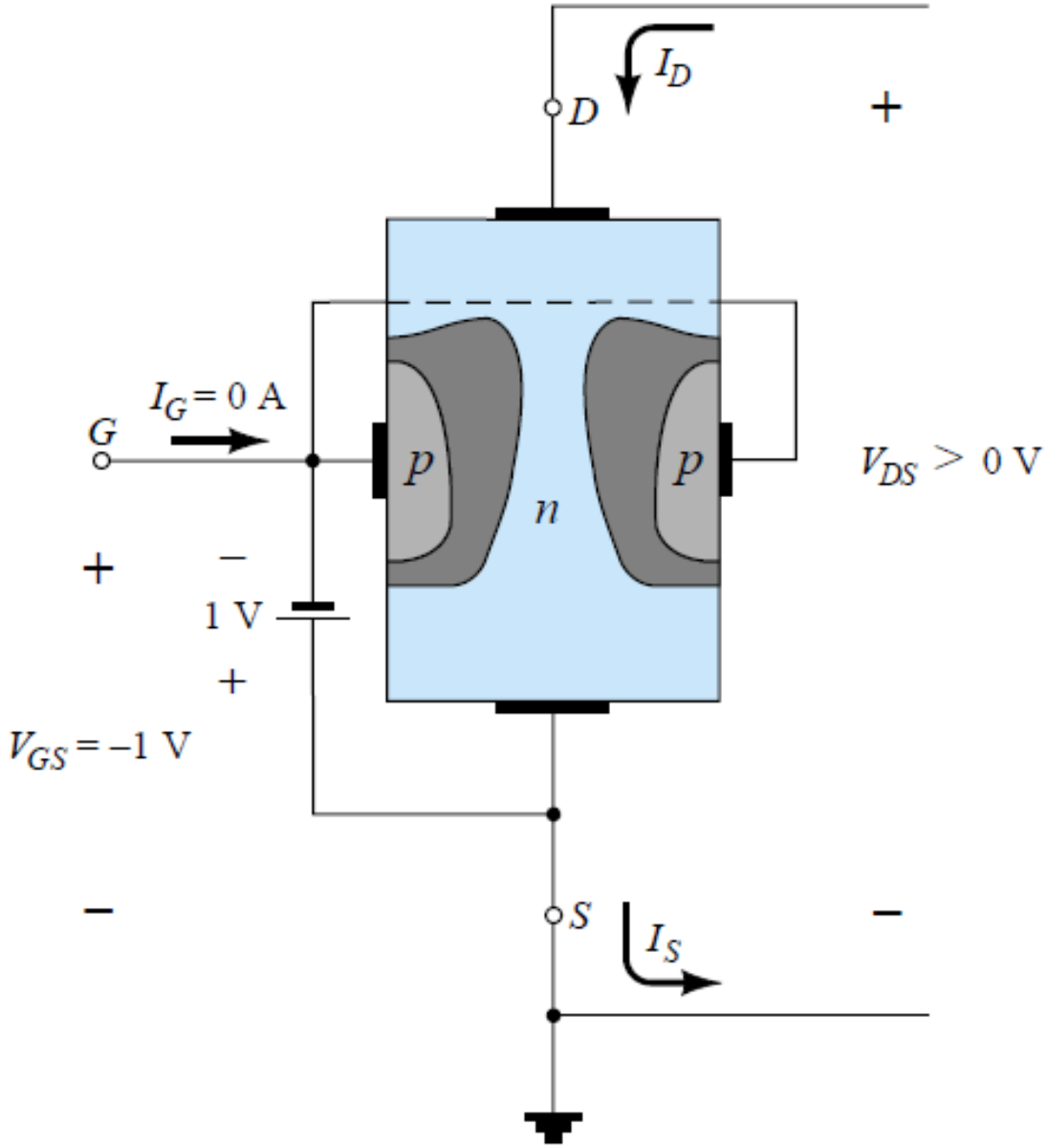


Figure 5.7 Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).



- The choice of notation I_{DSS} is derived from the fact that it is the *D*rain-to-*S*ource current with a short-circuit connection from gate to source.
- ***I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.***

$V_{GS} < 0$ V



$V_{GS} < 0$ V

- For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level.
- E.g. A negative voltage of -1 V is applied between the gate and source terminals for a low level of V_{DS}.
- The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}.
- The result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} for $V_{GS} = -1$ V.
- The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative.
- The pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative.
- Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off."

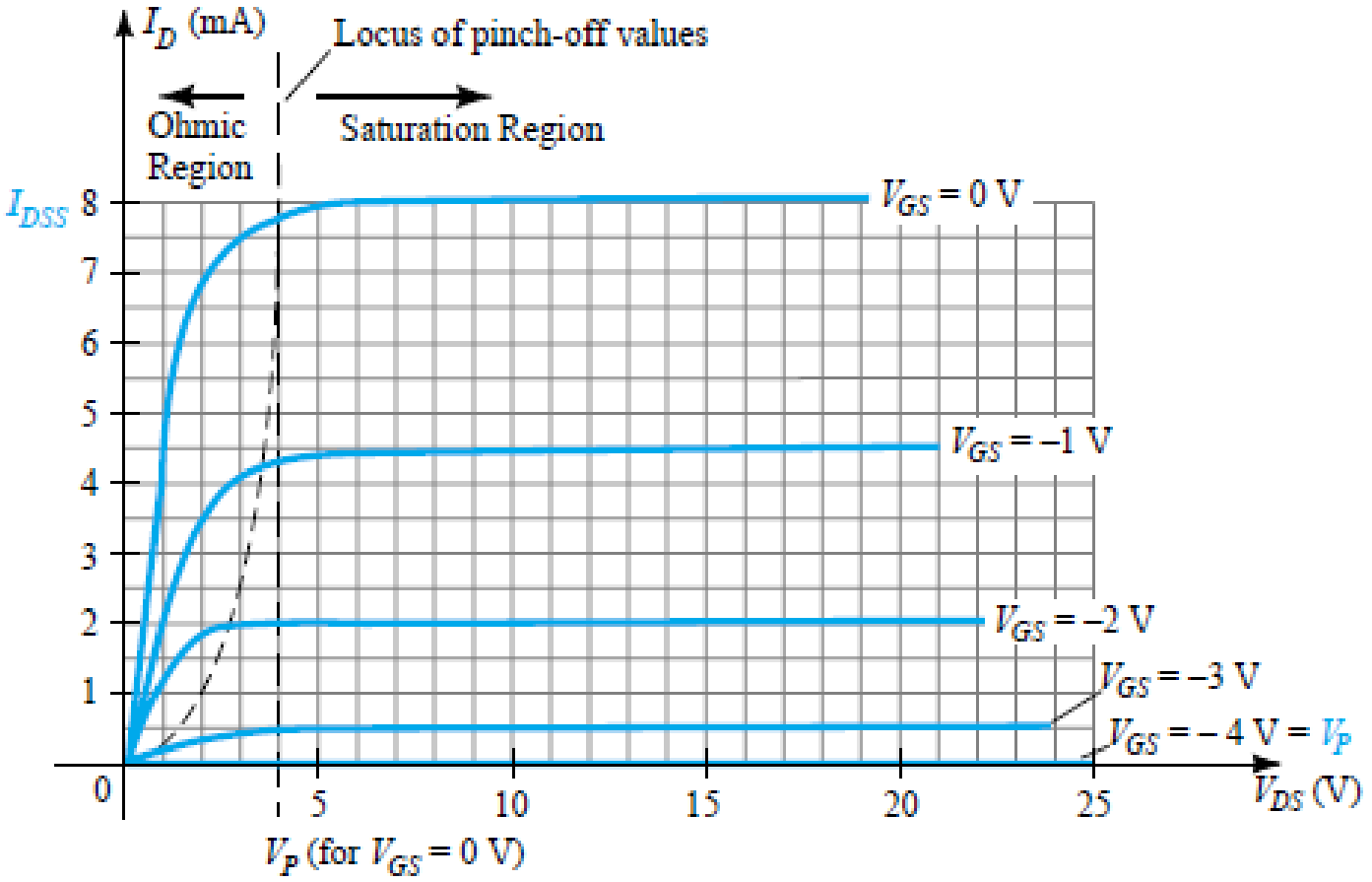


Figure 5.10 *n*-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

- *The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.*

Voltage-Controlled Resistor

- The region to the left of the pinch-off locus is referred to as the *ohmic* or *voltage-controlled resistance region.*
- *This region of the JFET can actually be employed* as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage.
- The slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ is a *function of the applied voltage* V_{GS}.
- As V_{GS} *becomes more* and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level.
- The following equation provides a good first approximation to the resistance level in terms of the applied voltage V_{GS}.

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

- r_o *is the resistance with* $V_{GS} = 0$ V *and* r_d *the resistance at a particular level* of V_{GS}.

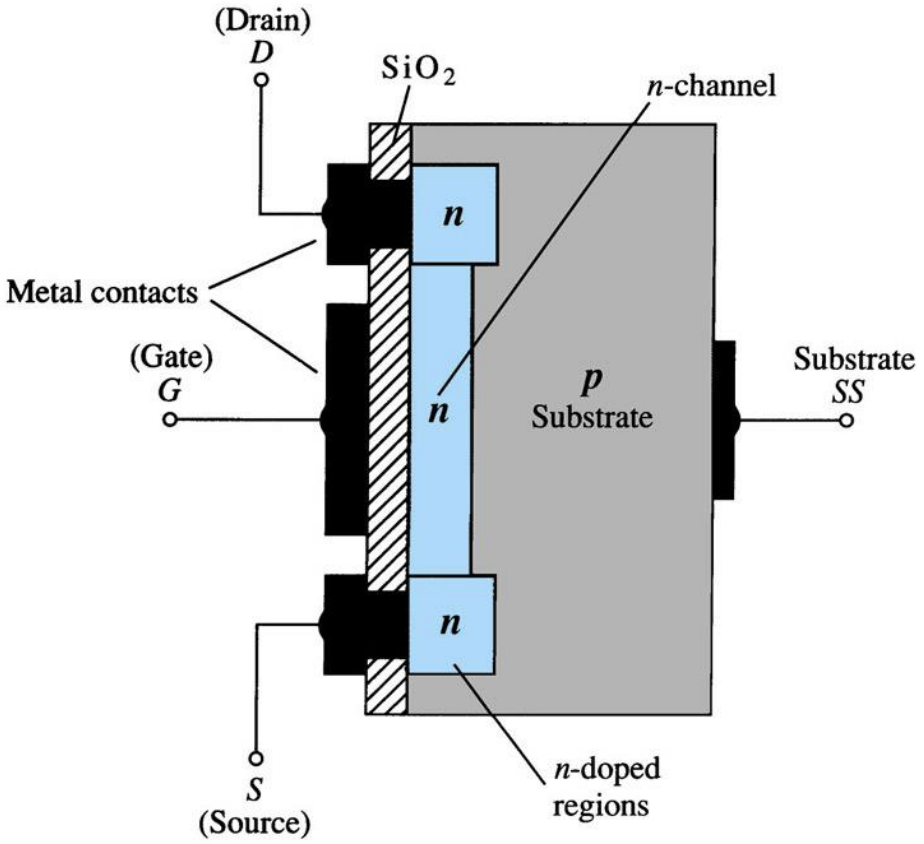
MOSFET

Have characteristics similar to JFETs

Two types of MOSFETs:

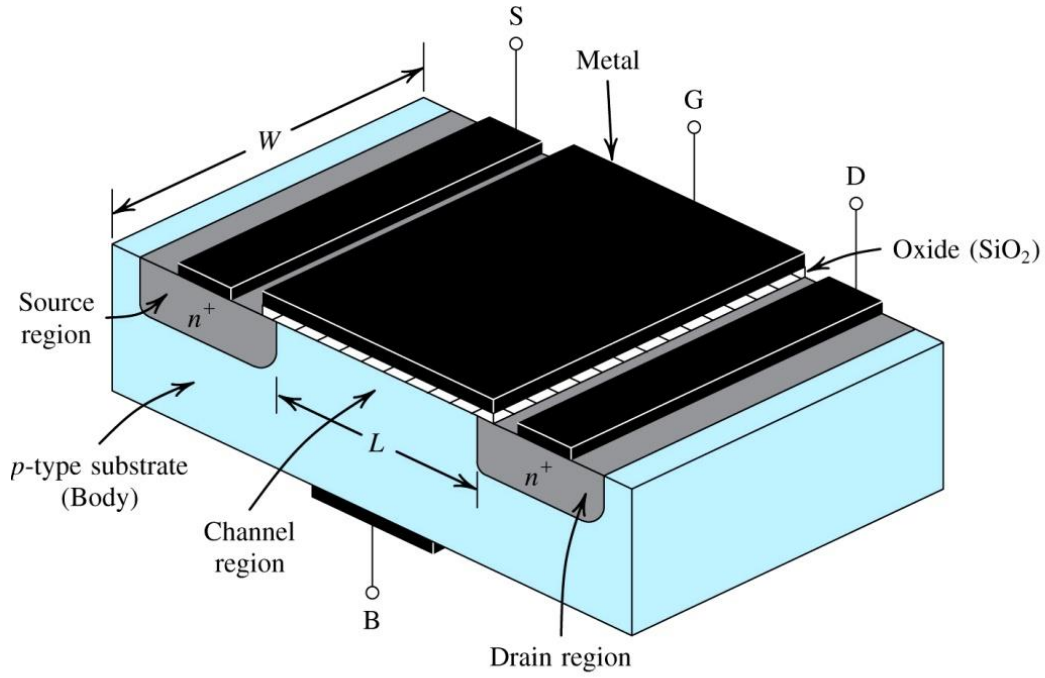
- Depletion mode MOSFET (D-MOSFET)
  - Operates in Depletion mode the same way as a JFET when $V_{GS} \leq 0$
  - Operates in Enhancement mode like E-MOSFET when $V_{GS} > 0$

- Enhancement Mode MOSFET (E-MOSFET)
  - Operates in Enhancement mode
  - $I_{DSS} = 0$ until $V_{GS} > V_T$ (threshold voltage)

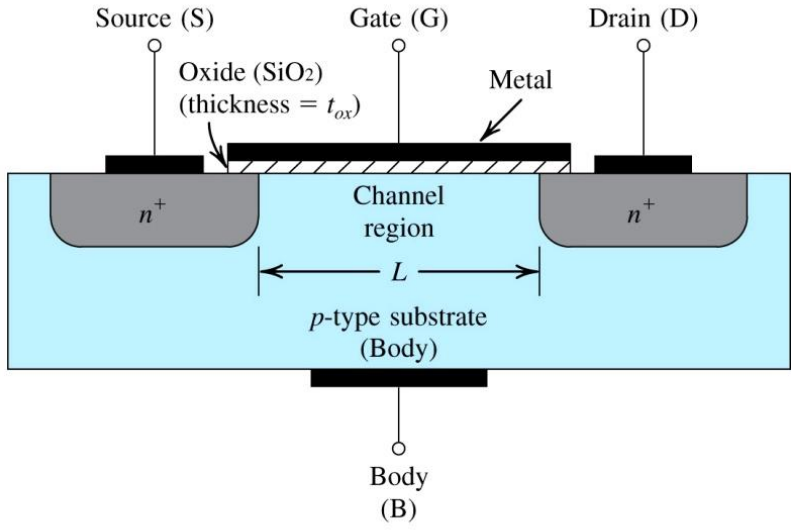


- The Drain (D) and Source (S) leads connect to the to n-doped regions
- These N-doped regions are connected via an n-channel
- This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

n-Channel MOSFET



(a)



(b)

MOSFET: Basics

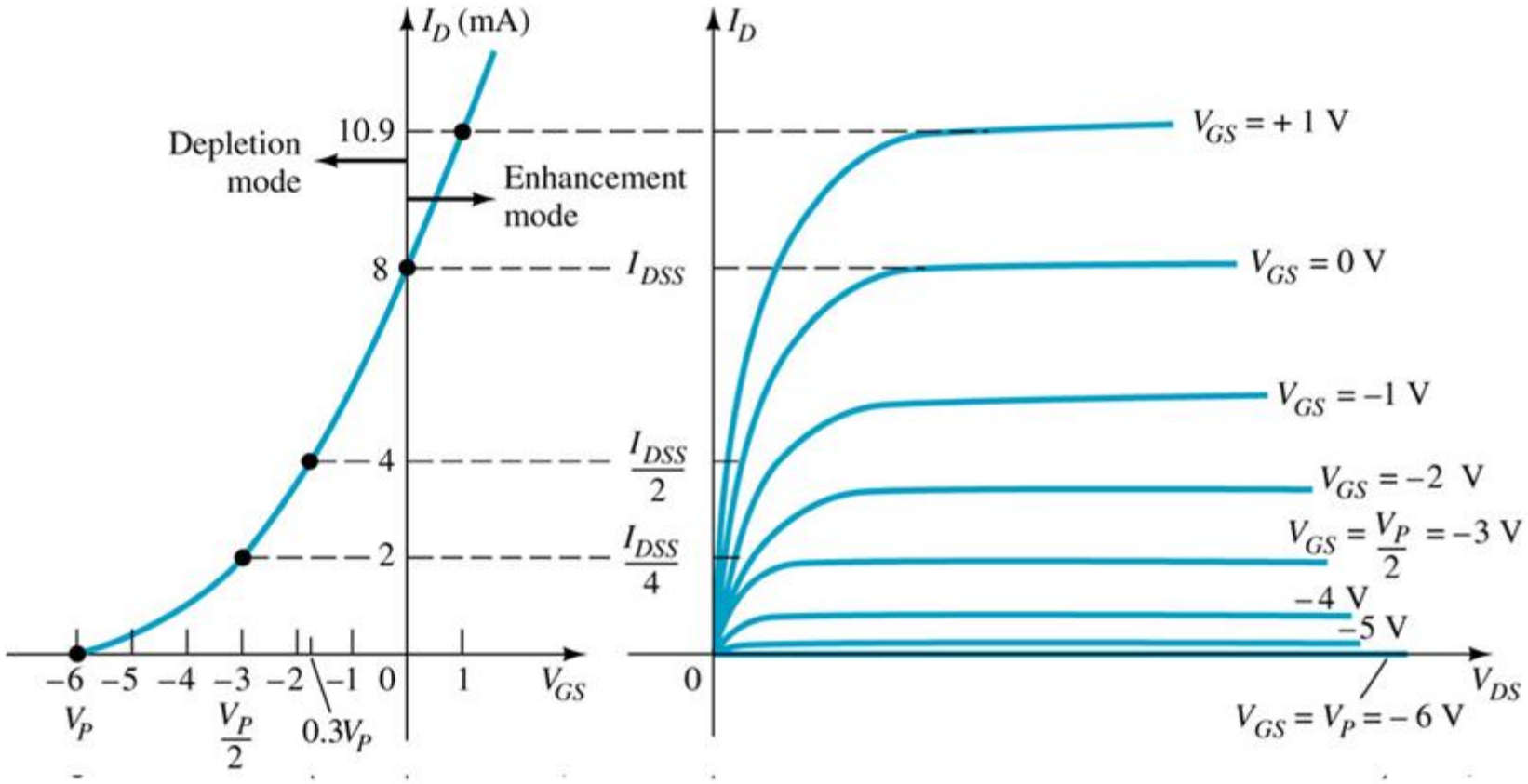
- Input resistance of a MOSFET is often that of the typical JFET.
- I_G is essentially zero amperes for dc-biased configurations.
- Metal-oxide-semiconductor FET:
  - *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact,
  - the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused.
- The insulating layer between the gate and channel has resulted in another name for the device: *insulated gate FET* or *IGFET*

- *Substrate:* A slab of *p*-type material is formed from a silicon base. It is the foundation upon which the device is constructed.
- The gate is connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO2) layer.
- *There is no direct electrical connection between the gate terminal and the channel of a MOSFET.*
- *It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.*

D-MOSFET: Basic Operation

A D-MOSFET operate in two modes:

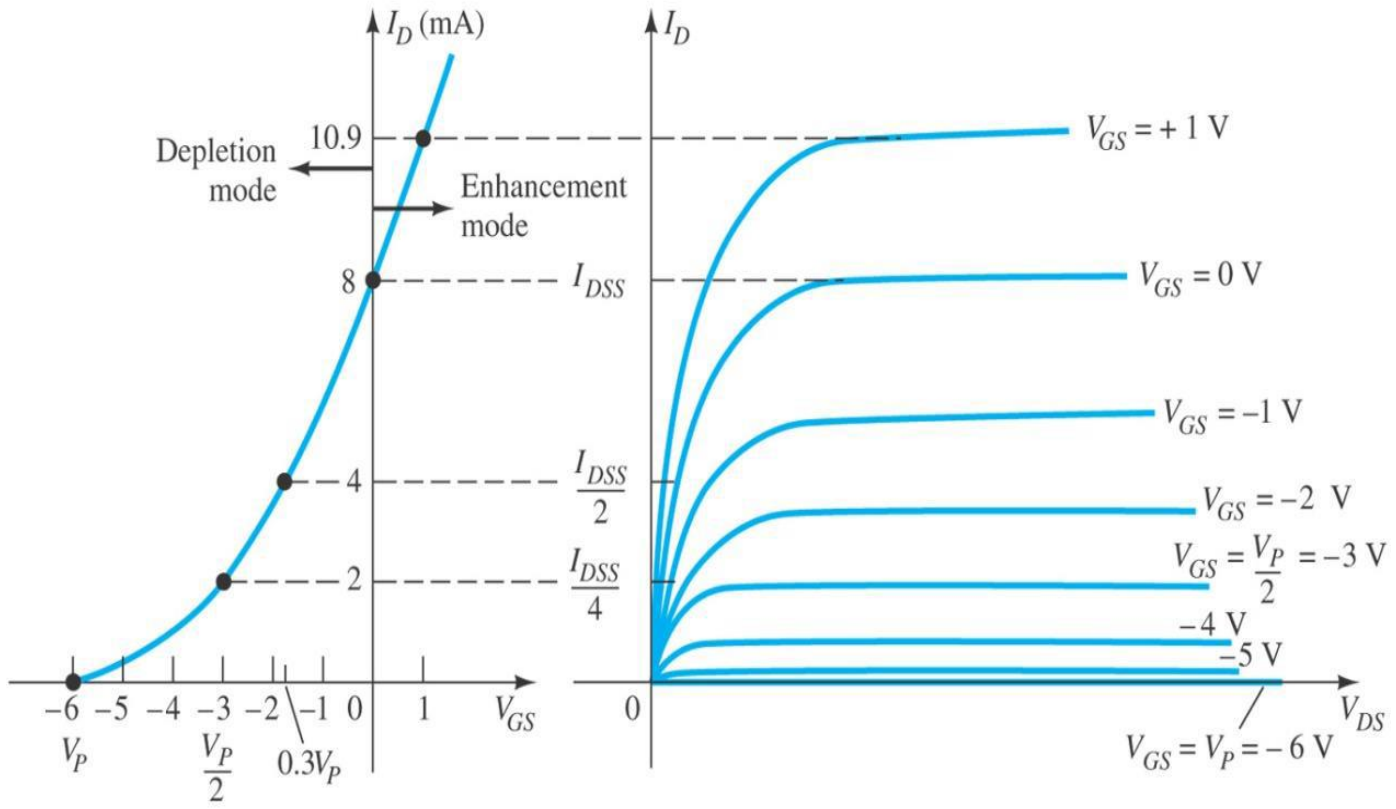
- **Depletion** mode or
- **Enhancement** mode



Depletion Mode

- **The characteristics are similar to a JFET.**
- When $V_{GS} = 0$ V, $I_D = I_{DSS}$
- When $V_{GS} < 0$ V, $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

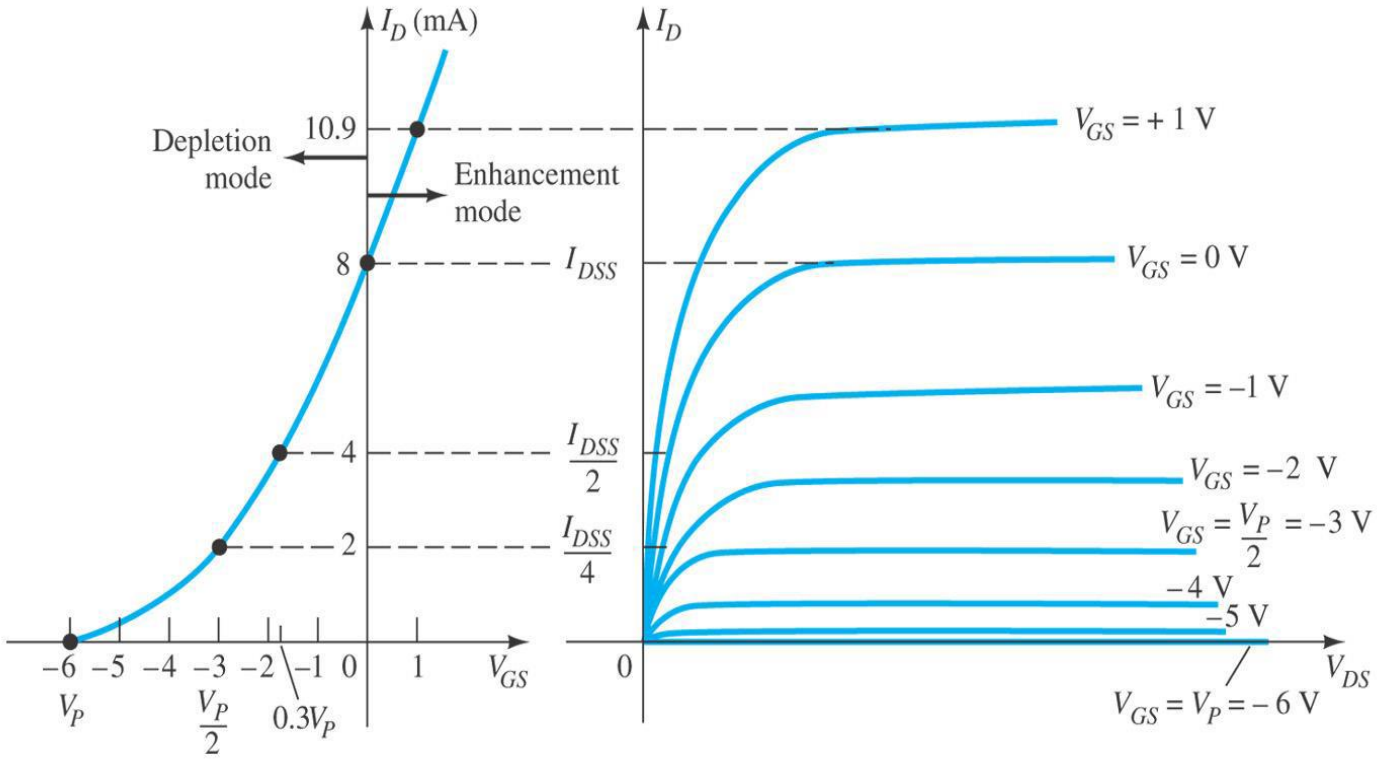
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



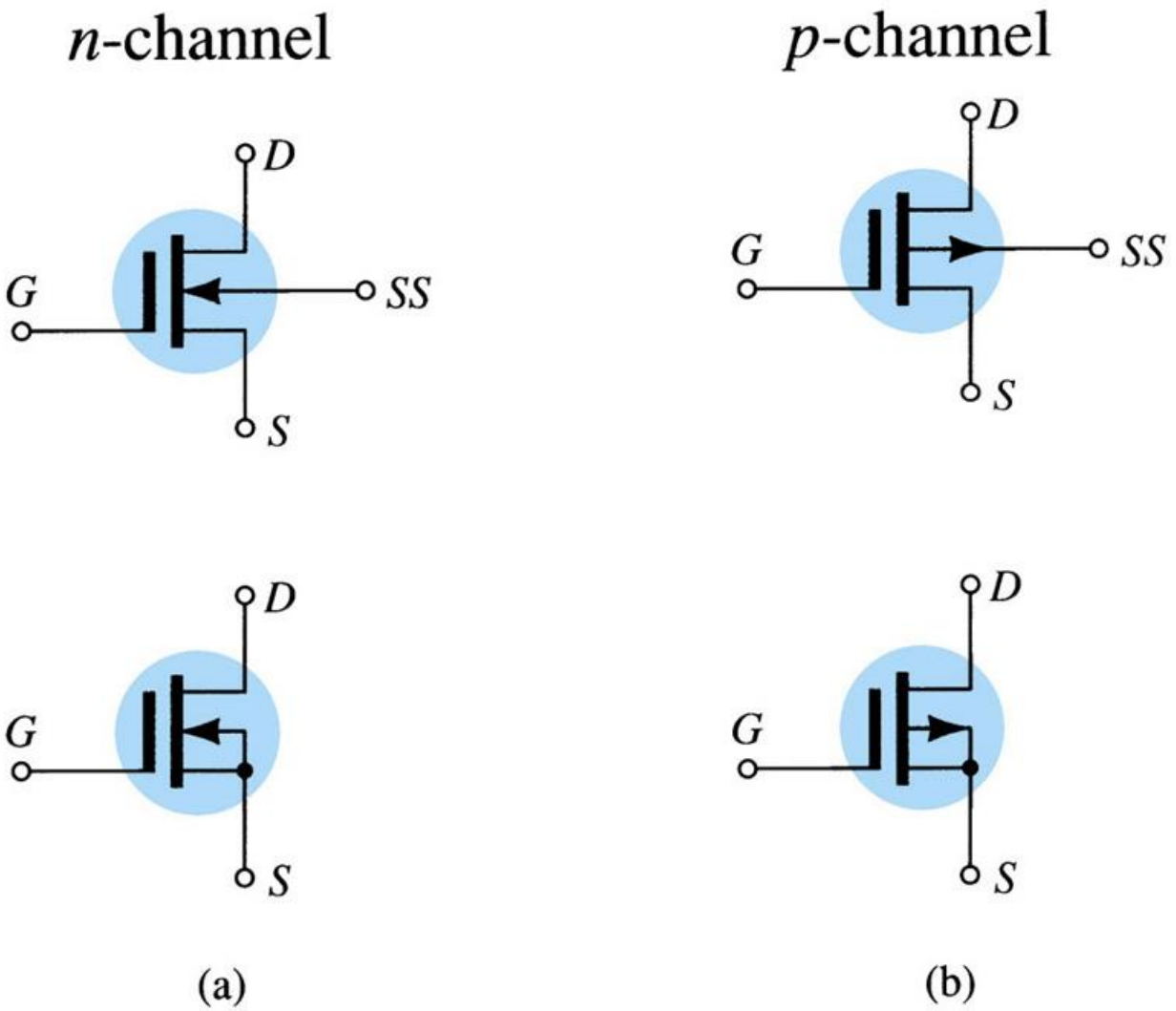
Enhancement Mode

- **Note that VGS is now a positive polarity**
- $V_{GS} > 0$ V
- I_D increases above I_{DSS}
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

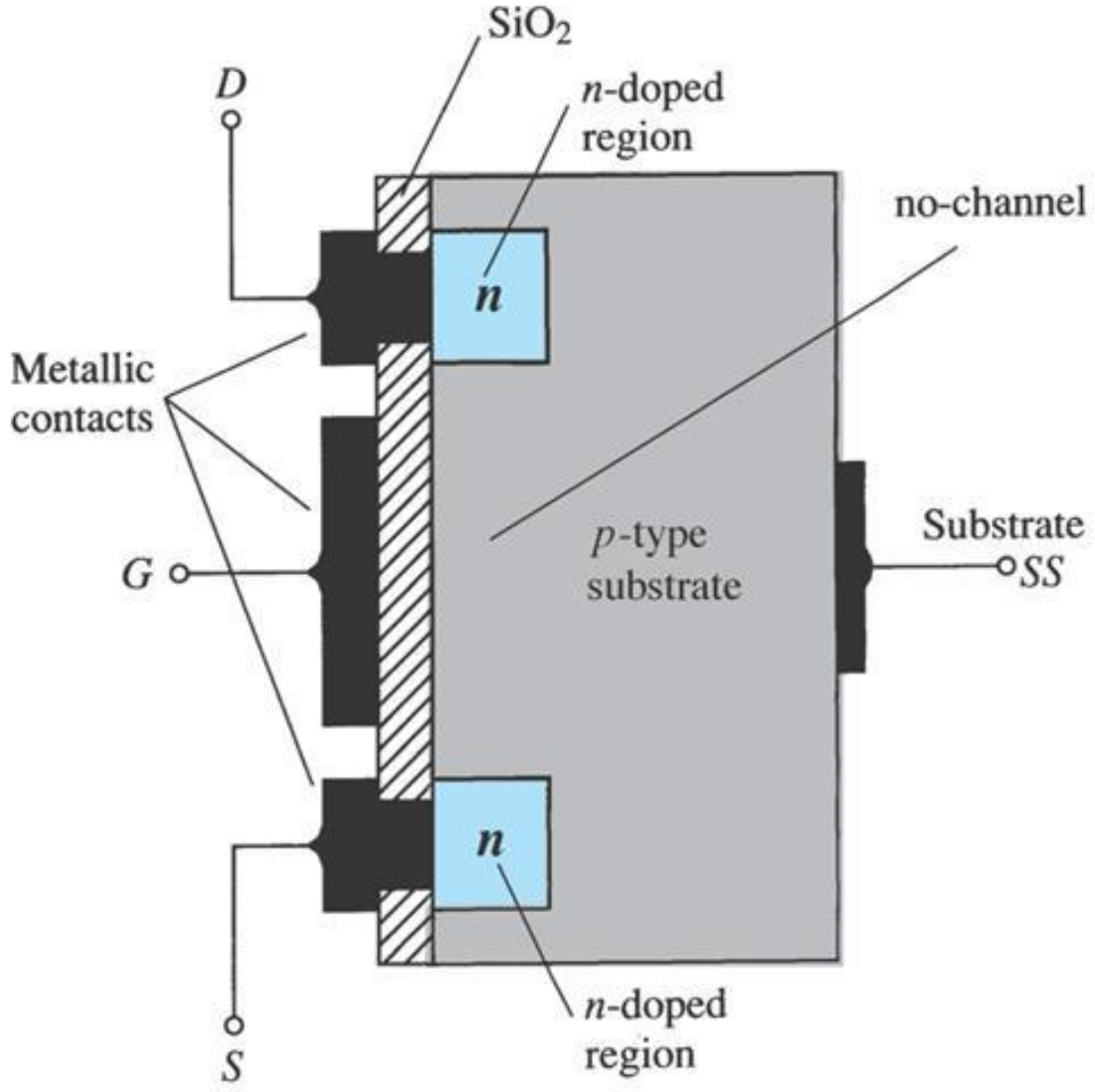


D-MOSFET Symbols



Enhancement-Type MOSFET

- The Drain (D) and Source (S) connect to the to n-doped regions.
- The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2
- **There is no channel**
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection called the Substrate (SS)



n-Channel Enhancement MOSFET

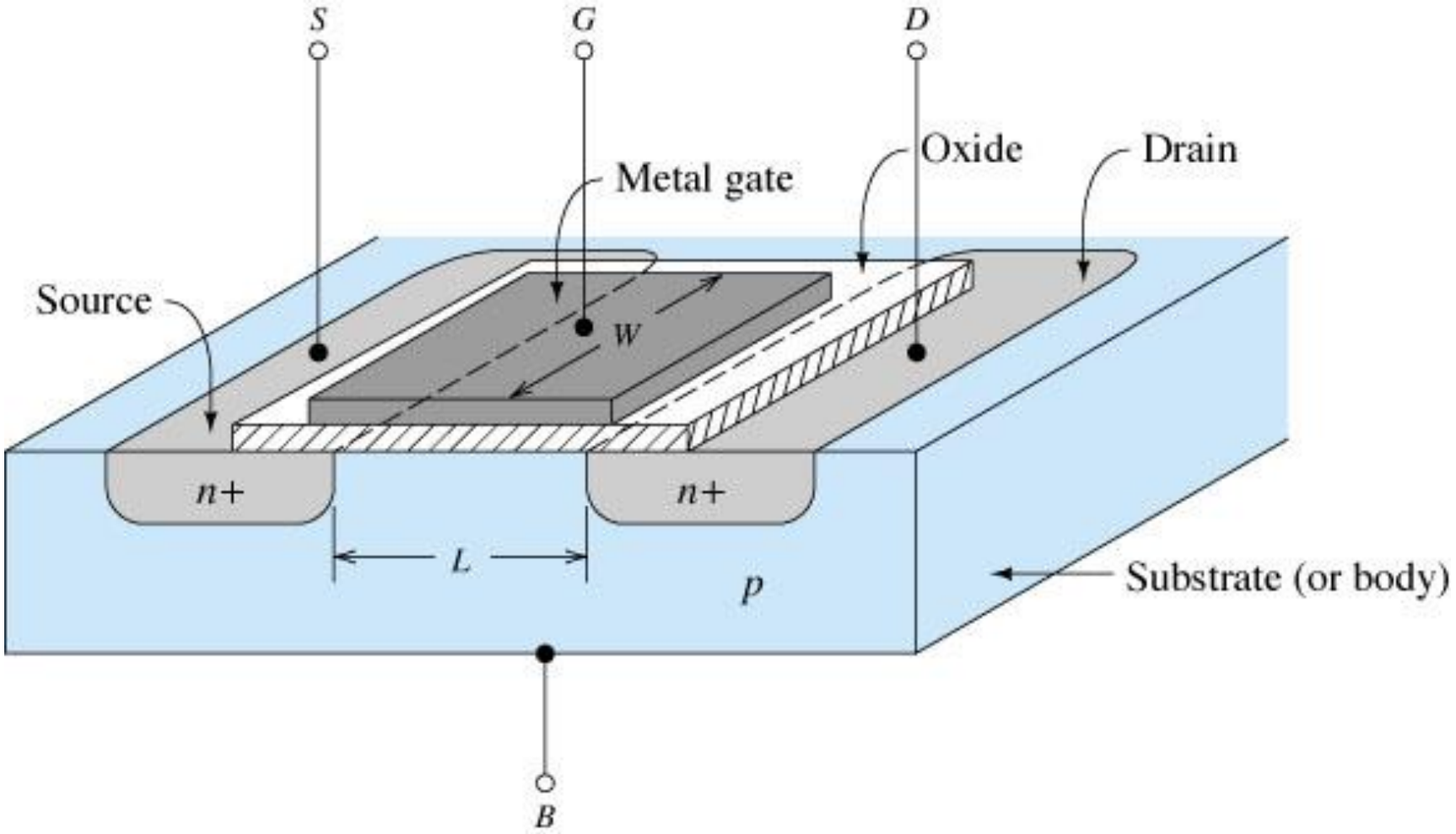
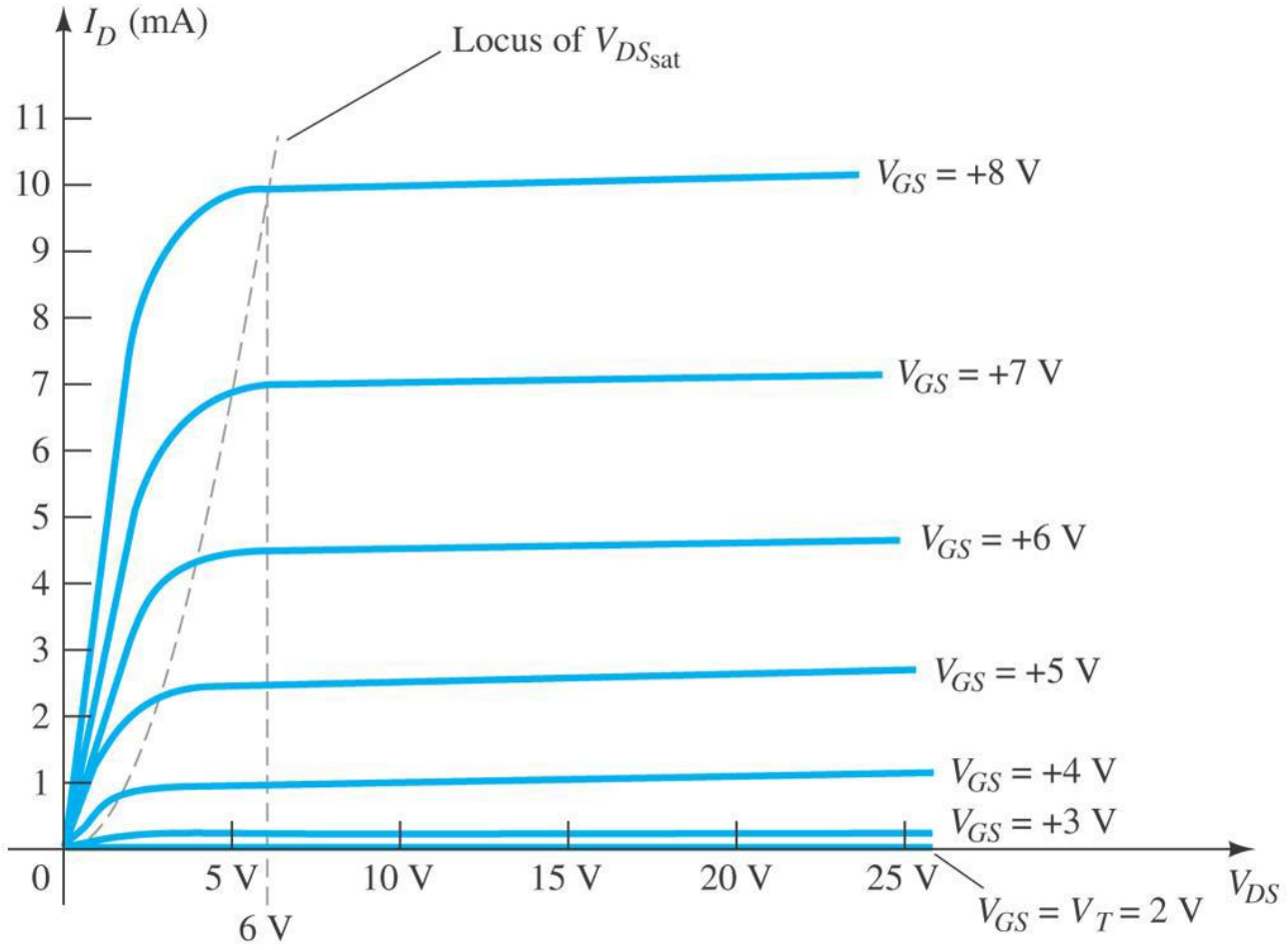


Figure: *n*-Channel Enhancement MOSFET showing channel length L and channel width W.

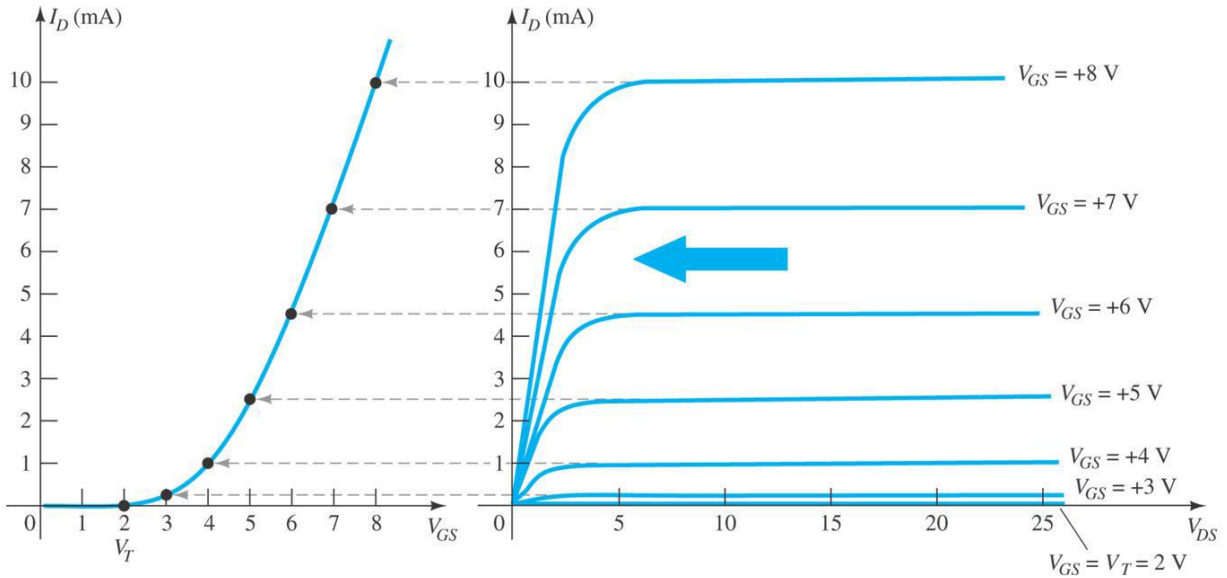
Basic Operation of the E-Type MOSFET

- E-type MOSFET operates only in the enhancement mode.
- V_{GS} is always positive.
- As V_{GS} increases, I_D increases .
- As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached.

- $V_{DSat} = V_{GS} - V_T$



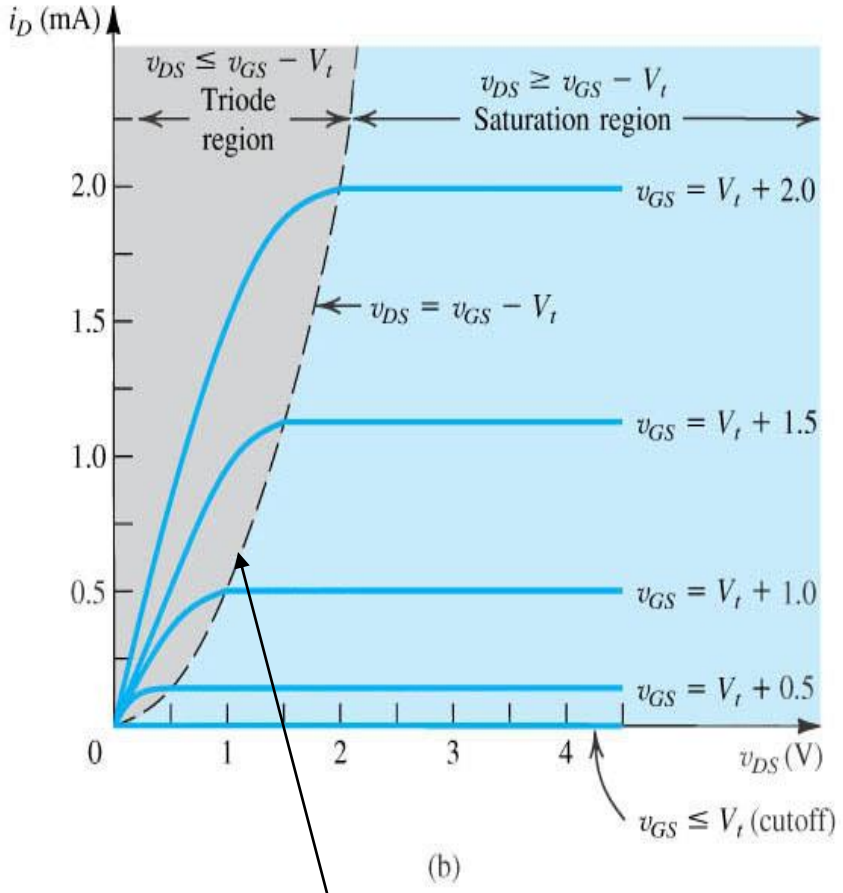
E-Type MOSFET Transfer Curve

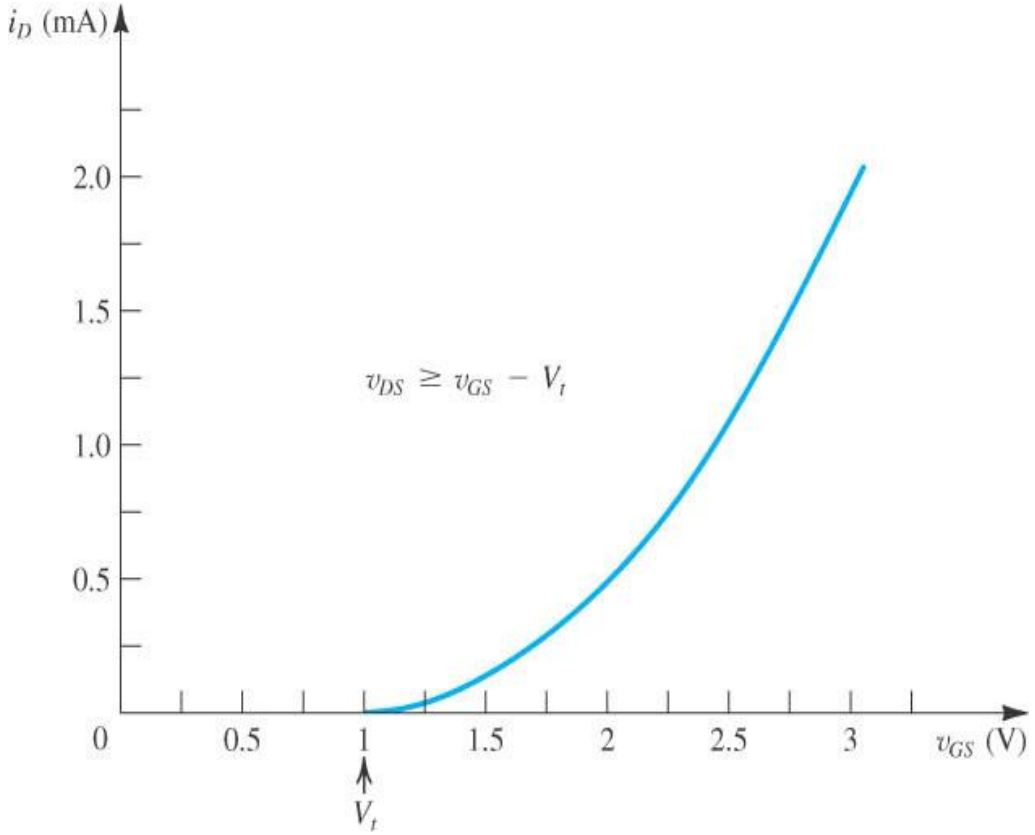


- To determine I_D given V_{GS}: $\mathbf{I_D = k(V_{GS} - V_T)^2}$
- Where: V_T = threshold voltage or voltage at which the MOSFET turns on
- *k*, a constant, can be determined by using values at a specific point and the formula

$$\mathbf{k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}}$$

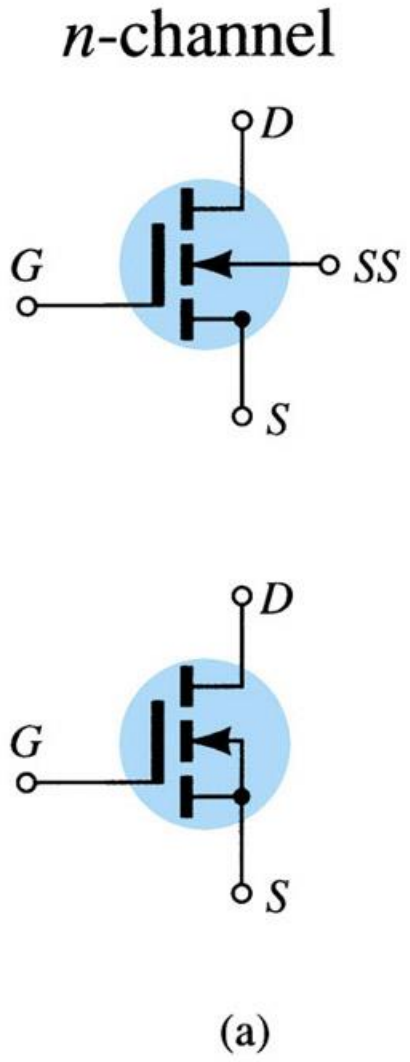
Current-Voltage Relationship of n-EMOSFET





Locus of points where

E-MOSFET Symbols

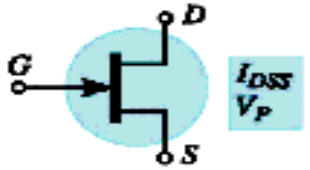


(a)

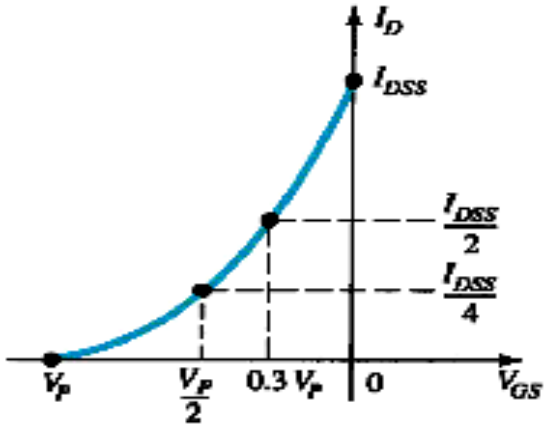
Summary:

JFET

$I_G = 0\ \text{A}, I_D = I_S$

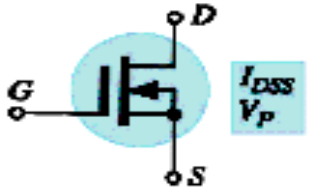


$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

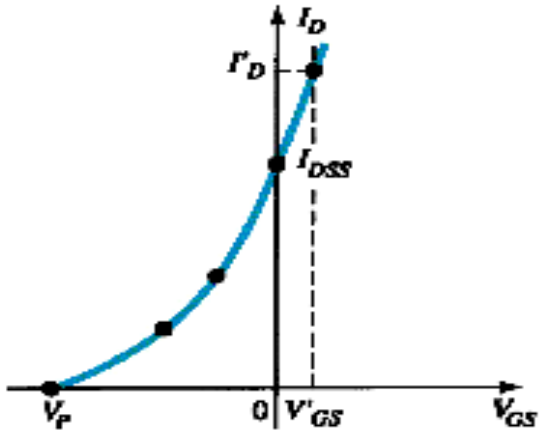


D-MOSFET

$I_G = 0\ \text{A}, I_D = I_S$

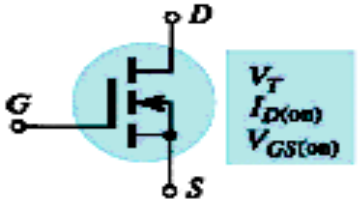


$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



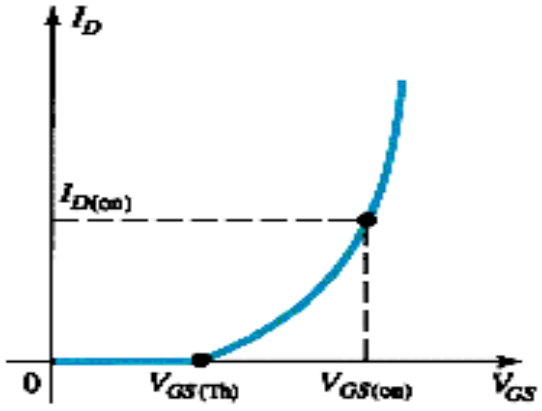
E-MOSFET

$I_G = 0\ \text{A}, I_D = I_S$



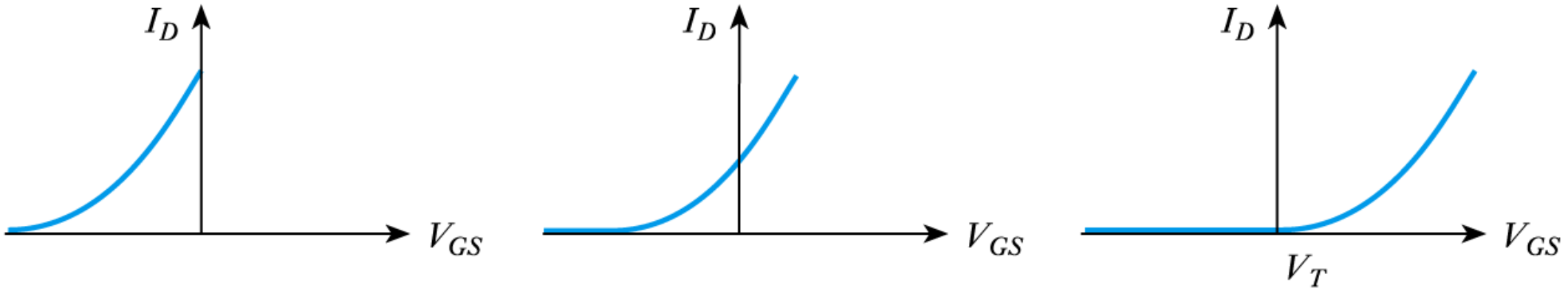
$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$



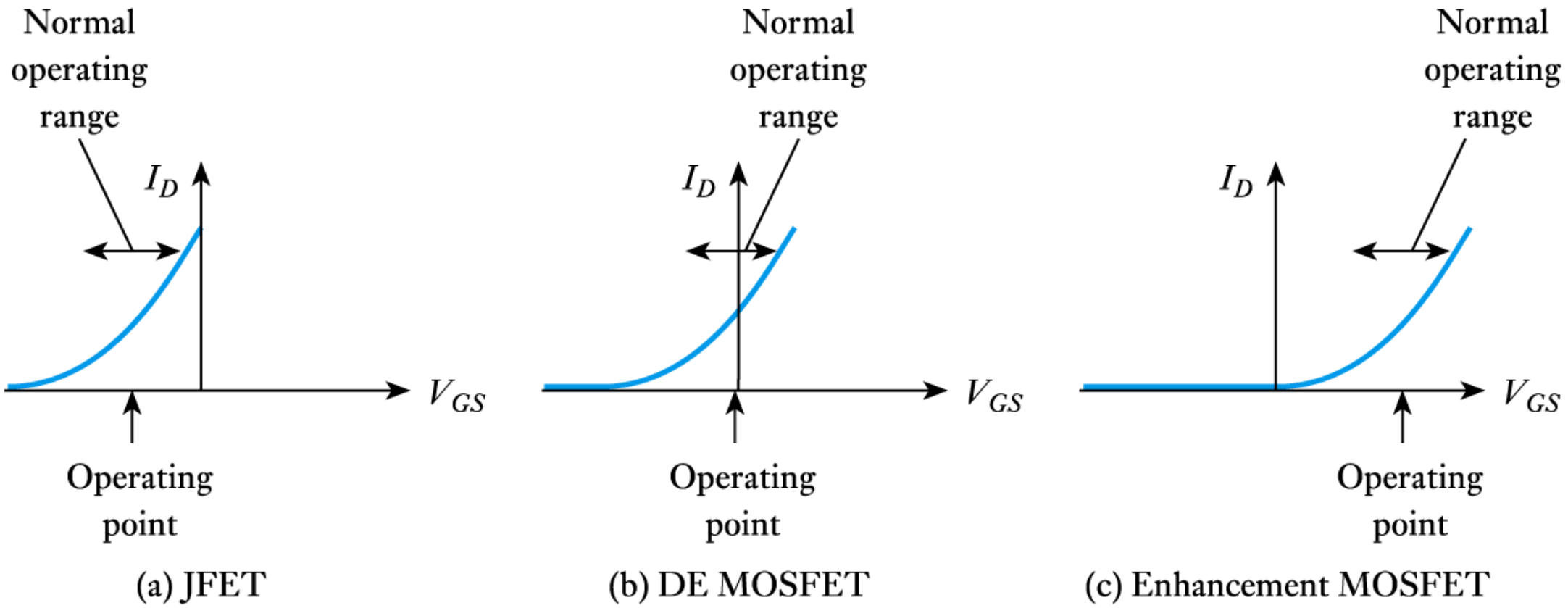
Transfer characteristics

- Similar shape for all forms of FET – but with a different offset
- Not a linear response, but over a small region might be considered to approximate a linear response



(a) JFET (b) DE MOSFET (c) Enhancement MOSFET

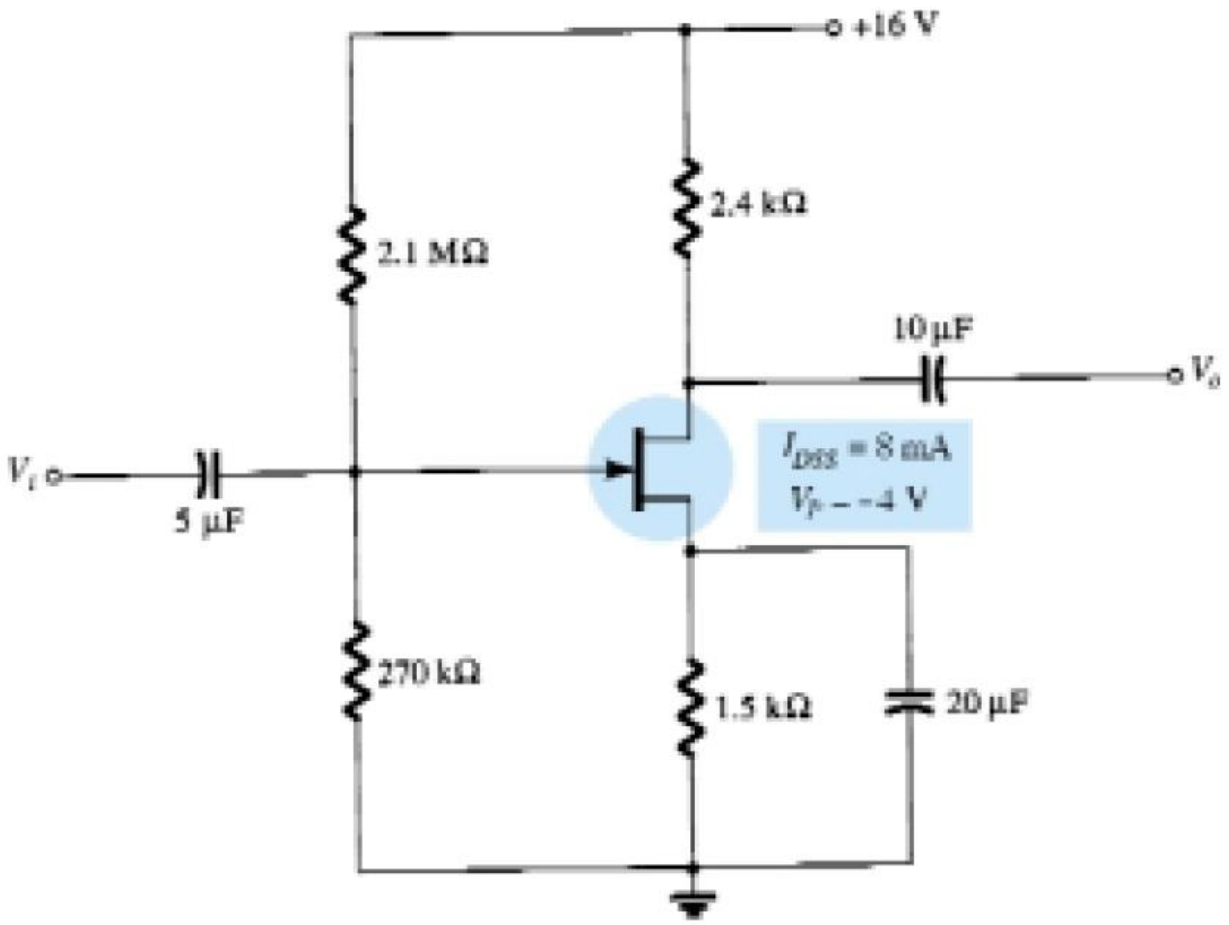
Normal Operating Ranges for FETs



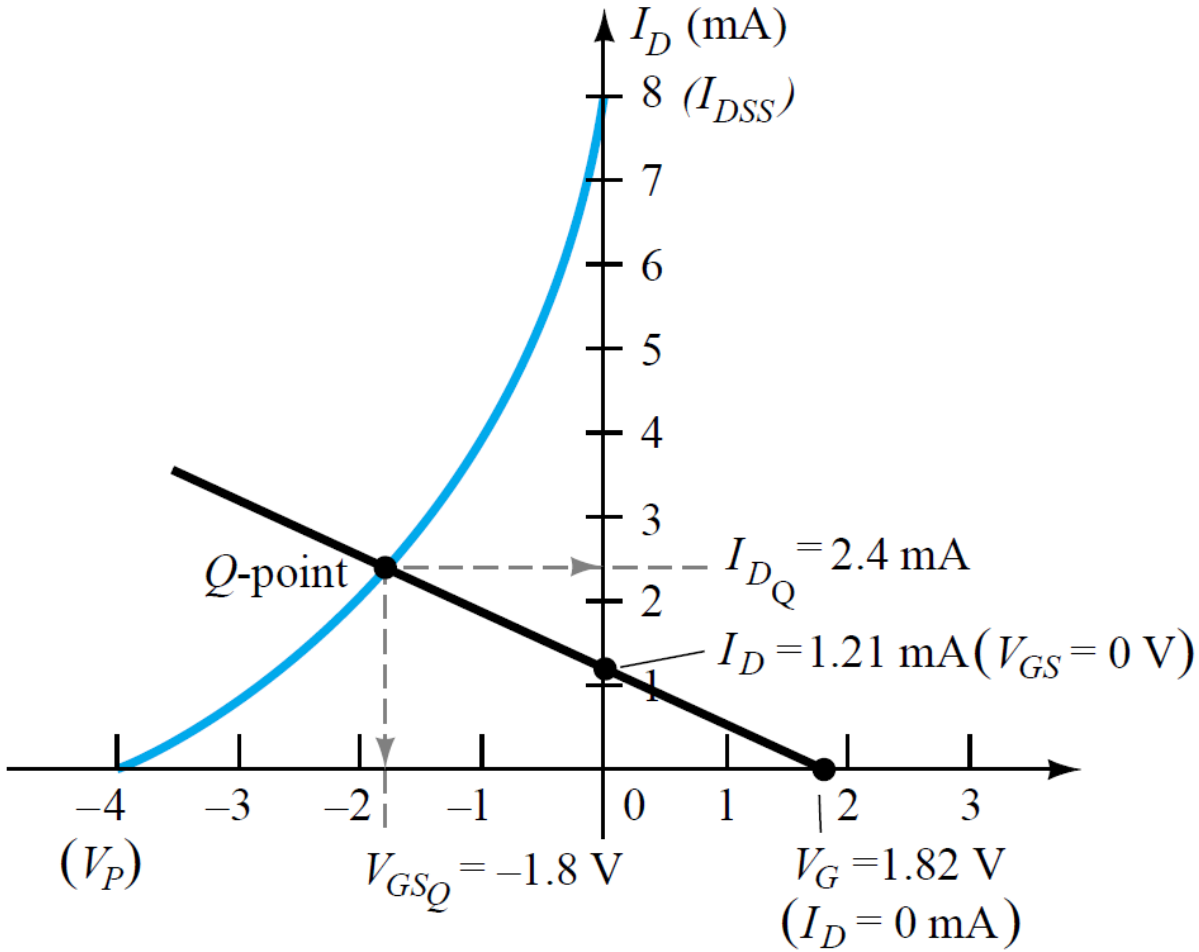
Example:

Determine:

- (a) I_{DQ} and V_{GSQ}.
- (b) V_D.
- (c) V_S.
- (d) V_{DS}.
- (e) V_{DG}.



- (a) For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation is:



- The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\ \text{k}\Omega)(16\ \text{V})}{2.1\ \text{M}\Omega + 0.27\ \text{M}\Omega}$$

$$= 1.82\ \text{V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\ \text{V}$$

When $V_{GS} = 0$ V:

$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

The resulting bias line appears on with quiescent values of

$$I_{D_Q} = \mathbf{2.4\text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8\text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$
$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$
$= \mathbf{10.24\text{ V}}$

(c) $V_S = I_D R_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$
$= \mathbf{3.6\text{ V}}$

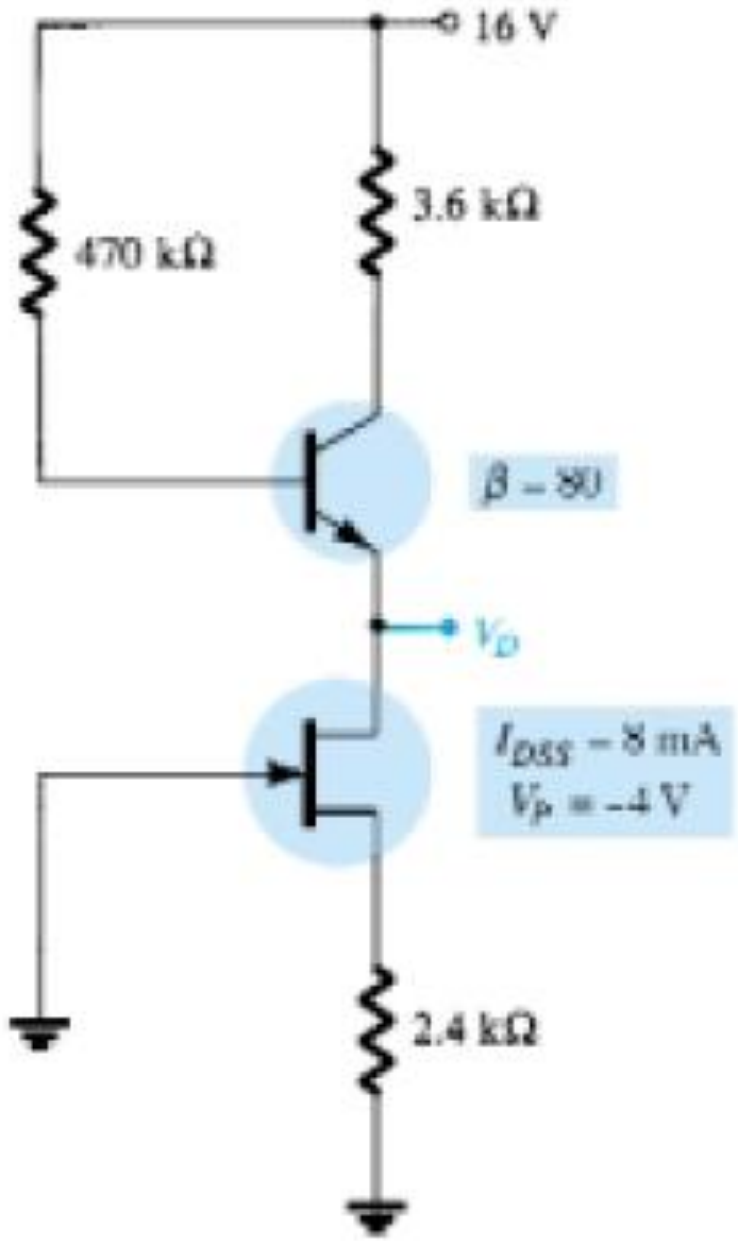
(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$
$= \mathbf{6.64\text{ V}}$
or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$
$= \mathbf{6.64\text{ V}}$

(e) V_{DG} can be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24\text{ V} - 1.82\text{ V}$$
$$= \mathbf{8.42\text{ V}}$$

Example:

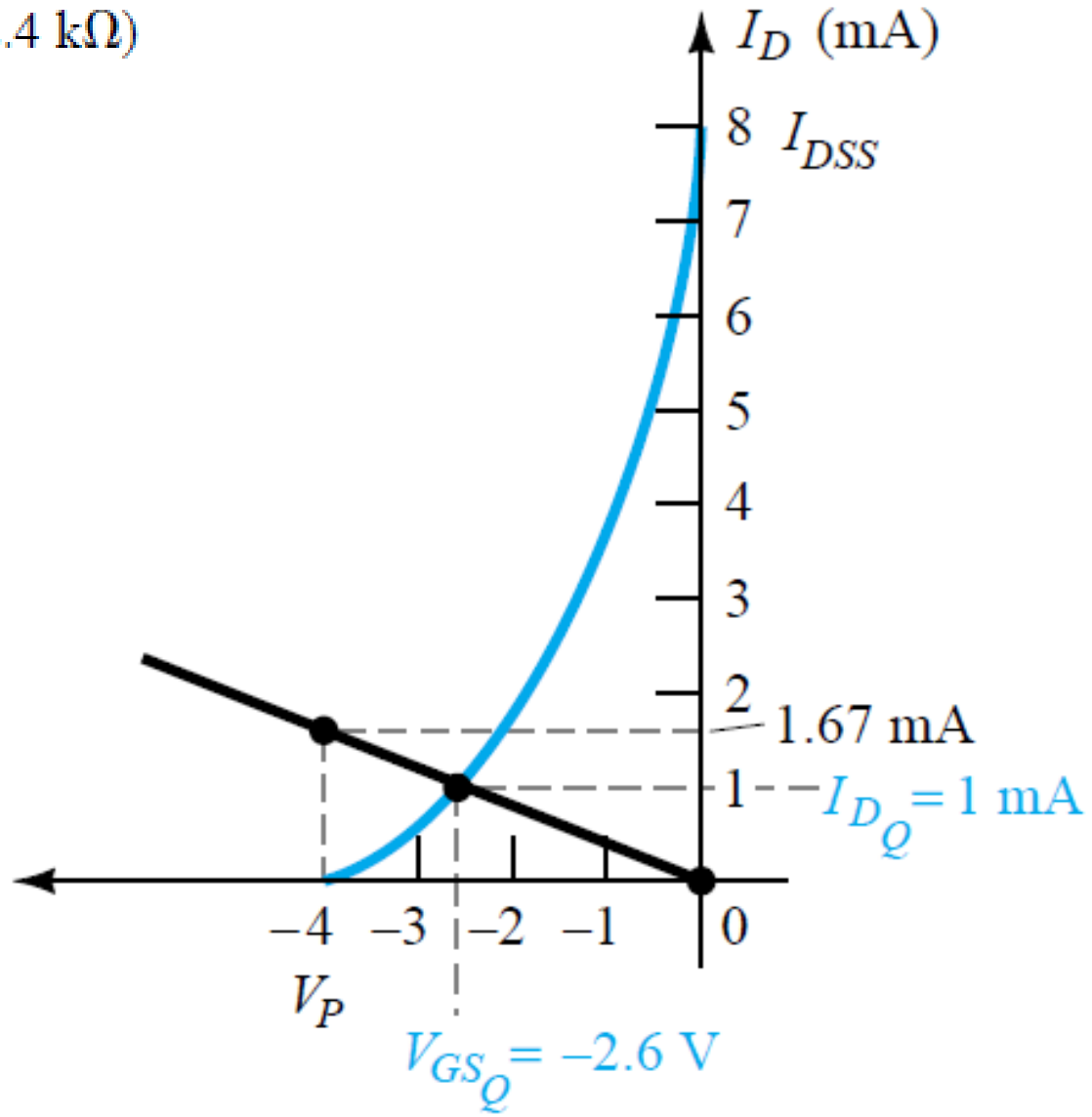
- Determine V_D



$$V_{GS} = -I_D R_S = -I_D(2.4\ \text{k}\Omega)$$

$$V_{GS_Q} = -2.6\ \text{V}$$

$$I_{D_Q} = 1\ \text{mA}$$



For the transistor,

$$I_E \cong I_C = I_D = 1 \text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{1 \text{ mA}}{80} = 12.5 \ \mu\text{A}$$

$$V_B = 16 \text{ V} - I_B(470 \text{ k}\Omega)$$

$$= 16 \text{ V} - (12.5 \ \mu\text{A})(470 \text{ k}\Omega) = 16 \text{ V} - 5.875 \text{ V}$$

$$= 10.125 \text{ V}$$

$$V_E = V_D = V_B - V_{BE}$$

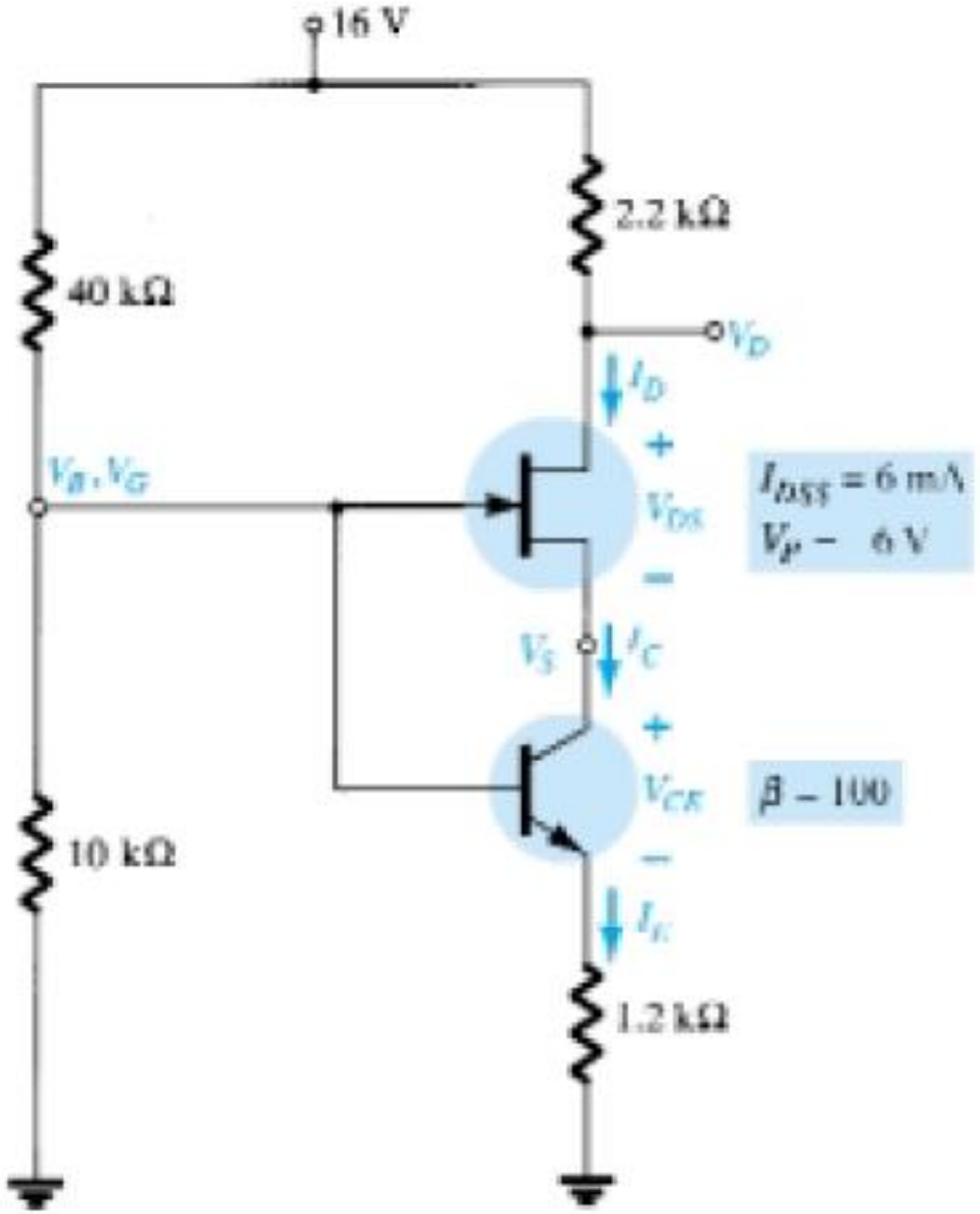
$$= 10.125 \text{ V} - 0.7 \text{ V}$$

$$= \mathbf{9.425 \text{ V}}$$

Example:

- Determine:

(a) V_G.
(b) V_{GSQ} and I_{DQ}.
(c) I_E.
(d) I_B.
(e) V_D.
(f) V_C.



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