Clippers and Clampers

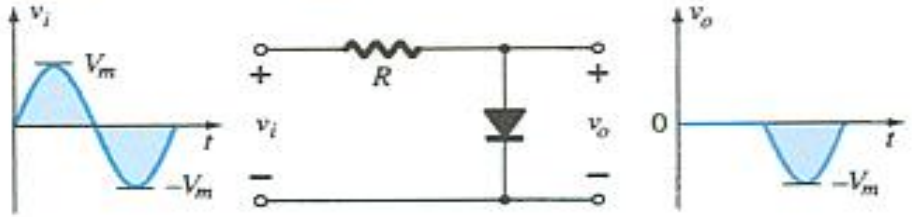
Semiconductor Devices and Circuits

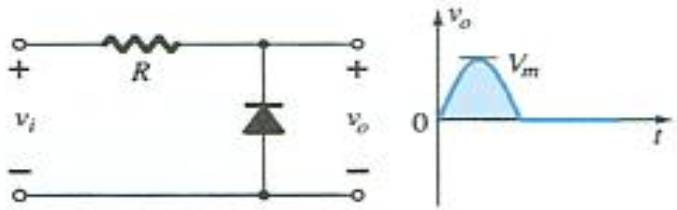
(ECE 181302)

3rd December 2021

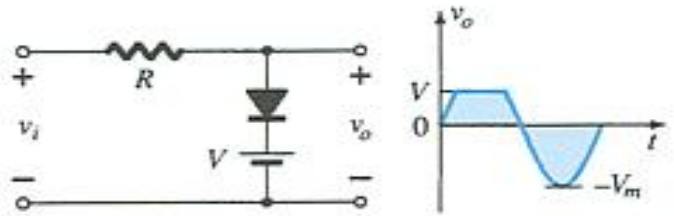
Summary of Clipper Circuits

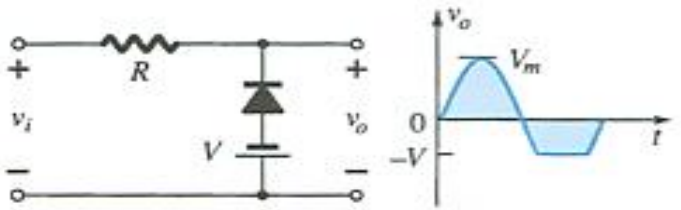
Simple Parallel Clippers (Ideal Diodes)

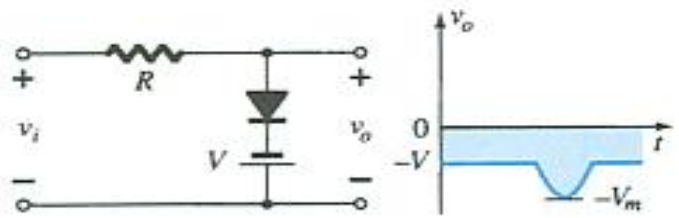


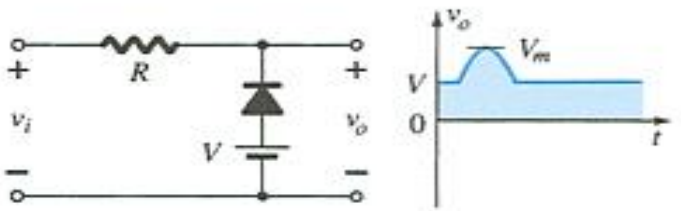


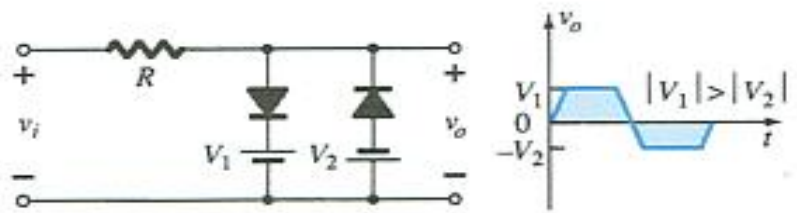
Biased Parallel Clippers (Ideal Diodes)











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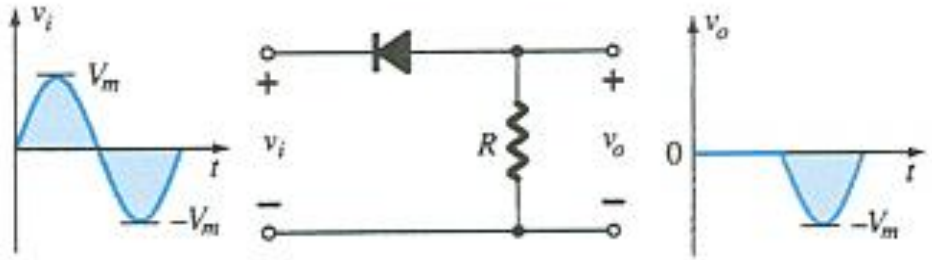
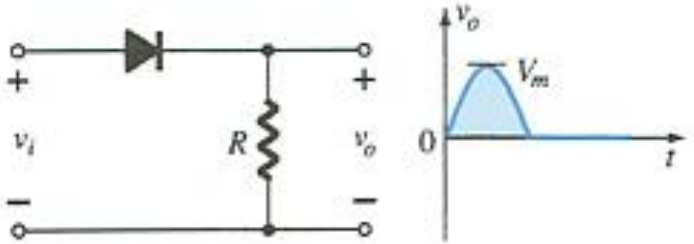
Simple Series Clippers (Ideal Diodes)

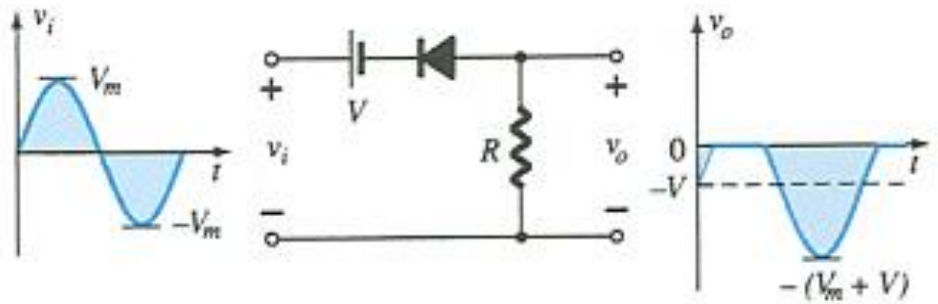
POSITIVE

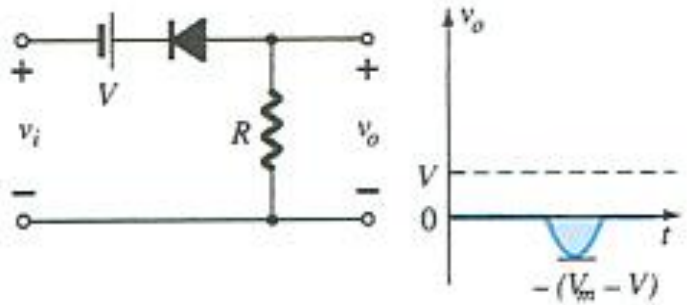


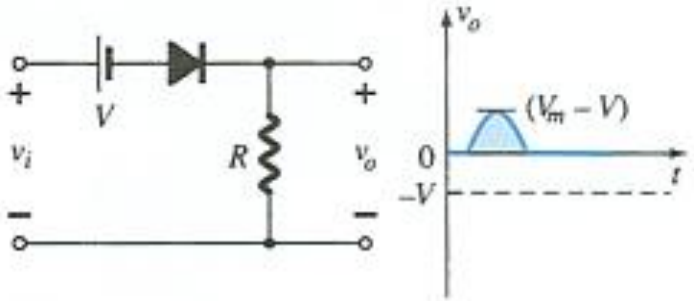
NEGATIVE

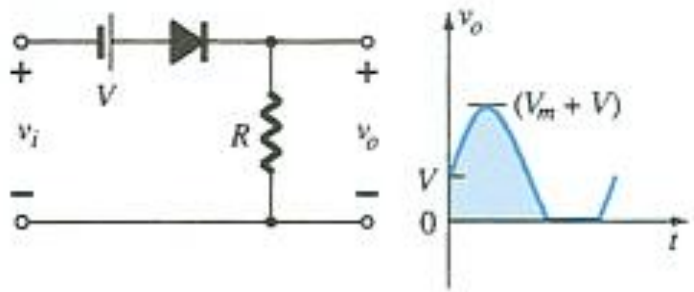


Biased Series Clippers (Ideal Diodes)

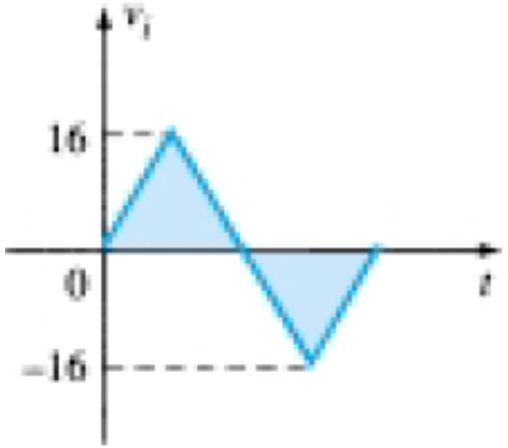


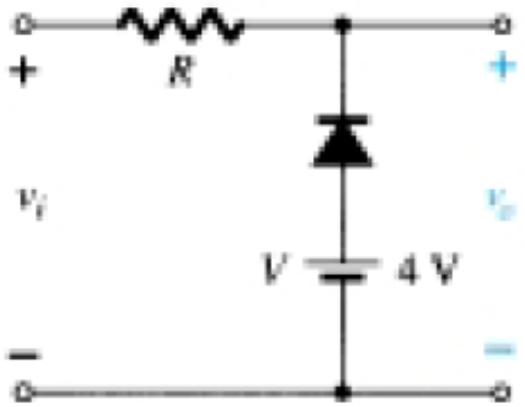




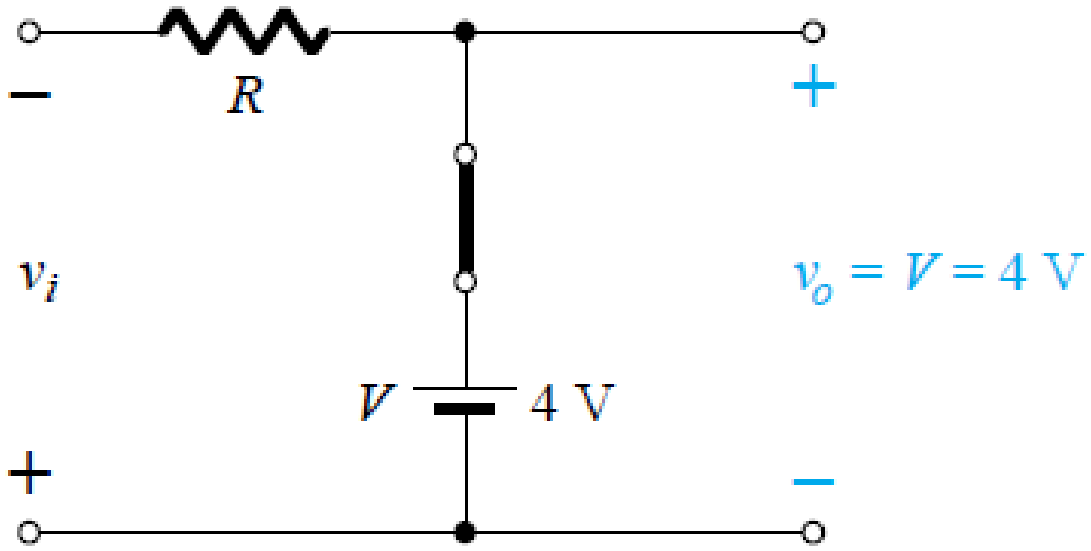


Example: Determine V_o

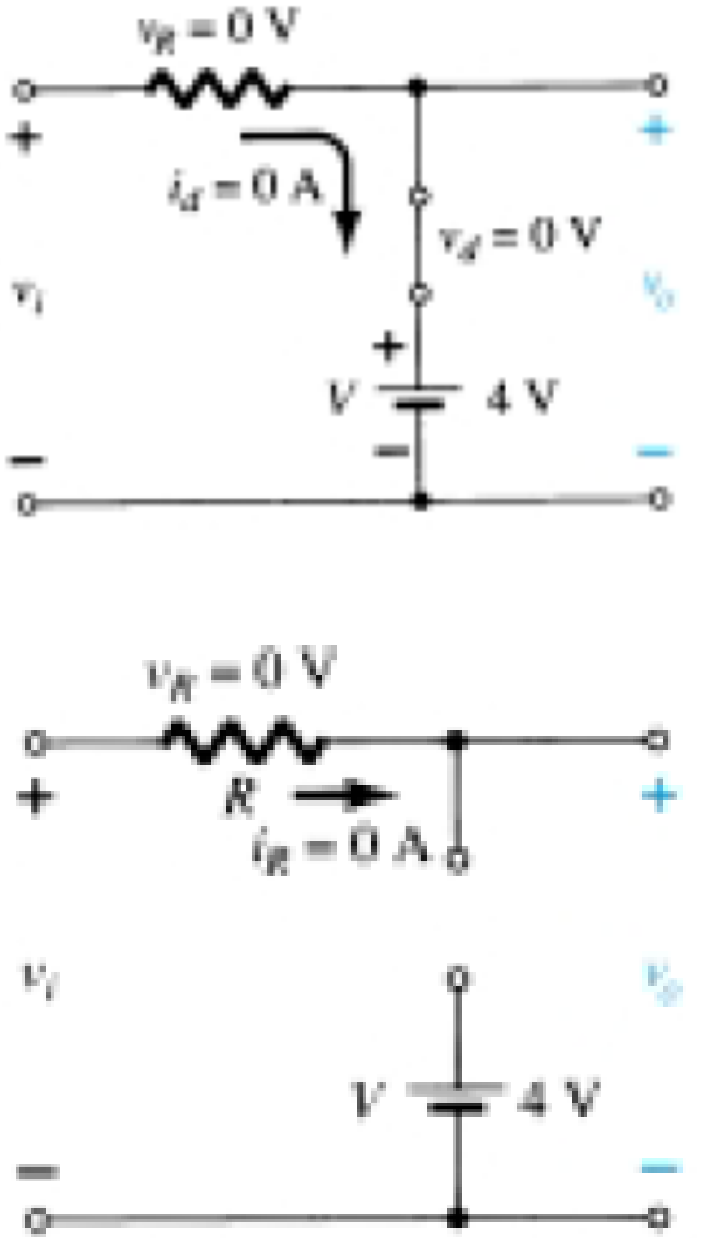


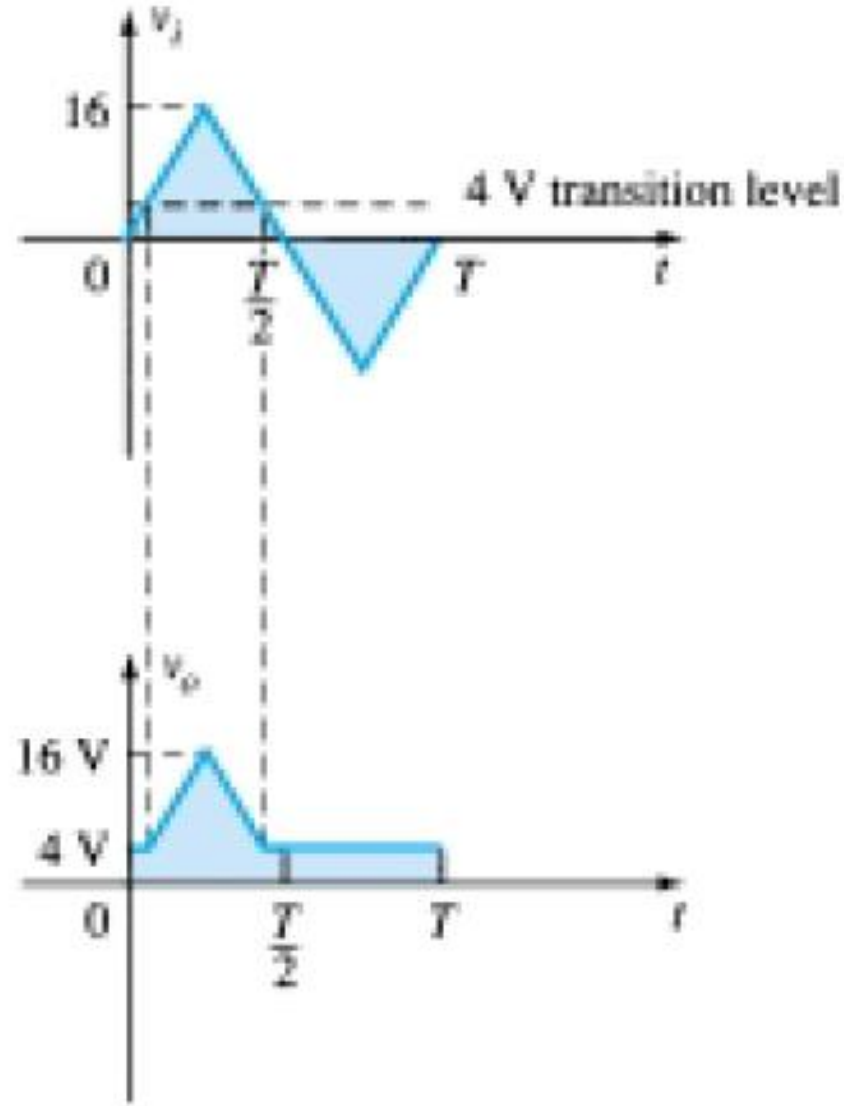


- The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the “on” state for the negative region of the input signal.
- For the negative region the network the defined terminals for *vo* require that *vo* = *V* = 4 V.



- The transition state can be determined from for the condition i_d = 0 A at v_d = 0 V. The result is v_i (transition) = V = 4 V.
- The 4 V dc (bias) is “pressuring” the diode to stay in the shortcircuit state. The input voltage must be greater than 4 V for the diode to be in the “off” state (RB the diode) or any input voltage less than 4 V will result in a short-circuited diode.
- For the open-circuit state v_o = v_i.

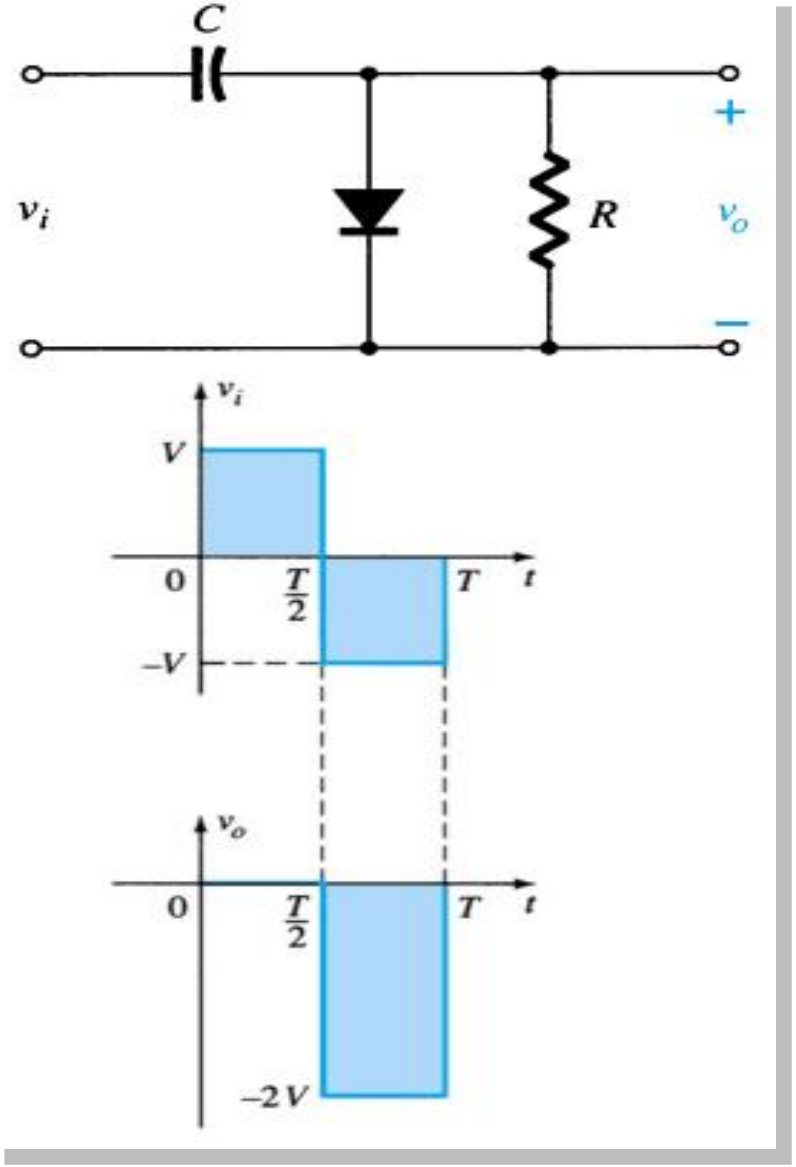



v_i
16
4 V transition level
0
$\frac{T}{2}$
T
t
v_o
16 V
4 V
0
$\frac{T}{2}$
T
t

Clamper

- Also known as dc restorers or clamped capacitors.
- Shifts an input signal by an amount defined by an independent voltage source.
- While clippers limit the part of the input signal that reaches the output according to some reference level(s), the entire input reaches the output in a clamping circuit – it is just shifted so that the maximum (or minimum) value of the input is “clamped” to the independent source.

- A diode and capacitor can be combined to “clamp” an AC signal to a specific DC level.
- The network will “clamp” a signal to a different dc level.
- The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift.



Note:

- Start the analysis of clamping network, by considering that part of the input signal that will forward bias the diode.
- During the period that the diode is in the “ON” state, assume that capacitor will charge up instantaneously to a voltage level determined by the network.
- Assume that during the period when the diode is in “OFF” state, capacitor will hold on its established voltage level.
- Keep in mind the general rule, that

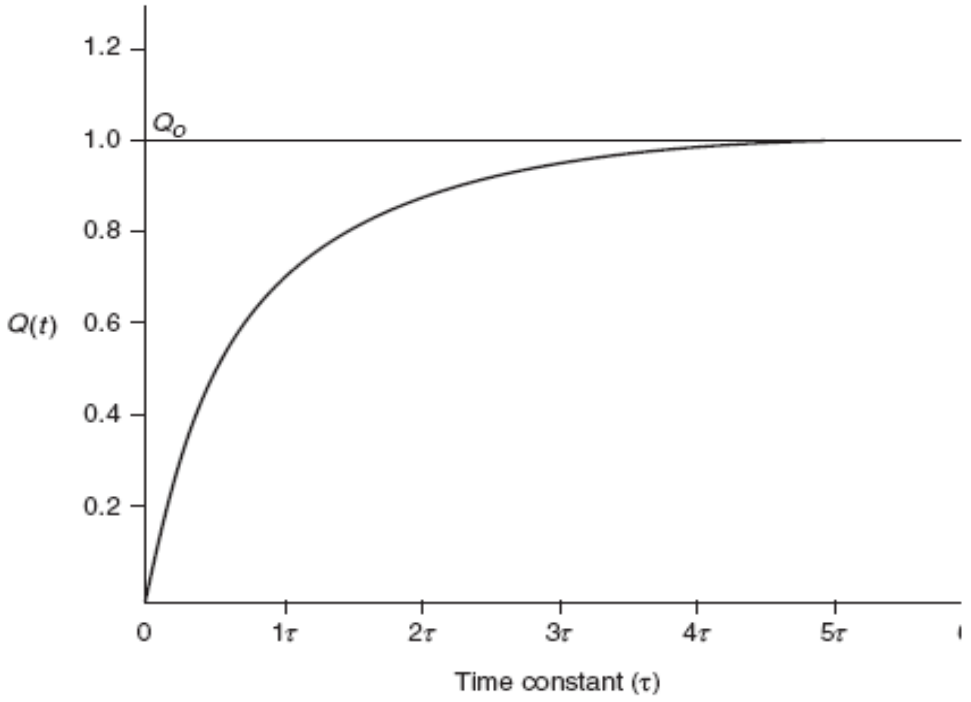
  Total swing of total output = Swing of input signal

- Before probing into the clamper circuit one must have a basic understanding of a transient *RC circuit.*
- From a series *RC transient circuit applied across a dc voltage E_O, the instantaneous* charge across the capacitor at any time is given by

$$Q(t) = Q_o\left(1 - e^{-t/RC}\right)$$

Q_0 *= E_0C where, C is the capacitance.*

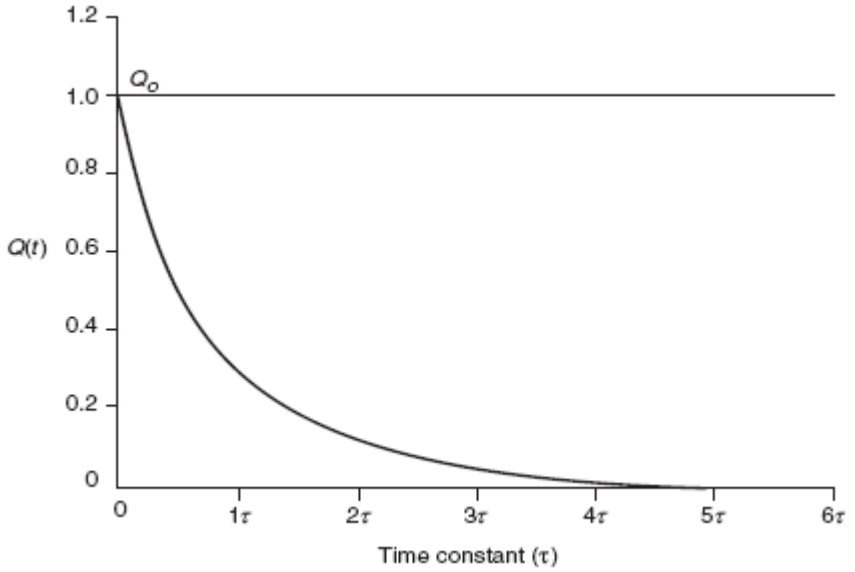
- Time constant $\tau = RC$. The rise time becomes smaller if we decrease the time constant.



Charging of a *RC circuit*

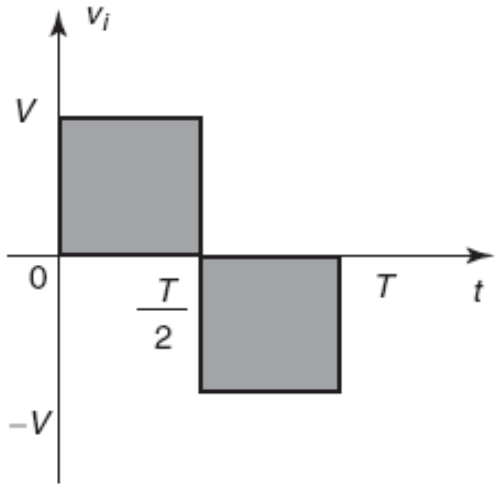
➢The discharge will occur quickly if the time constant of the circuit is decreased.

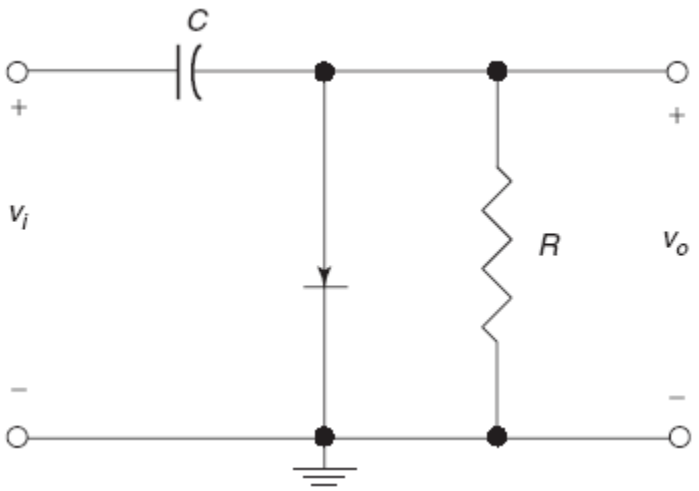
➢The magnitude of *R and C must be so chosen that the time constant, τ = RC, is large enough to ensure that the voltage across* the capacitor does not discharge significantly during the interval the diode is non-conducting.



Discharging of an *RC circuit*

➢ The clamping circuit will clamp the input signal to the zero level.





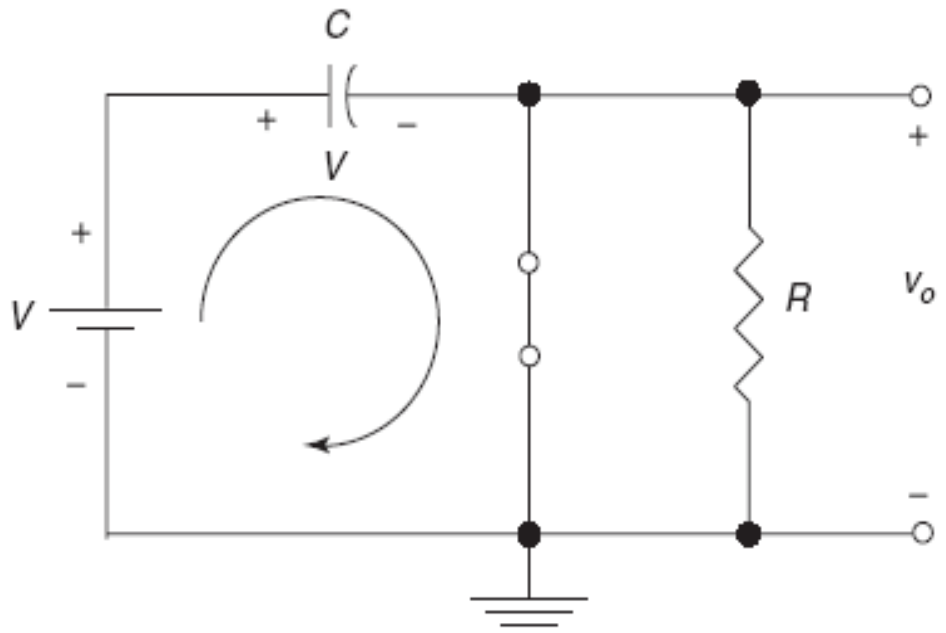
Simple clamper circuit

- During the interval 0 –*T/2,* with the diode in the ON state effectively "short out" the effect of the resistor *R.*
- The resulting *RC time constant is so small that the* capacitor will charge to *V volts very quickly. During* this interval the output voltage is directly across the short circuit and $v_o = 0$ *V.*
- During negative half cycle diode will be in the open-state condition. Applying KVL around the input loop of figure will result in:

$$-V - V - v_o = 0$$

$$\text{or,} \qquad v_o = -2\,\text{V}$$

- The negative sign results from the fact that the polarity of 2 V is opposite to the polarity defined for v_o.
- *For a clamping network the total swing of the* output is equal to the total swing of the input.

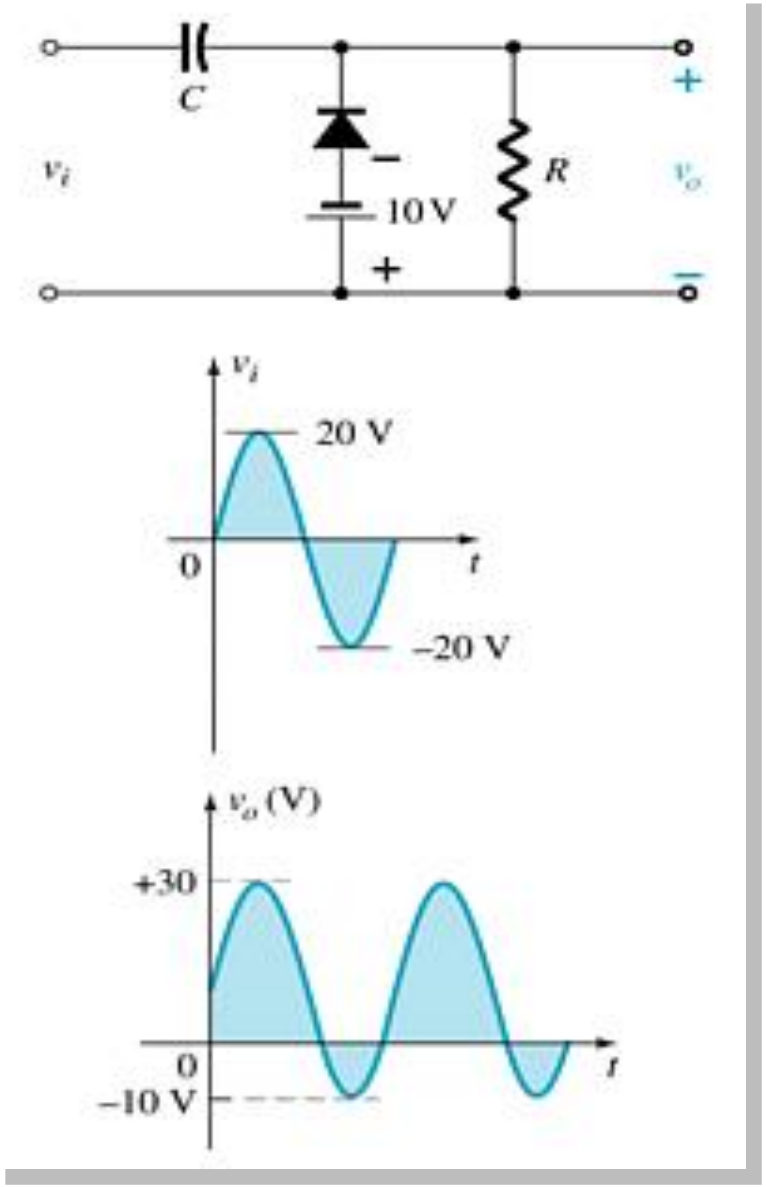


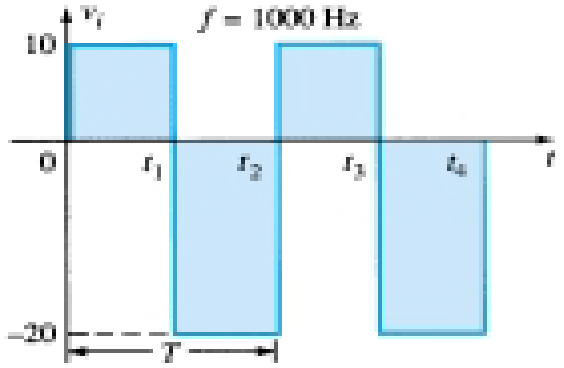
State of the circuit in the positive half-cycle

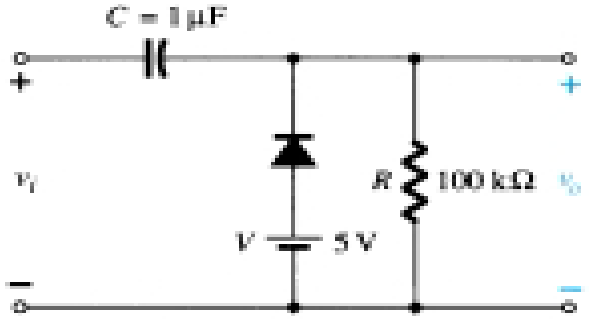
Biased Clamper Circuits

The input signal can be any type of waveform such as sine, square, and triangle waves.

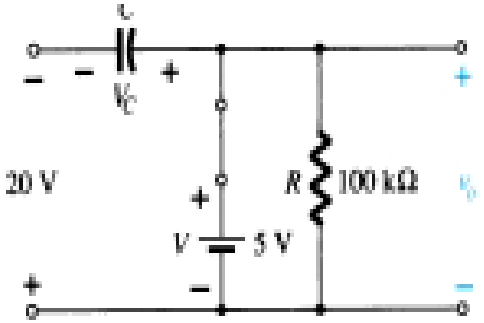
The DC source lets you adjust the DC clamping level.



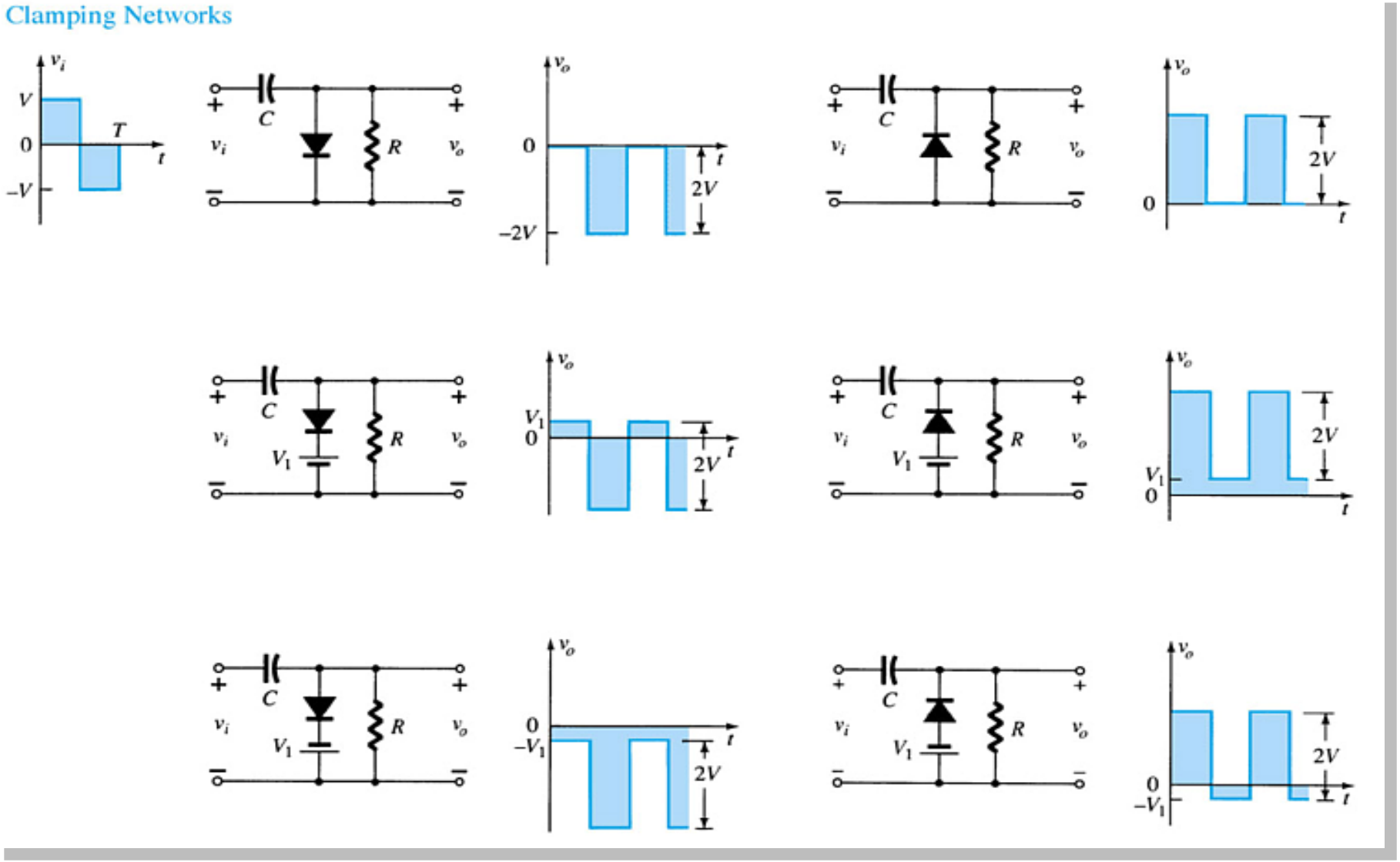




For t1-t2 cycle



Summary of Clamper Circuits



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References:

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