Module-1

Logic Families – Characteristics and Types

Table of Content

Learning Outcome:

After completing this module, you will be able to

1. **Understand need of logic digital ICs**
2. **Understand significance of logic families**
3. **Understand characteristics of logic families**
4. **Identify different types of logic families**
5. **Know about evolution of different logic families**

1.1 Introduction

The first logic circuit was developed using discrete circuit components. Using advance techniques, these complex circuits can be miniaturized and produced on a small piece of semiconductor material like silicon. Such a circuit is called integrated circuit (IC). Now-a-days, all the digital circuits are available in IC form. While producing digital ICs, different circuit configurations and manufacturing technologies are used. This results into a specific logic family. Each logic family designed in this way has identical electrical characteristics such as supply voltage range, speed of operation, power dissipation, noise margin etc.

In this module, we discuss significance and types of logic families. The positive and negative logic and its significance are also discussed. In addition to this, different characteristics which are the key parameters in deciding the logic family for any circuit design are discussed in detail. The module is concluded with explanation of the brief history of the logic family in terms of discrete logic circuits.

1.2 Significance of Logic families

Almost all electronic gadgets make use of different digital systems for their operation. All the digital systems use some kind of digital ICs. For the sake of simplicity in design and compatibility in constructing any complex digital system, all digital circuits (ICs) used in the design process should be from same logic family.

For the expansion of the system, it is necessary to connect different logic circuits together. In order to connect the output of one logic circuit to the input of another logic circuit, one must have circuit with similar characteristics. If the electrical IO characteristics of these logic circuits are not similar, there is a need to design an interfacing circuit to maintain the compatibility of digital logic ICs. This interfacing circuit will match the electrical characteristics of the logic circuits. This ensures the compatibility for proper operation of the circuit.

This is the key concept behind family for logic circuits. In a logic family, the family members have similar electrical characteristics. Digital logic circuit has to be designed considering these compatibilities of different logic families in terms of different characteristics and parameters associated with the families.

1.3 Types of logic families

As explained in previous section, logic families are the logic circuits having identical electrical parameters. It is a group of compatible ICs with the same logic levels and supply voltages for performing various logic functions. They are fabricated using a specific circuit configuration which is referred to as a **Logic family**. The circuit design of the basic gate of each logic family is the same.

The logic family is designed by considering the basic electronic components such as resistors, diodes, transistors, and MOSFET; or combinations of any of these components. Accordingly, logic families are classified as per the construction of the basic logic circuits. Many different logic families of digital ICs have been introduced commercially are listed in table 1.

Table 1. Logic families and the components used for construction of logic family

Name of logic family	Components used
DL(Diode Logic)	Diodes
RTL(Resistor Transistor Logic)	Resistors and transistors
DTL(Diode Transistor Logic)	Diodes, transistors and resistors
TTL(Transistor Transistor Logic)	Transistors and resistors
ECL(Emitter Coupled Logic)	Transistors and diodes
PMOS(P channel Metal Oxide Semiconductor Logic)	P- MOSFETs
NMOS(N channel Metal Oxide Semiconductor Logic)	N- MOSFETs
CMOS(Complementary Metal Oxide Semiconductor Logic)	P ï MOSFET and N-MOSFET

Logic families are classified according to the principle type of electronic components used in their circuitry as shown in Figure 1. They are

a. Bipolar ICs: which uses diodes and transistors (BJT)
b. Unipolar ICs: which uses MOSFETs

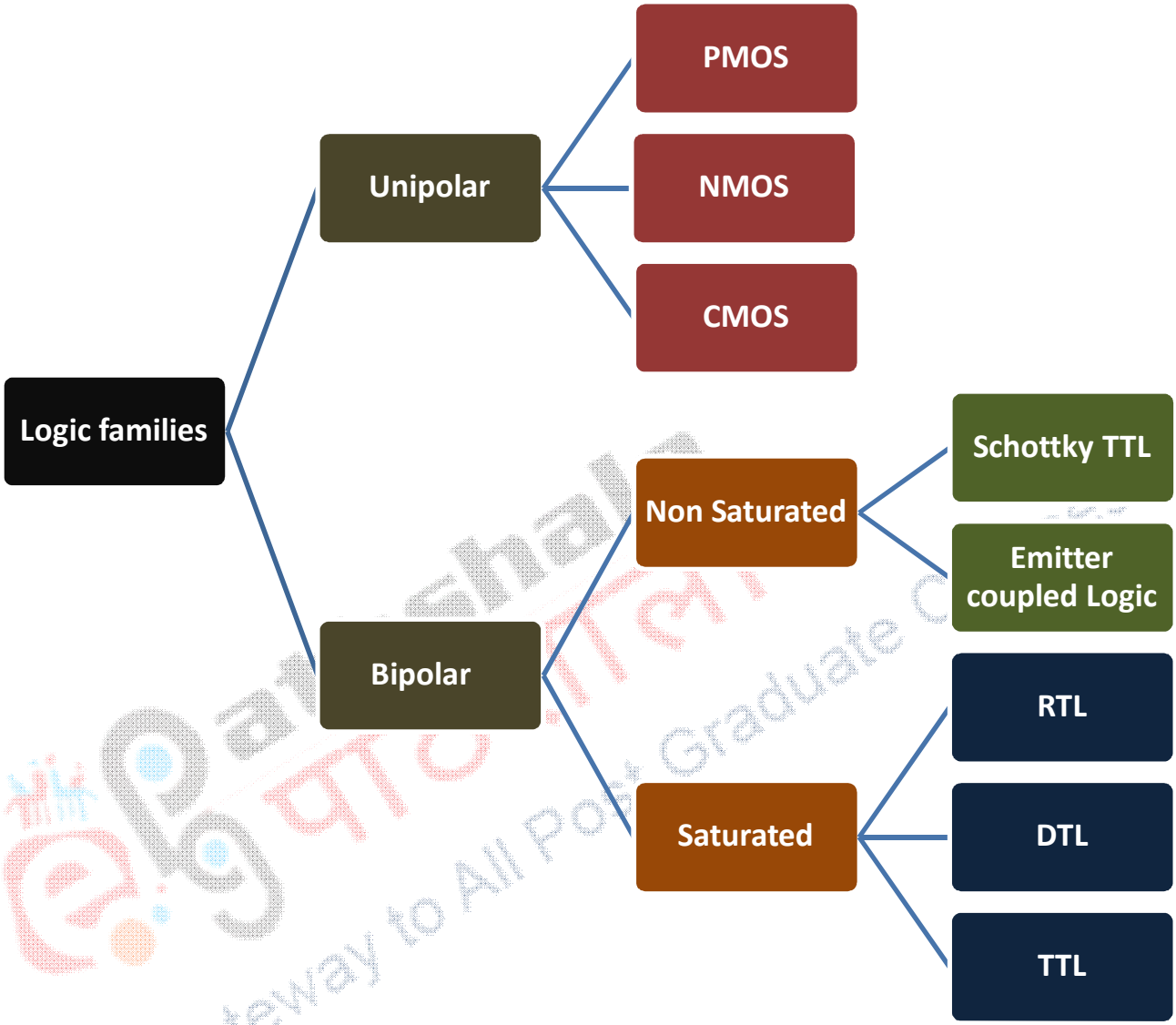

Figure 1 Classification of logic families

Out of the logic families mentioned above, DL, RTL and DTL are not very useful due to some inherent disadvantages while TTL, ECL and CMOS are widely used in many digital circuit design applications.

Each logic family is further classified based on the significant variation in the key parameters. This helps in improving the performance of that logic family. For example, TTL logic family has subfamilies such as low power TTL, Schottky TTL etc.

TTL has an extensive list of digital functions and is currently the most popular logic family. ECL is used in systems requiring high-speed operations. MOS is used in circuits requiring a high component density, whereas CMOS is used in systems requiring low power consumption.

These three families, TTL, ECL and CMOS have LSI devices and also a large number of MSI and SSI devices. SSI devices are those that come with a small number of gates or flip flops in one IC package. The limit on the number of circuits in SSI devices is number of pins in a package. A 14 pin package can accommodate only four two input gates because, each gate requires three external pins-two each for inputs and one each for output, for a total of 12 pins. The remaining two pins are needed for supplying power to the circuits.

TTL ICs are usually distinguished by numerical designations such as the 5400 and 7400 series. The former has wide operating temperature range and is suitable for military use and the latter has a narrower temperature range and is suitable for industrial use only. TTL SSI ICs such as 7404, 7400 etc are available in the market..

The most common ECL types are designated as the 10000 series. The 10102 provides four two input NOR gates. Note that the ECL gate may have two outputs, one for the NOR function and the other for the OR function. ECL gates have three terminals for power supply. VCC1 and VCC2 are usually connected to ground and VEE to a -5.2 Volt supply.

CMOS circuits are designated by the 4000 series. Only two NOR gates can be accommodated in the 4002 because of limited number of pins. The 4050 type provides six buffer gates. Both ICs have two unused terminals marked NC. The terminal marked Vdd requires a power supply voltage from 3 to 15 Volt while Vss is usually connected to ground.

1.4 Positive and Negative logic

A logic level is one of the several states a digital circuit can have. It is expressed in DC voltage with reference to ground. Usually, this term refers to binary logic level consisting of two states viz. low state or 0V or logic 0 and high state or +V or logic high. In addition to two state digital circuits, some circuits are three state or tri- state logic circuits. Third state or high impedance state is included in addition to two logic states i.e. logic 0 and logic 1. If the circuit is in this state, it is effectively cancelling the output.

Every logic gate accepts inputs and produces output in terms of logic and voltage levels. It is possible to interpret logic and voltage levels in terms of two types of logic configurations: positive logic and negative logic. Table-1 shows the two assignments that define positive and negative logic systems.

Table-1: Positive and Negative logic assignments

Positive logic	Negative logic
H = 1	H = 0
L = 0	L = 1

The binary signal at the input or output of the any gate has one of two values except during transition. One signal value represents logic 1 and other as logic 0. Since two signal values are assigned to two logic values, there exist two different assignments of signal to logic. Due to the principle of duality of Boolean algebra, an interchange of signal values assignment results in a dual function implementation.

Consider the two values of a binary signal as shown in Figure 2. One value must be higher than the other since the two values must be different in order to be distinct The higher level is designated as H and the lower level as L.

(a) Positive Logic (b) Negative Logic

Figure 2 :Logic level assignments

There are two choices of logic value assignment.

1. Choosing the high level H to represent logic 1defines positive logic(figure 2 (a))
2. Choosing the low level L to represent logic 1 defines negative logic(figure 2(b))

It is not the signal polarity that determines the type of logic; but rather the assignment of logic values according to the relative amplitudes of the signal. Integrated circuit data sheets define digital function in terms of H and L and not in terms of logic 0 or logic 1. It is up to the user to determine the positive and negative assignments. In each family, there is a range of voltage values that the circuit will recognize as a high or low level. Consider Table-2, to understand the logical interpretation of any gate. It is depends on the convention of positive or negative logic.

Table-2: Logical interpretation of logic gate behaviour

Logical implementation		**Physical implementation**		**Physical implementation**	
Gate Behaviour		**Positive logic**		**Negative logic**	
A B	Y	A B	AND	A B	OR
L L	L	0 0	0	1 1	1
L H	L	0 1	0	1 0	1
H L	L	1 0	0	0 1	1
H H	L	1 1	1	0 0	0

This table demonstrates how physical implementation of logic gate, changes with positive and negative logic implementations. A physical implementation of gate has two different representation depending on whether positive or negative logic is used. Positive logic inputs and outputs are also known as **Active High** signals. Negative logic inputs and outputs are also known as **Active Low** signals. Input and output polarity may be indicated by bubble or no bubble. Figure 3 indicates two different implementations namely positive logic AND gate and a negative logic OR gate for the same logic level implementation.

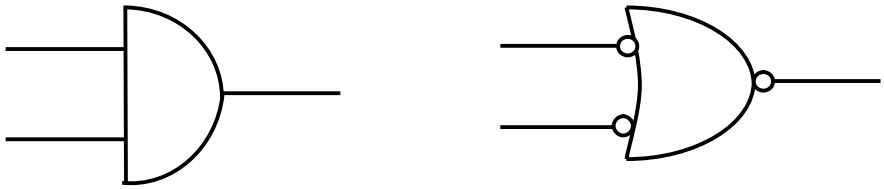

Figure 3: Positive logic and negative logic implementations of table 2

1.5 Characteristics of logic families

In this section, we discuss the different parameters which are used to characterize different logic families.

1. **HIGH-level input current, I_{IH}**. This is the current flowing into (taken as positive) or out of (taken as negative) an input, when a HIGH-level input voltage equal to the minimum HIGH-level output voltage specified for the family is applied. In the case of bipolar logic families such as TTL, the circuit design is such that this current flows into the input pin and is therefore specified as positive. In the case of CMOS logic families, it could be either positive or negative, and only an absolute value is specified in this case.
2. **LOW-level input current, I_{IL}**. The LOW-level input current is the maximum current flowing into (taken as positive) or out of (taken as negative) the input of a logic function, when the voltage applied at the input equals the maximum LOW-level output voltage specified for the family. In the case of bipolar logic families such as TTL, the circuit design is such that this current flows out of the input pin and is therefore specified as negative. In the case of CMOS logic families, it could be either positive or negative. In this case, only an absolute value is specified.
3. **HIGH-level output current, I_{OH}**. This is the maximum current flowing out of an output when the input conditions are such that the output is in the logic HIGH state. It is normally shown as a negative number. It informs us about the current sourcing capability of the output. The magnitude of I_{OH} determines the number of inputs the logic function can drive when its output is in the logic HIGH state. For example, for the standard TTL

family, the minimum guaranteed I_{OH} is ī 400 µA, which can drive 10 standard TTL inputs with each requiring 40 µA in the HIGH state.

4. **LOW-level output current, I_{OL}**. This is the maximum current flowing into the output pin of a logic function when the input conditions are such that the output is in the logic LOW state. It informs us about the current sinking capability of the output. The magnitude of I_{OL} determines the number of inputs the logic function can drive when its output is in the logic LOW state. For example, for the standard TTL family, the minimum guaranteed IOL is 16 mA, which can drive 10 standard TTL inputs with each requiring 1.6mA in the LOW state.
5. **HIGH-level input voltage, V_{IH}**. This is the minimum voltage level that needs to be applied at the input to be recognized as a legal HIGH level for the specified family. For the standard TTL family, a 2 V input voltage is a legal HIGH logic state.
6. **LOW-level input voltage, V_{IL}**. This is the maximum voltage level applied at the input that is recognized as a legal LOW level for the specified family. For the standard TTL family, an input voltage of 0.8 V is a legal LOW logic state.
7. **HIGH-level output voltage, V_{OH}**. This is the minimum voltage on the output pin of a logic function when the input conditions establish logic HIGH at the output for the specified family. In the case of the standard TTL family of devices, the HIGH level output voltage can be as low as 2.4V and still be treated as a legal HIGH logic state. It may be mentioned here that, for a given logic family, the VOH specification is always greater than the VIH specification to ensure output-to-input compatibility when the output of one device feeds the input of another.
8. **LOW-level output voltage, V_{OL}**. This is the maximum voltage on the output pin of a logic function when the input conditions establish logic LOW at the output for the specified family. In the case of the standard TTL family of devices, the LOW-level output voltage can be as high as 0.4V and still be treated as a legal LOW logic state. It may be mentioned here that, for a given logic family, the VOL specification is always smaller than the VIL specification to ensure output-to-input compatibility when the output of one device feeds the input of another.

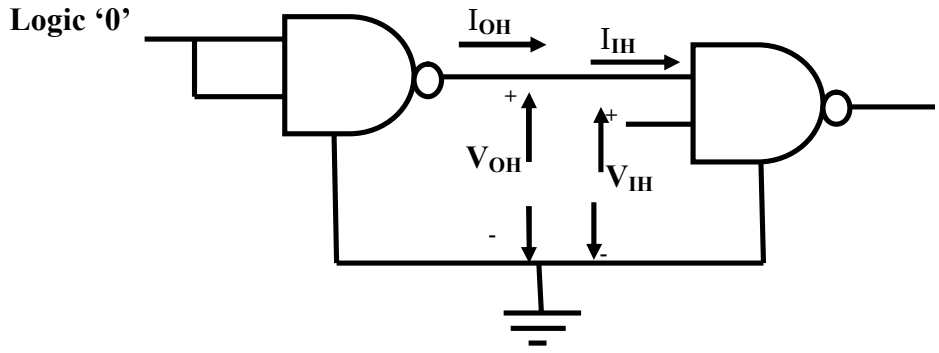

Figure 4 High level Input and output current and voltage requirements

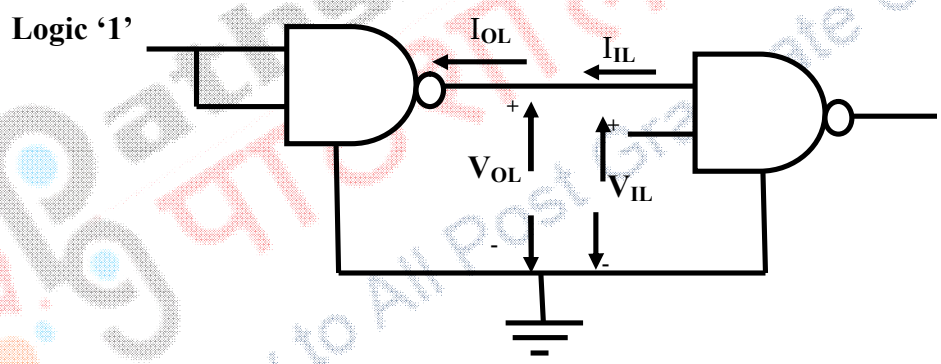

Figure 5 Low level Input and output current and voltage requirements

9. **Supply current, I_{CC}.** The supply current when the output is HIGH, LOW and in the high-impedance state is respectively designated as I_{CCH}, I_{CCL} and I_{CCZ}.
10. **Fan out**: It specifies the number of standard loads that the output of the gate can drive without affecting its normal operation. A standard load is usually defined as the amount of current needed by an input of another gate in the same family as shown in Figure 6. Sometimes, the termô loadingô is also used instead of ófan outô. This term is derived from the fact that the output of the gate can supply a limited amount of current above which it ceases to operate properly and is said to be overloaded. The output of the gate is usually connected to the inputs of similar gates.

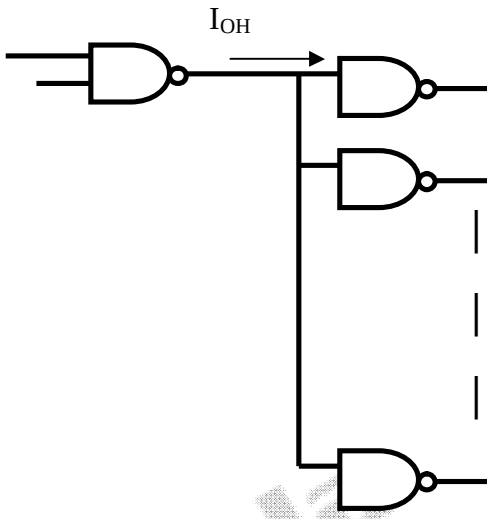

Figure 6 Fan out of logic gate is decided by number of loads connected to output of gate of same logic family

Each input consumes a certain amount of power from gate input so that, each additional connection adds to load the gate. These loading rules are listed for family of standard digital circuits. The rules specify the maximum amount of loading allowed for each output in the circuit.

Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded from it. Thus fan out is the maximum number of inputs that can be connected to the output of the gate and is expressed by a number.

The fanout capabilities of a gate must be considered while simplifying Boolean functions. One should use non inverting amplifiers or buffers to provide additional driving capabilities for heavy loads.

11. **Fan in:** This is the number of inputs of a logic gate. It is decided by the input current sinking capability of a logic gate as shown in Figure 7.

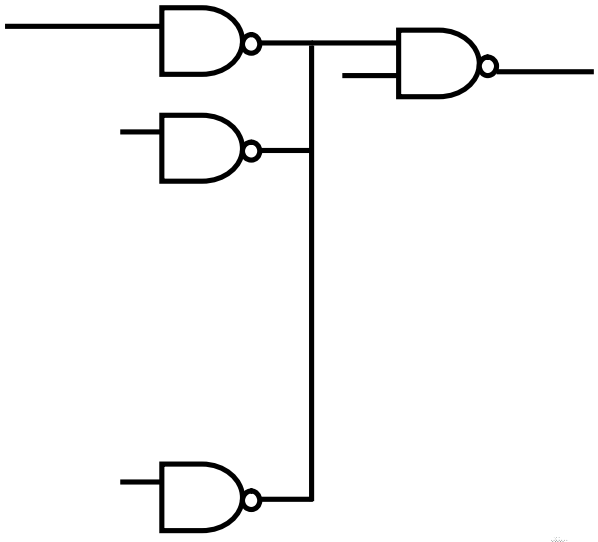

Figure 7 Fan in of logic gate

12. **Power Dissipation**: This is the power supplied required to operate the gate. It is expressed in milli-watt (mW) and represents actual power dissipated in the gate. It is the number that represents power delivered to gate from the power supply. The total power dissipated in the digital system is sum of power dissipated in each digital IC.
13. **Rise time, t_r:** This is the time that elapses between 10% and 90 % of the final signal level when the signal makes a transition from logic LOW to logic HIGH.
14. **Fall time, t_f:** This is the time that elapses between 90 and 10 % of the signal level when the signal makes a transition from logic LOW to logic HIGH
15. **Propagation delay *t*p:** The propagation delay is the time delay between the occurrence of change in the logical level at the input and before it is reflected at the output. It is the time delay between the specified voltage points on the input and output waveforms. Propagation delays are separately defined for LOW-to-HIGH and HIGH-to-LOW transitions at the output. In addition, we also define enable and disable time delays that occur during transition between the high-impedance state and defined logic LOW or HIGH states.

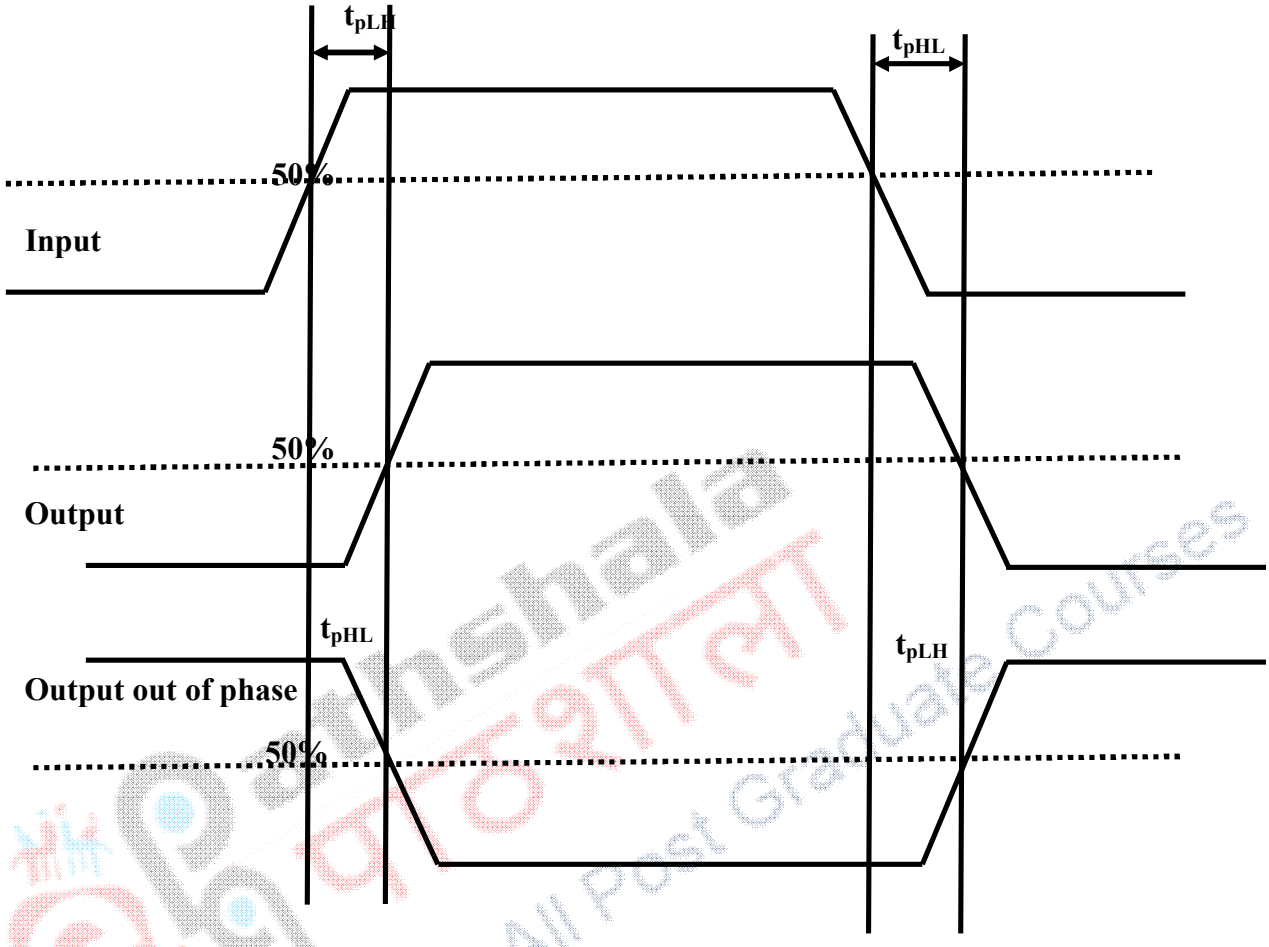

Figure 8 Propagation delay parameters

a. **Propagation delay t_{pLH}:** This is the time delay between the specified voltage points on the input and output waveforms with the output changing from LOW to HIGH.

b. **Propagation delay t_{pHL}:** This is the time delay between the specified voltage points on the input and output waveforms with the output changing from HIGH to LOW.

It is the average transition delay time for a signal to propagate from input to output when the binary signals change in value. The signal through gate takes a certain amount of time to propagate from the inputs to the output. The interval of time is defined as the propagation delay of the gate. Propagation delay is expressed in nanoseconds(ns)(1ns = 10^{-9} s). The signals travelling from input to output of the system pass through a number of gates. The propagation delay of the system is the sum of the propagation delays of all these gates. When

the speed of operation is important, each gate must have a small propagation delay and the digital circuit must have minimum number of gates between input and output.

16. **Disable time from the HIGH state, t_{pHZ}:** Defined for a tristate device, this is the time delay between the specified voltage points on the input and output waveforms with the tristate output changing from the logic HIGH level to the high-impedance state.
17. **Disable time from the LOW state, t_{pLZ}:** Defined for a tristate device, this is the time delay between the specified voltage points on the input and output waveforms with the tristate output changing from the logic LOW level to the high-impedance state.
18. **Enable time from the HIGH state, t_{pZH}:** Defined for a tristate device, this is the time delay between the specified voltage points on the input and output waveforms with the tristate output changing from the high-impedance state to the logic HIGH level.
19. **Power dissipation.** The power dissipation parameter for a logic family is specified in terms of power consumption per gate and is the product of supply voltage V_{CC} and supply current I_{CC}. The supply current is taken as the average of the HIGH-level supply current I_{CCH} and the LOW-level supply current I_{CCL}.
20. **Speed–power product.** The speed of a logic circuit can be increased, that is, the propagation delay can be reduced, at the expense of power dissipation. We may recall that, when a bipolar transistor switches between cut-off and saturation, it dissipates the least power, but has a large associated switching time delay. On the other hand, when the transistor is operated in the active region, power dissipation goes up, while the switching time decreases drastically. It is always desirable to have low values for both propagation delay, and power dissipation parameters. A useful figure-of-merit used to evaluate different logic families is the speedï power product, expressed in picojoules, which is the product of the propagation delay (measured in nanoseconds) and the power dissipation per gate (measured in milliwatts).
21. **Noise margin**: This is the maximum noise voltage added to the input signal of digital circuit that does not cause an undesirable change in the circuit output. There are two types of noise to be considered here
    a. DC noise :This is caused by a drift in the voltage levels of a signal

b. AC noise: This is caused by random pulse that may be created by other switching signals.

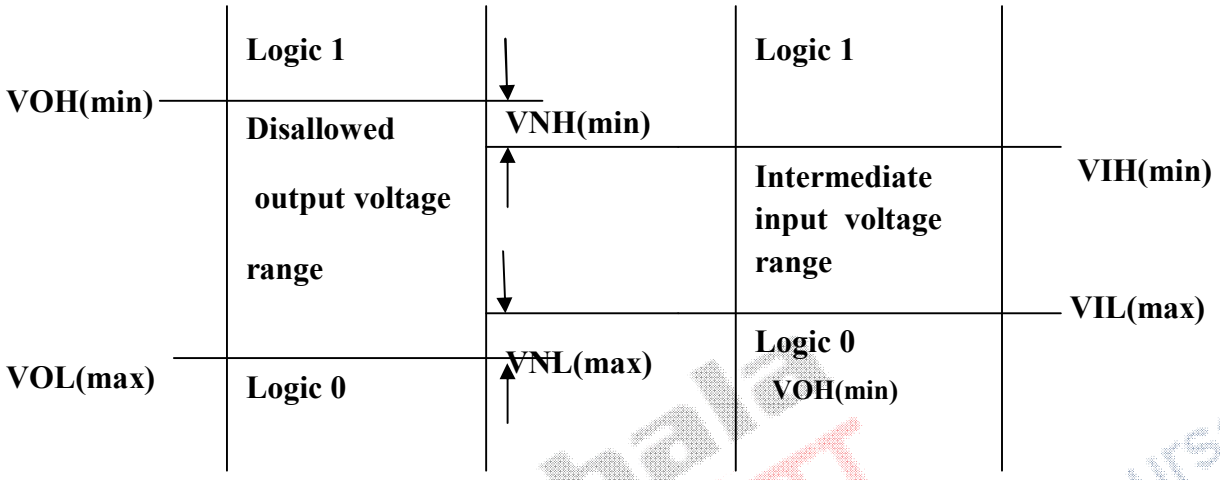

Figure 9 Noise Margin

This is a quantitative measure of noise immunity offered by the logic family. When the output of a logic device feeds the input of another device of the same family, a legal HIGH logic state at the output of the feeding device should be treated as a legal HIGH logic state by the input of the device being fed. Similarly, a legal LOW logic state of the feeding device should be treated as a legal LOW logic state by the device being fed. The legal HIGH and LOW voltage levels for a given logic family are different for outputs and inputs. Figure 9 shows the generalized case of legal HIGH and LOW voltage levels for output. As we can see from the two diagrams, there is a disallowed range of output voltage levels from VOL(max.) to VOH(min.) and an indeterminate range of input voltage levels from VIL(max.) to VIH(min.). Since VIL(max.) is greater than VOL(max.), the LOW output state can e tolerate a positive voltage spike equal to (VIL(max.) ī VOL(max)); and still be a legal LOW input. Similarly, VOH(min.) is greater than VIH (min.), and the HIGH output state can tolerate a negative voltage spike equal to (VOH(min.) ï VIH (min.)) and still be a legal HIGH input. Here, (VIL(max.) ī VOL(max.)) and (VOH(min.) ī VIH (min.)) are respectively known as the LOW-level and HIGH-level noise margin.

1.6 Evolution of logic families

As mentioned earlier, logic families are fabricated using basic components such as resistors, diode, transistors and MOSFETs. Let us consider the basic logic circuits used in earlier logic families consisting of only diodes and transistors. Let us start with Diode Logic family as shown in Figure 10.

A. Diode Logic Circuit

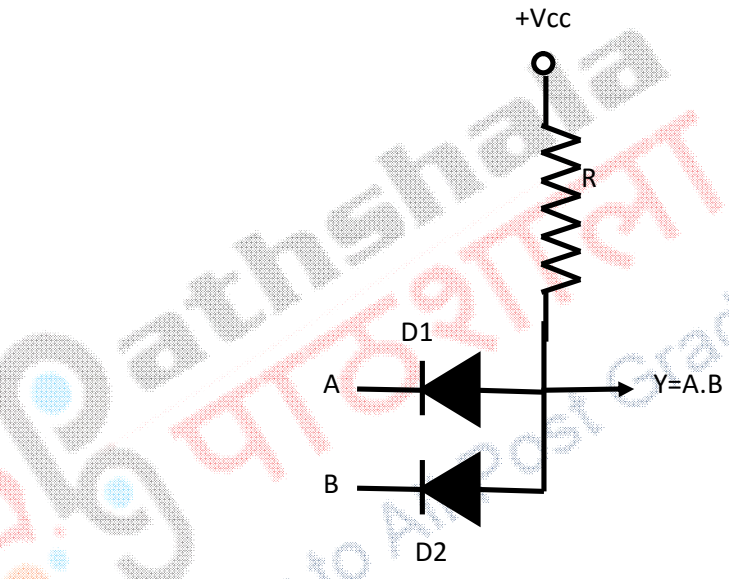

Figure 10 Diode Logic

In this logic circuit, diodes D1, D2 and Resistor R are fabricated into a single IC. A and B are inputs and Y is the output of the circuit. If A=0 and B=0, both diodes D1 and D2 are forward biased and output Y= 0V i.e. logic 0. When A=0 and B=1 or A=1 and B=0, either of D1 or D2 is forward biased making the output Y=0. However, if A=B=1, both the diodes D1 and D2 are reverse biased and Y=1. Hence, this circuit represents logical AND operation i.e. Y=A.B.

Truth Table

A	B	Y=A. B
0	0	0
0	1	0
1	0	0
1	1	1

B. Resistor Transistor Logic(RTL)

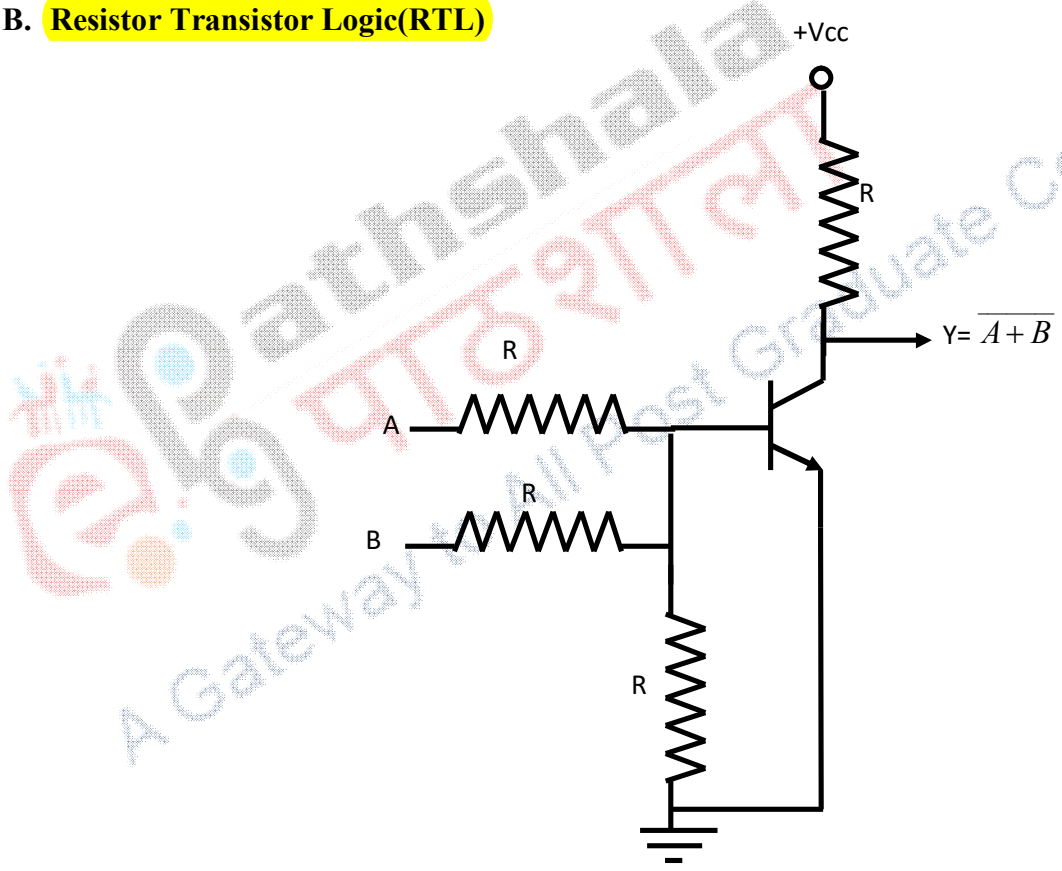

Figure 11 Resistor Transistor Logic

In this circuit, the transistor is OFF if any one of inputs A or B is logic 0. This is because the base emitter junction would be reverse biased. Hence, the output Y=1. When both A=B=1, transistor would be ON and output Y=0. Hence, this circuit acts as NOR gate. Truth table of the circuit is as shown below

Truth Table:

A	B	Y=A. B
0	0	1
0	1	1
1	0	1
1	1	0

C. Diode transistor Logic

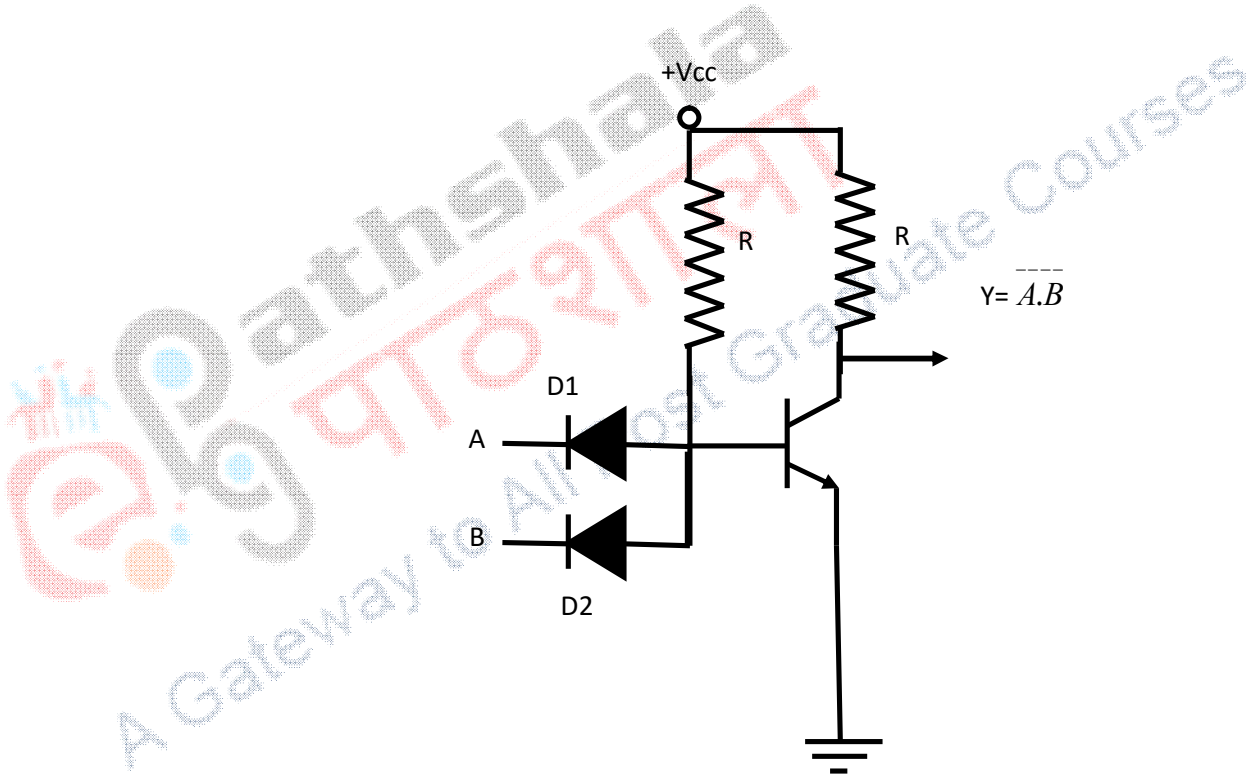

Figure 12 Diode Transistor Logic

In this circuit, diodes and transistors are fabricated into a single IC. When both inputs A and B is logic 0, diodes D1 and D2 are forward biased and the transistor is OFF. This is because, the emitter base junction of transistor is reverse biased and output Y is at logic 1. Hence, if one of the input is a logic 0 output Y is at logic level 1. On the other hand, if both A and B

are high, diodes are reverse biased and the transistor is ON and output Y is at logic 0. Therefore, this circuit behaves like simple NAND gate. The truth table is shown below

Truth Table:

A	B	Y=A. B
0	0	1
0	1	1
1	0	1
1	1	0

1.7 Summary:

In this module, the importance of using logic circuits in the form of digital ICs is discussed. One has to consider the logic circuits as the number of basic components fabricated into a single IC. Depending upon the components used for fabrication, the digital ICs are classified into different families as TTL, CMOS and ECL. One has to use the same logic family for designing the logic circuit in order to avoid complexity in the circuit design and address the issue of compatability. Different characteristics of the logic families such as noise margin, propagation delay are defined and discussed in detail. Importance of these parameters in the design of digital circuits are analyzed and is referred to as figure of merit. This decides the performance of the logic IC family. Lastly, evolution of the logic families was explained considering basic logic circuits such as RTL, DTL etc.