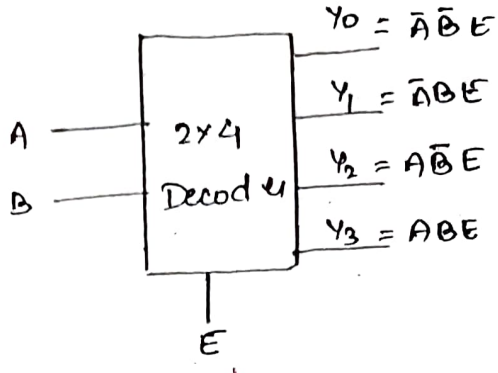
Decoder:

*) Decoder is many to many ckts which is used to decode binary to other codes such as

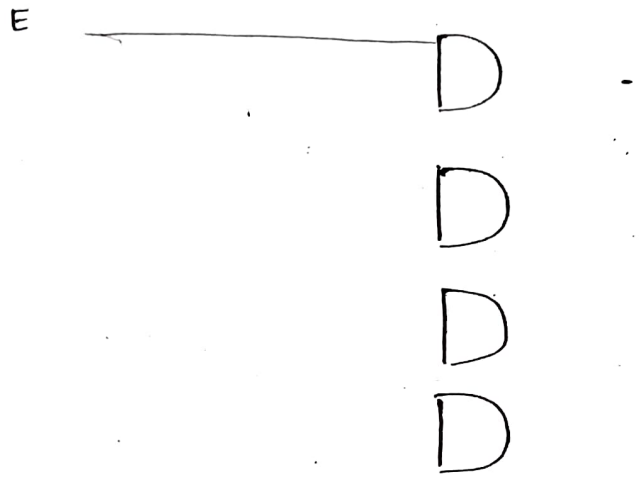
- binary to octal (3 x 8)
- BCD to decimal (4x10)
- binary to hex (4 x 16)



E	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

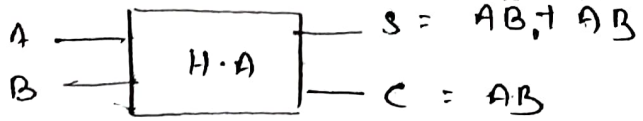
* enable may be present.

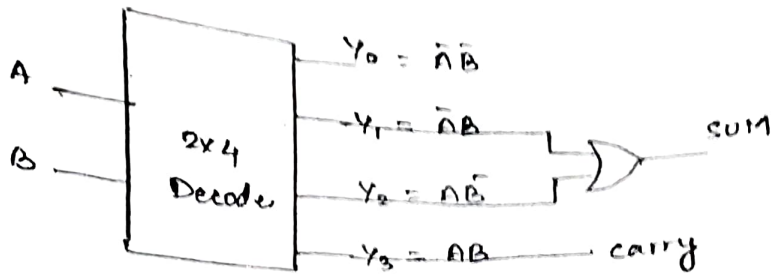
** Decoder & De-mux → selection line present
internal circuits remain same.



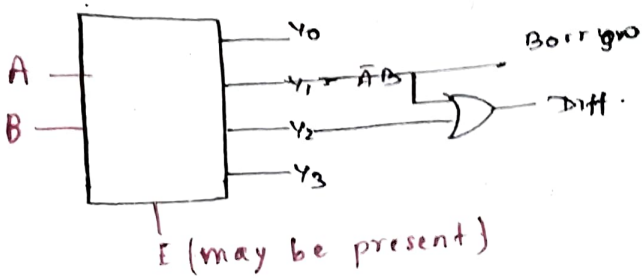
Note · 2×4 Decoder ⟶ 1×4 Demux
3×8 Decoder ⟶ 1×8 Demux
4×16 Decoder ⟶ 1×16 Demux
8×256 " ⟶ 1×256 "

Q Implement H.A using decoder ckt



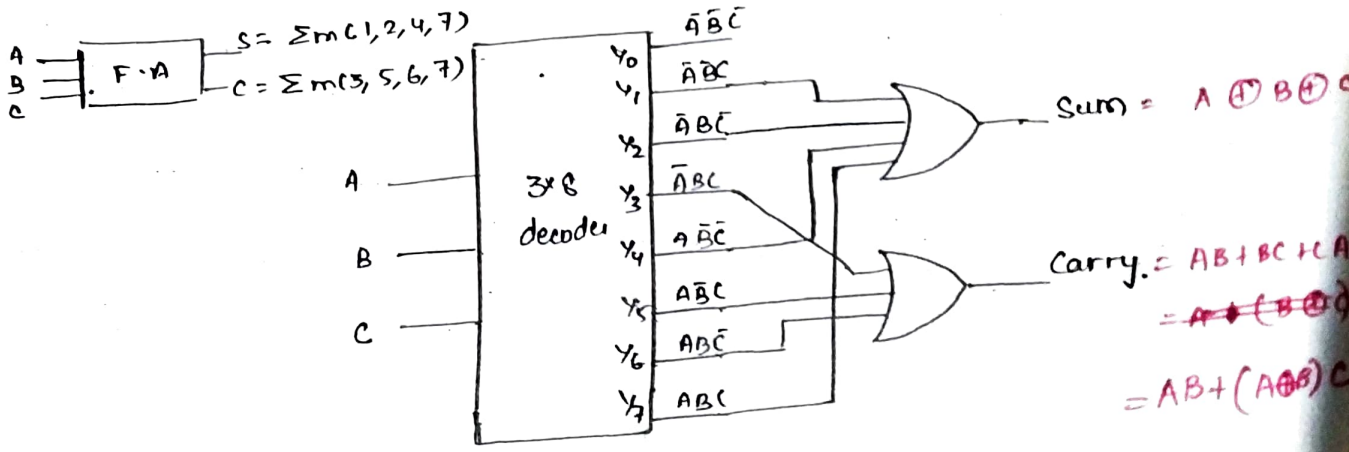


For H.S



So H.S & H.A can be implemented using one 2x4 decoder & 1 OR gate.

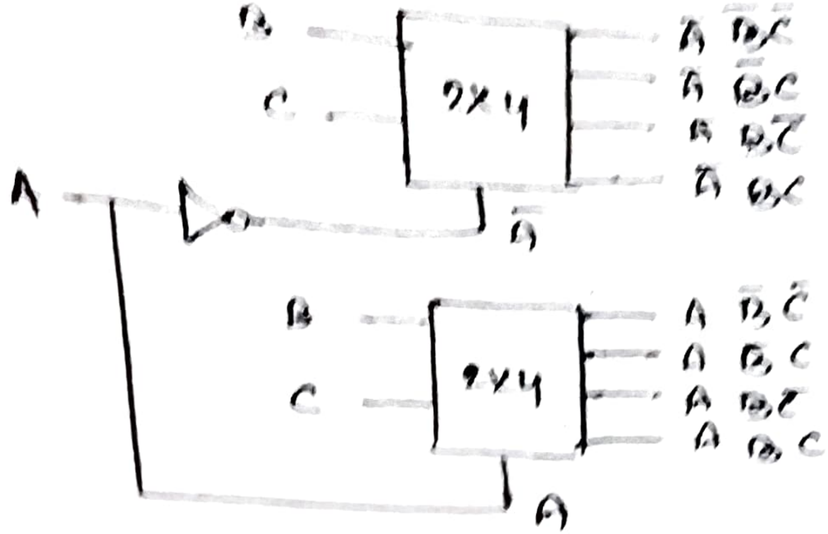
Full adder using 3x8 decoder



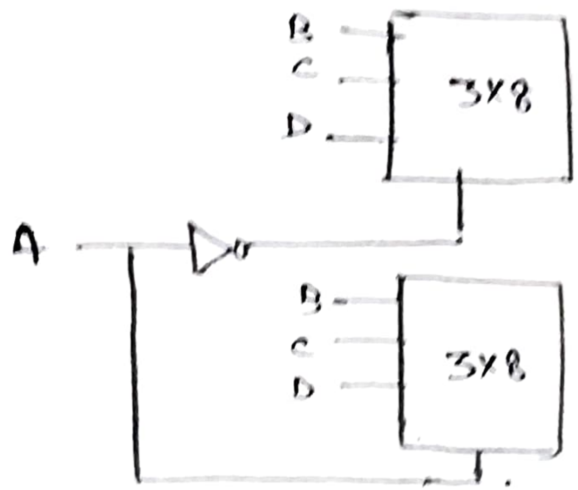
2 OR gate & 1 3:8 decoder

Imp!

3×8 ——— 2×4 (general model)



4×16 ——— 3×8

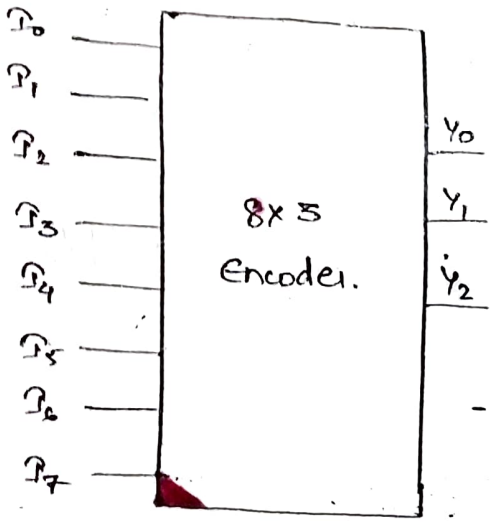


Moris Mano

ENCODER

- Encoder is a combinational ckt which has many many i/p & many o/p's
- It is used to convert other codes to binary such as
  - octal to binary. (8x3)
  - Decimal to BCD (10x4)
  - Hex to binary (16x4)

8x3 Encoder

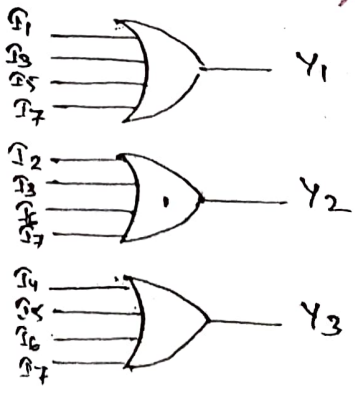


I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

In Encoder one of the i/p line is high & corresponding binary is available at the o/p.

Imp:

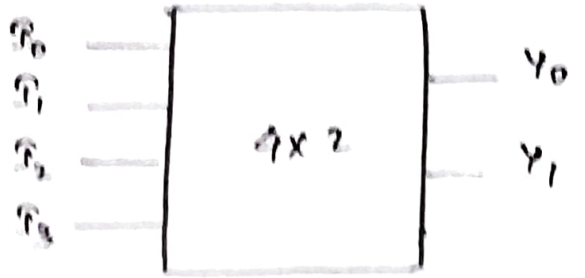
$$Y_0 = I_1 + I_3 + I_5 + I_7$$
$$Y_1 = I_2 + I_3 + I_6 + I_7$$
$$Y_2 = I_4 + I_5 + I_6 + I_7$$



Priority Encoder

In Priority encoder, binary o/p is available for the i/p corresponding to the highest priority i/p line & if multiple i/p are logic one.

4x2 priority Encoder



I_3	I_2	I_1	I_0	Y_1	Y_0
0	0	0	1	0	0
0	0	1	x	0	(1)
0	0	x	x	(1)	0
0	(1)	x	x	(1)	(1)
(1)	x	x	x	(1)	(1)

$$Y_1 = I_3 + \bar{I}_3 I_2$$

$$\boxed{Y_1 = I_3 + I_2}$$

By distribution theorem

$$Y_0 = I_3 + \bar{I}_3 \bar{I}_2 I_1$$

$$\boxed{Y_0 = I_3 + \bar{I}_2 I_1}$$