Logic gates

NOT, AND, OR } Basic gate

NAND, NOR } Universal gates

EXOR, EXNOR } exclusive gate

→ exclusive gates are used in arithmatic circuits such as comparators, code converters, parity generators.

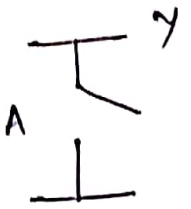
NOT gate or Inverter

Symbol

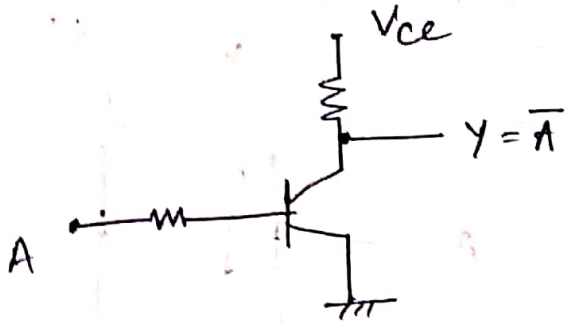
Truth table

A	Y
0	1
1	0

switch circuit



Transistor circuit

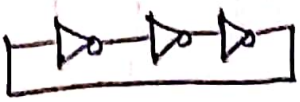


→ A — A = Buffer

A — Ā — A = Buffer

→ Even no. of NOT gate connected gives Buffer

→ odd no. of NOT gate in following manner gives astable multivibrator



AND gate

Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Switch circuit

Commulative law:

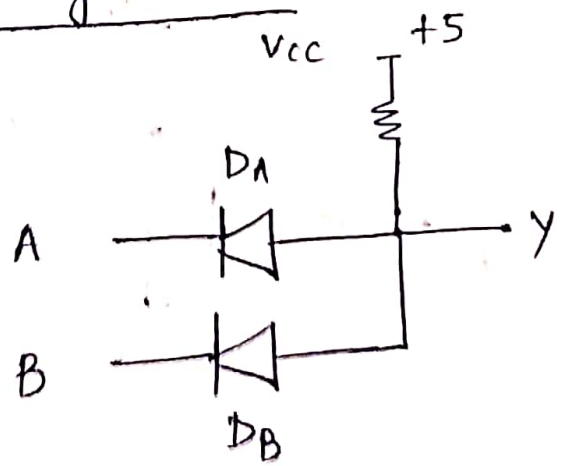
$A \cdot B = B \cdot A$ satisfied.

Associative law:

$ABC = (AB)C = (AC)B = (BC)A$

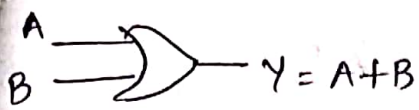
satisfied

AND gate using diodes:



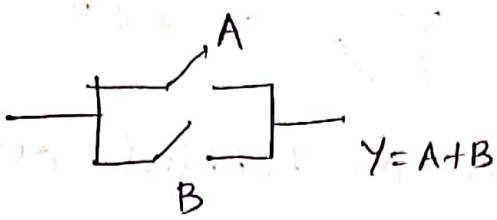
A	B	D_A	D_B	Y
0	0	on	on	0
0	1	on	off	0
1	0	off	on	0
1	1	off	off	1

OR gate



Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

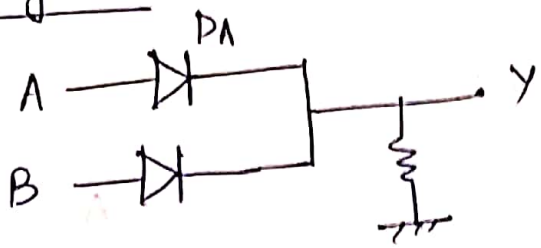


switch circuit

Commulative law: $A+B = B+A$ Satisfied

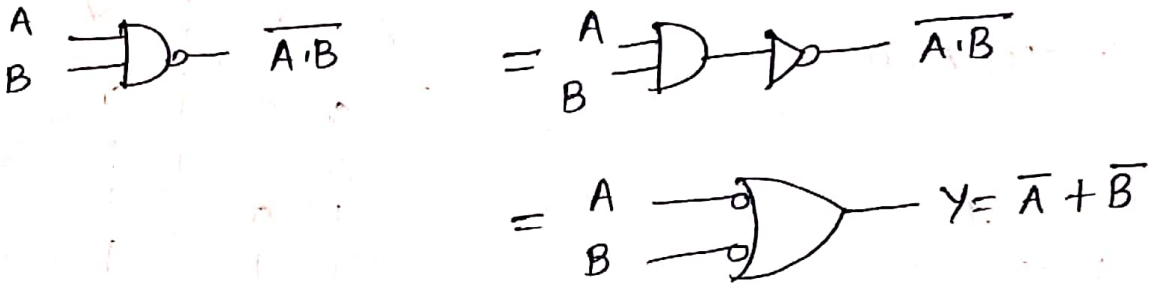
Associative law: $A+B+C = (A+B)+C = A+(B+C) \neq (A+C)+B$ Satisfied

Diode circuit of OR gate:



A	B	D_A	D_B	Y
0	0	open	open	0
0	1	open	SC	1
1	0	SC	open	1
1	1	SC	SC	1

NAND gate

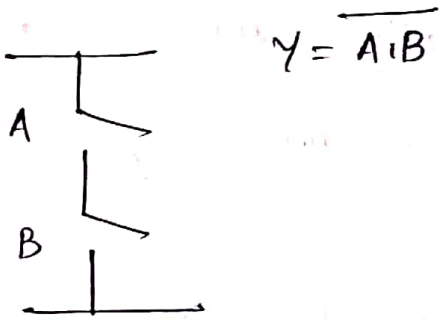


→ NAND gate is also called as bubbled. OR gate.

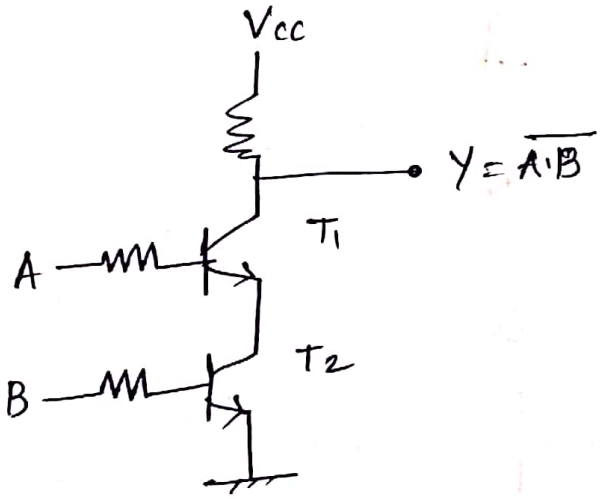
Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

switch ckt



Transistor diagram:

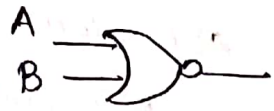


A	B	T_1	T_2	Y
0	0	open	open	1
0	1	open	sc	1
1	0	sc	open	1
1	1	sc	sc	0

Commulative law: $\overline{A \cdot B} = \overline{B \cdot A}$ satisfied

Associative law: $\overline{(A \cdot B)}\, C \neq \overline{ABC}$ not satisfied.

NOR gate



$Y = \overline{A+B}$

$= \overline{A} \cdot \overline{B}$

$\cong$

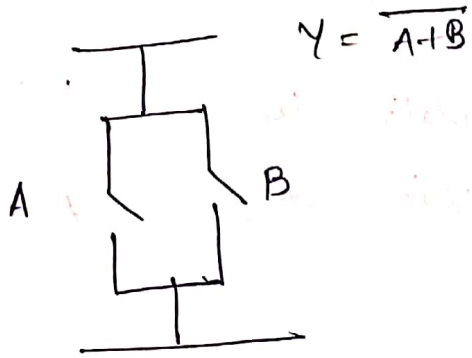
$=$

→ NOR gate is also called bubbled AND.

Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

switch ckt

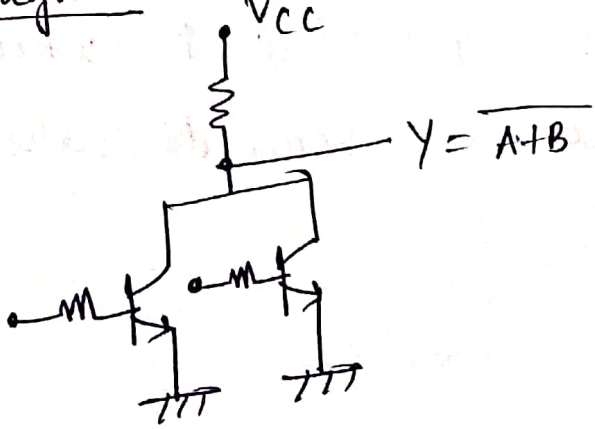


Commulative law: $\overline{A+B} = \overline{B+A}$ satisfied

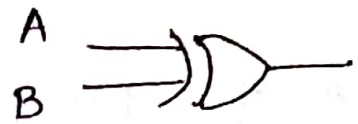
Associative law: $\overline{A+B+C} \neq \overline{(A+B)+C}$ not satisfied.

$\neq \overline{(A+C)+B}$

Transistor diagram:



EX-OR gate:



$Y = A \oplus B$

$= A\bar{B} + \bar{A}B$ ..... SOP form

$= (A+B)(\bar{A}+\bar{B})$ ... POS form

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Note:

if $A=B$, $o/p = 0$

if $A \neq B$, $o/p = 1$

Commulative law: $A \oplus B = B \oplus A$ satisfied

Associative law: $A \oplus B \oplus C = (A \oplus B) \oplus C$ satisfied.

$= A \oplus (B \oplus C)$

Imp *

$A \oplus A = 0$

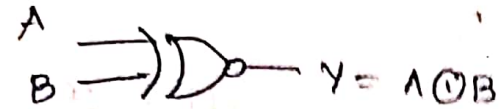
$A \oplus \bar{A} = 1$

$A \oplus 0 = A$

$A \oplus 1 = \bar{A}$

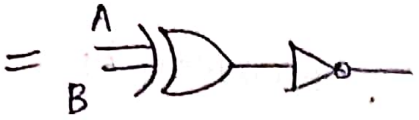
Note: In EXOR gate, o/p is logic 1 when no. of 1's at the i/p is odd no., hence its called 'odd no. detector circuit'

EX-NOR gate



$= \bar{A}B + A\bar{B}$ ... POS

$= (A+\bar{B})(\bar{A}+B)$ ... SOP



Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Note:

if $A = B$, $o/p = 1$

if $A \neq B$, $o/p = 0$

$A \odot B = \overline{A \oplus B}$

$A \odot B \odot C = \overline{A \oplus B \oplus C}$

ommulative law: $A \odot B = B \odot A$ Satisfied

sociative law:

$A \odot B \odot C \neq (A \odot B) \odot C$

$A \odot B \odot C \odot D = ((A \odot B) \odot C) \odot D$

associative law satisfied for even no. of i/p,
not satisfied for odd no. of i/p.

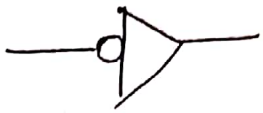
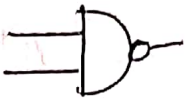
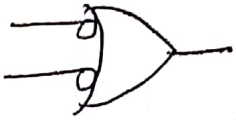
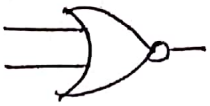
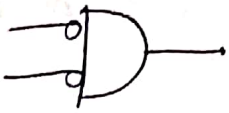
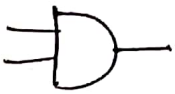
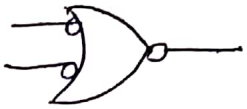
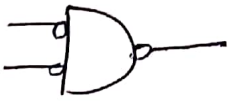
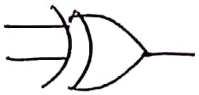
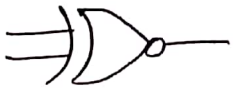
$A \odot A = 1$

$A \odot \bar{A} = 0$

$A \odot 0 = \bar{A}$

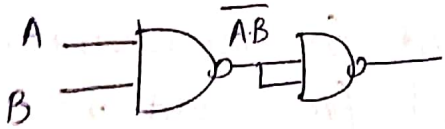
$A \odot 1 = A$

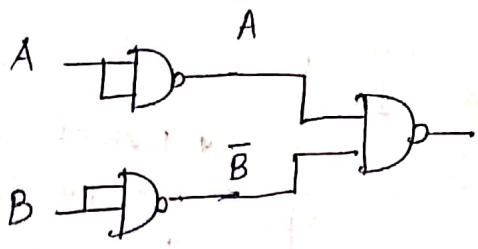
* EXNOR gate is also called even ~~odd~~ no. of 1's detector circuit since o/p is 1 for even no. of i/p combination are 1.

Logic gate	Alternate Symbol	
		
		Bubbled OR
		Bubbled AND
		
		
		
		.... verify each

NAND as universal gate

NOT:  $\overline{A \cdot A} = \overline{A}$

AND: 

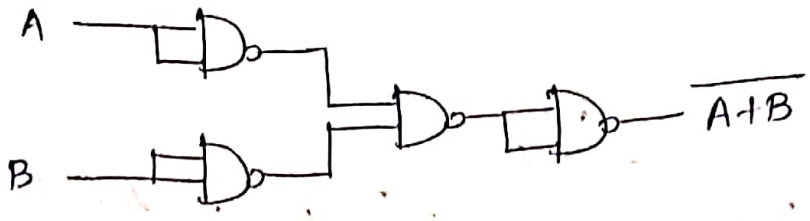
OR:  = 

$\overline{\overline{A} \cdot \overline{B}}$

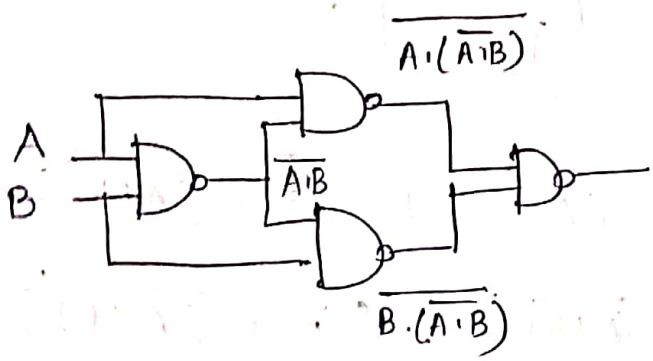
$= \overline{\overline{A}} + \overline{\overline{B}}$

$= A + B$

NOR:



EXOR:



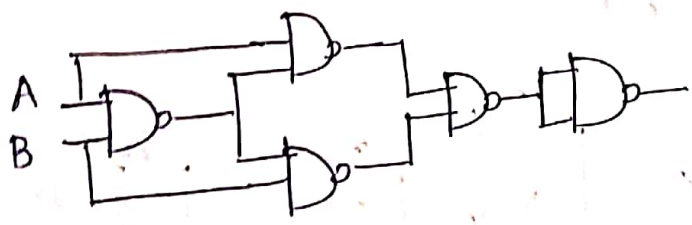
$$Y = \overline{\overline{(A\cdot(\overline{AB}))}\cdot\overline{(B\cdot(\overline{AB}))}}$$

$$= A(\overline{A\cdot B}) + B(\overline{A\cdot B})$$

$$= A(\overline{A}+\overline{B}) + B(\overline{A}+\overline{B})$$

$$= A\overline{B} + \overline{A}B$$

EXNOR:



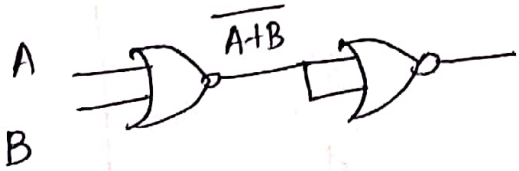
$$Y = AB + \overline{A}\,\overline{B}$$

NOR as universal gate

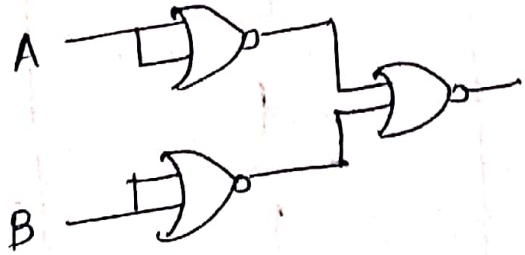
NOT:

$\overline{A+A} = \overline{A}$

OR:

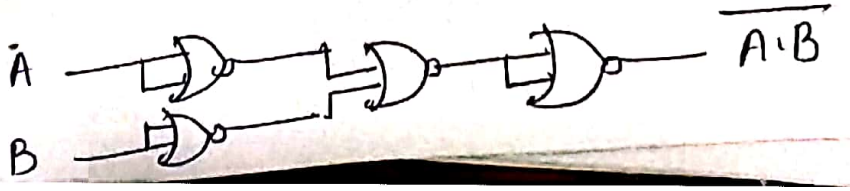


AND:

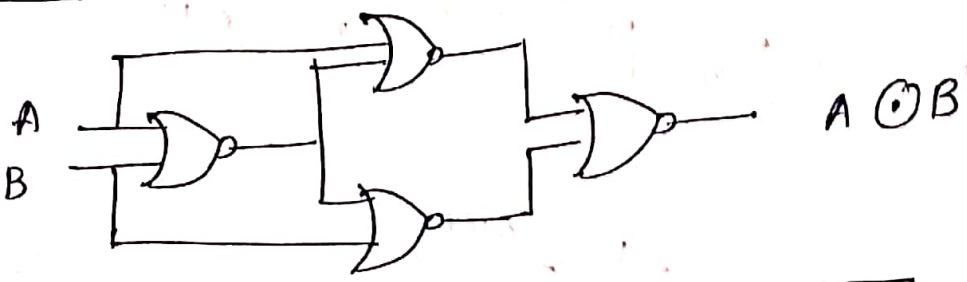


$\overline{\overline{A}+\overline{B}} = A\cdot B$

NAND:



EXNOR:



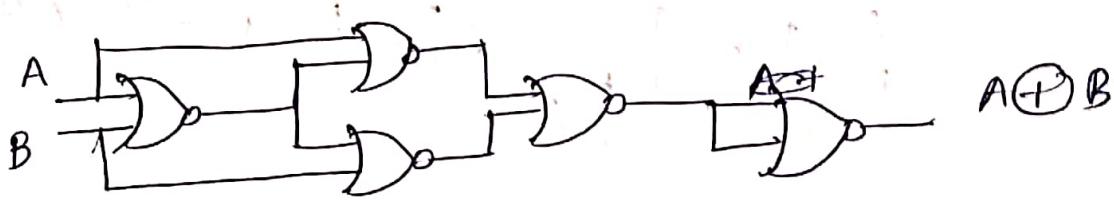
$$\overline{\left(\bar{A} + \overline{(A+B)}\right) + \left(\bar{B} + \overline{(A+B)}\right)}$$

$$= \left(\bar{A} + \overline{(A+B)}\right) \cdot \left(\bar{B} + \overline{(A+B)}\right)$$

$$= \left(\bar{A} + \bar{B}\,\bar{A}\cdot\bar{B}\right)\left(\bar{B} + \bar{A}\,\bar{B}\right)$$

$$= AB + \bar{A}\,\bar{B}$$

EXOR:



Logic gate	No. of NAND	No. of NOR
NOT	1	1
AND	2	3
OR	3	2
EXOR	4	5
EXNOR	5	4
NOR	4	1
NAND	1	4