Course Project

Modeling of MOS Transistor using Verilog-A in QUCS

Name: Ritesh Jha
Roll No: EE24M059
Course: MOS Device Modelling (EE5341)

1. Abstract

This project implements and analyzes a Level-3 DC MOSFET model using Verilog-A. Both n-channel and p-channel devices are modeled, and their output and transfer characteristics are obtained under varying conditions of channel-length modulation (λ). Furthermore, a CMOS inverter composed of these devices is simulated to observe its voltage transfer characteristics. The influence of λ on device behavior and inverter performance is validated through comparative analysis.

2. Introduction

MOSFET modeling plays a crucial role in predicting circuit performance prior to fabrication. The Level-3 MOS model provides an enhanced physical representation over the Level-1 and Level-2 models by incorporating effects such as body bias and channel-length modulation while maintaining computational simplicity. In this project, the Verilog-A implementation of a Level-3 model is used to simulate DC characteristics for n-MOS and p-MOS devices. Subsequently, a CMOS inverter is analyzed to study how λ affects the voltage transfer curve and output swing.

3. Objectives

1. To implement the model using Verilog-A for circuit-level simulation.
2. To simulate and verify the device's I–V characteristics in QUCS.

4. Simulation Setup

4.1 Software Used

- **Verilog-A modeling & waveform plotting :** Qucs Studio

4.2 Parameters Used

Parameter	n-MOS	p-MOS
W (μm)	5	10
L (μm)	0.2	0.25
VTO (V)	0.4	-0.4
KP (A/V²)	5×10^{-4}	2.5×10^{-4}
GAMMA (V½)	0.5	0.5
PHI (V)	0.45	0.45
LAMBDA (V^{-1})	0, 0.1	0, 0.1
Temperature (K)	300	300

5. Methodology

5.1 n-Channel MOSFET Characteristics

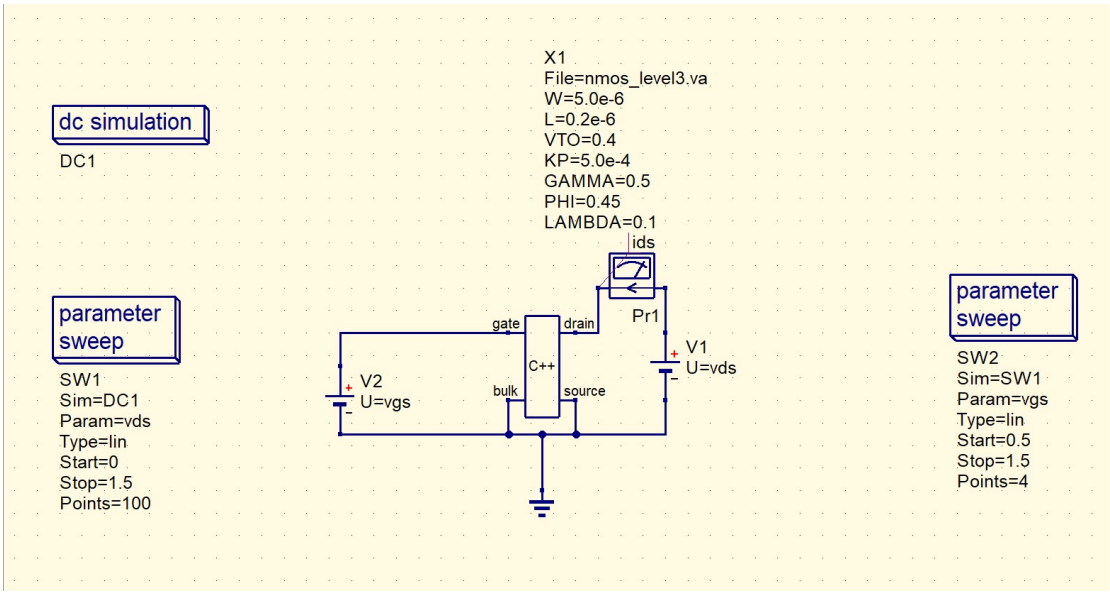

Figure.1 Schematic for NMOS Level-3 Model

(i) **Output Characteristics (ID–VDS):**
Plotted for VGSV_{GS}VGS = 0.5 V → 1.5 V (step 0.3 V), VBS=0VV_{BS}=0 VVBS =0V.
The curves exhibit the expected quadratic rise in the linear region, followed by current saturation at higher VDSV_{DS}VDS .
Increasing λ introduces finite slope in the saturation region due to channel-length modulation.

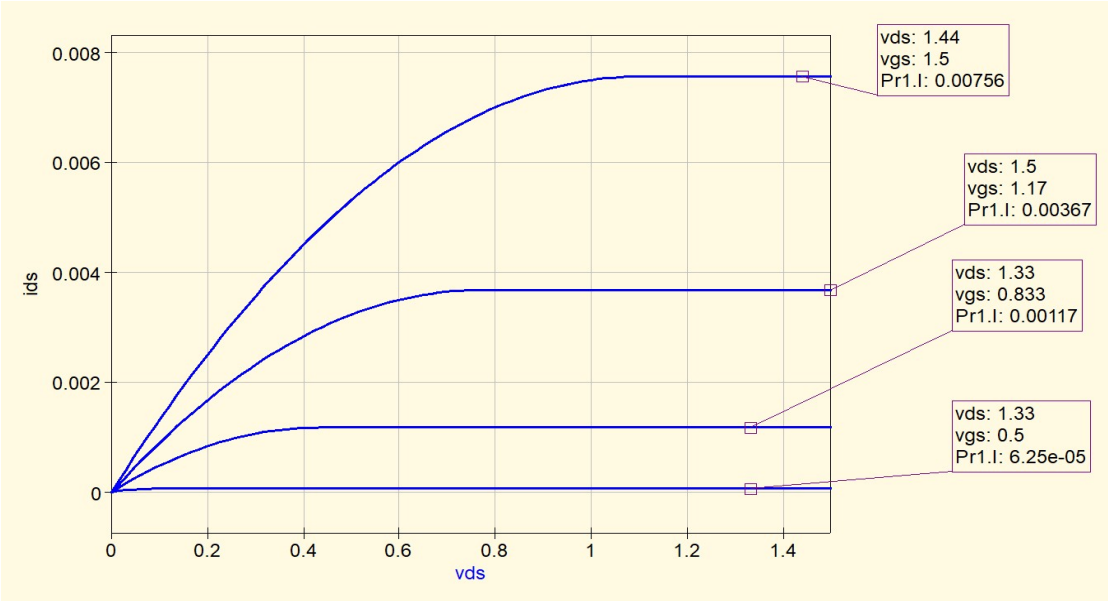

Figure.2(a) Id vs Vds plot for λ=0

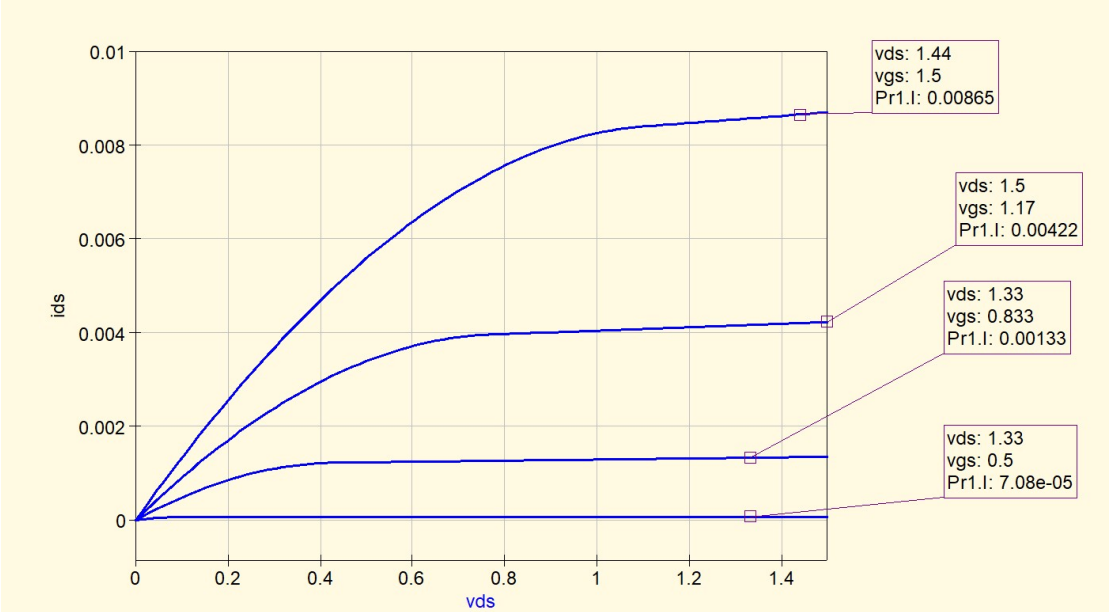

Figure2(b) Id vs Vds plot for λ=0.1

(ii) **Transfer Characteristics (ID–VGS):**
Simulated at VDSV_{DS}VDS = 0.1 V → 1.3 V in steps of 0.4 V.
The threshold voltage (~0.4 V) marks the onset of conduction. The higher VDSV_{DS}VDS values produce larger drain currents as expected.

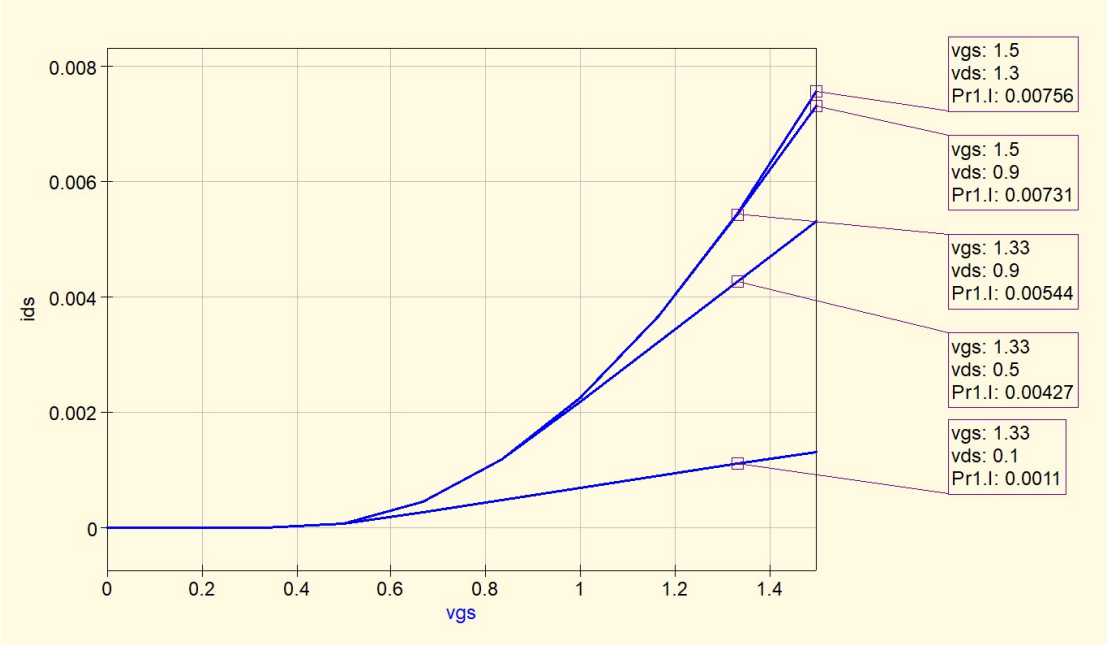

Figure2(c) Id vs Vgs plot for λ=0

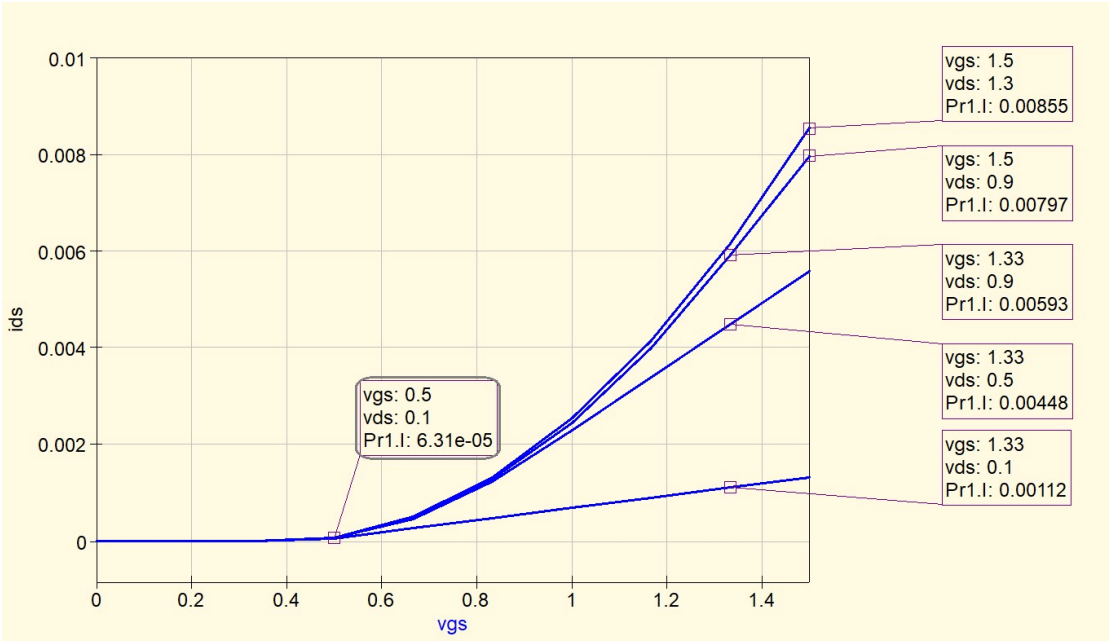

Figure2(d) Id vs Vgs plot for λ=0.1

5.2 p-Channel MOSFET Characteristics

Similar plots were generated for the p-MOS device. The characteristics mirror those of the n-MOS but with reversed polarity. The inclusion of $\lambda = 0.1\ V^{-1}$ produces the same qualitative slope increase in the saturation region.

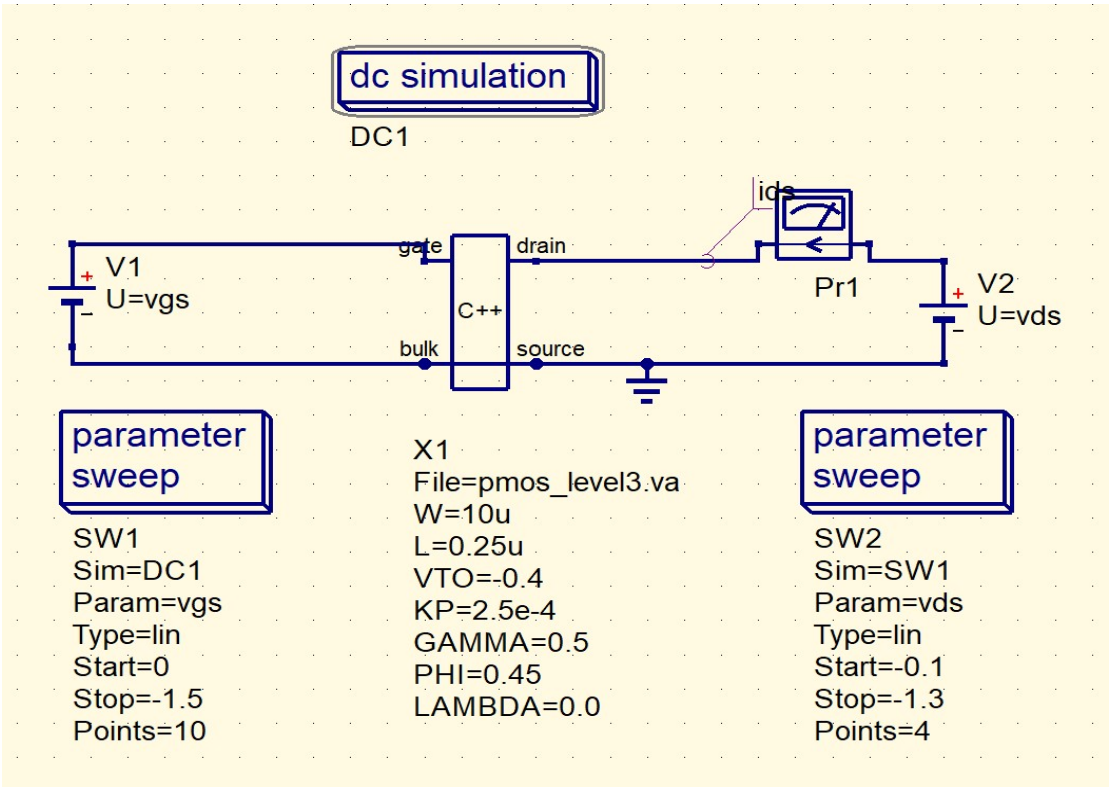

Figure.3 Schematic for PMOS Level-3 Model

(i) **Output Characteristics (ID–VDS):**
Plotted for VGSV_{GS}VGS = 0.5 V → 1.5 V (step 0.3 V), VBS=0VV_{BS}=0 VVBS =0V.
The curves exhibit the expected quadratic rise in the linear region, followed by current saturation at higher VDSV_{DS}VDS .
Increasing λ introduces finite slope in the saturation region due to channel-length modulation.

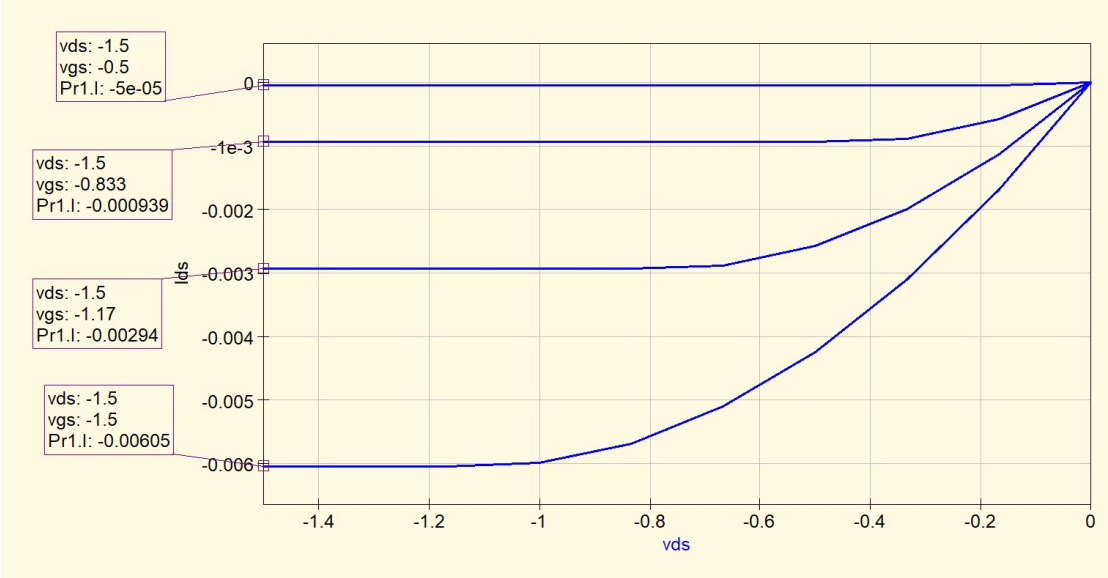

Figure.4(a) Id vs Vds plot for λ=0

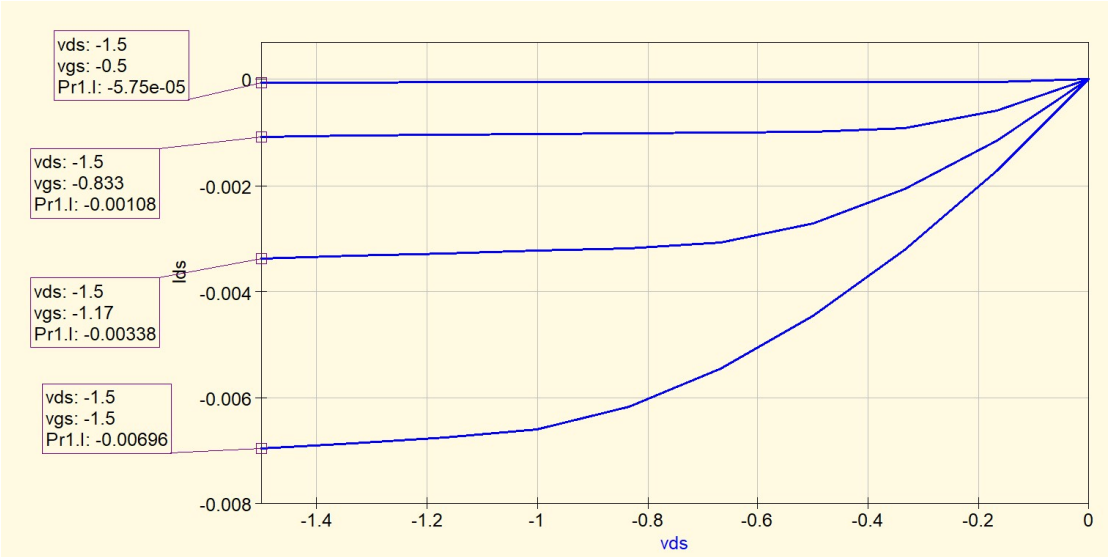

Figure.4(b) Id vs Vds plot for λ=0.1

(ii) **Transfer Characteristics (ID–VGS):**
Simulated at VDSV_{DS}VDS = 0.1 V → 1.3 V in steps of 0.4 V.
The threshold voltage (~0.4 V) marks the onset of conduction. The higher VDSV_{DS}VDS values produce larger drain currents as expected.

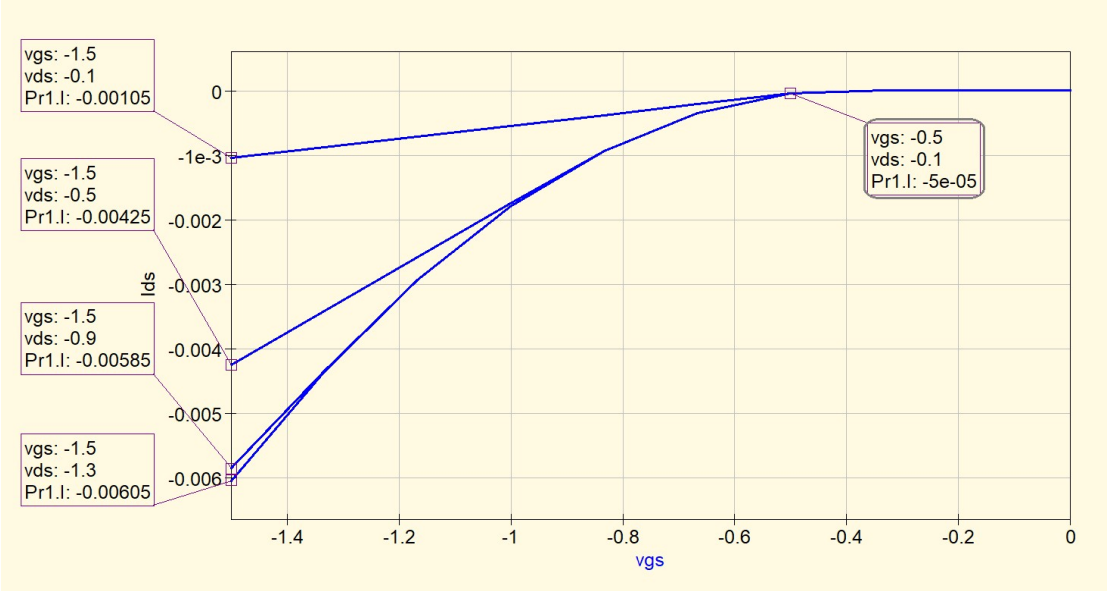

Figure.4(c) Id vs Vgs plot for λ=0

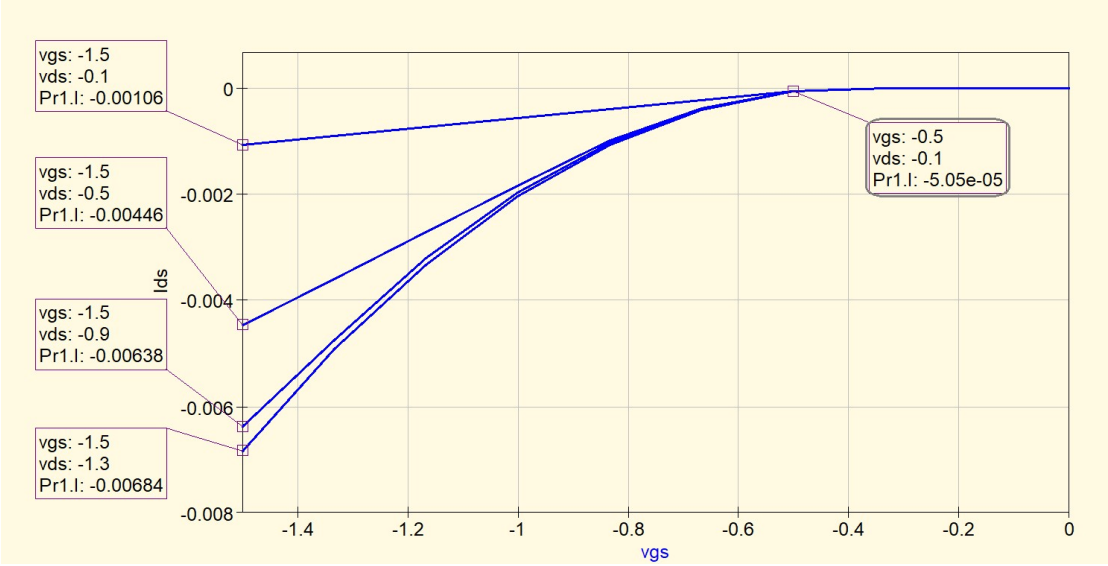

Figure.4(d) Id vs Vgs plot for λ=0.1

6. CMOS Inverter Analysis

A CMOS inverter was constructed using the above n-MOS and p-MOS transistors. The input voltage was swept from 0 V to 1.5 V with supply VDD=1.5VV_{DD}=1.5 VVDD =1.5V.
For $\lambda = 0.01\ V^{-1}$, the inverter exhibits a sharp transition with high gain and symmetric switching threshold.
When $\lambda = 0.1\ V^{-1}$, the finite output resistance of both transistors causes degraded logic levels and a reduced noise margin.

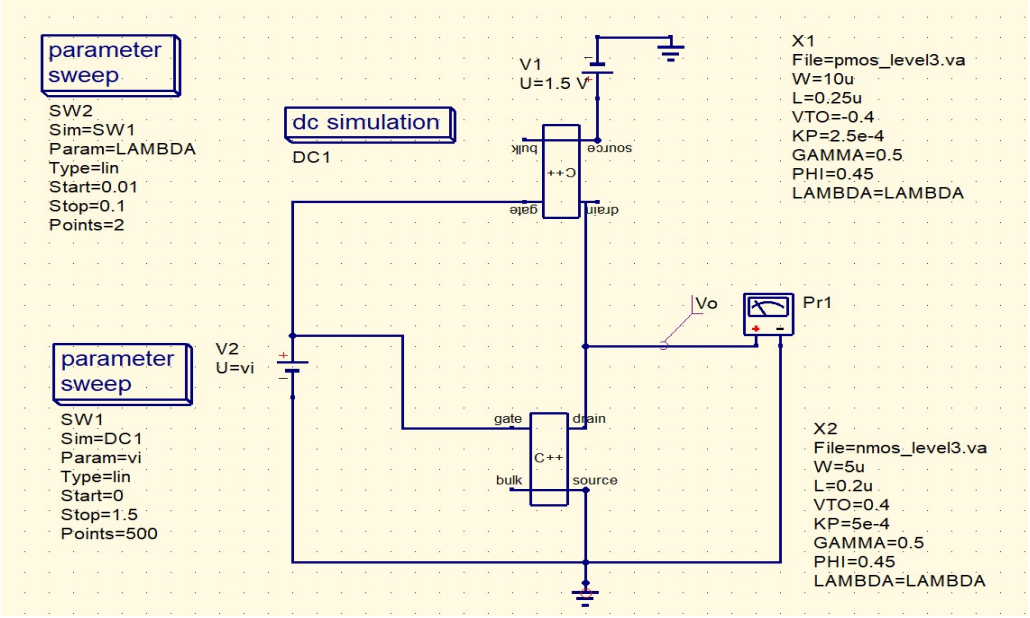

Figure.5 Schematic of CMOS Inverter Using Level-3 Model

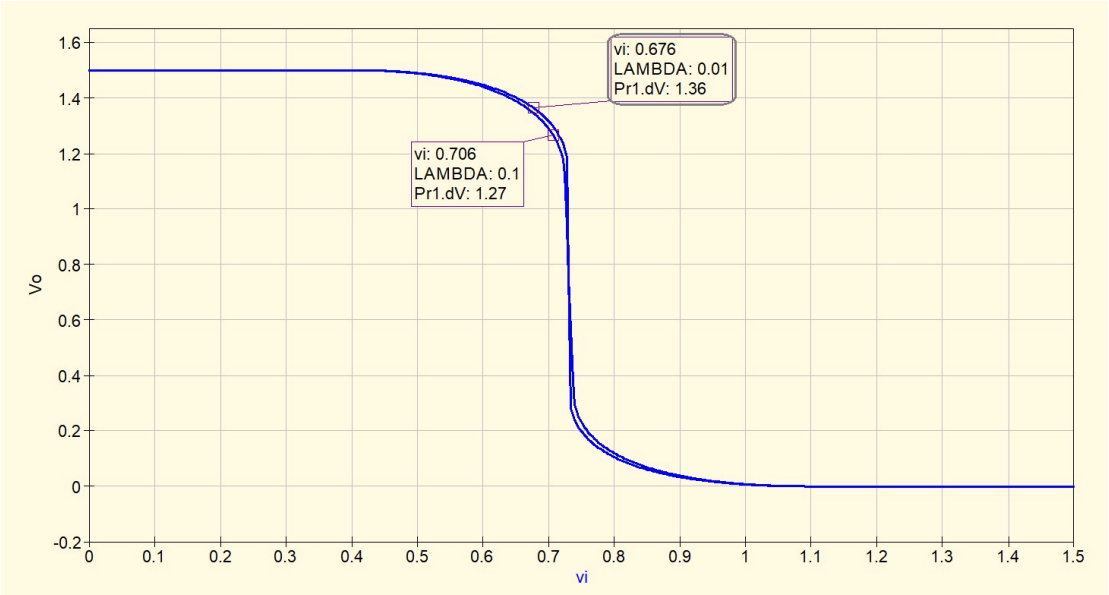

Figure.6 Vout vs Vin plot for varying λ

7. Conclusion

In this project, Level-3 MOSFET models for n-channel and p-channel devices were implemented using Verilog-A, and a CMOS inverter was analyzed under varying channel-length modulation (λ). The following conclusions can be drawn:

Effect of λ on NMOS and PMOS devices:

- For λ = 0, the drain current (ID) reaches saturation at high VDS values, showing ideal flat saturation regions in the output characteristics (ID–VDS).
- For λ = 0.1, the drain current increases slightly with VDS in the saturation region, indicating non-zero output conductance due to channel-length modulation.
- Transfer characteristics (ID–VGS) remain qualitatively similar for both λ values, but the absolute current in saturation increases with higher λ.
- Overall, increasing λ introduces a more realistic representation of short-channel effects, with the slope in the saturation region reflecting finite output resistance.

CMOS inverter behavior:

- For λ = 0.01, the inverter exhibits a sharp voltage transfer curve (VTC) with near-ideal logic levels and high switching gain. The output switches cleanly between logic high and low.
- For λ = 0.1, the VTC shows a slightly reduced gain and a less ideal transition region due to increased drain currents in saturation. The logic levels remain functional but output resistance affects the slope and switching sharpness.
- The comparison shows that higher λ values reduce the output resistance of transistors, affecting inverter performance and slightly degrading noise margins.

General observations:

- Channel-length modulation is an important factor in short-channel MOSFET modeling, as it directly impacts saturation current, output resistance, and inverter switching behavior.
- Level-3 MOS models successfully capture these effects while maintaining computational simplicity, making them suitable for both device-level and circuit-level simulations.