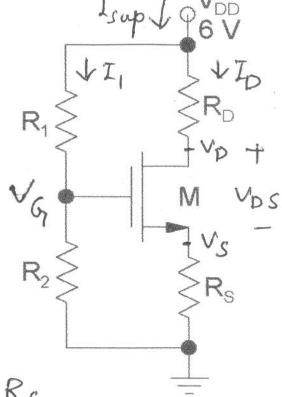
1. Consider the NMOS (M) discrete biasing circuit shown in the figure. Choose the values of $R_1$, $R_2$, $R_D$, and $R_S$, in order to satisfy the following performance requirements: a) the circuit should be under the *best biasing*, b) the power drawn from the supply should be 660 μW, and should be split in the ratio of 1:10 between the $R_1$-$R_2$ and $R_D$-M-$R_S$ branches, and c) at the bias point, the body factor ($\chi$) should be 0.158. Also, find $g_m$, $g_{mb}$, and $r_0$ of M at the bias point. Data for M: $V_{TN0} = 0.8$ V, $\gamma = 0.4\ V^{1/2}$, $2\phi_F = 0.6$ V, $(W/L) = 16$, $\lambda = 0.125\ V^{-1}$. **15**




$P_D = V_{DD} \times I_{sup} = 660\,\mu W \Rightarrow I_{sup} = 110\,\mu A = I_1 + I_D \Rightarrow \boxed{I_1 = 10\,\mu A \quad I_D = 100\,\mu A}$ (1:10)

Body terminal not shown ⇒ implies that it is connected to most −ve pot. (gnd).

Body factor $\chi = \dfrac{\gamma}{2\sqrt{2\phi_F + V_{SB}}} = 0.158 = \dfrac{0.4}{2\sqrt{0.6 + V_{SB}}} \Rightarrow \boxed{V_{SB} = 1V} \Rightarrow V_S = 1V = I_D R_S$

$\Rightarrow \boxed{R_S = 10\,k\Omega}$ ckt under best biasing ⇒ $V_{DS} = \dfrac{V_{DD}}{3} = 2V$ (3-element o/p branch)

$\Rightarrow I_D R_D = 3V \Rightarrow \boxed{R_D = 30\,k\Omega}$ $V_{TN} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) = 1V$

$I_D = \dfrac{k_n'}{2}\dfrac{W}{L}(V_{GS} - V_{TN})^2 \times (1 + \lambda V_{DS})$ ($\lambda V_{DS}$ can't be neglected, ∵ it is = to 0.25!)

$\Rightarrow \boxed{V_{GS} = 1.5V} \Rightarrow V_G = 2.5V = \dfrac{R_2}{R_1 + R_2} V_{DD}$ & $I_1 = \dfrac{V_{DD}}{R_1 + R_2} \Rightarrow R_1 + R_2 = 600\,k\Omega$

$\Rightarrow \boxed{R_2 = 250\,k\Omega}$ & $\boxed{R_1 = 350\,k\Omega}$

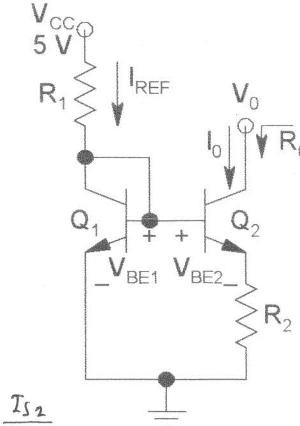
$g_m = K_n V_{GT}(1 + \lambda V_{DS}) = \sqrt{2K_n I_D(1 + \lambda V_{DS})} = 4 \times 10^{-4}\ \mho = \boxed{0.4\,m\mho}$

$g_{mb} = \chi g_m = 6.32 \times 10^{-5}\ \mho = \boxed{63.2\,\mu\mho}$

$r_o = \dfrac{1 + \lambda V_{DS}}{\lambda I_D} = \boxed{100\,k\Omega}$

———— × ————

2. Consider the BJT Widlar current source shown in the figure. Neglect base current, and assume $I_{S2} = 2I_{S1} = 0.2$ pA.
   a) Show that in order to minimize the total resistance requirement of the circuit for a given value of $I_0$, $R_1$ and $R_2$ must be chosen to be equal to $V_T/I_0$ and $R_1\ln(2V_1/V_T)$ respectively, where $V_1 = V_{CC} - V_{BE1}$. **3**
   b) Hence, evaluate the *self-consistent* values of $I_{REF}$, $V_{BE1}$, $V_{BE2}$, $R_1$, and $R_2$, to produce $I_0 = 10\ \mu$A. **7**
   c) Find $V_{0,min}$ and $R_0$ of the designed circuit if $V_{A2} = 130$ V. **3**
   d) What is the minimum required value of $\beta_2$ for the result of $R_0$ obtained in part c) to hold? Justify. **2**




a) $V_{BE_1} = V_{BE_2} + I_o R_2 \Rightarrow I_o R_2 = V_{BE_1} - V_{BE_2} = V_T \ln \frac{I_{REF}}{I_{S1}} - V_T \ln \frac{I_o}{I_{S2}} = V_T \ln \frac{I_{REF}}{I_o}\frac{I_{S2}}{I_{S1}}$

$\therefore R_2 = \frac{V_T}{I_o} \ln \frac{2 I_{REF}}{I_o}$ $(\because I_{S2} = 2I_{S1})$ & $I_{REF} = \frac{V_{CC}-V_{BE1}}{R_1} = \frac{V_1}{R_1} \Rightarrow R_2 = \frac{V_T}{I_o}\ln\frac{2V_1}{I_o R_1}$

$R_{Total} = R_1 + R_2 \Rightarrow$ To find $R_{Total,min}$, $\frac{dR_{Total}}{dR_1} = 0 = 1 - \frac{V_T}{I_o R_1}$ (neglecting any change in $V_{BE1}$ wrt $R_1$)

$\therefore \boxed{R_1 = \frac{V_T}{I_o}}$ & $\boxed{R_2 = R_1 \ln \frac{2V_1}{V_T}}$ (Shown)

b) $R_1 = \frac{V_T}{I_o} = \boxed{2.6\ k\Omega}$ & $R_2 = 2.6\ k\Omega \times \ln\frac{2(5-V_{BE1})}{0.026}$ $V_{BE1}$ not known as yet.

$I_{REF} = \frac{V_{CC}-V_{BE1}}{R_1}$ & $V_{BE1} = V_T \ln\frac{I_{REF}}{I_{S1}} = V_T\ln\frac{V_{CC}-V_{BE1}}{I_{S1}R_1} = 26\,mV \times \ln\frac{5-V_{BE1}}{0.1\,pA\times 2.6\,K}$

Only one iteration with a starting guess of $V_{BE1}$ of 0.7 V yields convergence with $\boxed{V_{BE1}=0.612\ V}$

$\therefore \boxed{R_2 = 15.1\,K}$ $\boxed{I_{REF} = 1.7\,mA}$ & $\boxed{V_{BE2} = 0.461\,V}$ $\left(= V_T\ln\frac{I_o}{I_{S2}}\right)$

Check: $V_{BE1}-V_{BE2} = \underline{0.151\,V}$ & $I_o R_2 = \underline{0.151\,V}$ → Consistent.

c) $V_{o,min} = V_{CE2}(SS) + I_o R_2 = \boxed{0.35\,V}$ $R_o = r_{o2}(1+g_{m2}R_2)$ assuming $r_{\pi 2} \gg R_2$

$r_{o2} = \frac{V_{A2}}{I_o} = \underline{13\,M\Omega}$ $g_{m2} = \frac{I_o}{V_T} = \frac{10\,\mu A}{26\,mV}$ $\Rightarrow R_o = 88.5\,M\Omega \sim \boxed{90\,M\Omega}$

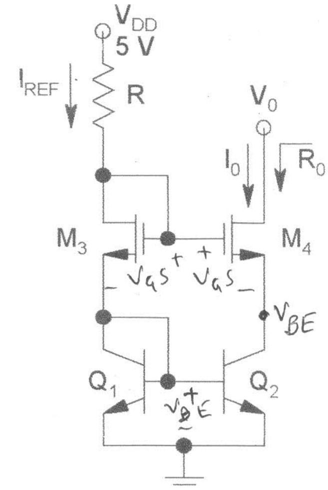
d) For the result of part c) to hold, $r_{\pi 2} \geq 10R_2 \Rightarrow \beta_2 r_{E2} \geq 10 R_2 \Rightarrow \boxed{\beta_2 \geq 58}$

3. In the BiMOS (combination of BJT and MOS) Cascode current source shown in the figure, transistors $Q_1$-$Q_2$ and $M_3$-$M_4$ are matched pairs. Neglect base current and body effect, and assume $\lambda V_{DS}$ and $V_{CE}/V_A$ both are $\ll 1$. Data: for $Q_2$: $V_A = 130$ V; for $M_3$-$M_4$: $V_{TN0} = 0.7$ V, $k_N' = 40\ \mu A/V^2$, $\lambda = 0.01\ V^{-1}$.

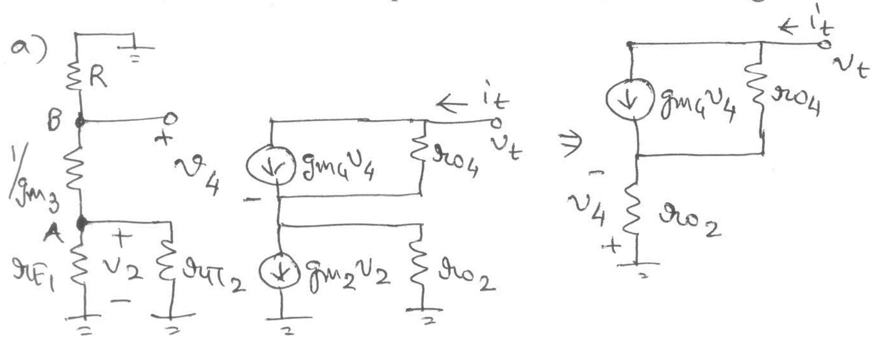
a) Clearly draw the *complete (i.e., without making any approximations)* ac small-signal midband equivalent of the circuit, and then making suitable approximations *and physically justifying them*, show that the output resistance ($R_O$) can be expressed as $R_O \approx g_{m4}r_{o4}r_{o2}$. 7

b) Choose the values of $I_{REF}$, R, and (W/L) of $M_3$-$M_4$, such that $I_O = 10\ \mu A$ when $V_O$ is at its minimum permissible value for proper operation. 4

c) What is the output resistance $R_O$ of the designed circuit? 4




a)




Pts. A & B are at ac gnd (∵ the left branch has no source) ⇒ $v_2 = 0 \Rightarrow g_{m2}v_2 = 0$.
$v_4$ appears across $r_{o2}$, with polarity shown.
Standard form ⇒ by inspection:
$R_0 = \frac{v_t}{i_t} = r_{o4}(1+g_{m4}r_{o2}) \simeq \boxed{g_{m4}r_{o2}r_{o4}}$

b) $Q_1$-$Q_2$ & $M_3$-$M_4$ matched ⇒ $I_0 = I_{REF} = \underline{10\,\mu A}$ $\quad V_{0,min} = V_{BE} + \Delta V_{4,min} = 0.7 + 0.08 = \underline{0.78\,V}$

∴ $V_{GS} = \Delta V_{4,min} + V_{TN0} = \underline{0.78\,V}$ & $I_{REF} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_3 (V_{GS} - V_{TN0})^2 = 10\,\mu A$ (neglecting $\lambda V_{DS}$, ∵ max value of $\lambda V_{DS} \sim 0.05$, $\ll 1$)

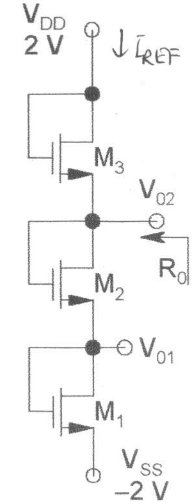
$\Rightarrow \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 78.1 \simeq \boxed{78}$ (matched)

& $I_{REF} = \frac{V_{DD} - (V_{BE} + V_{GS})}{R} \Rightarrow R = \frac{5 - (0.7 + 0.78)}{10\,\mu A} = \boxed{352\,k\Omega}$

c) $g_{m4} = K_n V_{GT} = \sqrt{2 K_n I_0} = 2.5 \times 10^{-4}\ ℧ = \boxed{0.25\,m℧}$ $\quad r_{o4} = \frac{1}{\lambda I_0} = \boxed{10\,M\Omega}$ $\quad r_{o2} = \frac{V_{A2}}{I_0} = \boxed{13\,M\Omega}$

$\Rightarrow R_0 = g_{m4}r_{o2}r_{o4} = \boxed{32.5\,G\Omega}$ !!! (mind-bogglingly large → approaching almost an ideal current source!)

4. All transistors in the circuit shown in the figure are put in separate wells, with their body terminals connected to their respective source terminals. It is desired to produce reference voltages $V_{01}$ and $V_{02}$ of −0.6 V and +0.6 V respectively. Data: MFS = 0.5 μm, $k'_N = 40\ \mu A/V^2$, $V_{TN0} = 0.8$ V, $\gamma = 0.4\ V^{1/2}$, $2\phi_F = 0.6$ V, $\lambda = 0.1\ V^{-1}$.




a) Which of the three transistors ($M_1$-$M_3$) would you pick to be the minimum-sized unit transistor in order for the circuit to dissipate the least dc power? *You have to justify your reasoning quantitatively*. Calculate this power. **5**

b) Based on the scheme chosen in a), determine the W and L for each of the transistors, and compute the total area of the circuit (*attempt should be made to reduce this area as much as possible*). **4**

c) Calculate the output resistance ($R_0$) of the voltage reference $V_{02}$. Based on this answer, comment on the suitability of use for this voltage reference. What steps would you take to improve the performance? **6**

a) All transistors have bodies connected to their respective sources ⇒ $V_{TN} = V_{TN0}$.

Let $Z = (V_{GS} - V_{TN0})^2 \times (1 + \lambda V_{DS})$. For $M_1$ & $M_3$: $V_{GS_1} = V_{DS_1} = V_{GS_3} = V_{DS_3} = 1.4V \Rightarrow \boxed{Z = 0.4104\ V^2}$

For $M_2$: $V_{GS_2} = V_{DS_2} = 1.2V \Rightarrow \boxed{Z = 0.1792\ V^2}$ ∴ $M_2$ has min. value of Z, ∴ it should be picked to be the min sized unit transistor in order to produce least dc power dissipation of the ckt.

∴ $I_{REF} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_2 \times Z = \boxed{3.6\ \mu A}$ & $P_D = (V_{DD} + |V_{SS}|) \times I_{REF} = \boxed{14.4\ \mu W}$

b) For min area, choose $W_2 = L_2 = MFS = \boxed{0.5\ \mu m}$ $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 = \frac{2 I_{REF}}{K_n' \times 0.4104} = \boxed{0.44}$

$\Rightarrow W_1 = W_3 = MFS = \boxed{0.5\ \mu m}$ & $L_1 = L_3 = \boxed{1.14\ \mu m}$

Total area $= \sum WL = 0.5\ \mu m \times (0.5\ \mu m + 1.14\ \mu m \times 2) = \boxed{1.4\ \mu m^2}$

c) Looking back from $V_{02}$, $R_o = \frac{1}{g_{m3}} \| \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)$ (neglecting $r_o$)

$g_{m1} = g_{m3} = K_n V_{GT}(1 + \lambda V_{DS}) = \sqrt{2 K_n I_D (1 + \lambda V_{DS})} = 1.2 \times 10^{-5}\ ℧ \Rightarrow \frac{1}{g_{m1}} = \frac{1}{g_{m3}} = 83.3K$

$g_{m2} = 1.8 \times 10^{-5}\ ℧ \Rightarrow \frac{1}{g_{m2}} = 55.6K \Rightarrow R_o = 83.3K \| 138.9K = \boxed{52\ k\Omega}$

Check: $r_{o1} = r_{o3} = \frac{1 + \lambda V_{DS}}{\lambda I_D} = 3.2\ M\Omega \gg \frac{1}{g_{m1}}, \frac{1}{g_{m3}}$; $r_{o2} = 3.1\ M\Omega \gg \frac{1}{g_{m2}}$ → assumption justified.

For a voltage ref., o/p res. of 52 kΩ is totally unacceptable (which should ideally be close to zero).

One way to reduce Ro is to increase gm by either increasing (W/L) (thus increasing area) or by increasing IREF (thus increasing power dissipation) ⇒ actually these two are related.

Note: Low power & low area do not necessarily produce the best performance.