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SUMMER INTERNSHIP PROJECT IN IIT GUWAHATI
"Design of low power bandpass digital filter for biomedical applications". You need to design a Bandpass filter of bandwidth 0.5 - 40Hz for the ECG signal"

BAND-PASS FILTER DESIGN FOR ECG

Readme.txt file for details about the Verilog and Matlab files in the below drive link & PPT has my learning throughout this project.

https://nitturl-my.sharepoint.com/:f:/g/personal/108118097_nitt_edu/EgtIe6oF1X5LhaAaBAbP5jgB6OfxG34mJkJeeh7ftc-Mtg?e=1wUgVh

Data set MIT-BIH Arrhythmia Database :: Filename= "100m.mat"

'100m.info' contains the specification in raw ECG samples

```
Source: record mitdb/100
val has 1 row (signal) and 650000 columns (samples/signal)
Duration:    30:05
Sampling frequency: 360 Hz  Sampling interval: 0.002777777778 sec
Row Signal  Gain    Base    Units
1   MLII    200 0   mV

To convert from raw units to the physical units shown
above, call the 'rdmat.m' function from the wfdb-matlab
toolbox: https://physionet.org/physiotools/matlab/wfdb-app-matlab/
```

Gain is 200 and has to be adjusted in Matlab data set respectively

```
load('100m.mat');
ECGsignal = val/200 ;%200 is gain
fs = 360; %sampming frequency as given in .info file
```

https://www.physionet.org/content/mitdb/

The recordings were digitized at 360 samples per second per channel with 11-bit resolution over a 10 mV range.

Two or more cardiologists independently annotated each record; disagreements were resolved to obtain the computer-readable reference annotations for each beat (approximately 110,000 annotations in all) included with the database.

1. ECG Filter design using the inbuilt function in MATLAB to calculate filter coefficients.
2. ECG Filter design without using the inbuilt function in MATLAB to calculate filter coefficients. (Windowing technique is exploited).

SPECIFIACTION USED

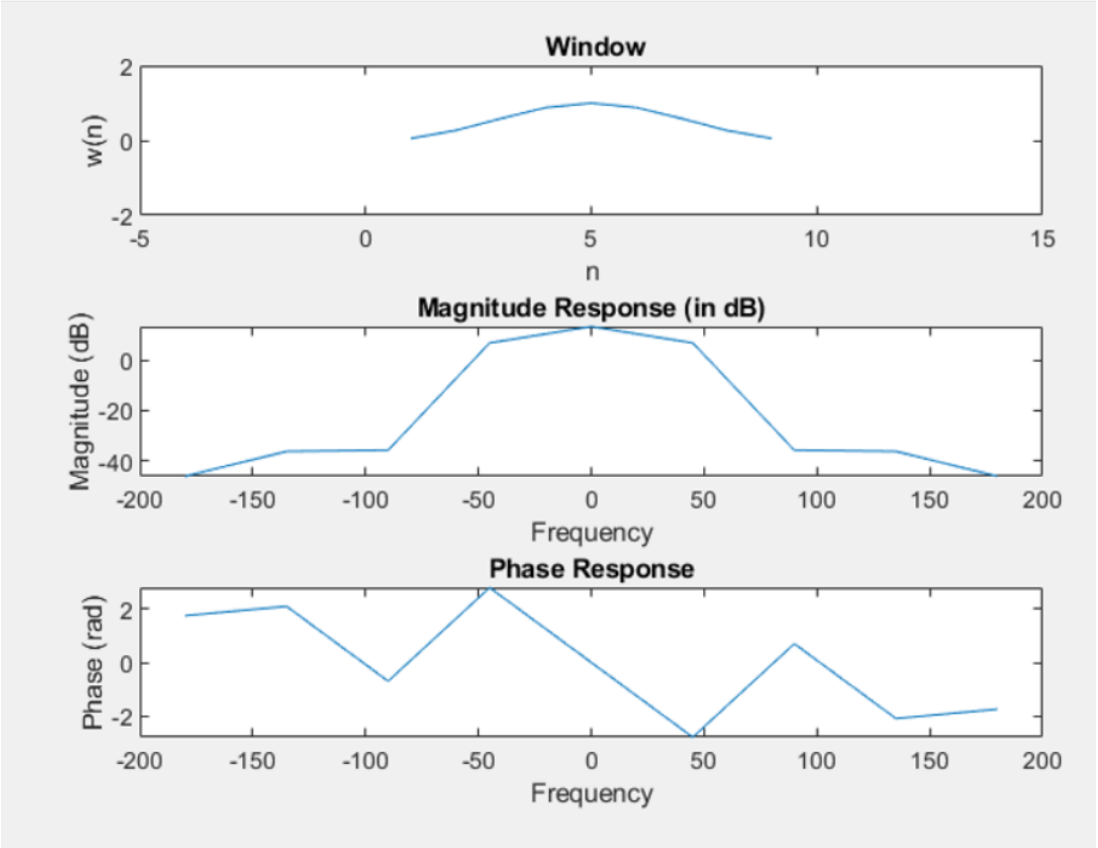
- Stop band attenuation AS = −20 log $[\![\delta\_s]\!]$ = **50db**
- Bandwidth = **0.5 - 40 Hz**
- **Length of the filter = 9**
- **Sampling Frequency = 360 Hz**
- No of taps = 9
- **Order = 8**

Linear phase FIR filter is employed for better design quality

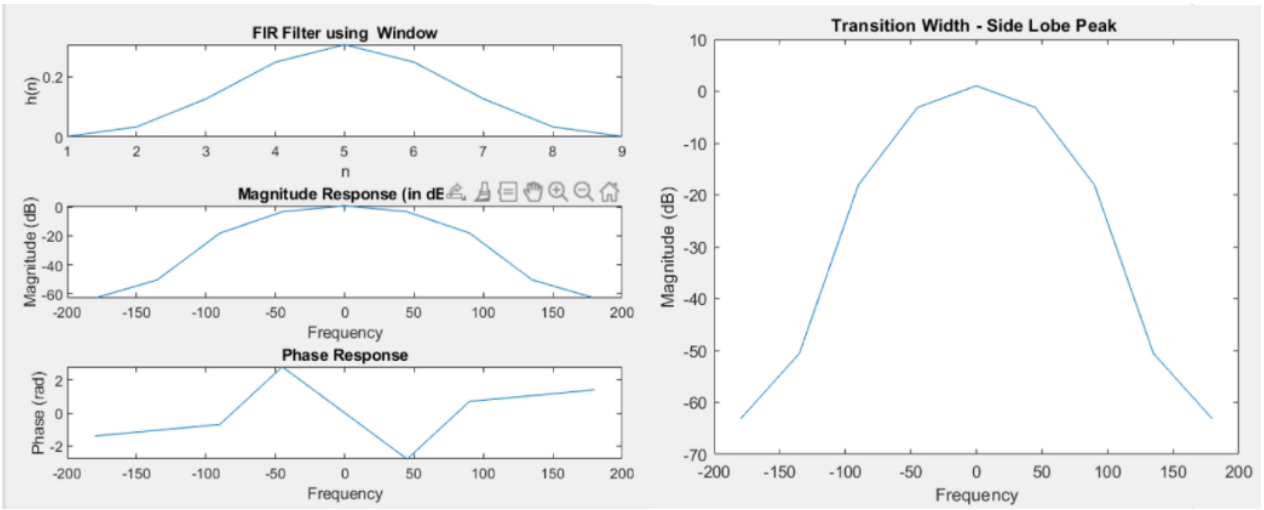
- **TYPE 1**
- **Symmetrical (β=0 or Π)**
- **N= odd**
- h(n)=h(N-1-n) where N is the length of the filter
- Best choice to design Adjust the comment line to use a different windowing function in Matlab.

Based on transition width lobe and stopband attenuation, various window coefficients are estimated. It turns out to be as follows

Now among different window function, **we select Kaiser window function for this application because its provides maximum stopband attenuation as compared to other window functions and also has a ripple control parameter and it is also more efficient in terms of the number of coefficients to meet the same specifications.**



Kaiser window is one of the useful and optimum windows, optimum in sense of providing large main lobe width for the given stop-band attenuation which gives the sharpest transition width and it also provides flexible transition bandwidth.

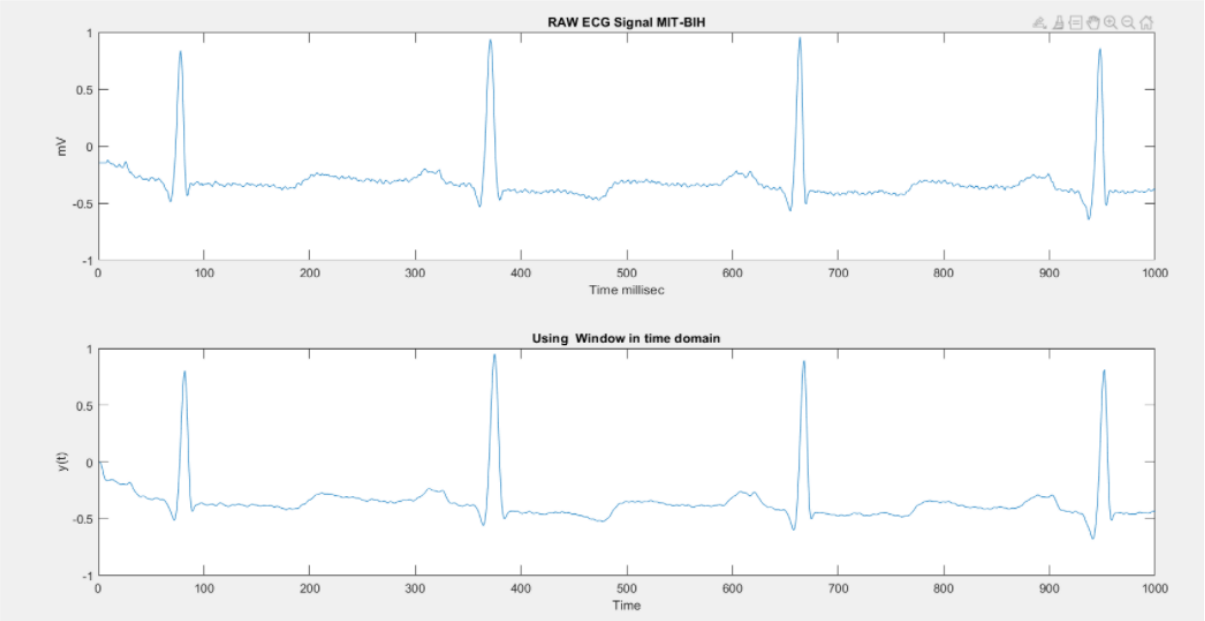


FOR THE REMAINING WINDOW, GO THROUGH THE ECG FILTER.ppt for results

SHAPE PARAMETER (beta) = 4.5513

h(n) = [0.0019 0.0336 0.1266 0.2488 0.3072 0.2488 0.1266 0.0336 0.0019]

File name = '100.txt' has fixed point implemention of sampled floating point raw data of ECG from MIT-BIH Arrhythmia Database which used as raw feed input in Xilinx VIVADO TEST FIGURE.



obtained coeffients [h] = [0.0019 0.0336 0.1266 0.2488 0.3072 0.2488 0.1266 0.0336 0.0019]

(using kaiser window)

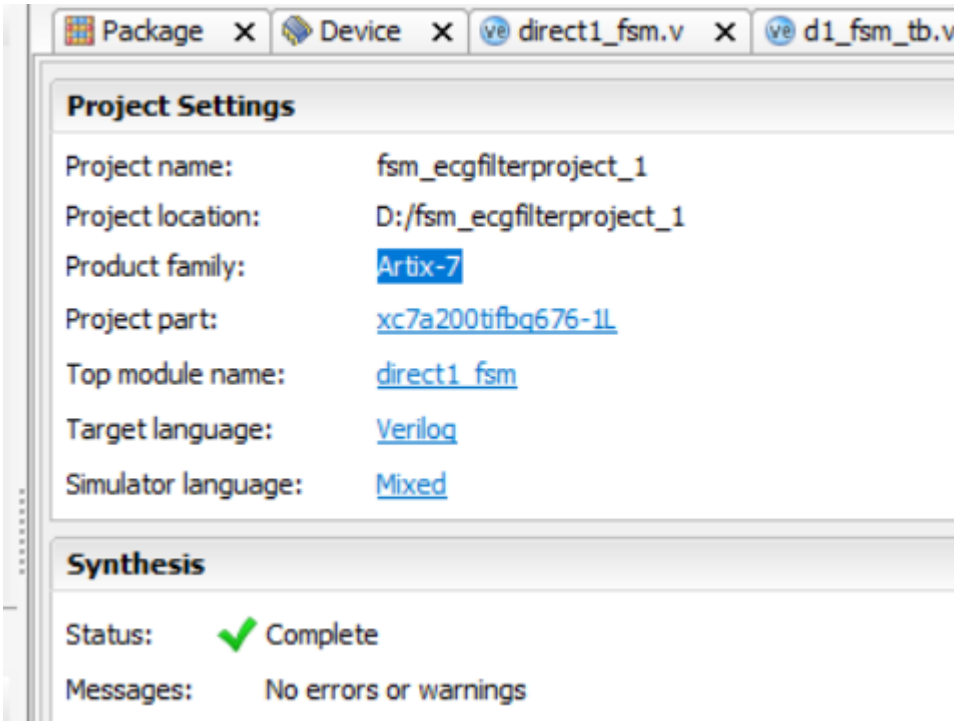
These coefficients are also fixed by multiplying with 2^8 =256 and approximated

to get 8 bit fixed pt representation for declaring parameter in Verilog code

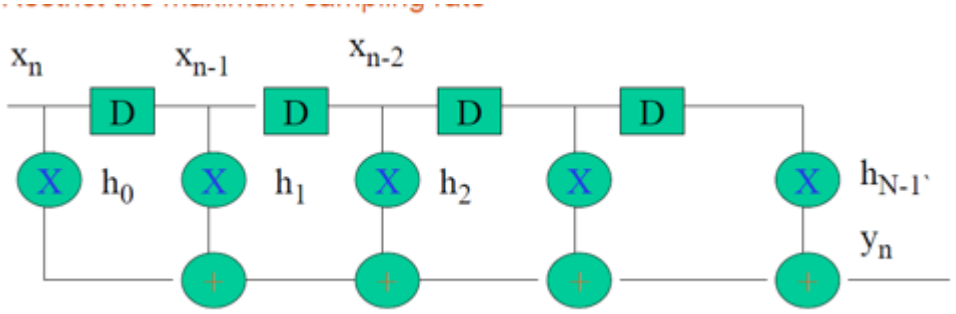
h= [0 9 32 64 79 64 32 9 0]

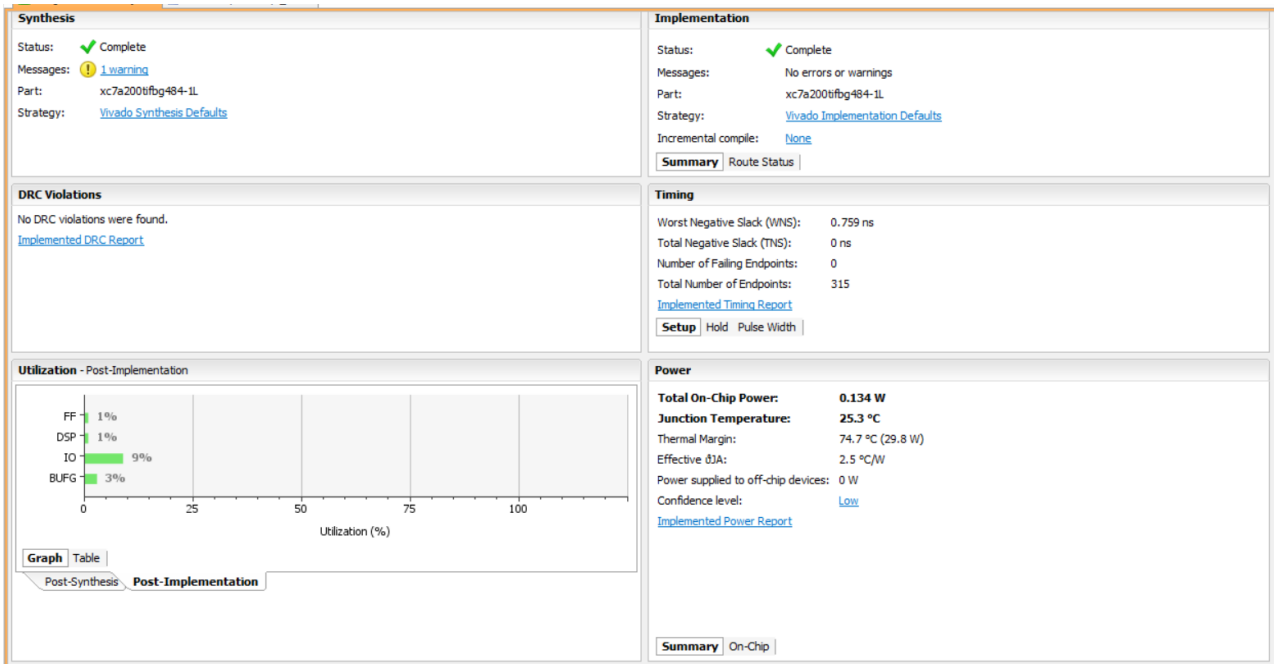
The above is the coefficient after fixing.

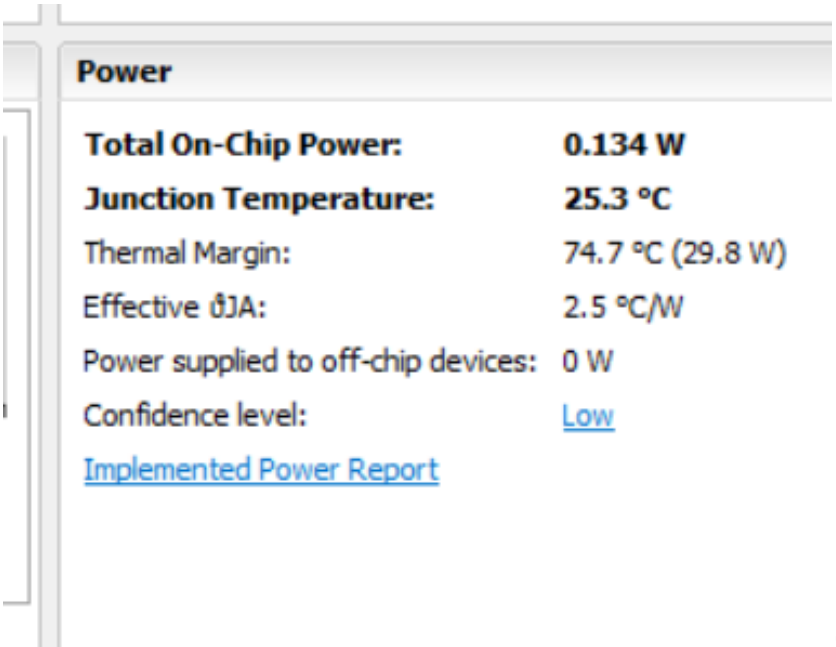
BOARD USED: Artix 7 board



Direct Form 1:Unfolded: single state without input





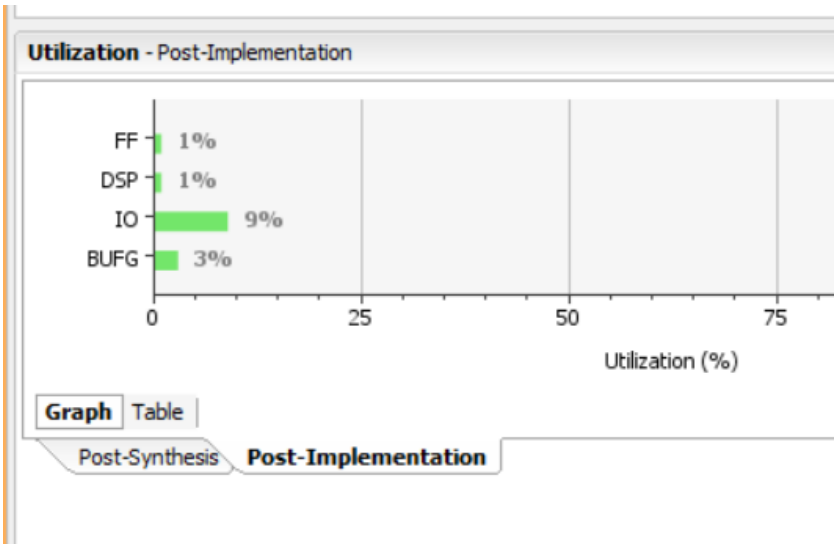


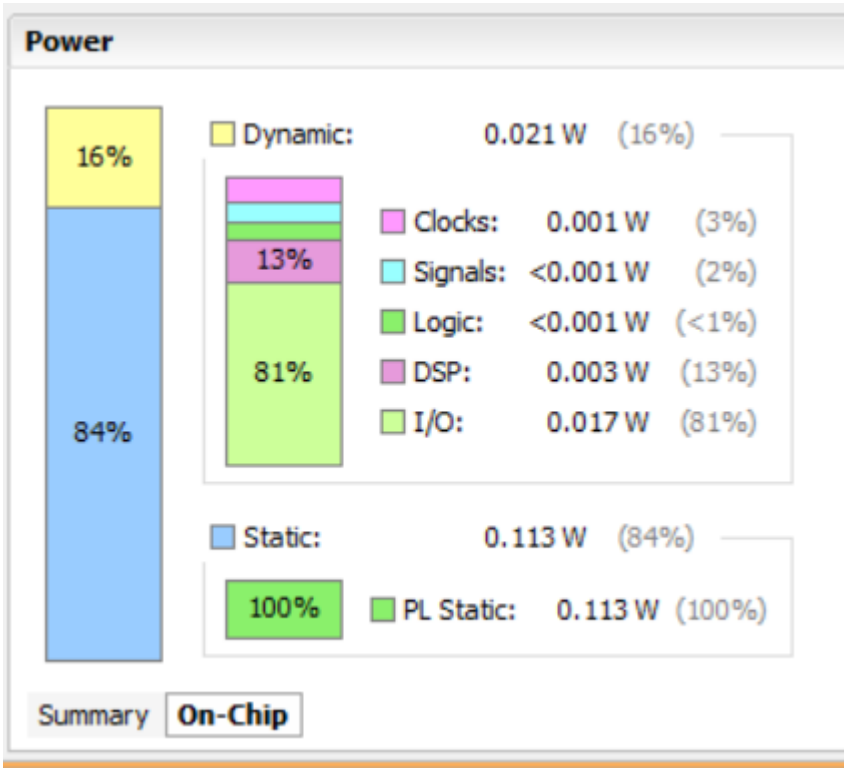
direct form 1 :unfolded

Resource	Utilization	Available	Utilization %
FF	32	269200	0.01
DSP	8	740	1.08
IO	26	285	9.12
BUFG	1	32	3.13

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	0	0	134600	0.00
LUT as Logic	0	0	134600	0.00
LUT as Memory	0	0	46200	0.00

Slice Registers	32	0	269200	0.01
Register as Flip Flop	32	0	269200	0.01
Register as Latch	0	0	269200	0.00
F7 Muxes	0	0	67300	0.00
F8 Muxes	0	0	33650	0.00



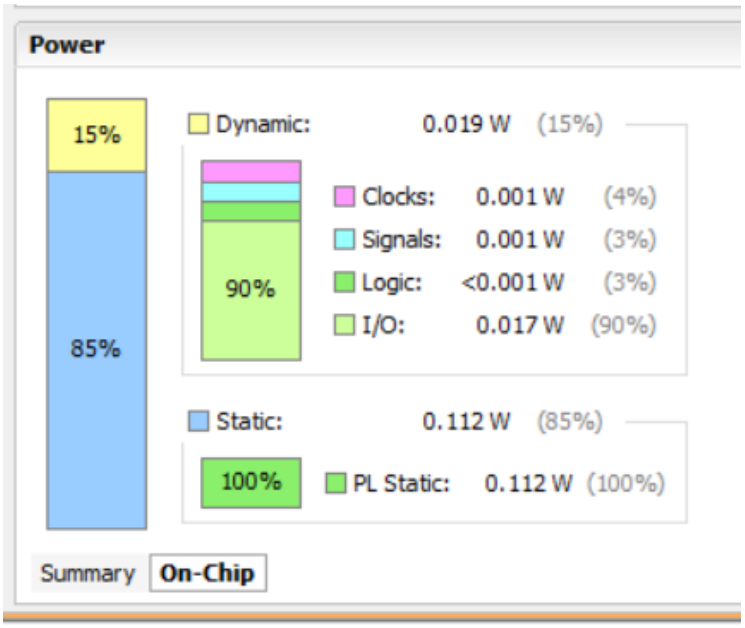


DIRECT FORM 1 UNFOLDED: using continuous assignment and Dff for delay

Power

Total On-Chip Power:	**0.132 W**
Junction Temperature:	**25.2 °C**
Thermal Margin:	74.8 °C (39.6 W)
Effective ϑJA:	1.9 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report



Synthesis

Status:	✔ Complete
Messages:	No errors or warnings
Part:	xc7a200tifbg676-1L
Strategy:	Vivado Synthesis Defaults

Implementation

Status:	✔ Complete
Messages:	No errors or warnings
Part:	xc7a200tifbg676-1L
Strategy:	Vivado Implementation Defaults
Incremental compile:	None

Summary | Route Status

DRC Violations

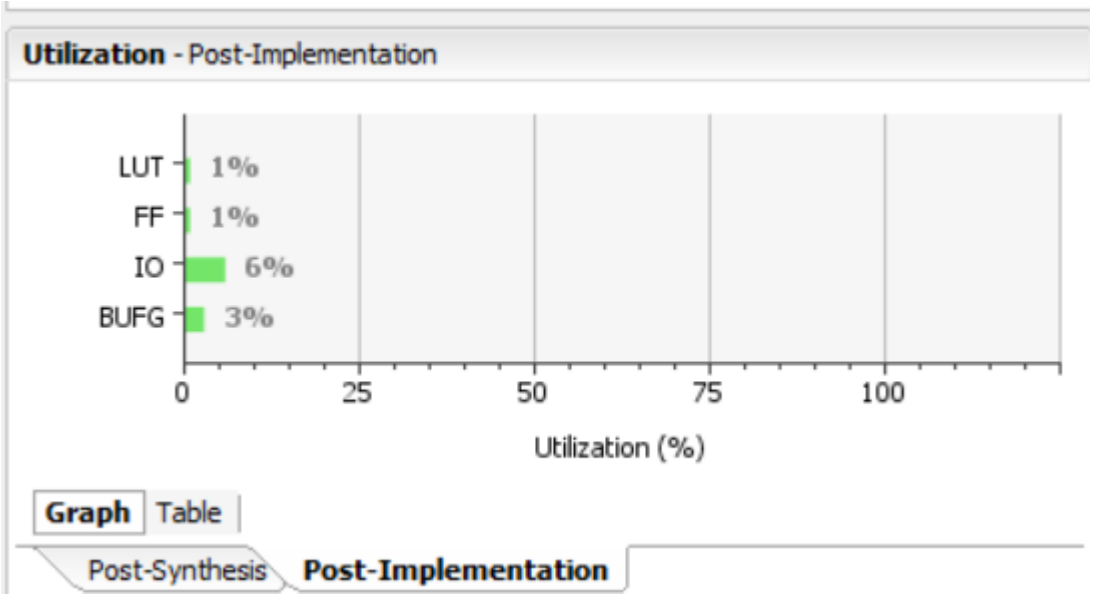
No DRC violations were found.

Implemented DRC Report

Timing

Worst Negative Slack (WNS):	1.121 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	88

Implemented Timing Report



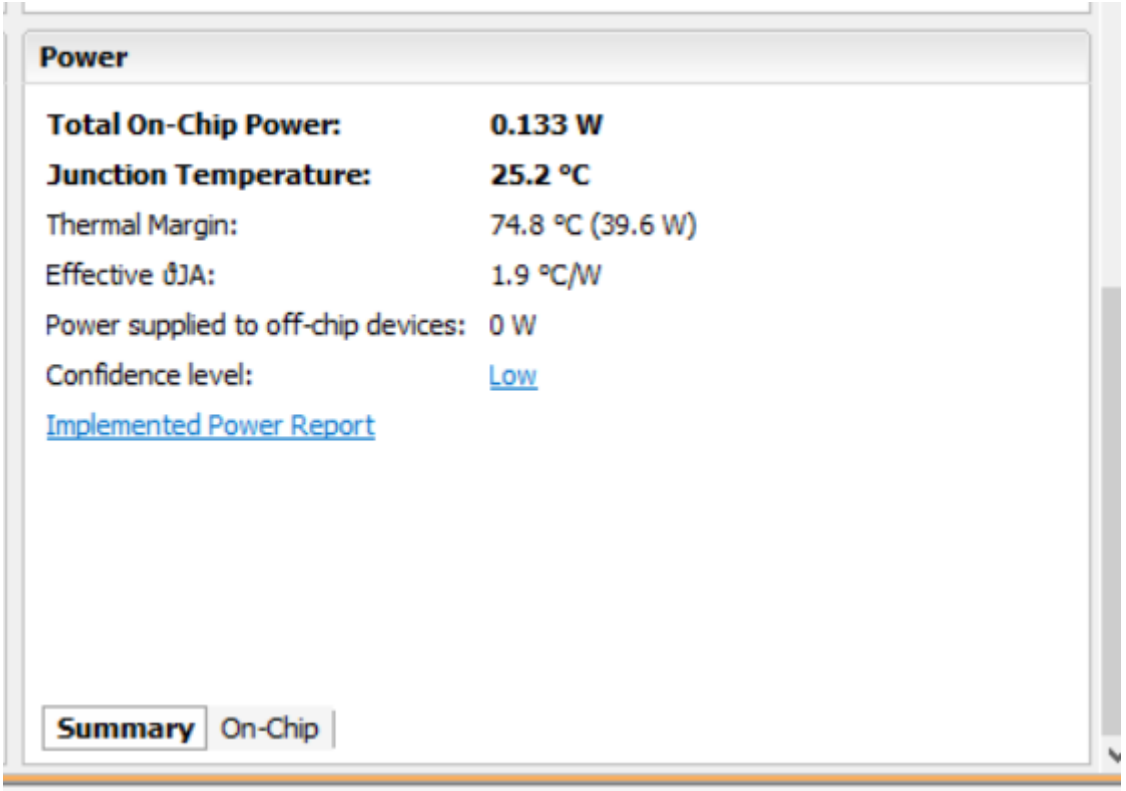
Slice Logic

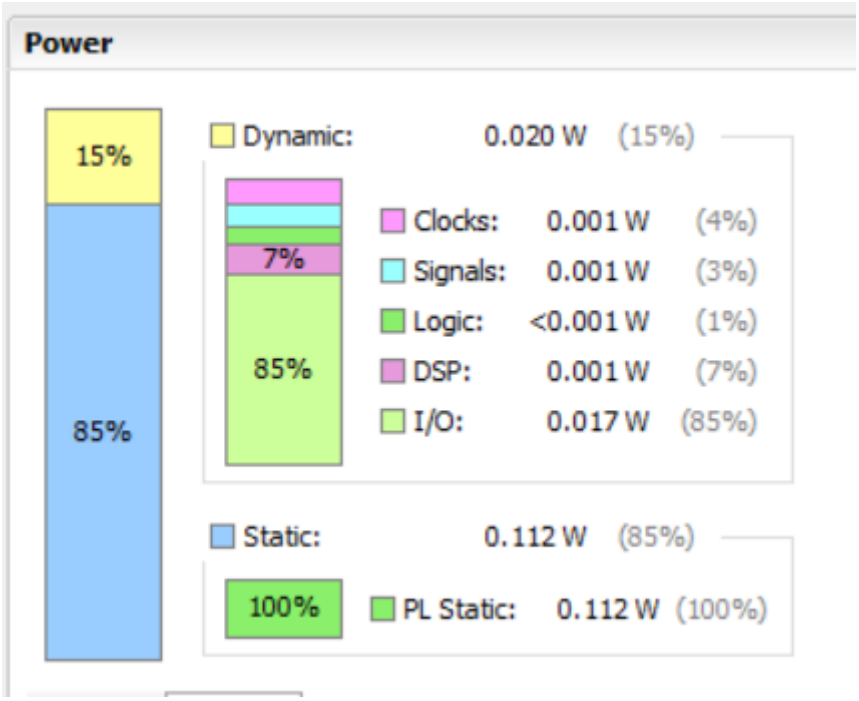
```
+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |  123 |     0 |    134600 |  0.09 |
|   LUT as Logic          |  123 |     0 |    134600 |  0.09 |
|   LUT as Memory         |    0 |     0 |     46200 |  0.00 |
| Slice Registers         |   72 |     0 |    269200 |  0.03 |
|   Register as Flip Flop |   72 |     0 |    269200 |  0.03 |
|   Register as Latch     |    0 |     0 |    269200 |  0.00 |
| F7 Muxes                |    0 |     0 |     67300 |  0.00 |
| F8 Muxes                |    0 |     0 |     33650 |  0.00 |
+-------------------------+------+-------+-----------+-------+
```

Resource	Utilization	Available	Utilization %
LUT	114	134600	0.08
FF	72	269200	0.03
IO	25	400	6.25
BUFG	1	32	3.13

FOLDED STRUCTURE: DIRECT FORM 1

SINGLE STATE USING ALWAYS BLOCK

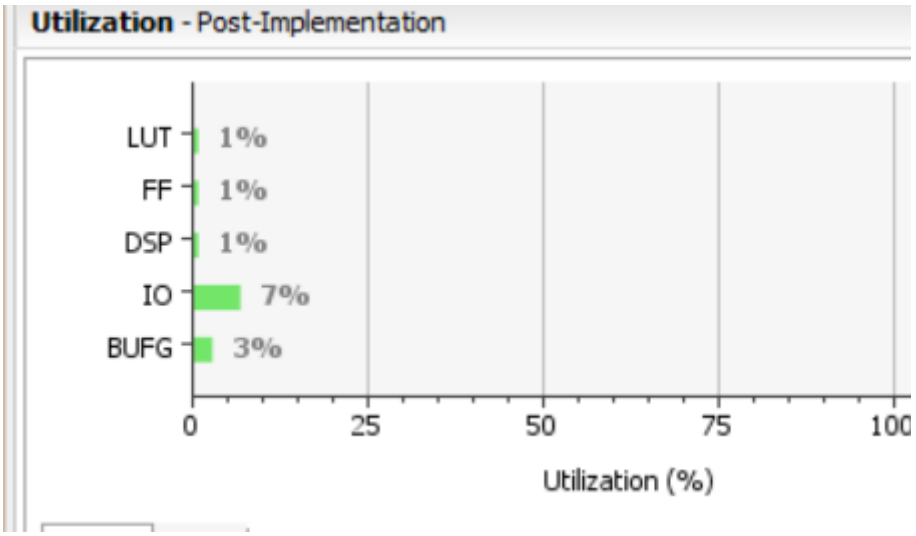




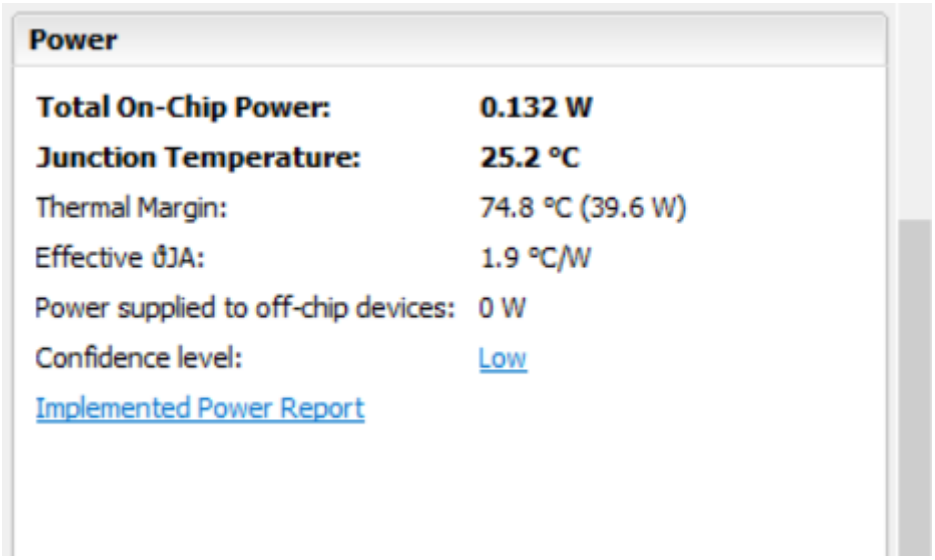
Slice Logic

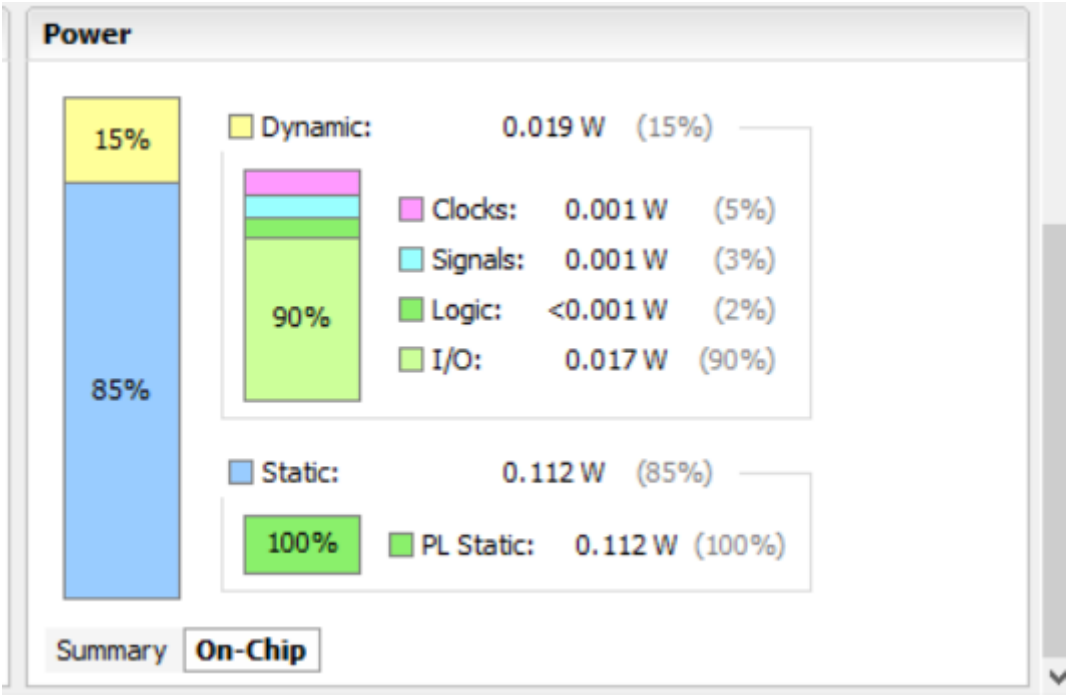
Site Type	Used	Fixed	Available	Util%
Slice LUTs*	20	0	134600	0.01
LUT as Logic	20	0	134600	0.01
LUT as Memory	0	0	46200	0.00
Slice Registers	57	0	269200	0.02
Register as Flip Flop	57	0	269200	0.02
Register as LatcH	0	0	269200	0.00
F7 Muxes	0	0	67300	0.00
F8 Muxes	0	0	33650	0.00

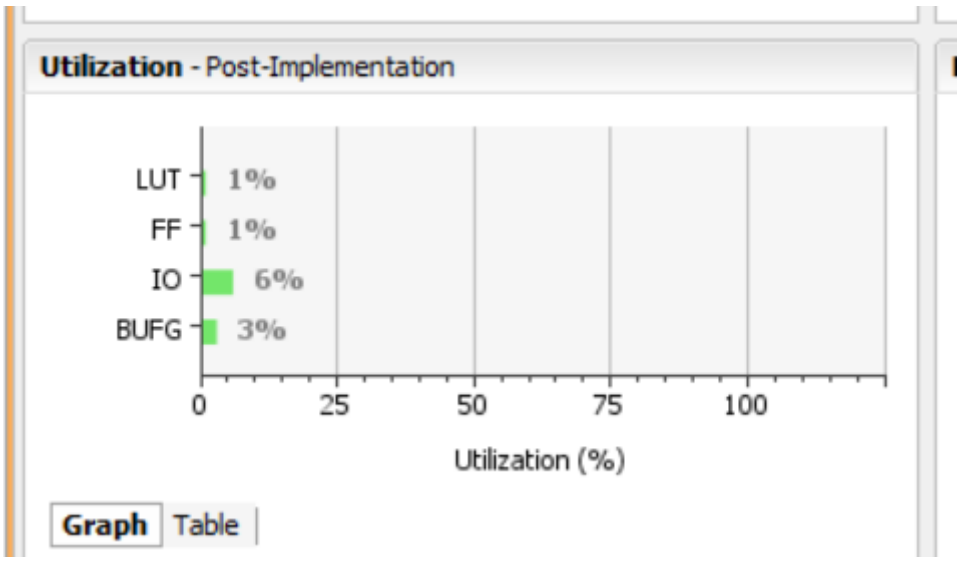
Resource	Utilization	Available	Utilization %
LUT	20	134600	0.01
FF	57	269200	0.02
DSP	3	740	0.41
IO	26	400	6.50
BUFG	1	32	3.13



FOLDED STRUCTURE: DIRECT FORM 1 USING ASSIGN AND DFF MODULE







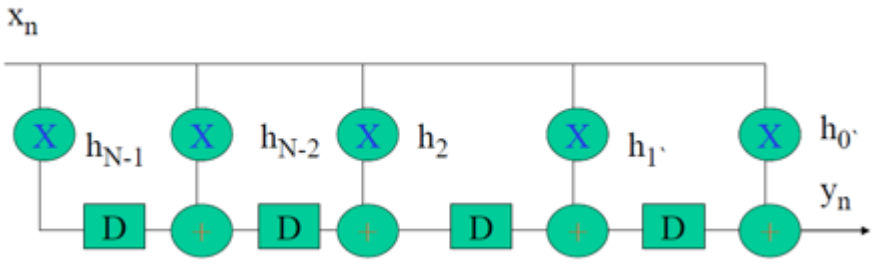
Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
LUT	100	134600	0.07
FF	72	269200	0.03
IO	25	400	6.25
BUFG	1	32	3.13

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	106	0	134600	0.08
LUT as Logic	106	0	134600	0.08
LUT as Memory	0	0	46200	0.00
Slice Registers	72	0	269200	0.03
Register as Flip Flop	72	0	269200	0.03
Register as Latch	0	0	269200	0.00
F7 Muxes	0	0	67300	0.00
F8 Muxes	0	0	33650	0.00

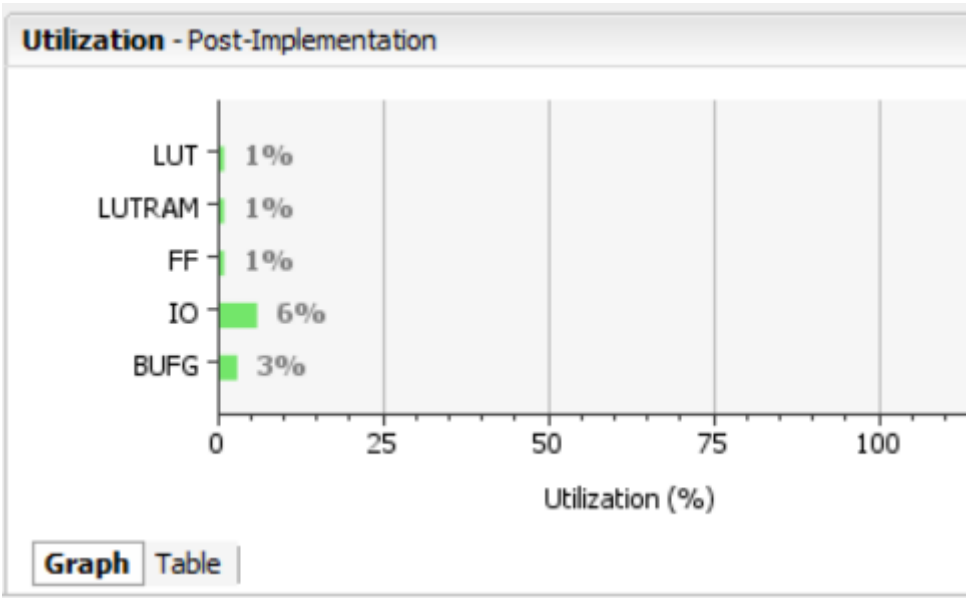
TRANSPOSE PIPELINE STRUCTURE (with DFF as delay element) Direct form II



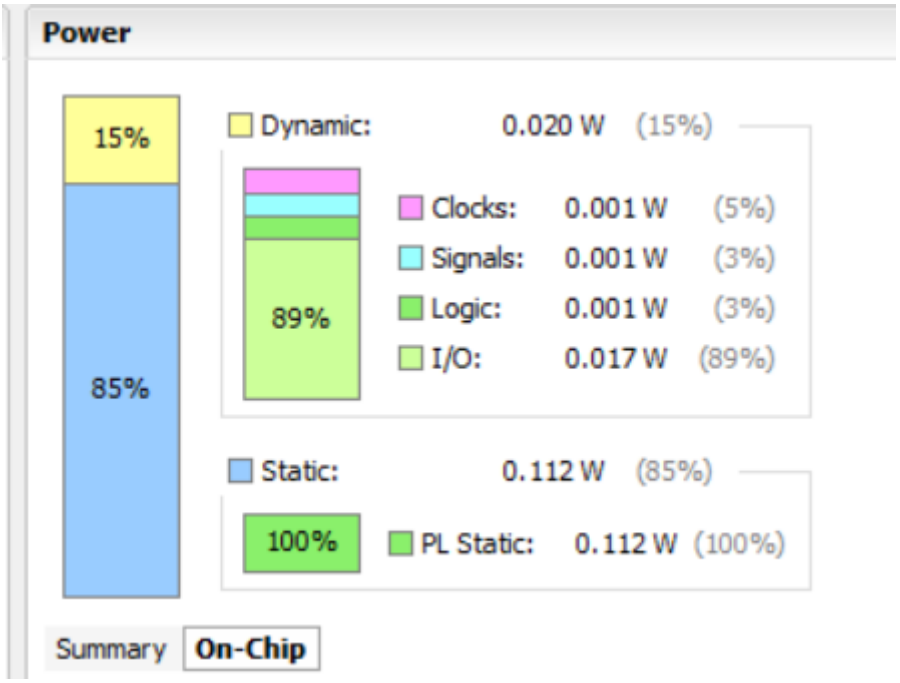
Power

Total On-Chip Power:	**0.132 W**
Junction Temperature:	**25.2 °C**
Thermal Margin:	74.8 °C (39.6 W)
Effective ϑJA:	1.9 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report



Resource	Utilization	Available	Utilization %
LUT	115	134600	0.09
LUTRAM	4	46200	0.01
FF	115	269200	0.04
IO	25	400	6.25
BUFG	1	32	3.13



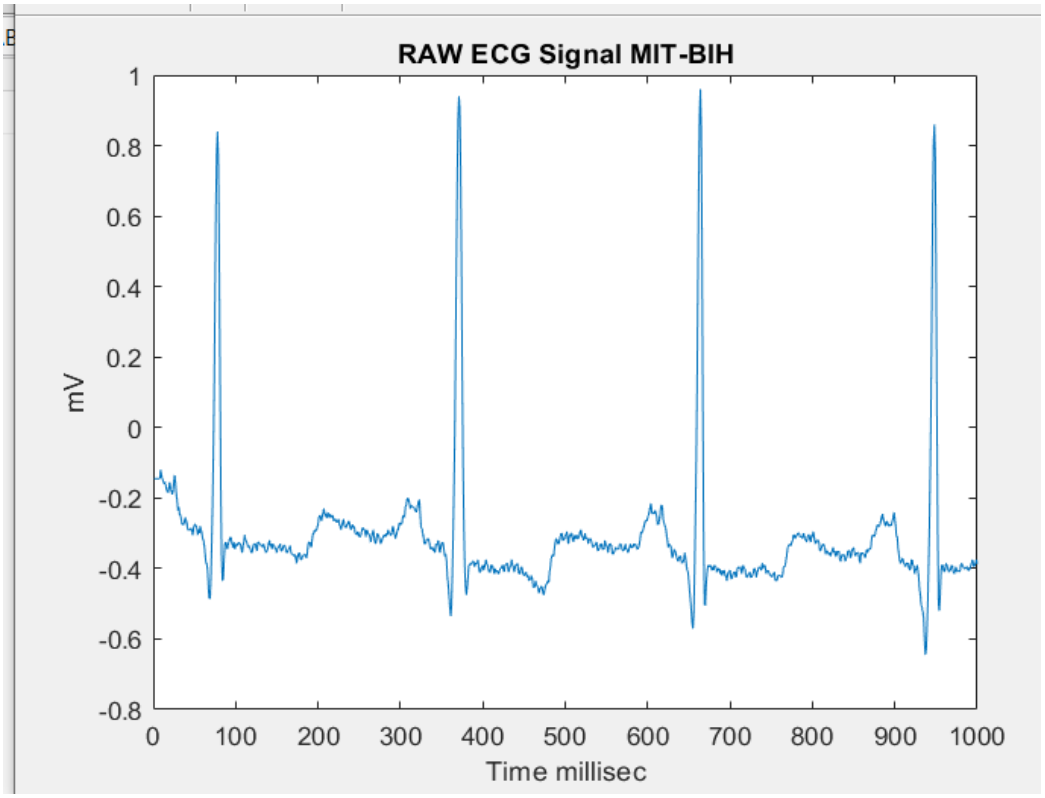
Slice Logic

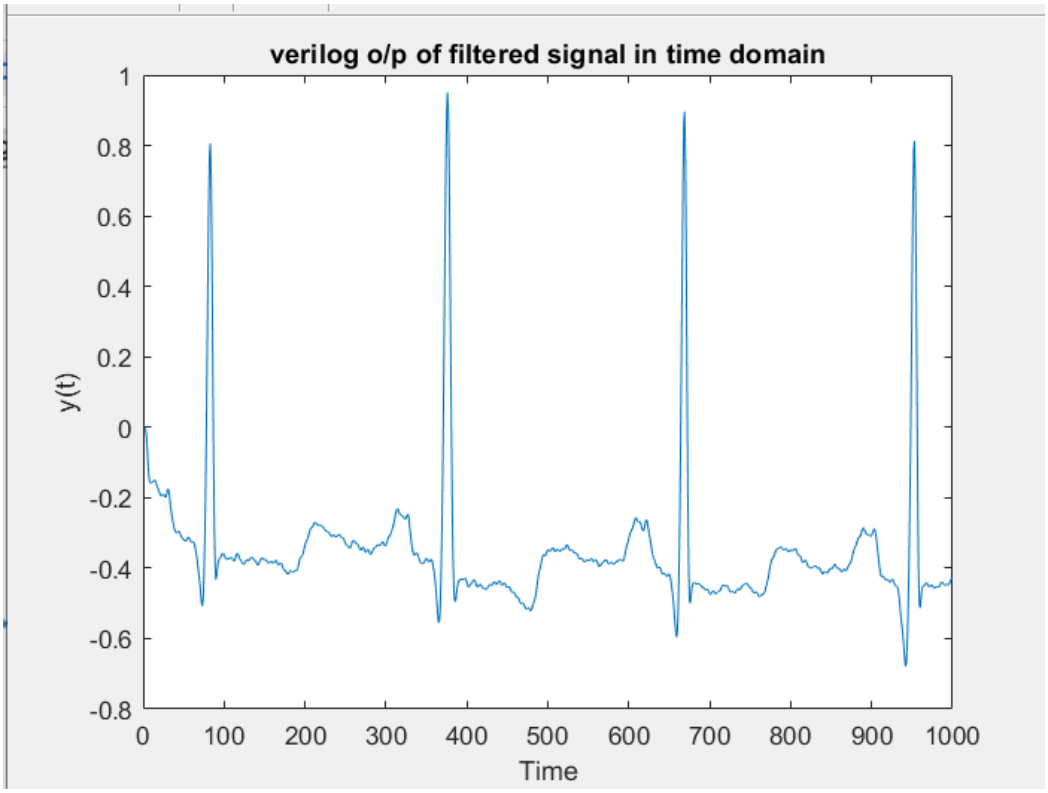
Site Type	Used	Fixed	Available	Util%
Slice LUTs*	123	0	134600	0.09
LUT as Logic	119	0	134600	0.09
LUT as Memory	4	0	46200	<0.01
LUT as Distributed RAM	0	0		
LUT as Shift Register	4	0		
Slice Registers	115	0	269200	0.04
Register as Flip Flop	115	0	269200	0.04
Register as Latch	0	0	269200	0.00
F7 Muxes	0	0	67300	0.00
F8 Muxes	0	0	33650	0.00

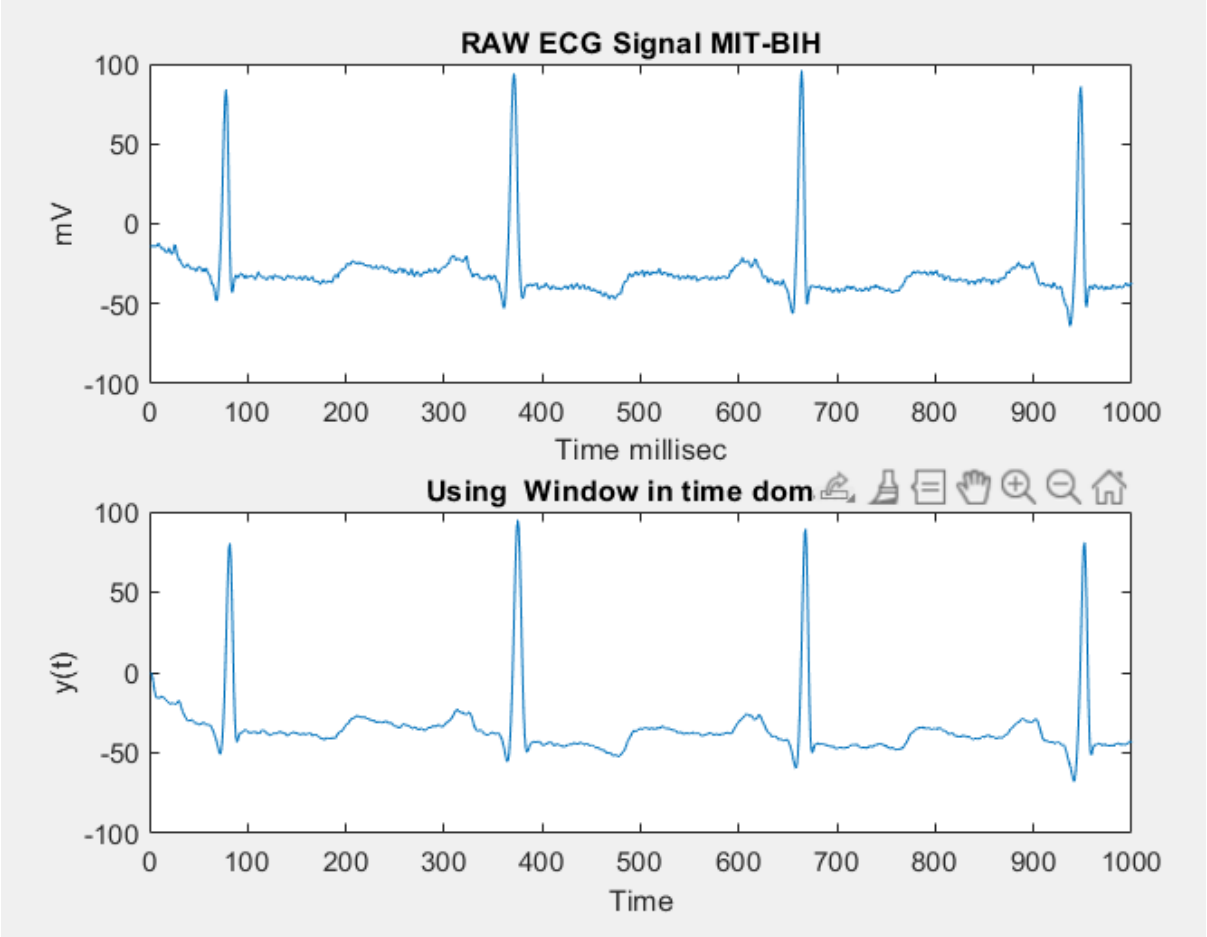
RESULTS &COMPARISION :

TYPES	STRUCTURE	POWER	I/O PORTS
Direct form 1	Unfolded structure using continuous assignment	0.134 W	9%
Direct form 1	Unfolded structure using always & single state without input	0.132 W	7%
Direct form 1	Folded structure using continuous assignment	0.132 W	6%
Direct form 1	Folded structure using always, a single state without input	0.133 W	6%
Transpose form	Pipelined structure with continuous assignment	0.132 W	6%

After executing the .txt file from the Verilog test bench in Matlab, the result exactly matched the Matlab output







Below is the Matlab convolved output using inbuilt convolution function

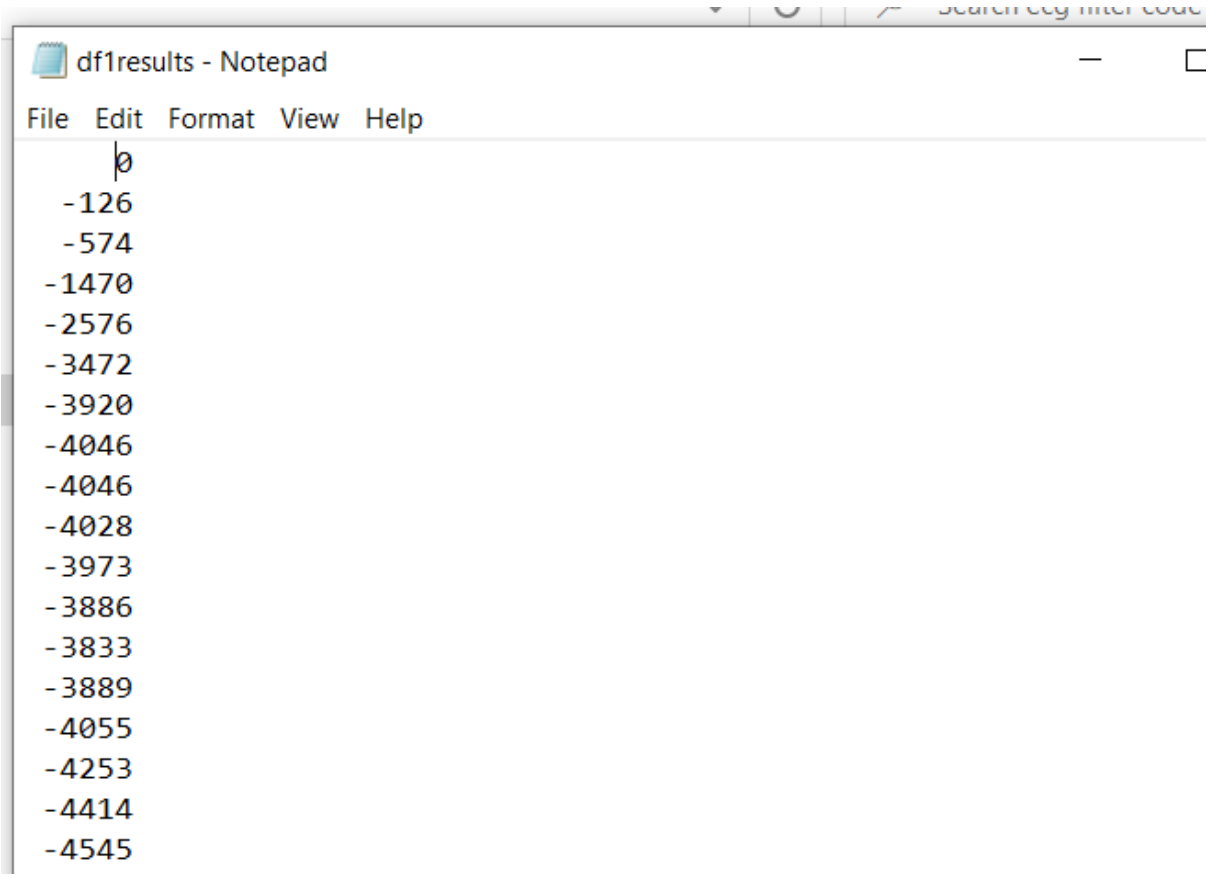
Command Window

```
h =

     0     9    32    64    79    64    32     9     0


y0 =

  Columns 1 through 9

          0        -126        -574       -1470       -2576       -3472       -3920       -4046       -4046

  Columns 10 through 18

      -4028       -3973       -3886       -3833       -3889       -4055       -4253       -4414       -4545

  Columns 19 through 27

      -4697       -4872       -4988       -4983       -4890       -4846       -4931       -5070       -5081

  Columns 28 through 36

      -4878       -4590       -4482       -4722       -5226       -5785       -6241       -6591       -6895

  Columns 37 through 45

      -7193       -7455       -7639       -7703       -7657       -7564       -7526       -7605       -7771

  Columns 46 through 54

      -7937       -8042       -8092       -8142       -8220       -8290       -8273       -8156       -8022
```

COMPARE THE MATLAB OUTPUT AND VERILOG OUTPUT

```
         0        -126        -574       -1470       -2576       -3472       -3920       -4046       -4046

Columns 10 through 18

     -4028       -3973       -3886       -3833       -3889       -4055       -4253       -4414       -4545

Columns 19 through 27

     -4697       -4872       -4988       -4983       -4890       -4846       -4931       -5070       -5081
```

“df1results.txt”



” BOTH THE RESULTS ARE MATCHING”

^THANK YOU FOR YOUR GUIDANCE, Meenali Janveja Mam ^1000