Sri Krishna College of Engineering & Technology

SRI KRISHNA INSTITUTIONS COIMBATORE

Department of Electrical and Electronics Engineering

18EE501-POWER ELECTRONICS

Module I- DC to DC Converter

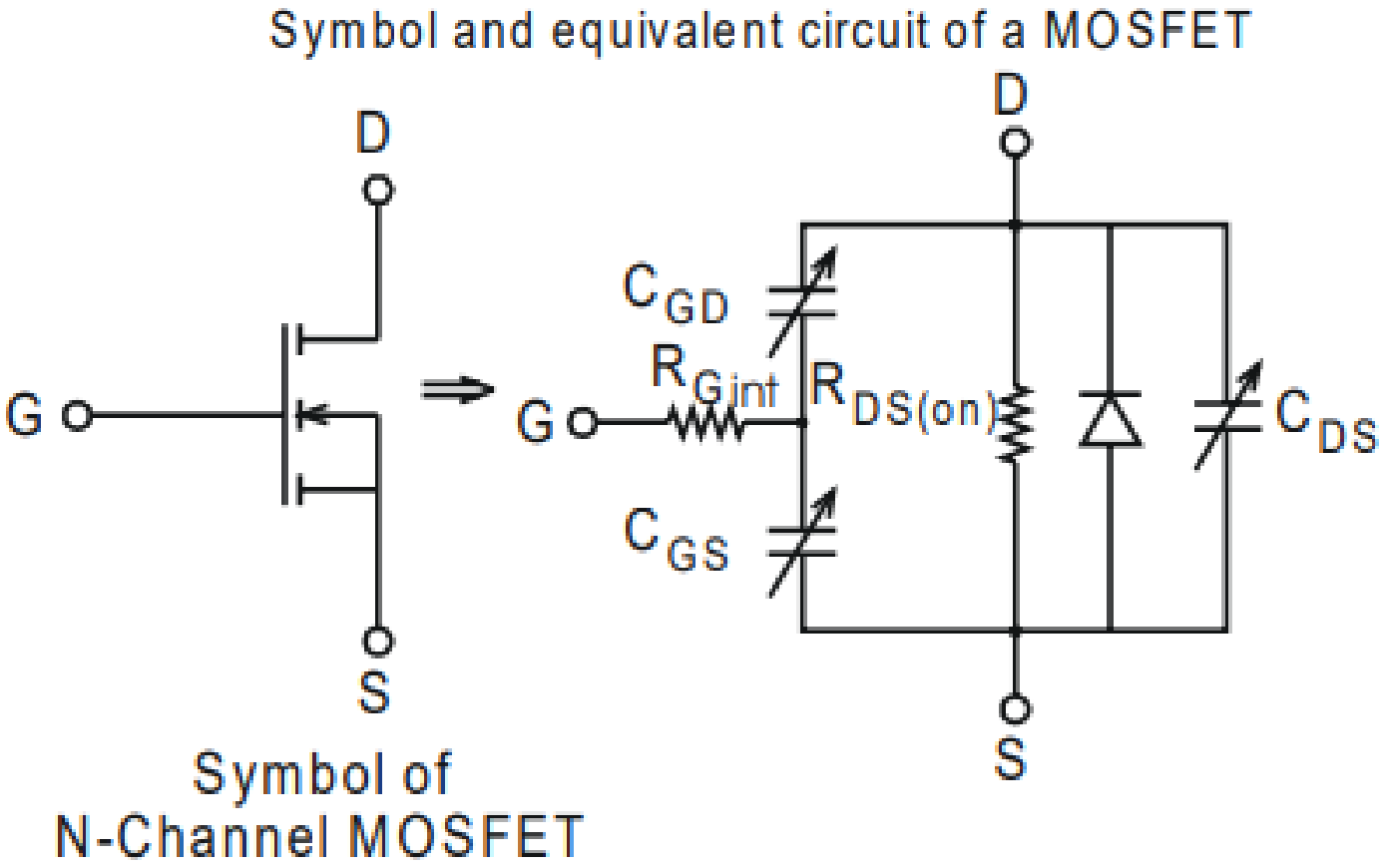
Topic- 1.2 Protection and Gate Drive Circuits

Introduction

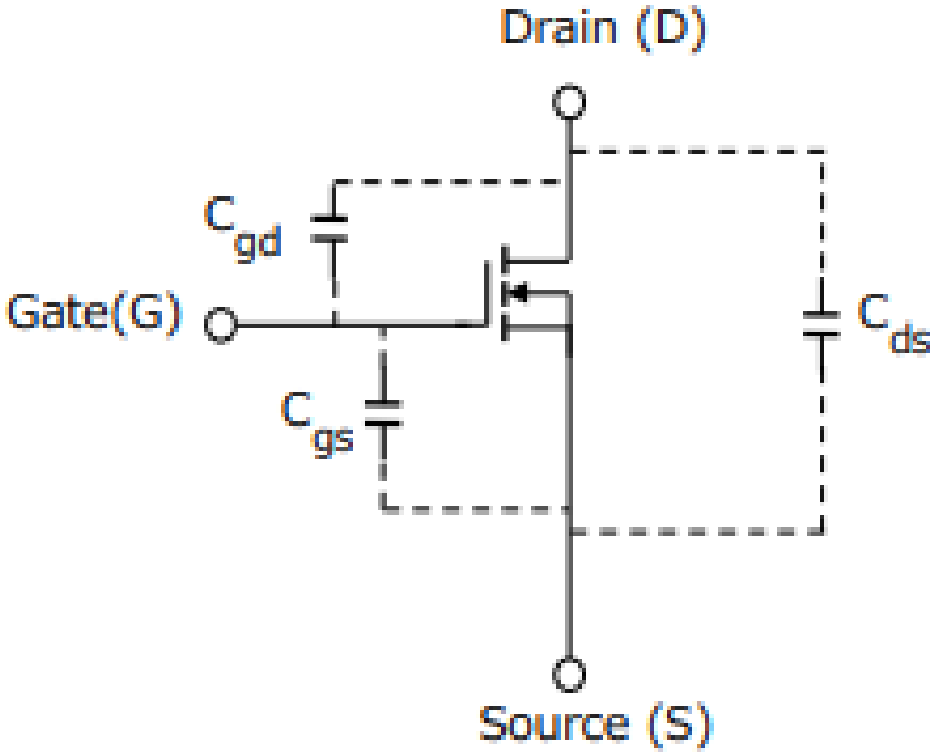
- MOSFET Gate Driver is a specialized circuit that is used to drive the gate of power MOSFETs effectively and efficiently in high-speed switching applications.

MOSFET

- It is the key component in high frequency, high efficiency switching applications across the electronics industry.
- It must be driven from a low impedance source capable of sourcing and sinking sufficient current to provide for fast insertion and extraction of the controlling charge



N-Channel MOSFET and an equivalent model of the same with three inter-junction parasitic capacitances, namely: CGS, CGD and CDS



Input capacitance $C_{iss} = C_{gd} + C_{gs}$

Output capacitance $C_{oss} = C_{ds} + C_{gd}$

Reverse Transfer capacitance $C_{rss} = C_{gd}$

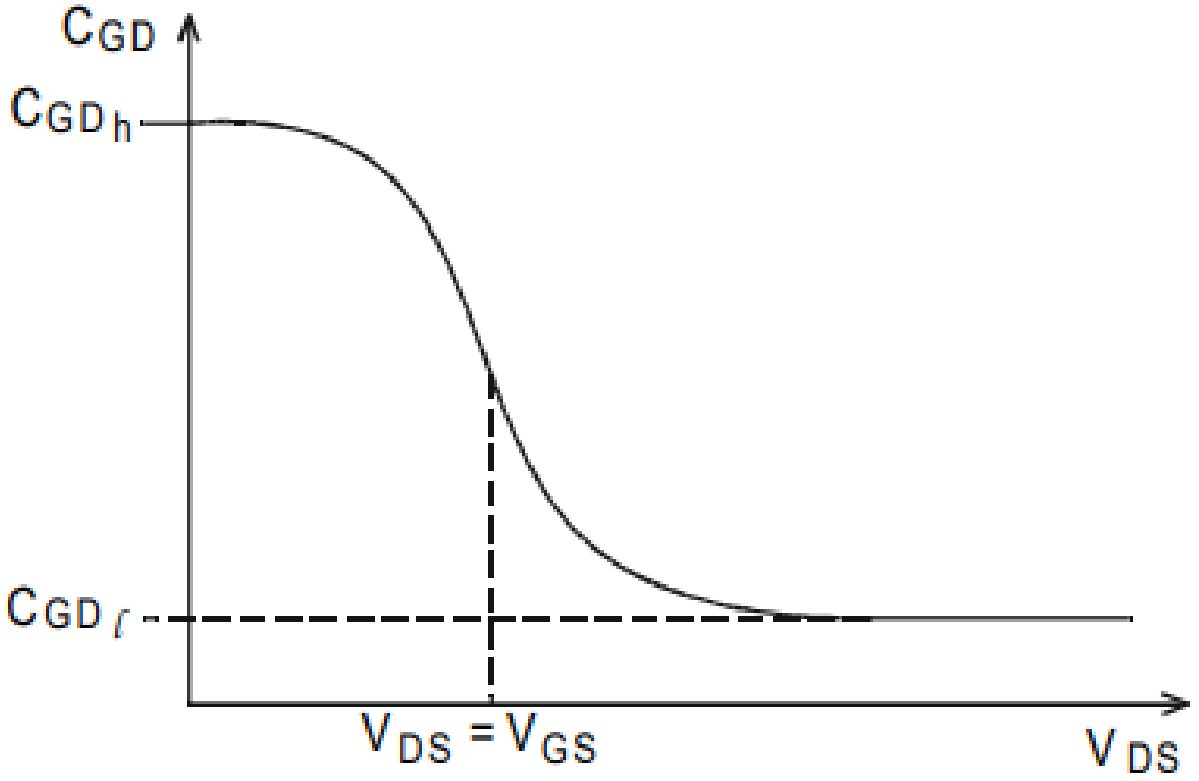


Fig. (3B) C_{GD} variation with respect to V_{DS}

the CGD, decreases rapidly as the Drain to Source voltage rises, as shown in Fig

the high value of CGD is called CGDh, while the low value of CGD is termed CGDl.

- To understand Turn-on and Turn-off phenomena of the Power MOSFET, we will assume clamped inductive switching as it is the most widely used mode of operation.
- This is shown in Fig. (4A) and Fig. (4B).
- A model of MOSFET is shown with all relevant components, which play a role in turn-on and turn-off events.
- As stated above, MOSFET's Gate to Source Capacitance CGS needs to be charged to a critical voltage level to initiate conduction from Drain to Source.

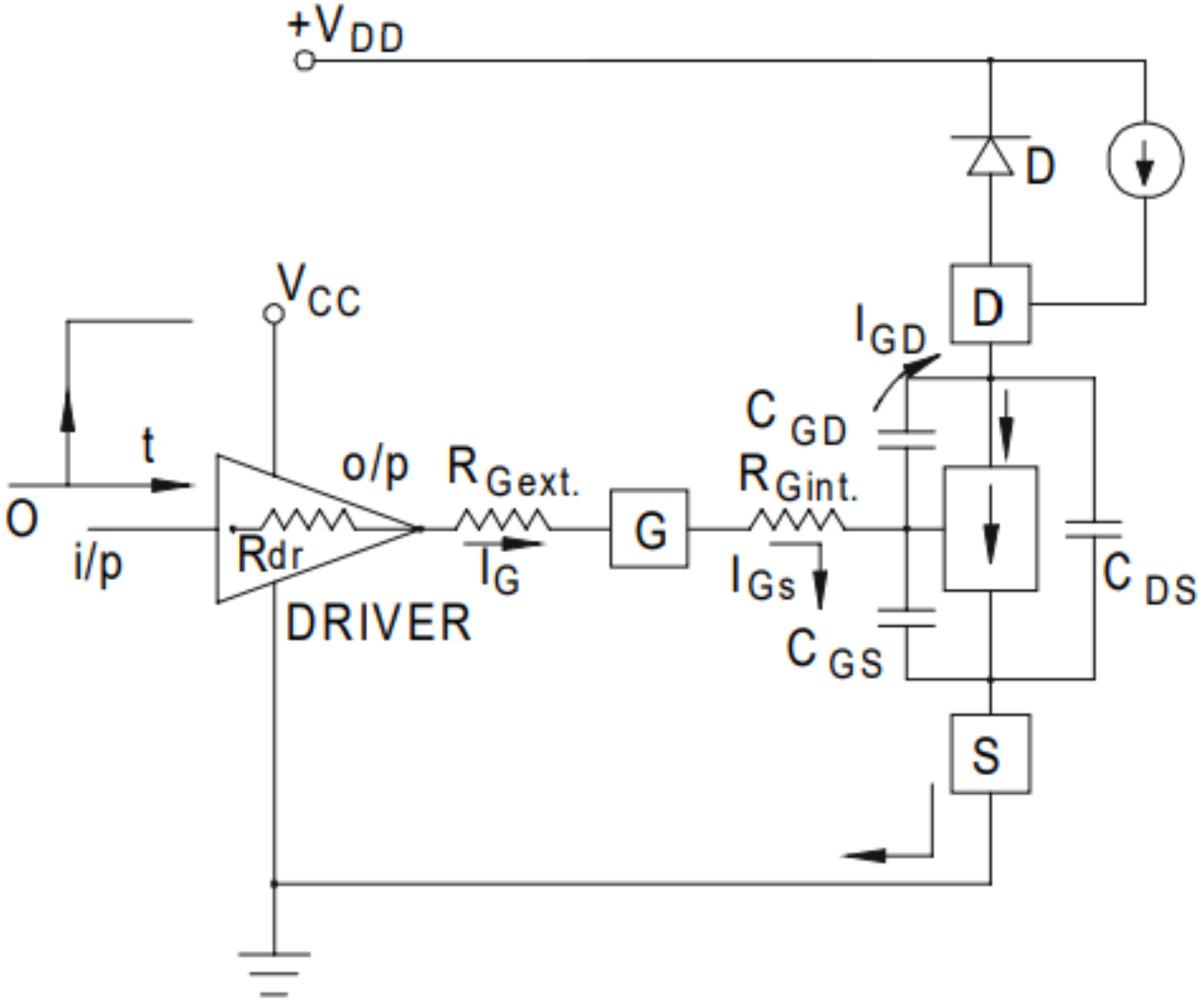


Fig (4A) A MOSFET being turned on by a driver in a clamped inductive load.

- The clamped inductive load is being shown by a current source with a diode D connected antiparallel across the inductor.

- The MOSFET has its intrinsic internal Gate resistance, called RGint. As described above, the inter-junction parametric capacitances (CGS, CGD and CDS) are shown and connected at their proper points.

- VDD represents the DC Bus voltage to the Drain of the MOSFET through the clamped inductive load.

- The Driver is supplied by Vcc of value Vp and its ground is connected to the common ground of VDD and is returned to the Source of the MOSFET.
- The output from the Driver is connected to the Gate of the MOSFET through a resistor RGext.

- Now when a positive going pulse appears at the input terminal of the Driver, an amplified pulse appears at the output terminal of the Driver with an amplitude Vp.

- This is fed to the Gate of the MOSFET through RGext.

- As one can see the rate of rise of voltage, VGS, over Gate and Source terminals of the MOSFET is governed by value of the total resistance in series (Rdr+RGext+RGint) and total effective value of capacitance (CGS+CGD).

- Rdr stands for the output source impedance of the Driver.

- Rgext is the resistance one generally puts in series with the Gate of a MOSFET to control the turn-on and turn-off speed of the MOSFET.

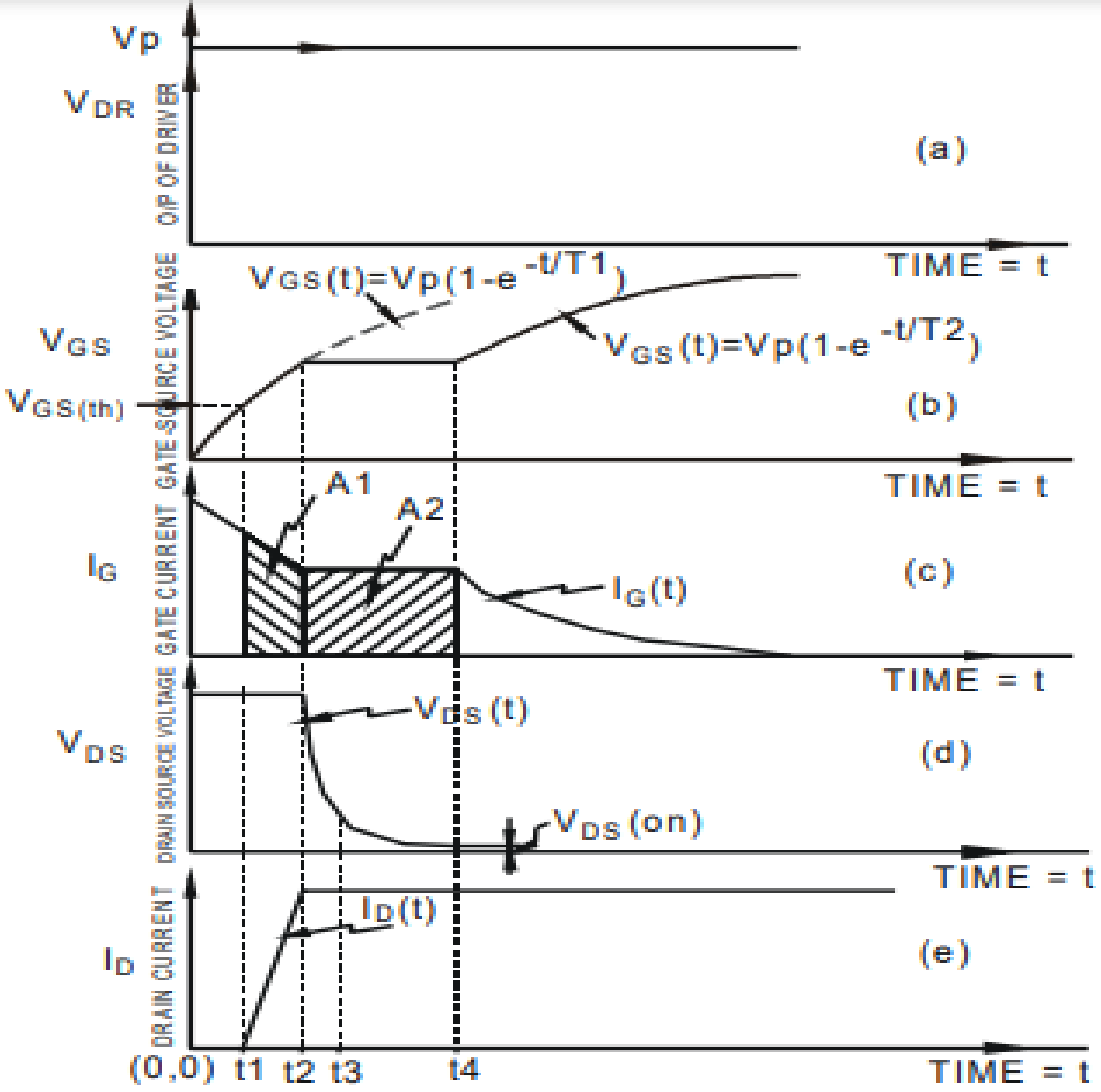


Fig. (5) MOSFET turn on sequence

The waveforms drawn in Fig. (5) show variation of different parameters with respect to time, so as to clearly explain the entire turn-on sequence.

- From time zero to t1 , (CGS+CGDl) is exponentially charged with a time constant T1=(Rdr+RGext+RGint)x(CGS+CGDl), until Gate-to-source voltage reaches VGS(th).

- In this time period, neither the Drain voltage nor the Drain current are affected, i.e. Drain voltage remains at VDD and Drain current has not commenced yet.

- This is also termed turn-on delay. Note that between 0 to t1 , as VGS rises, IGS falls exponentially, more or less like a mirror image of VGS, because from the point of view of circuit analysis, it is an RC Circuit.

- After time t1 , as the Gate-to-Source voltage rises above VGS(th), MOSFET enters linear region

- At time t1 , Drain current commences, but the Drain to Source voltage VDS is still at VDD.

- However, after t1 , ID builds up rapidly.

- As can be seen in Fig. (3B), from time t1 to t2 , CGD increases from C GDl to CGDh and current available from the Driver is diverted to charge this increased value of CGDh.

- Between t1 and t2 , the Drain current increases linearly with respect to VGS .

- At time t2 , the Gate to Source voltage enters the Miller Plateau level.

- At time t2 , the Drain voltage begins to fall rapidly, while the MOSFET is carrying full load current.

- During the time interval, t2 to t4 , VGS remains clamped to the same value and so does IGS.

- Beyond t4 , VGS begins to exponentially rise again with a time constant T2 = (Rdr+RGext+RGint)x(CGS+CGDh).

- During this time interval the MOSFET gets fully enhanced, the final value of the VGS determining the effective RDS(on).

- When VGS reaches its ultimate value, VDS attains its lowest value, determined by VDS= IDSx RDS(on) .

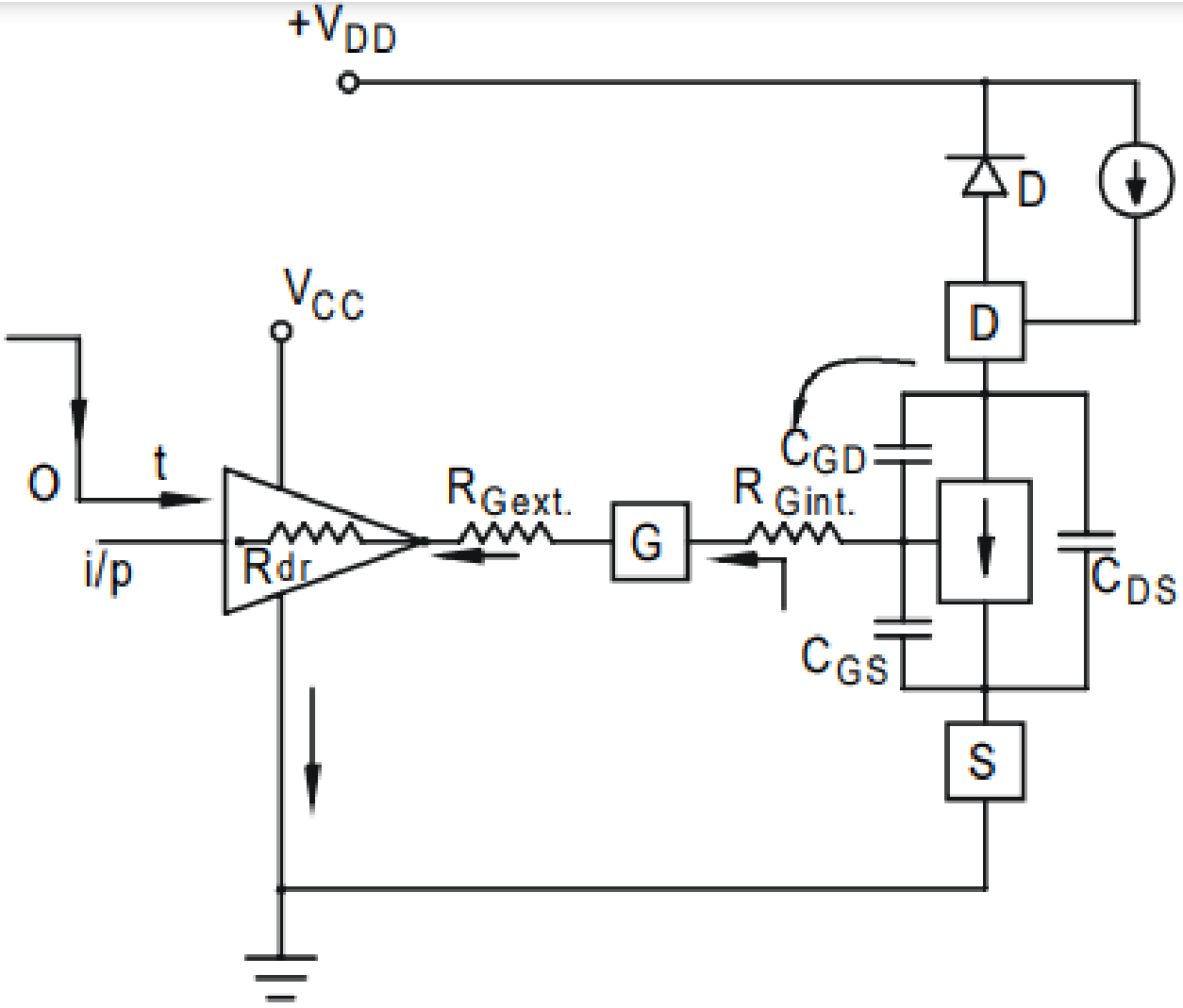


Fig. (4B) A MOSFET being turned off by a driver in a clamped inductive load.

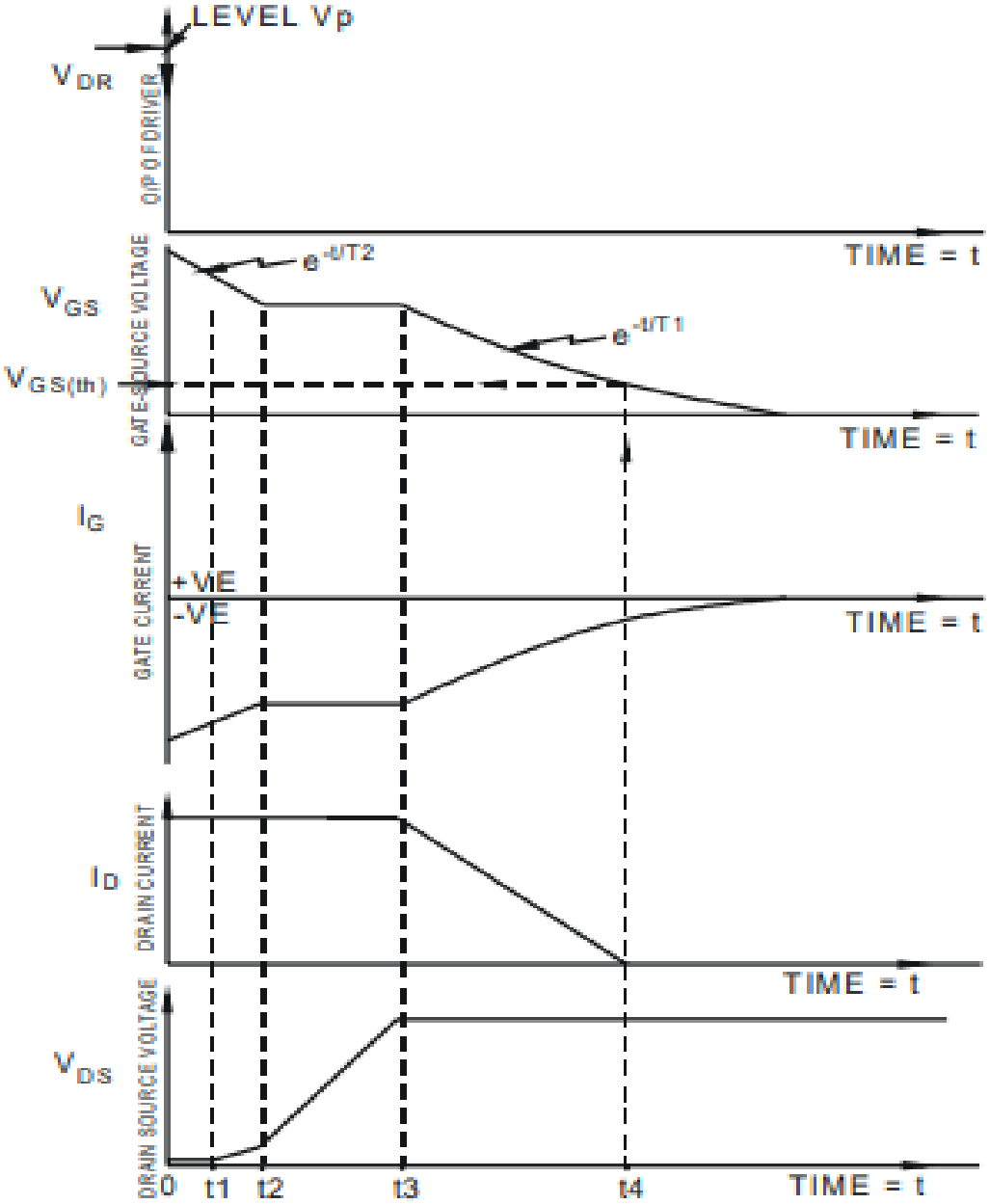


Fig. (7) MOSFET turn off sequence

- The turn-off phenomenon is shown in Fig. (7).

- As can be expected, when the output from the Driver drops to zero for turning off MOSFET, VGS initially decays exponentially at the rate determined by time constant T2= (Rdr+RGext+RGint)x(CGS+CGDh) from time 0 to t1 ;

- however, after t4 , it decays exponentially at the rate determined by T1 = (Rdr+RGext+RGint)x(CGS+CGDl)

- From t = 0 to t = t1 , the gate current is flowing through CGS and CGD capacitances of MOSFET.

- Notice that the drain current ID remains unchanged during this time interval, but the Drain Source voltage VDS just begins to rise.

- From t1 to t2 , VDS rises from ID x RDS(on) towards its final off state value of VDS(off), where it is clamped to the DC Bus voltage level by the diode in the clamped inductive switching circuit being studied.

- This time interval also corresponds to the Miller region as far as the gate voltage is concerned as mentioned above, which keeps VGS constant

- During the next time interval, the VGS begins to fall further below VGS(th).

- CGS is getting discharged through any external impedance between Gate and Source terminals.

- The MOSFET is in its linear region and Drain current ID drops rapidly towards zero value.

- Remember that the Drain Voltage VDS was already at its off state value VDS(off) at the beginning of this interval.

- Thus at t4 , the MOSFET is fully turned off.

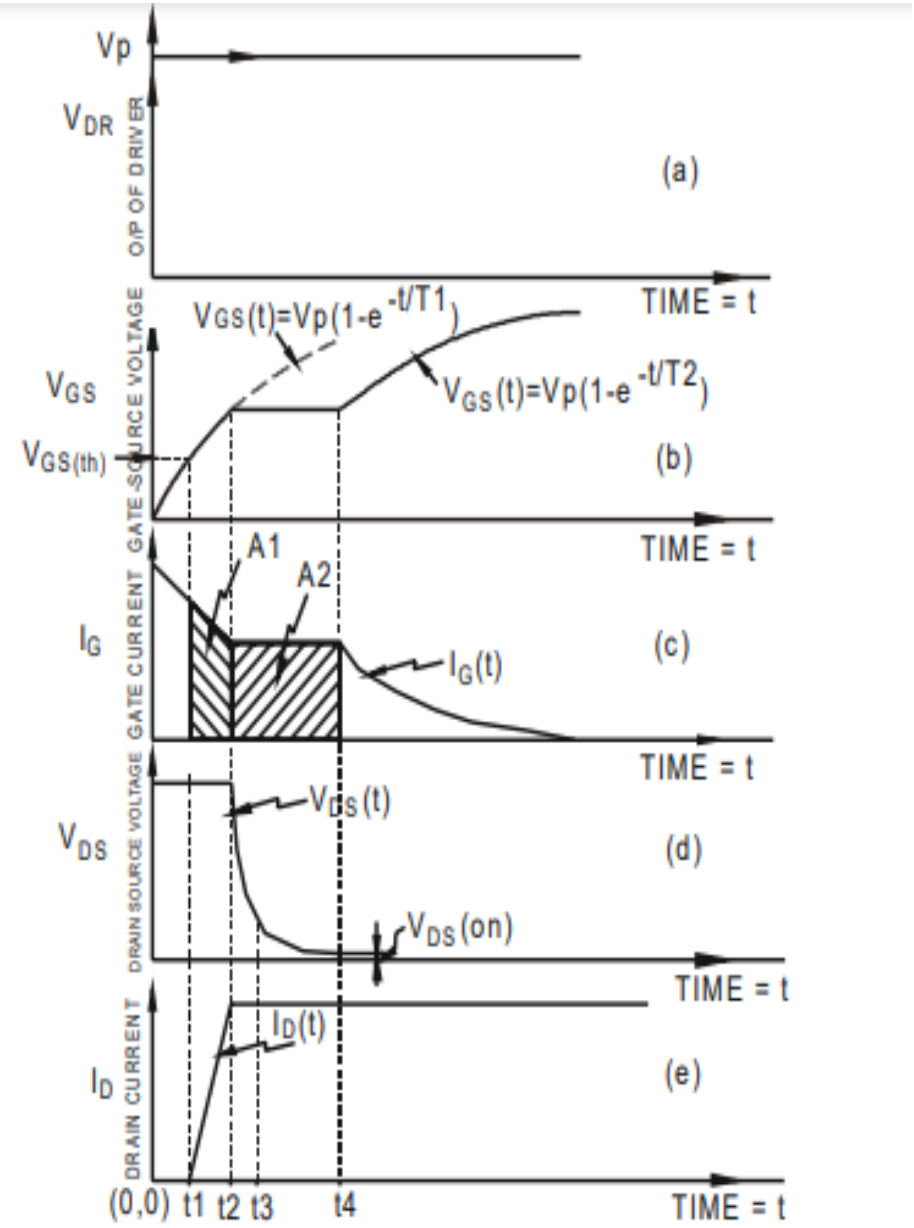


Fig. (5) MOSFET turn on sequence

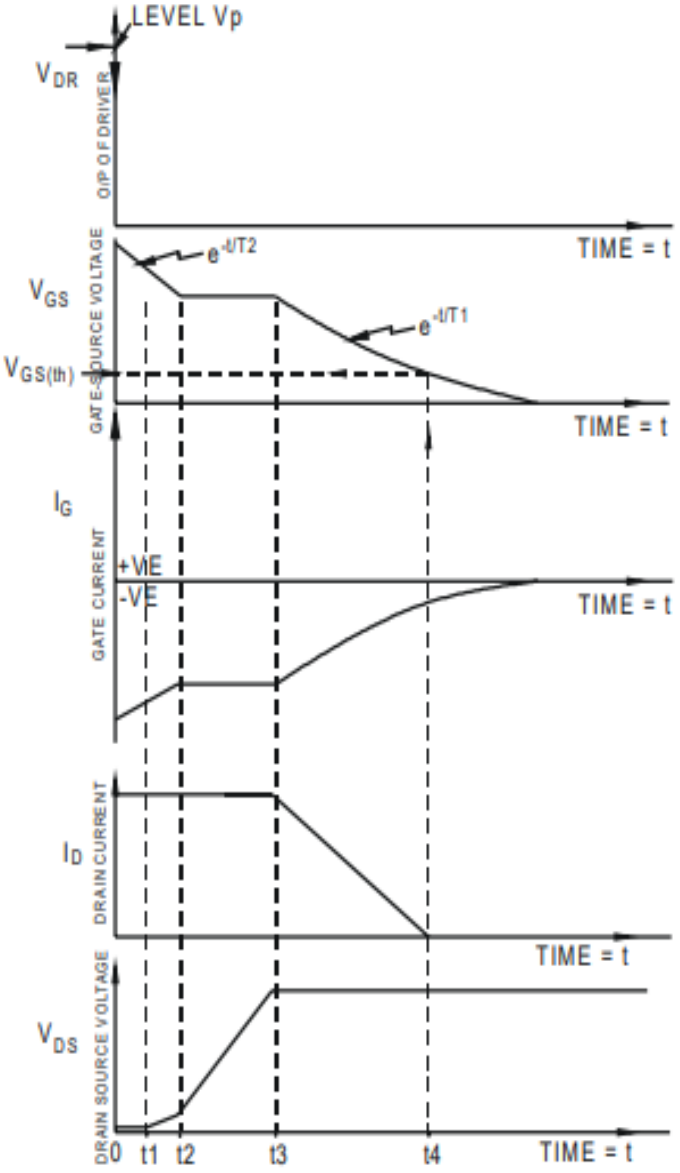


Fig. (7) MOSFET turn off sequence

Protection of Power semiconductor devices (SCR,MOSFET,IGBT,..)

- Power semiconductor devices need protection circuits, which are called snubber circuits, because they have a limited SOA at turn-on and turn-off transitions.
- The objective of snubber is to help the semiconductor device during switching transitions to survive the voltage and current stresses that can cause its failure.
- These stresses are caused by the interruption of the current at turn-off and the collapse of the voltage at turn-on.

Power semiconductor devices commonly protected against:

1. **di/dt**
2. **dv/dt**
3. **Voltage spike or over-voltage**
4. **Over-current**
5. **Gate-under voltage**
6. **Overvoltage at gate**
7. **Excessive temperature rise**
8. **Electro-static discharge**

➢di/dt Protection

- ➢If the rate of rise of anode current, i.e. di/dt is large as compared to the spread velocity of carriers, local hot spots will be formed near the gate connection. This localized heating my destroy the device
- ➢The value of di/dt can be maintained below acceptable limit by using a small inductor, called di/dt inductor in series with the anode circuit.
- ➢Typical di/dt limit value of SCRs are 20-500 A/μ-sec.

➢dv/dt Proctection

- ➢If the rate of rise of suddenly applied voltage across device is high, the device may get turned on. It leads to false operation of the thyristor circuits.
- ➢Typical values of dv/dt are 20-500 V/μ-sec.
- ➢False turn-on of a thyristor by large dv/dt can be prevented by using a snubber circuit in parallel with the device.

Design of Snubber Circuits

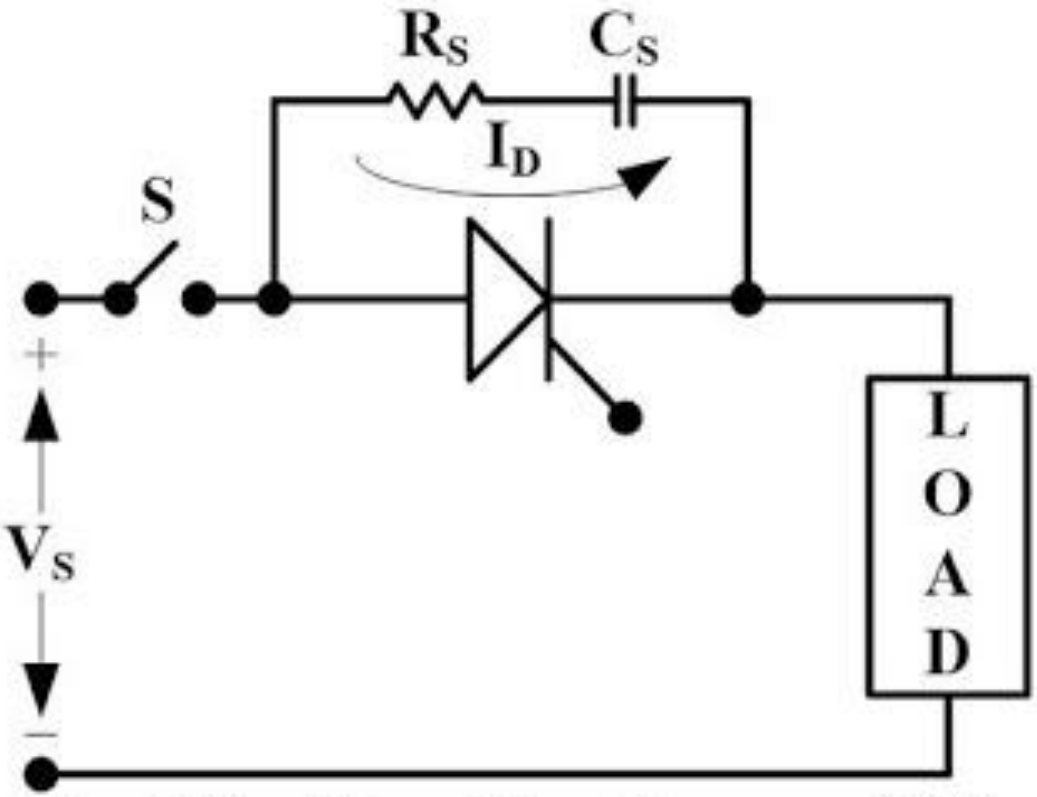


Fig. 1 Snubber Circuit across SCR

- When switch S is closed, a sudden voltage appears across the circuit as given in Fig. 1. Capacitor Cs behaves like a short circuit, Therefore voltage across SCR is zero.

- With the passage of time, Voltage across Cs builds up at a slow rate such that dv/dt across Cs and therefore across SCR is less than the specified maximum dv/dt rating.

- Before SCR is fired by gate pulse, Cs charges to full voltage Vs. When the SCR is turned ON, capacitor discharges through the SCR and sends a current equal to Vs/(Resistance of local path forward by Cs and SCR).

- In order to limit the magnitude of discharge current ID, a resistance Rs is inserted in series with Cs.

- In actual practice, Rs, Cs, and the load circuit parameters should be such that dv/dt across Cs during its charging is less than the specified dv/dt rating of the SCR, and discharge current at the turn ON of SCR is within reasonable limits.

Over-voltage Protection

- Transient over-voltages causes either maloperation of the circuit by unwanted turn-ON of a thyristor or permanent damage to the device due to reverse breakdown. A thyristor may be subjected to internal or external over-voltages.

- Large voltages may be generated internally during the commutation of a thyristor. External over-voltages are caused due to the interruption of current flow in an inductive circuit and also due to lightening strokes on the lines feeding the thyristor system.

- The effect of over-voltages is usually minimized by using RC circuits and non-linear resistors called voltage clamping device (Varistors)

Over-current Protection

- Over-current protection is achieved by the use of circuit breakers (CB) and fast acting fuse.
- A circuit breaker has long tripping time, Therefore generally it is used against surge currents of long duration.
- A fast acting current limiting fuse (FACLF) is used against a large surge currents of very short duration.
- The tripping time of CB and the fusing time of FACLF must be properly coordinated with the rating of device

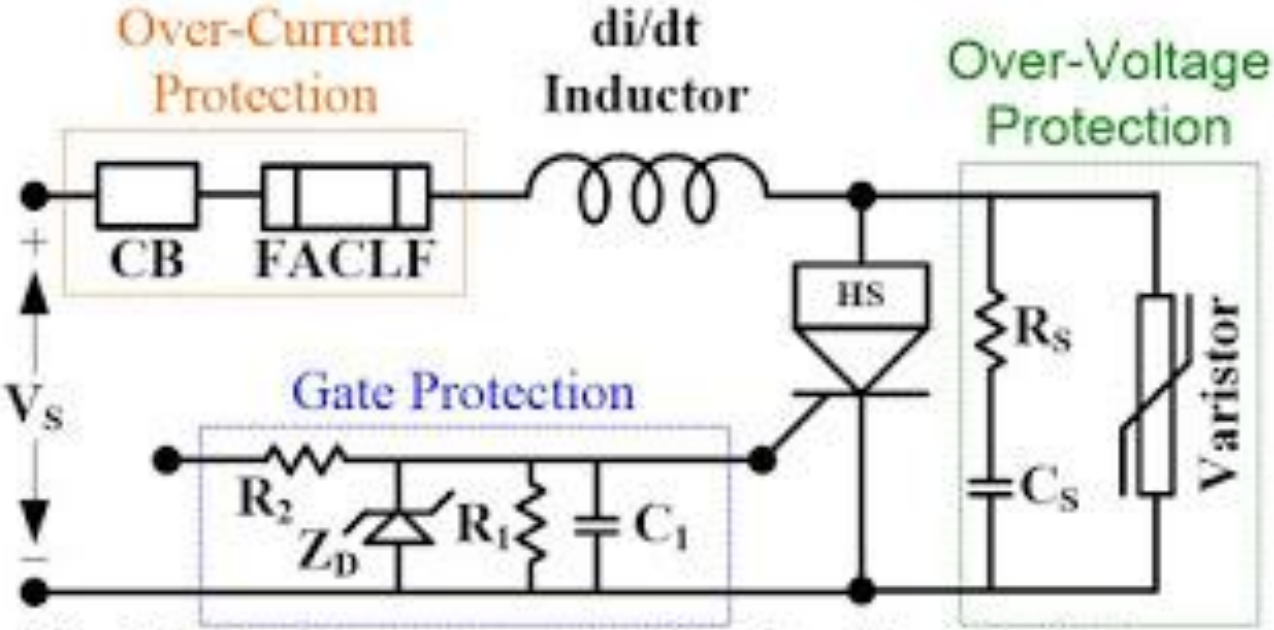


Fig. 3 Circuit components showing the Thyristor protection.

(CB: Circuit Breaker, FACLF: Fast acting current limiting fuse, HS: Heat Sink, and ZD: Zener diode)

Gate Protection

- Over-voltages across the gate circuit can cause false triggering of the SCR, while Over-current may raise junction temperature beyond specified limit leading to its damage.

- Protection against over-voltages is achieved by connecting a zener diode (ZD) across the gate circuit as given in Fig. 3. A resistor R2 connected in series with the gate circuit provides protection against over-currents.

- Protection against undesirable firing is obtained by using shielded cables or twisted gate leads.

- A capacitor and a resistor are also connected across gate to cathode to bypass the noise signals. ($C<0.1\mu F$)

ASSESSMENT

Technical Quiz: Click here

Assignment: Click here


THANK
YOU