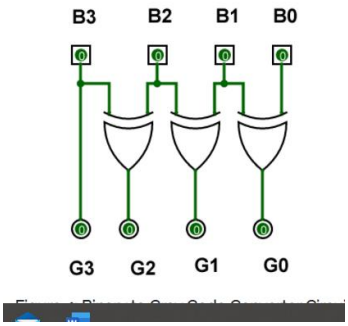
BINARY TO GRAY

$B_3 = G_3$

$B_2 \oplus B_3 = G_2$

$B_1 \oplus B_2 = G_1$

$B_0 \oplus B_1 = G_0$



GRAY TO BINARY

$G_0 \oplus G_1 \oplus G_2 \oplus G_3 = B_0$

$G_1 \oplus G_2 \oplus G_3 = B_1$

$G_2 \oplus G_3 = B_2$

$G_3 = B_3$

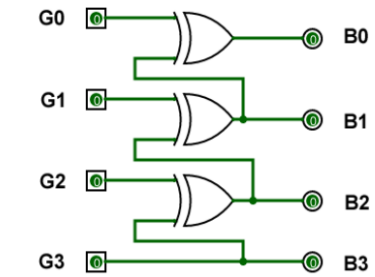


Figure-3: Gray to Binary Code Converter Circuit

Gray code

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

XOR

Natural-binary code

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

XNOR

Conversion from gray to binary:

The Most Significant Bit (MSB) of the binary code is always equal to the MSB of the given binary number.

Other bits of the output binary code can be obtained by checking gray code bit at that index. If current gray code bit is 0, then copy previous binary code bit, else copy invert of previous binary code bit.

Encoders convert 2^N i/p to N o/p.
Building blocks of encoder- OR gate

Decoders convert N i/p to 2^N o/p.
It is convenient to use an AND gate as the basic decoding element for the output because it produces logic "1" output only when all of its inputs are logic "1".

Enable in decoder: Enable allows the decoders outputs to be turned "ON" or "OFF" as required. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0. Only a small change in the implementation is required: the Enable input is fed into the AND gates which produce the outputs.

>>Both are combinational ckts.
>>Decoder IC – 8870
>>NOT IC – 7404
>>OR IC – 7403
>>AND IC – 7408
>>BCD to 7 Segment-Decoding Process
Other ICs:
>>NAND-7400
>>NOR-7402
>>XOR-7486
>>3 I/p NAND-7410

Flip-Flop . is a 1-bit memory cell.
Flip flop is an electronic circuit with two stable states that can be used to store binary data
>>FF is bistable, i.e., can store 1or 0.
>>A group of FFs is a register.
>>0-Reset ; 1- Set; Use next state;

State		Inputs				
Present state	Next state S	R	J	K	D	T
0	0 0	X	0	X	0	0
0	1 1	0	1	X	1	1
1	0 0	1	X	1	0	1
1	1 X	0	X	0	1	0

- JK toggles when J=1,K=1;
- T=1 when Qn+1=Q'
- Sequential Ckt AKA Latch
- Basic latch consists of 2 inverters.

SR(NAND GATE SR):

The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs.

TRUTH TABLE PRINT Add

Serial No.	clock	S	R	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	1	0	1	0	1	Reset
3	1	1	0	0	1	1	0	set
4	1	1	1	1	0	0	0	INVALID

D:

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input.

Why R is inverted?

SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

TRUTH TABLE PRINT Add

Serial No.	clock	D	Q(n-1)	Q'(n-1)	Q	Q'	Remark
1	0	0	X	X	0	1	No Change
2	0	1	0	1	0	1	No change
3	1	0	0	1	0	1	Reset
4	1	1	0	1	1	0	set

JK: In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other to form JK ff.

TRUTH TABLE PRINT Add

Serial No.	clock	J	K	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	0	0	1	0	1	No change
3	1	0	1	0	1	0	1	Reset
4	1	1	0	0	1	1	0	set
5	1	1	1	1	0	0	1	toggle

T: T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change

TRUTH TABLE Add Print

Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	0	1	0	1	0	1	No Change
3	1	0	0	1	0	1	No change
4	1	1	0	1	1	0	Toggle

Race Around Condition In JK Flip-flop

– For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race Around

Condition) can be avoided by ensuring that the clock input is at logic "1" only for a very short time. This introduced the concept of Master Slave JK flip flop.

Master Slave JK flip flop –
The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop. The circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop.

Truth Table : Where inputs are given in all possible combinations and corresponding to the input combination there is one output on right hand side.
Excitation Table : Where Output is given and we have to deduce possible inputs for that output..
Characterisitic Table has the control input (D or T) as the first column, the current state as the middle column, and the next state as the last column and tells us how the control bit affects the current state to produce the next state.

Edge triggered: An edge-triggered is a device in which all the timing requirements have cleverly been subsumed into the clock's falling (usually) edge. During the fall of the clock, the input is isolated, then sampled, then the sampled value is transferred to the output stage.

Clock Signal: In electronics and especially synchronous digital circuits, a **clock signal** (historically also known as logic beat) oscillates between a high and a low state and is used like a metronome to coordinate actions of digital circuits

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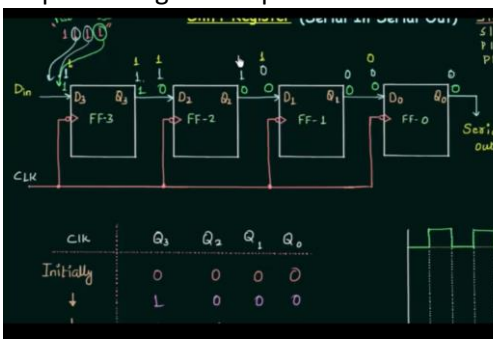
- **Register**- group of ffs to increase storage capacity
- D ff is best for registers.
- **Bound to follow the clock**.

- **Load** is an independent control that allows to store the data for longer than clock pulse's time.
- Data can be entered in the form of:
  Serial form(Temporal code)
  Parallel form(Special code)
- **Fan**-in is a term that defines the maximum number of digital inputs that a single logic gate can accept.
- **fan-out** is the number of gate inputs driven by the output of another single logic gate.

- **Types of registers**:
  >> i/p or o/p
  SISO
  SIPO
  PISO
  PIPO
  >> application
  Shift Reg (SISO)
  Storage Reg (PIPO)

- **SISO**

>ADV: Useful for long distance transmission.
>Shift right mode-
>$D_{in=}$ MSB<-**1** 1 1 1->LSB
>LSB is sent first.
>Every clock pulse triggers the next input
>DISADV: Requires 2x more clock pulses to get the op in order.



- **SIPO**

>No. of clock pulses required = no. of bits = no. of ffs
>After the last bit is transferred, the op is taken out of each D-ff.

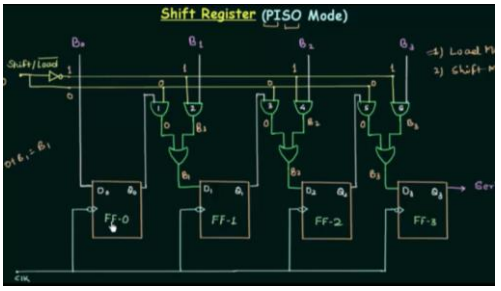
- **PIPO**

>Storage Reg/ Buffer Reg.
>ADV: Requires on 1 clk pulse to store the data. Vv fast.
>I/p data when Clk=1, and make clk=0 when i/p is done. Then value is stored.
>When i/p changed for next clk=1, then values are overwritten.

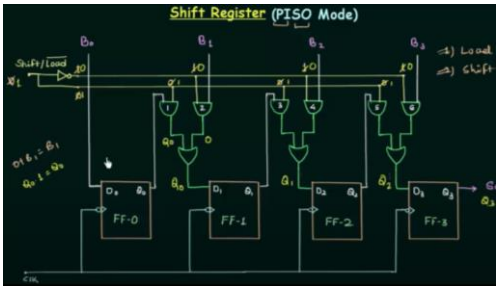
- **PISO**

>Q_{n-1} is connected to D_n via a combinational circuit
>MODES OF WORKING:
Load mode
Shift mode

Load mode:
> Here, Load=0. The combinational ckt ultimately puts in the value of D_{in} bit into D_n, i.e., $D_n=D_{in}$ bit



Shift mode:
>Here, Shift=1. So, via the combinational ckt, Q_{n-1} will be put into D_n, i.e., $D_n=Q_{n-1}$.
Hence shifting of i/p is done and o/p is obtained via serial o/p mode.



- Shifting a binary code to left by one bit = X2
- Shifting a binary code to right by one bit = /2
- **parallel load of a shift register =** all ffs are pre-set with data
- A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as **Universal**

The **SN54/ 74LS95B** is a 4-bit Shift Register with serial and parallel synchronous operating modes.

It has both serial and parallel modes of i/p and o/p.
The mode (SISO/ PIPO) is decided by the Mode control input(S) and two clock input (CP_1) and (CP_2).
When,
S=1
->> CP_2 enabled
->> every ↓ triggers an i/p change
->> Parallel i/p taken from (P_0-P_3) to o/p at (Q_0-Q_3). *[PIPO mode]*
S=0
->> CP_1 enabled
->> every ↓ triggers an i/p change
->> Serial i/p taken from DS to $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ (right shift). *[SISO mode]*

Counters- stores (or displays) the number of times a particular event has taken place.

2 types:

- **Asynchronous-** only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops. Also called RIPPLE counter.

DISADVS:
>high-frequency applications are limited because of internal propagation delays

- **Synchronous-** has one global clock which drives each flip flop so output changes in parallel.

ADVS:
>can operate on higher frequency.
>does not have cumulative delay

- The parallel outputs of a counter circuit represent the **Clock count**
- The maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops is **0 to $2^n - 1$**

Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. The MOD of the Johnson counter is 2n if n flip-flops are used. The main advantage of the Johnson counter counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD.

Ring counter is a type of **counter** composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or "**ring**" structure.

LIST OF EXPERIMENTS:

1. To analyze the truth table of binary to gray and gray to binary converter using combination of NAND gates and to understand the working of binary to gray and gray to binary converter with the help of LEDs display.
2. To analyze the truth table of 4×2 decoder/de-multiplexer using NOT (7404) and AND (7408) logic gate ICs and 2×4 encoder using OR (7403) logic gate IC and to understand the working of 4×2 decoder and 2 * 4 encoder circuit with the help of LEDs display.
3. To verify the truth table and timing diagram of RS, JK, T and D flip-flops by using NAND & NOR gates ICs and analyze the circuit of RS, JK, T and D flip-flops with the help of LEDs display.
4. To analyze the circuit and truth table of 4-bit SIPO (serial input parallel output) shift register by using IC 7474 (D flip flop).
5. Analysis and Synthesis of Multi-bit Sequential Circuits using Shift Registers.
6. To verify the truth table and timing diagram of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter by using JK flip flop ICs and analyze the circuit of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter with the help of LEDs display.

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