ASSIGNMENT-1

CSE-511 COMPUTER ARCHITECTURE

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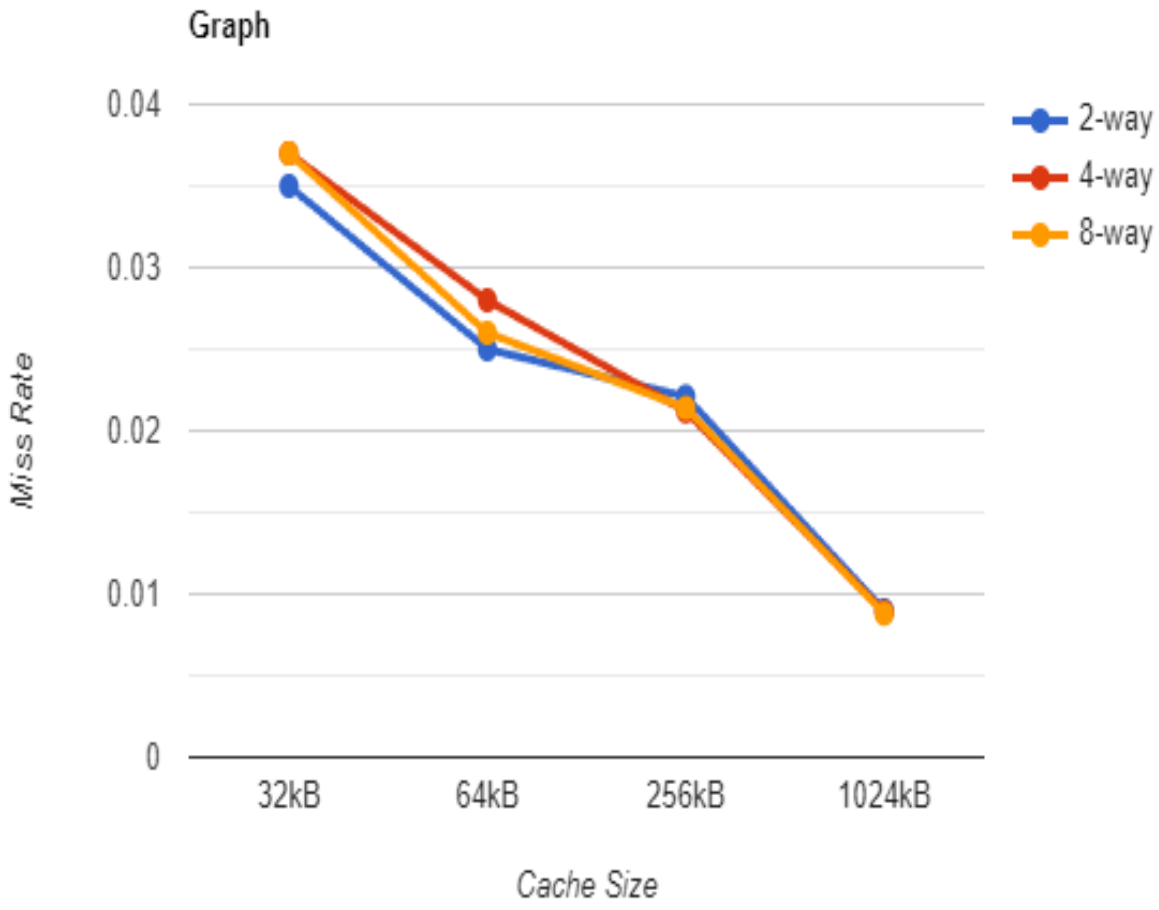

Cache Size	Associativity	Miss Rate
32kB	4	0.037
64kB	2	0.025
64kB	4	0.028
64kB	8	0.026
265kB	2	0.0221
256kB	4	0.0212
1024kB	4	0.0089
1024kB	8	0.0088

Observations:

We can observe that increasing the cache size and associativity helps in reducing the miss rate. Increased associativity, especially for small caches, decrease the number of conflict misses and hence decreases the miss rate. Increasing associativity beyond four-way provides only a small decrease in miss rate. This happens because increasing the cache size will reduce the capacity misses, given the same line size, since more blocks can be accommodated. Higher associativity can be related to the mapping strategy adopted. Since each set will have more blocks, so there's less chance of a conflict between two addresses which both in the same set. We can also recall the 2:1 cache rule, which states that the miss rate of a mapped cache of size N and the miss rate of a 2-way set associative cache of size N/2 are the same.