**Performance Test**

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**Branch: UIC Section /Group : B/2**

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**Subject Name : MICROPROCESSOR AND INTERFACING Subject Code:CAT-352**

1. **Differentiate between the master and slave mode of DMA 8257**

**Ans-**

* **In slave mode, the command word is transferred to 8257 and the status word is transferred from 8257. In master mode, these lines are used to send the high-order byte of the generated address to the latch. This address is further latched using the ADSTB signal.The master and 8257 is in slave mode**
* For verbal exchange among the processor and inner check in of 8257, D7-zero/A15-eight are the bi-directional information traces are used. The enter traces A3-zero are used to pick inner check in of 8257 for verbal exchange with the processor.
* IOR\* and IOW\*are the enter traces of 8257 that the processor reads and writes to the inner registers of 8257.
* The output pins of 8257 are MR\*, MW\*, and A7-, which can be tristate with the aid of using 8257.
* **The hold state and 8257 is in master mode**

**•** D70/A158 lines are used as unidirectional address output lines for sending out the Most Significant Byte of the address from 8257.

• The output lines of 8257 are A30 which are used to send out the Least Significant 4 bits of address in 8257. Output lines of 8257 are A74 which are used to send out the most significant bits in 8257.

• The output pins of 8257 are IOR\*, IOW\*, MR\* and MW\*. If the operation required is DMA read machine cycle the signals MR\* and IOW\* will be activated by 8257. The IOR \* and MW \* signals are inactive. If the required operation is a DMA typewriter cycle, the IOR \* and MW \* signals are asserted by 8257. However, the signals MR \* and IOW \* will be inactive. These are the conditions when the processor remains stopped and the 8257 remains in master mode.

1. **Critically analyze and explain the bit pattern of the accumulator for SIM instruction.**

Ans - In 8085 Instruction set, SIM (Set Interrupt Mask) and RIM (Read Interrupt Mask) instructions can perform mask and unmask RST7. 5, RST6. 5, and RST5. 5 interrupt pins and can also read their status

In 8085 Instruction set, SIM stands for “Set Interrupt Mask”. It is 1Byte instruction and it is a multipurpose instruction. The main uses of SIM instructions are –

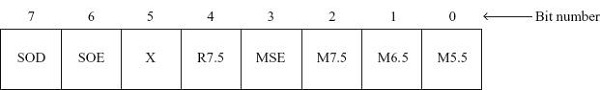
• Masking / unmasking of RST7.5, RST6.5, and RST5.5

• Reset to 0 RST7.5 Flip-flop

• Performs serial output of data

| **Mnemonics, Operand** | **Opcode(in HEX)** | **Bytes** |
| --- | --- | --- |
| SIM | 30 | 1 |

When SIM instruction is executed then the content of the Accumulator decides the action to be taken. So before executing the SIM instruction, it is mandatory to initialize Accumulator with the required value. The meaning and purpose of the various bits of the accumulator when SIM is executed has been depicted below –



Note : that except bit 5, which is a don't care bit, the other bits of the Accumulator decide the effect of executing the SIM instruction. Masking of interrupts: Only the LS 4 bits of the accumulator are used for masking or unmasking of interrupts.

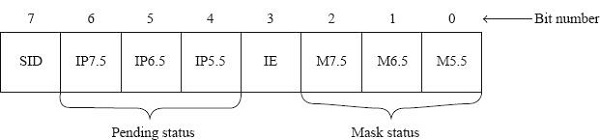
In 8085 Instruction set, **RIM** stands for “Read Interrupt Mask”. It is a 1-Byte multi-purpose instruction. It is used for the following purposes.

* To check whether RST7.5, RST6.5, and RST5.5 are masked or not;
* To check whether interrupts are enabled or not;
* To check whether RST7.5, RST6.5, or RST5.5 interrupts are pending or not;
* To perform serial input of data.

| **Mnemonics, Operand** | **Opcode(in HEX)** | **Bytes** |
| --- | --- | --- |
| RIM | 20 | 1 |

To get the status information about the interrupt system, RIM instruction provides status information about interrupt system and this instruction can be used for serial input of data. Through this RIM instruction, 8085 can know which interrupt is masked or unmasked, etc. The contents of the Accumulator after the execution of the RIM instruction provide this information.

Thus, it is essential to look into the Accumulator contents after the RIM instruction is executed. The meaning of the various bits of the Accumulator after RIM is executed is shown in the following figure –



Mask status of interrupts: The LS 3 bits of the accumulator are used to provide mask status of interrupts. Note that they are not used for masking or unmasking. Masking or unmasking has to be done using the SIM instruction.

1. **Critically analyze and the differentiate between serial data transfer and parallel data transfer.**

**Ans -**

| **Sr. No.** | **Key** | **Serial Transmission** | **Parallel Transmission** |
| --- | --- | --- | --- |
| 1 | Definition | Serial Transmission is the type of transmission in which a single communication link is used to transfer the data from an end to another. | On other hand Parallel Transmission is the transmission in which multiple parallel links are used that transmit each bit of data simultaneously. |
| 2 | Bit transmission | In case of Serial Transmission only one bit is transferred at one clock pulse. | On other hand in case of Parallel Transmission, eight bits transferred at one clock pulse. |
| 3 | Cost Efficient | As single link is used in Serial Transmission, comparatively low cost is required for its implementation hence it is cost efficient. | On other hand multiple links need to be implemented in case of Parallel Transmission hence more cost is required and hence it is not cost efficient. |
| 4 | Performance | As single bit gets transmitted per clock in case of Serial Transmission, its performance is comparatively lower as compared to Parallel Transmission. | However on other hand as already mentioned that 8 bits get transferred per clock in case of Parallel transmission hence it is more efficient in performance. |
| 5 | Preference | As single bit gets transmitted per clock and only single link is implemented in Serial Transmission, it is more preferred for long distance transmission. | However on other hand as multiple bits get transferred and multiple links need to be implemented in case of Parallel Transmission, it is preferred only for short distance. |
| 6 | Complexity | Already mentioned due to single link implementation circuit having Serial Transmission is less complex as compared to that of Parallel Transmission. | However on other hand due to multiple link implementation circuit having Parallel Transmission is more complex as compared to that of Serial Transmission. |