ELL 782
Minor Exam

2020-21 Semester-I

- All questions are 10 marks each.
- Please do not submit hand-written answers or diagrams.
- You are not allowed to copy from each other or from the web.
- This is an open-book, open-internet exam. These sources can be consulted for knowledge and information.
- The question paper has 2 pages
- Submit all your answers as a single pdf document. You can use MS Word of LaTeX to create this document.

1. We know that in an edge sensitive latch, the input signal has to be stable for t_{hold} units of time after the negative edge. Let us consider a pipeline stage between latches L1 and L2. Suppose the output of L1 is *ready* immediately after the negative edge, and almost instantaneously reaches the input of L2 because of a very short path through the logic between latches L1 and L2. In this case, we violate the hold time constraint at L2. How can this situation be avoided?
   [Maximum length: 0.5 pages with 1 diagram]
2. How are the number of pipeline stages, the clock frequency, and the IPC interrelated? What stops us from having a 1000-stage pipeline?
   [Maximum length: 0.5 pages, explain pointwise]
3. Is recursion a desirable feature in programs in the context of the Return Address Stack (RAS)? How can we make the RAS aware of a recursive pattern in the program? Can you propose an optimization for the RAS when our workloads have a lot of recursive function calls.
   [Maximum length: 0.75 pages]
4. Modern BTBs are very large because the program size has increased significantly over the last decade. However, we need fast BTB access times. We would prefer access times that are a fraction of a cycle or at the most 1 cycle. What do we do if we (for example) need to store 512 KB of BTB data, but a 512 KB memory structure takes 5 cycles to access, whereas a 32 KB structure takes just 1 cycle to access?
   [Maximum length: 1 page]

5. Why do we need privileged registers such as *oldPC* and *oldSP*? Design a mechanism that achieves the same purpose without requiring additional privileged registers. Note that this will require a fair amount of additional hardware support and some kind of a software-hardware contract.
   [Maximum length: 1 page with diagrams]
6. Describe the hardware implementation of the free list (used in register renaming). This should include details of implementing the circular queues. [Maximum length: 0.5 pages]