

ELL-782: Computer Architecture

Quiz 1

Time: 1 hour 30 minutes

Maximum Marks 30

Q1. Consider the following code snippet and select the correct option.

(2 Marks)

```
movh r0, 0xFB12
movh r1, 0x1212
cmp r0, r1
```

1. SimpleRISC does not support these instructions.
2. Flags.GT=0 and Flags.E=0
3. Flags.GT=1 and Flags.E=1
4. Flags.GT=0 and Flags.E=1
5. Flags.GT=1 and Flags.E=0
6. Flags.GT=1 and Flags.E retains the previous value

Q2. Select the correct option to execute the code correctly in a SimpleRisc Pipeline: (3 Marks)

```
add r1, r2, r3
add r4, r1, 3
add r8, r5, r6
add r9, r8, r5
add r10, r11, 12
add r13, r10, 2
```

1.

```
add r1,r2,r3
add r8,r5,r6
add r10,r11,r12
add r4, r1, 3
nop
add r9, r8, r5
add r13, r10, 2
```
2.

```
add r1,r2,r3
add r8,r5,r6
add r10,r11,r12
add r9, r8, r5
add r4, r1, 3
add r13, r10, 2
```

3. add r1,r2,r3
add r8,r5,r6
add r10,r11,r12
nop
add r4, r1, 3
add r9, r8, r5
add r13, r10, 2

4. add r1,r2,r3
add r8,r5,r6
add r10,r11,r12
add r4, r1, 3
add r13, r10, 2
add r9, r8, r5

Q3. Which of the following SimpleRISC codes will find the LCM of two positive numbers:
(3 Marks)

1. mov r1, 12
mov r2, 14
mov r3, 1
mov r4, r1
.loop:
mod r5, r4, r2
cmp r5,0
beq .lcm
add r3,r3,r2
mul r4,r1,r3
b .loop
.lcm:
mov r0,r4

2. mov r1, 12
mov r2, 14
mov r3, 1
mov r4, r1
.loop:
div r5, r4, r2
cmp r5,1
beq .lcm
add r3,r3,1
mul r4,r1,r3
b .loop
.lcm:
mov r0,r4

3. mov r1, 12
mov r2, 14
mov r3, 1
mov r4, r1

```

.loop:
    mod r5, r4, r2
    cmp r5, 0
    beq .lcm
    add r3, r3, 1
    mul r4, r1, r3
    b .loop
.lcm:
    mov r0, r4
4. None of the above

```

Q4. Select the incorrect statement.

(2 Marks)

- A: The stack pointer maintains a pointer to the bottom of the stack.
 B: 'Call' and 'ret' change the PC value.
 C: The performance of a processor is dependent on the manufacturing technology, architecture, and compiler optimizations.
 D: An in-order processor can execute instructions in an order that is not consistent with the program order.
1. Only A
 2. Both A and D
 3. Both A and C
 4. All statements are correct

Q5. Consider the following SimpleRISC code. What is the minimum number of stalls required in this code? Assume that for a 5-stage pipeline, the *beq* instruction is a taken branch and no delayed branches are supported, there is no forwarding and no code rearrangement is allowed?

(3 Marks)

```

add r1, r2, r3
sub r4, r4, r3
mul r2, r1, r2
beq .foo
.next:
    add r5, r2, r1
    ld r6, 8[r5]
    mul r8, r6, r10
    ....
    ....
.foo
    ld r1, 0[r3]
    b .next

```

1. 13
2. 14
3. 12
4. 8

Q6. You are given a 32-bit number 'n' stored in the register 'r0', you need to write a **one-line SimpleRISC code** to set the odd numbered bits from 1 to 16 to zero, and the most significant bits from 16 to 32 to 0. Store the final result in the register 'r1'.

Convention: The LSB is numbered as bit 1 and the MSB is numbered as bit 32.

(2 Marks)

Q.7. Write an iterative program to compute the factorial of a number stored in the register 'r0'. Save the final result in the register 'r1'.

(4 Marks)

Q.8. You are given two programs P1 and P2. For P1, 10% of the instructions have a load-use hazard, and 15% of its instructions are the taken branches. For P2, 20% of the instructions have a load use hazard, and 5% of its instructions are the taken branches. What will be the CPI of the two programs? Assume that the ideal CPI is 1. Assume forwarding. There are no delayed branches.

(3 Marks)

1. CPI of P1=1.4 and CPI of P2=1.4
2. CPI of P1=1.3 and CPI of P2=1.4
3. CPI of P1=1.3 and CPI of P2=1.3
4. None of the above



Q.9. Write a SimpleRISC program to compute x^n , where x and n are the natural numbers. Assume that x is passed through r0, n through r1, and the return value is passed back to the original program via r0.

(4 Marks)

Q.10. Write a SimpleRISC program to test if a number stored in r0 is prime or not. Save the result in r1. If the number is prime, set r1 to 1, otherwise set it to 0.

(4 Marks)