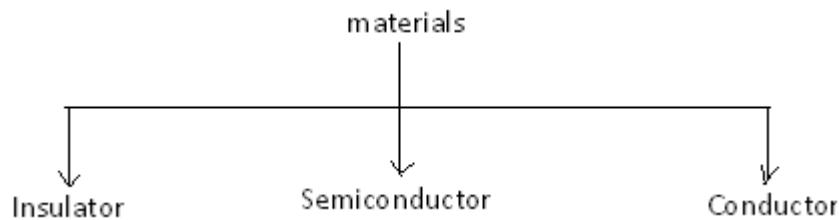


UNIT 1

SEMICONDUCTOR PHYSICS

1.0 INTRODUCTON

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.



Insulator: An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Eg: Paper, Mica, glass, quartz. Typical resistivity level of an insulator is of the order of 10^{10} to $10^{12} \Omega\text{-cm}$. The energy band structure of an insulator is shown in the fig.1.1. Band structure of a material defines the band of energy levels that an electron can occupy. Valance band is the range of electron energy where the electron remain bended too the atom and do not contribute to the electric current. Conduction bend is the range of electron energies higher than valance band where electrons are free to accelerate under the influence of external voltage source resulting in the flow of charge.

The energy band between the valance band and conduction band is called as forbidden band gap. It is the energy required by an electron to move from balance band to conduction band i.e. the energy required for a valance electron to become a free electron.

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$$

For an insulator, as shown in the fig.1.1 there is a large forbidden band gap of greater than 5eV. Because of this large gap there a very few electrons in the CB and hence the conductivity of insulator is poor. Even an increase in temperature or applied electric field is insufficient to transfer electrons from VB to CB.

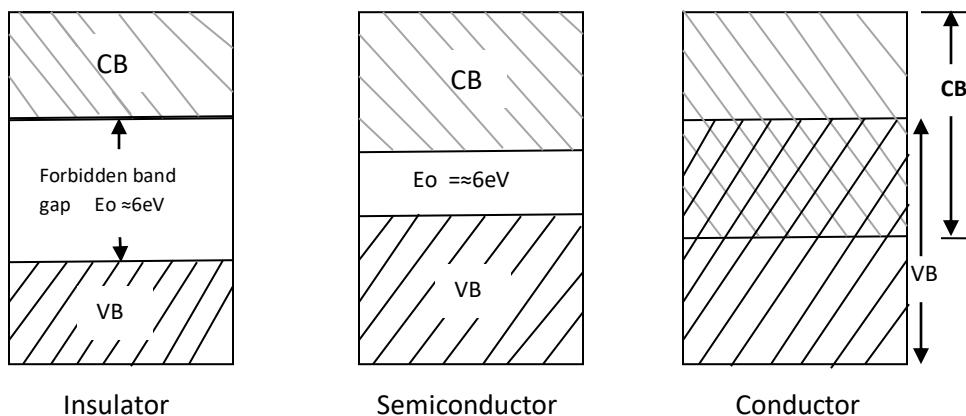


FIG:1.1 Energy band diagrams insulator, semiconductor and conductor

Conductors: A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity. Eg: Copper, Aluminum, Silver, Gold. The resistivity of a conductor is in the order of 10^{-4} and 10^{-6} $\Omega\text{-cm}$. The Valance and conduction bands overlap (fig1.1) and there is no energy gap for the electrons to move from valance band to conduction band. This implies that there are free electrons in CB even at absolute zero temperature (0K). Therefore at room temperature when electric field is applied large current flows through the conductor.

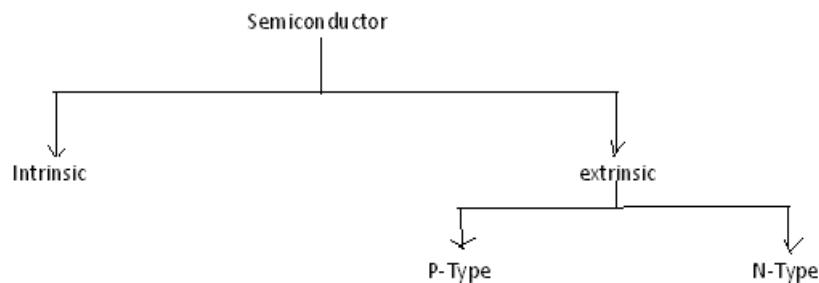
Semiconductor: A semiconductor is a material that has its conductivity somewhere between the insulator and conductor. The resistivity level is in the range of 10 and 10^4 $\Omega\text{-cm}$. Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons. The forbidden band gap is in the order of 1eV. For eg., the band gap energy for Si, Ge and GaAs is 1.21, 0.785 and 1.42 eV, respectively at absolute zero temperature (0K). At 0K and at low temperatures, the valance band electrons do not have sufficient energy to move from V to CB. Thus semiconductors act a insulators at 0K. as the temperature increases, a large number of valance electrons acquire sufficient energy to leave the VB, cross the forbidden bandgap and reach CB. These are now free electrons as they can move freely under the influence of electric field. At room temperature there are sufficient electrons in the CB and hence the semiconductor is capable of conducting some current at room temperature.

Inversely related to the conductivity of a material is its resistance to the flow of charge or current. Typical resistivity values for various materials' are given as follows.

Insulator	Semiconductor	Conductor
$10^{-6} \Omega\text{-cm}$ (Cu)	$50\Omega\text{-cm}$ (Ge)	$10^{12} \Omega\text{-cm}$ (mica)
	$50 \times 10^3 \Omega\text{-cm}$ (Si)	

Typical resistivity values

1.0.1 Semiconductor Types



A pure form of semiconductors is called as intrinsic semiconductor. Conduction in intrinsic sc is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used. Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.

Let us consider the structure of Si. A Si atomic no. is 14 and it has 4 valance electrons. These 4 electrons are shared by four neighboring atoms in the crystal structure by means of covalent bond. Fig.

1.2a shows the crystal structure of Si at absolute zero temperature (0K). Hence a pure SC acts has poor conductivity (due to lack of free electrons) at low or absolute zero temperature.

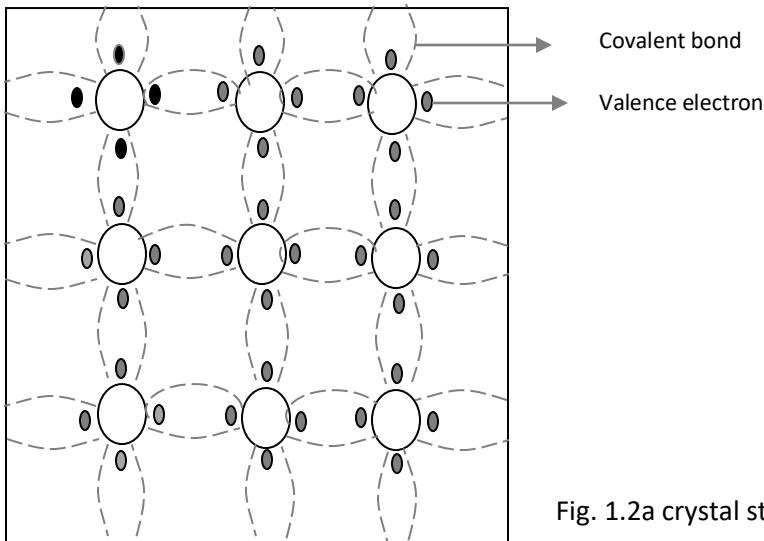


Fig. 1.2a crystal structure of Si at 0K

At room temperature some of the covalent bonds break up to thermal energy as shown in fig 1.2b. The valance electrons that jump into conduction band are called as free electrons that are available for conduction.

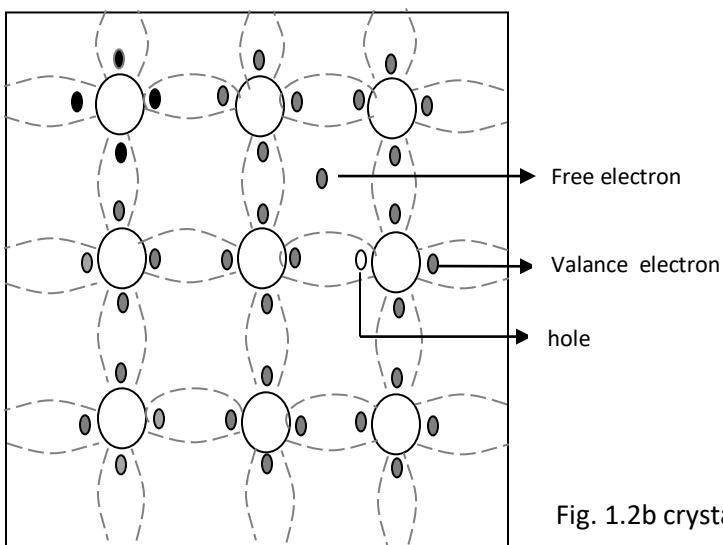


Fig. 1.2b crystal structure of Si at room temperature0K

The absence of electrons in covalent bond is represented by a small circle usually referred to as hole which is of positive charge. Even a hole serves as carrier of electricity in a manner similar to that of free electron.

The mechanism by which a hole contributes to conductivity is explained as follows:

When a bond is incomplete so that a hole exists, it is relatively easy for a valence electron in the neighboring atom to leave its covalent bond to fill this hole. An electron moving from a bond to fill a hole moves in a direction opposite to that of the electron. This hole, in its new position may now be filled by an electron from another covalent bond and the hole will correspondingly move one more step in the direction opposite to the motion of electron. Here we have a mechanism for conduction of electricity which does not involve free electrons. This phenomenon is illustrated in fig1.3

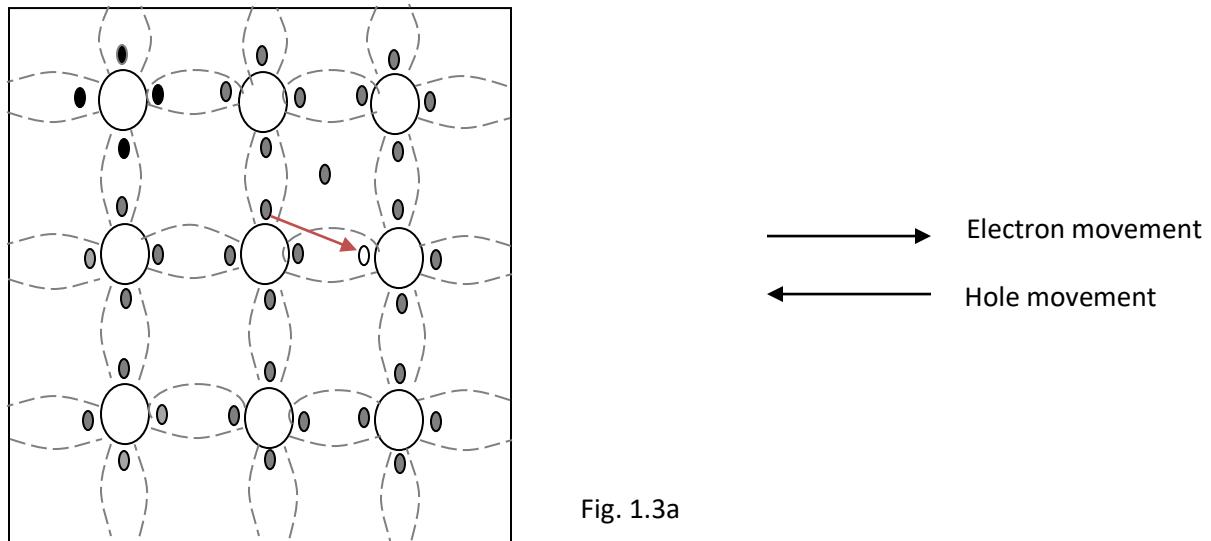


Fig. 1.3a

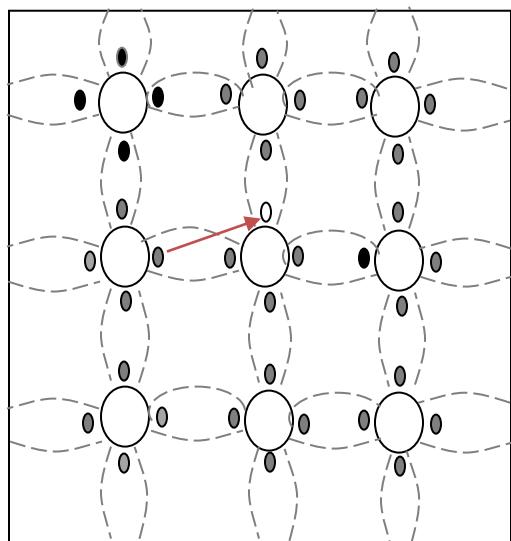


Fig. 1.3b

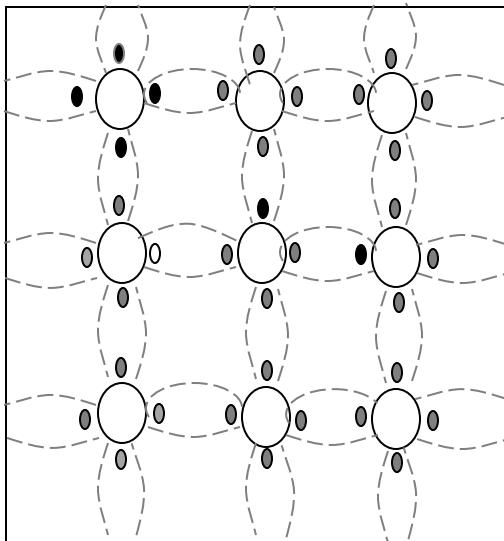


Fig. 1.3c

Fig 1.3a show that there is a hole at ion 6. Imagine that an electron from ion 5 moves into the hole at ion 6 so that the configuration of 1.3b results. If we compare both fig1.3a &fig 1.3b, it appears as if the hole has moved towards the left from ion6 to ion 5. Further if we compare fig 1.3b and fig 1.3c, the hole moves from ion5 to ion 4. This discussion indicates the motion of hole is in a direction opposite to that of motion of electron. Hence we consider holes as physical entities whose movement constitutes flow of current.

In a pure semiconductor, the number of holes is equal to the number of free electrons.

1.0.2 EXTRINSIC SEMICONDUCTOR:

Intrinsic semiconductor has very limited applications as they conduct very small amounts of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor. By adding impurities it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping. The amount of impurity added is 1 part in 10^6 atoms.

N type semiconductor: If the added impurity is a pentavalent atom then the resultant semiconductor is called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.

A pentavalent impurity has five valance electrons. Fig 1.3a shows the crystal structure of N-type semiconductor material where four out of five valance electrons of the impurity atom(antimony) forms covalent bond with the four intrinsic semiconductor atoms. The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily

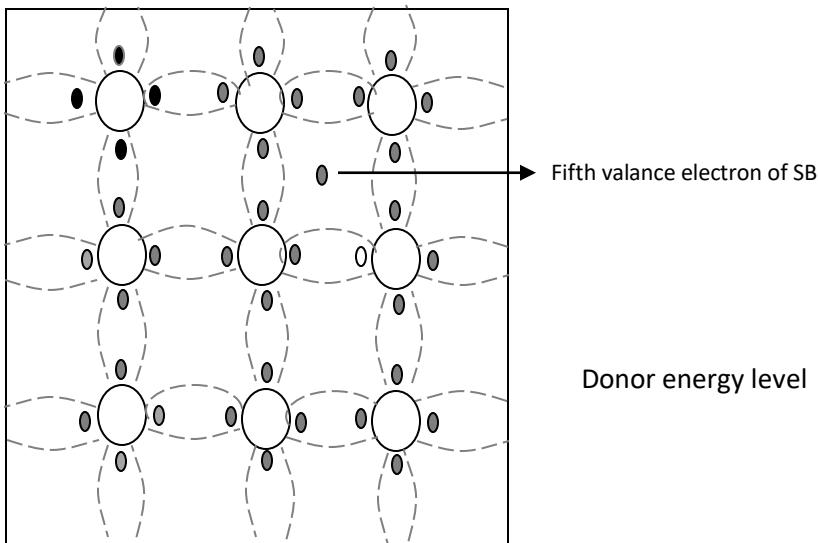


Fig. 1.3a crystal structure of N type SC

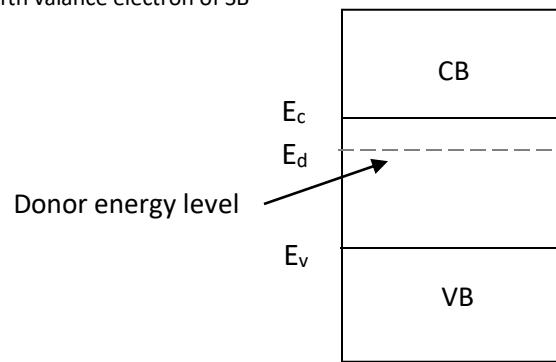


Fig. 1.3b Energy band diagram of N type

excited from the valence band to the conduction band by the application of electric field or increasing the thermal energy. The energy required to detach the fifth electron from the impurity atom is very small of the order of 0.01 eV for Ge and 0.05 eV for Si.

The effect of doping creates a discrete energy level called donor energy level in the forbidden band gap with energy level E_d slightly less than the conduction band (fig 1.3b). The difference between the energy levels of the conducting band and the donor energy level is the energy required to free the fifth valence electron (0.01 eV for Ge and 0.05 eV for Si). At room temperature almost all the fifth electrons from the donor impurity atom are raised to conduction band and hence the number of electrons in the conduction band increases significantly. Thus every antimony atom contributes to one conduction electron without creating a hole.

In the N-type sc the no. of electrons increases and the no. of holes decreases compared to those available in an intrinsic sc. The reason for decrease in the no. of holes is that the larger no. of electrons present increases the recombination of electrons with holes. Thus current in N type sc is dominated by electrons which are referred to as majority carriers. Holes are the minority carriers in N type sc

P type semiconductor: If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium , indium etc.

The crystal structure of p type sc is shown in the fig1.3c. The three valence electrons of the impurity (boon) forms three covalent bonds with the neighboring atoms and a vacancy exists in the fourth bond giving rise to the holes. The hole is ready to accept an electron from the

neighboring atoms. Each trivalent atom contributes to one hole generation and thus introduces a large no. of holes in the valence band. At the same time the no. electrons are decreased compared to those available in intrinsic sc because of increased recombination due to creation of additional holes.

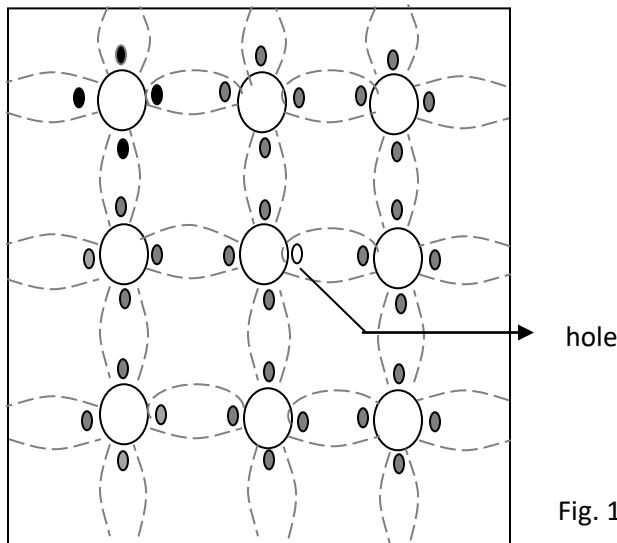


Fig. 1.3c crystal structure of P type sc

Thus in P type sc , holes are majority carriers and electrons are minority carriers. Since each trivalent impurity atoms are capable accepting an electron, these are called as acceptor atoms. The following fig 1.3d shows the pictorial representation of P type sc

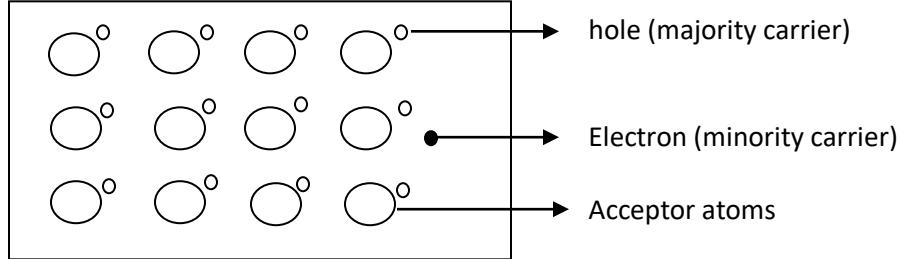


Fig. 1.3d crystal structure of P type sc

- The conductivity of N type sc is greater than that of P type sc as the mobility of electron is greater than that of hole.
- For the same level of doping in N type sc and P type sc, the conductivity of an Ntype sc is around twice that of a P type sc

1.0.3 CONDUCTIVITY OF SEMICONDUCTOR:

In a pure sc, the no. of holes is equal to the no. of electrons. Thermal agitation continue to produce new electron- hole pairs and the electron hole pairs disappear because of recombination. with each electron hole pair created , two charge carrying particles are formed .

One is negative which is a free electron with mobility μ_n . The other is a positive i.e., hole with mobility μ_p . The electrons and hole move in opposite direction in a an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within the intrinsic sc is given by

$$\begin{aligned} J &= J_n + J_p \\ &= q n \mu_n E + q p \mu_p E \\ &= (n \mu_n + p \mu_p)qE \\ &= \sigma E \end{aligned}$$

Where n=no. of electrons / unit volume i.e., concentration of free electrons

P= no. of holes / unit volume i.e., concentration of holes

E=applied electric field strength, V/m

q= charge of electron or hole I n Coulombs

Hence, σ is the conductivity of sc which is equal to $(n \mu_n + p \mu_p)q$. he resistivity of sc is reciprocal of conductivity.

$$P = 1/\sigma$$

It is evident from the above equation that current density with in a sc is directly proportional to applied electric field E.

For pure sc, $n=p=n_i$ where n_i = intrinsic concentration. The value of n_i is given by

$$n_i^2 = AT^3 \exp(-E_{GO}/KT)$$

$$\text{therefore, } J = n_i (\mu_n + \mu_p) q E$$

$$\text{Hence conductivity in intrinsic sc is } \sigma = n_i (\mu_n + \mu_p) q$$

Intrinsic conductivity increases at the rate of 5% per $^{\circ}\text{C}$ for Ge and 7% per $^{\circ}\text{C}$ for Si.

Conductivity in extrinsic sc (N Type and P Type):

The conductivity of intrinsic sc is given by $\sigma = n_i (\mu_n + \mu_p) q = (n \mu_n + p \mu_p)q$

For N type , $n \gg p$

$$\text{Therefore } \sigma = q n \mu_n$$

For P type , $p \gg n$

Therefore $\sigma = q p \mu_p$

1.0.4 HALL EFFECT:

The Hall coefficient useful for the determination of the charge carriers and type is defined as the ratio of the induced electric field to the product of the current density and the applied magnetic field.

- This effect is also useful for the determination of the magnetic field in most of the magnetometers.

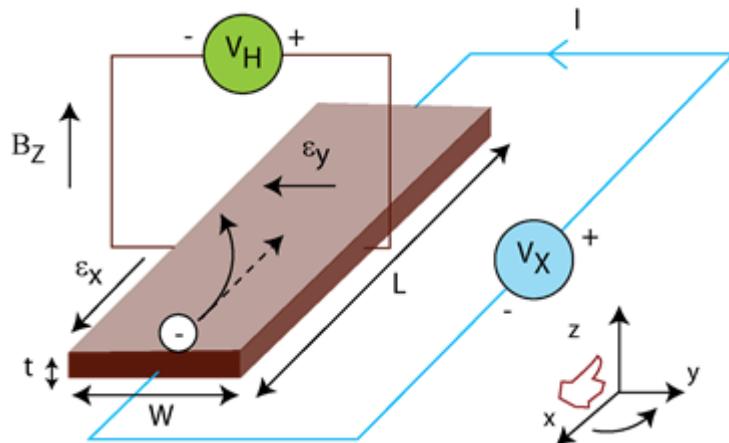


Figure 1.4: Schematic of Hall effect set up.

Consider a rectangular bar with thickness, t , Length L , and width W , as shown in Figure 1.4 and the current I flows through the sample in the presence of magnetic field applied perpendicular to the current direction, i.e., along the thickness direction.

Under this situation, the magnetic field exerts a transverse force on the moving charge carriers, which tends to push them to one side of the sample as shown in the Figure 26.01.

- The buildup of the charges at the sides of the sample will eventually balance the magnetic influence, resulting in a measurable voltage difference between the two sides of the conductor. This is called the Hall Effect.

For a simple metal, where there is only one type of charge carrier, the Hall voltage V_H can be computed by setting net Lorentz force to zero.

$$\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B}) = \mathbf{0} \rightarrow q\mathbf{E} = -\mathbf{v} \times \mathbf{B}$$

$$-\mathbf{B} \times \mathbf{E} = \mathbf{B} \times (\mathbf{v} \times \mathbf{B}) = \mathbf{v} \mathbf{B}^2 - \mathbf{B}(\mathbf{v} \cdot \mathbf{B})$$

The transverse components of this equation are

$$v = E \times B / B^2 \Rightarrow E/B$$

We get

$$V_H = EW = \frac{vBIT}{nLte} = -\frac{IB}{nne}$$

The Hall coefficient can be found as

$$R_H = \frac{E_y}{J_x B} = \frac{V_H t}{IB} = -\frac{1}{ne}$$

The unit of R_H is expressed as m^3/C . This concludes that the type of charge carrier and its density can be estimated from the sign and the value of Hall co-efficient R_H . It can be obtained by studying the variation of V_H as a function of I for a given B.

The above equation also concludes that Hall effect differentiates between positive charges moving in one direction and negative charges moving in the opposite.

1.0.5 CHARGE DENSITIES IN P TYPE AND N TYPE SEMICONDUCTOR:

Mass Action Law:

Under thermal equilibrium for any semiconductor, the product of the no. of holes and the concentration of electrons is constant and is independent of amount of donor and acceptor impurity doping.

$$n.p = n_i^2$$

where n = electron concentration

p = hole concentration

n_i^2 = intrinsic concentration

Hence in N type sc , as the no. of electrons increase the no. of holes decreases. Similarly in P type as the no. of holes increases the no. of electrons decreases. Thus the product is constant and is equal to n_i^2 in case of intrinsic as well as extrinsic sc.

The law of mass action has given the relationship between free electrons concentration and hole concentration. These concentrations are further related by the law of electrical neutrality as explained below.

Law of electrical neutrality:

Sc materials are electrically neutral. According to the law of electrical neutrality, in an electrically neutral material, the magnitude of positive charge concentration is equal to that of negative charge concentration. Let us consider a sc that has N_D donor atoms per cubic centimeter and N_A acceptor atoms per cubic centimeter i.e., the concentration of donor and acceptor atoms are N_D and N_A respectively. Therefore N_D positively charged ions per cubic centimeter are contributed by donor atoms and N_A negatively charged ions per cubic centimeter are contributed by the acceptor atoms. Let n, p is concentration of free electrons and holes respectively. Then according to the law of neutrality

$$N_D + p = N_A + n \quad \dots \dots \dots \text{eq 1.1}$$

For N type sc, $N_A = 0$ and $n \gg p$. Therefore $N_D \approx n$ \dots \dots \dots \text{eq 1.2}

Hence for N type sc the free electron concentration is approximately equal to the concentration of donor atoms. In later applications since some confusion may arise as to which type of sc is under consideration at the given moment, the subscript n or p is added for N type or P type respectively. Hence eq 1.2 becomes $N_D \approx n_n$

Therefore current density in N type sc is $J = N_D \mu_n q E$

And conductivity $\sigma = N_D \mu_n q$

For P type sc, $N_D = 0$ and $p \gg n$. Therefore $N_A \approx p$

$$\text{Or } N_A \approx p_p$$

Hence for P type sc the hole concentration is approximately equal to the concentration of acceptor atoms.

Therefore current density in N type sc is $J = N_A \mu_p q E$

And conductivity $\sigma = N_A \mu_p q$

Mass action law for N type, $n_n p_n = n_i^2$

$$p_n = n_i^2 / N_D \quad \text{since } (n_n \approx N_D)$$

Mass action law for P type, $n_p p_p = n_i^2$

$$n_p = n_i^2 / N_A \quad \text{since } (p_p \approx N_A)$$

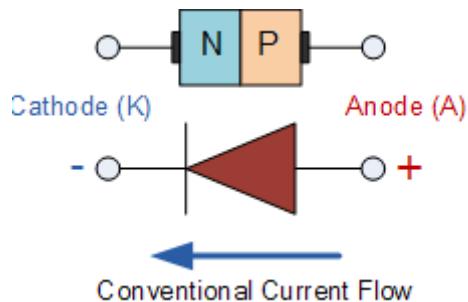
UNIT 2

JUNCTION DIODE CHARACTERISTICS

1.1 QUANTITATIVE THEORY OF PN JUNCTION DIODE:

1.1.1 PN JUNCTION WITH NO APPLIED VOLTAGE OR OPEN CIRCUIT CONDITION:

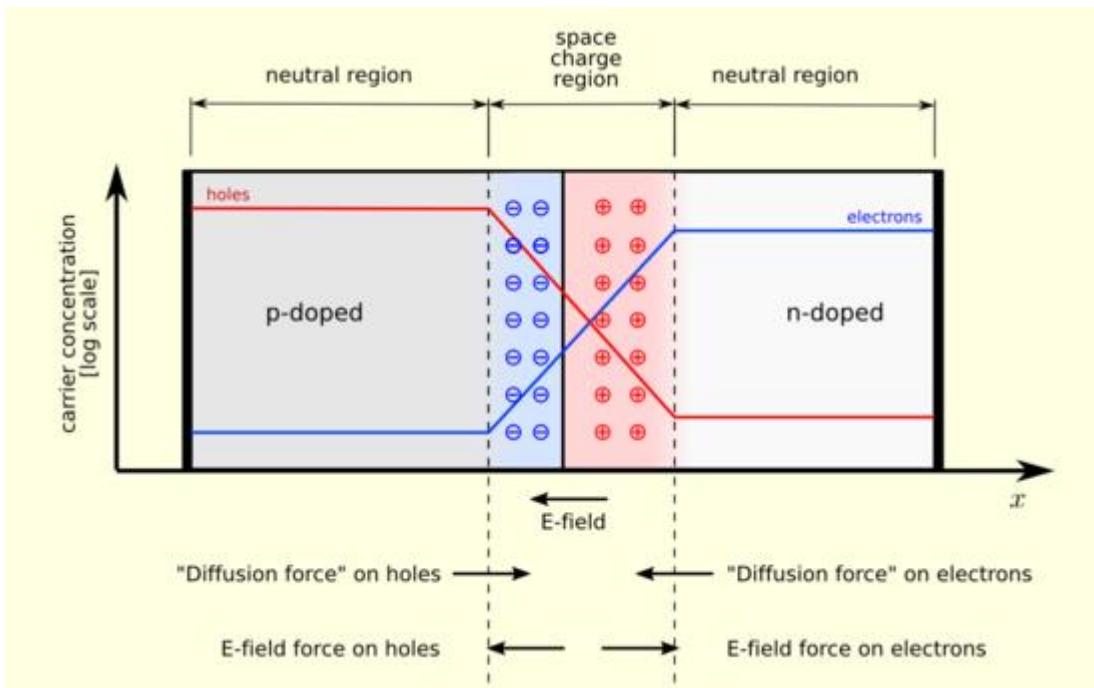
In a piece of semiconductor, if one half is doped by p type impurity and the other half is doped by n type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in the fig the n type material has high concentration of free electrons, while p type material has high concentration of holes. Therefore at the junction there is a tendency of free electrons to diffuse over to the P side and the holes to the N side. This process is called



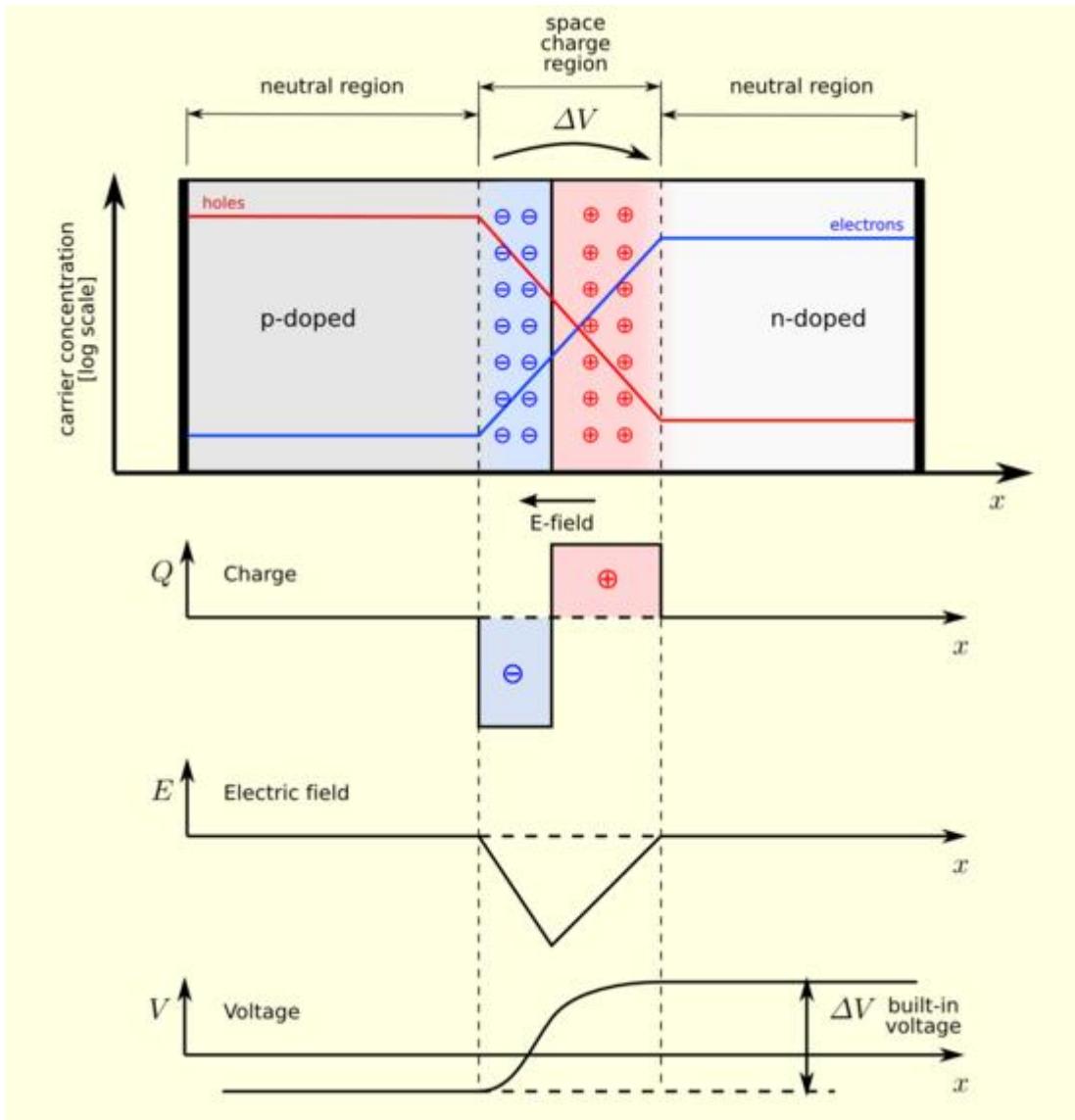
diffusion. As the free electrons move across the junction from N type to P type, the donor atoms become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling the holes. Therefore a negative charge is developed on the p -side of the junction..This net negative charge on the p side prevents further diffusion of electrons into the p side. Similarly the net positive charge on the N side repels the hole crossing from p side to N side. Thus a barrier is set up near the junction which prevents the further movement of charge carriers i.e. electrons and holes. As a consequence of induced electric field across the depletion layer, an electrostatic potential difference is established between P and N regions, which are called the potential barrier, junction barrier, diffusion potential or contact potential, V_o . The magnitude of the contact potential V_o varies with doping levels and temperature. V_o is 0.3V for Ge and 0.72 V for Si.

The electrostatic field across the junction caused by the positively charged N-Type region tends to drive the holes away from the junction and negatively charged p type regions tend to drive the electrons away from the junction. The majority holes diffusing out of the P region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing a

negatives pace charge in a previously neutral region. Similarly electrons diffusing from the N region expose positively ionized donor atoms and a double space charge builds up at the junction as shown in the fig. 1.7



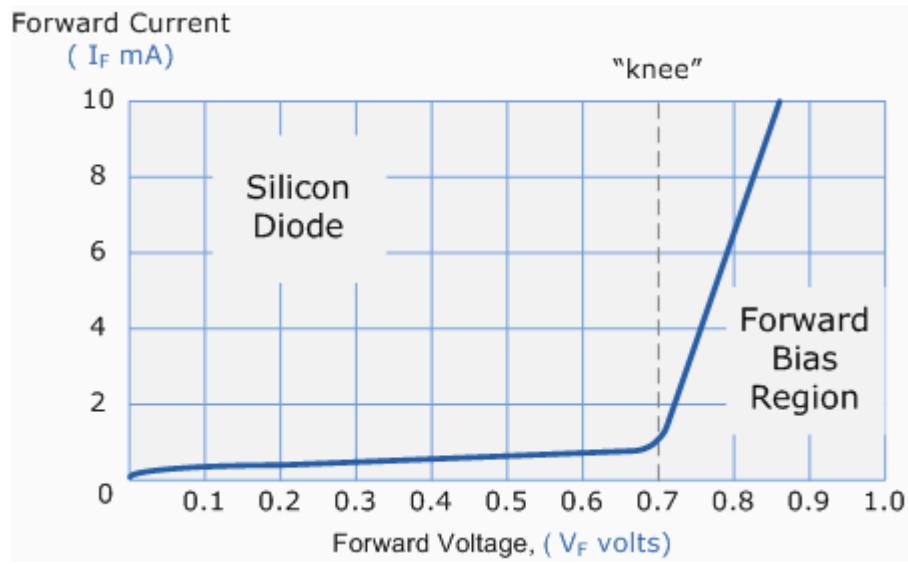
It is noticed that the space charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus the double space of the layer causes an electric field to be set up across the junction directed from N to P regions, which is in such a direction to inhibit the diffusion of majority electrons and holes as illustrated in fig 1.7. The shape of the charge density, ρ , depends upon how diode id doped. Thus the junction region is depleted of mobile charge carriers. Hence it is called depletion layer, space region, and transition region. The depletion region is of the order of $0.5\mu\text{m}$ thick. There are no mobile carriers in this narrow depletion region. Hence no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is $p= N_A$ and to its right it is $n= N_D$.



1.1.2 FORWARD BIASED JUNCTION DIODE

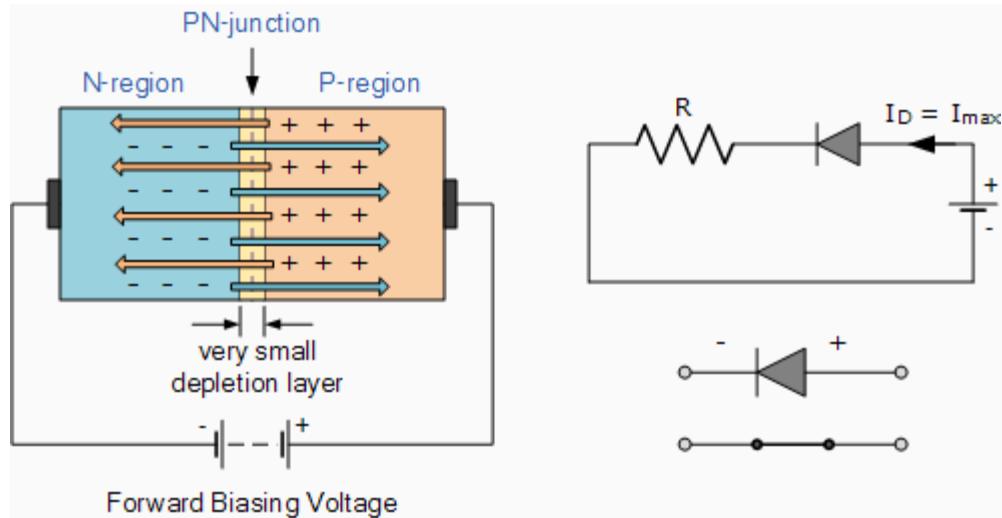
When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

Forward Characteristics Curve for a Junction Diode



The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

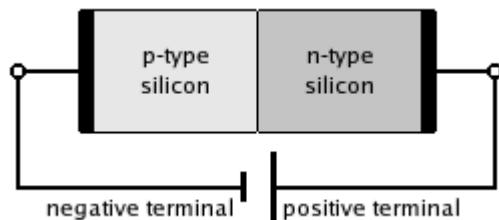
Forward Biased Junction Diode showing a Reduction in the Depletion Layer



This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow.

Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

1.1.2 PN JUNCTION UNDER REVERSE BIAS CONDITION:

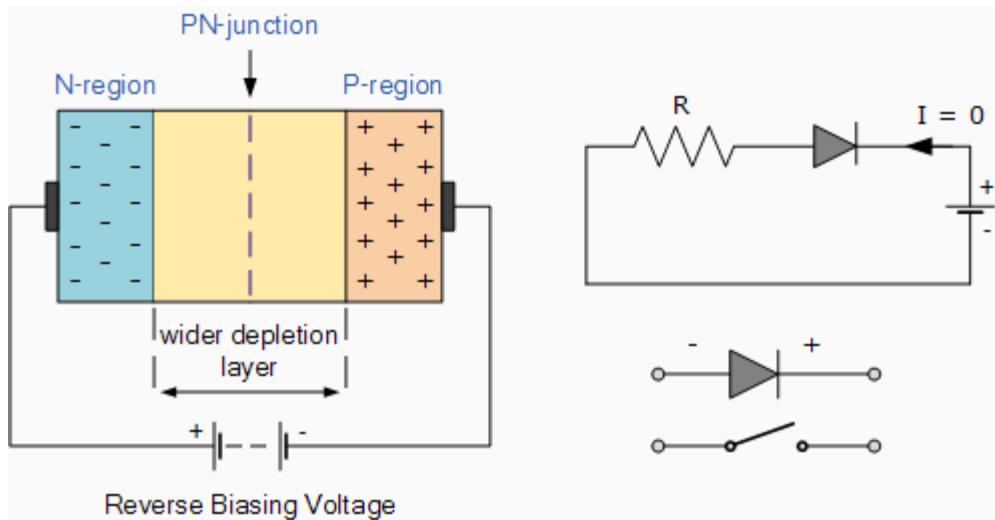


A silicon p–n junction in reverse bias.

Reverse Biased Junction Diode

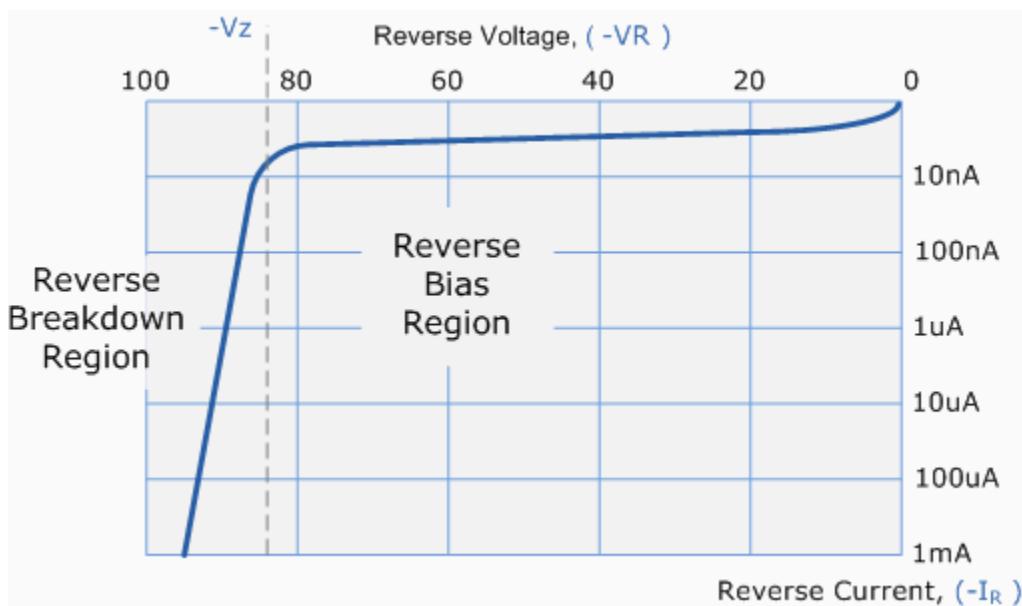
When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Reverse Biased Junction Diode showing an Increase in the Depletion Layer



This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage V_r applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

Reverse Characteristics Curve for a Junction Diode



Sometimes this avalanche effect has practical applications in voltage stabilizing circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset

maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes** and are discussed in a later tutorial.

1.2 VI CHARACTERISTICS AND THEIR TEMPERATURE

DEPENDENCE: Diode terminal characteristics equation for diode junction current:

$$I_D = I_o (e^{\frac{V}{nV_T}} - 1)$$

Where $V_T = kT/q$;

V_D _ diode terminal voltage, Volts

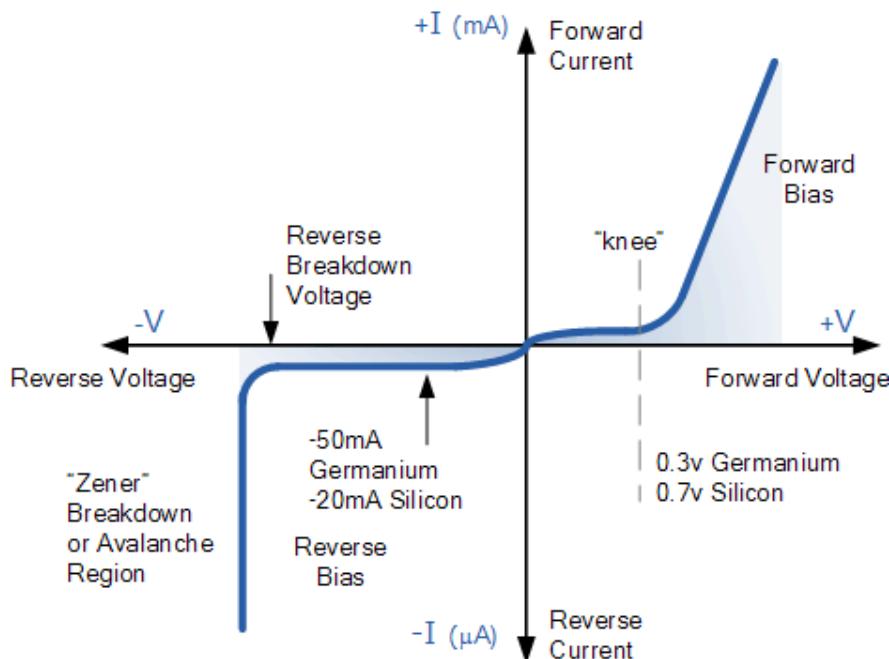
I_o _ temperature-dependent saturation current, μA

T _ absolute temperature of p-n junction, K

k _ Boltzmann's constant $1.38 \times 10^{-23} J/K$

q _ electron charge $1.6 \times 10^{-19} C$

η = empirical constant, 1 for Ge and 2 for Si



Temperature Effects on Diode

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as shown in Fig. 1.24. It has been found experimentally that the reverse saturation current I_o will just about double in magnitude for every $10^\circ C$ increase in temperature.

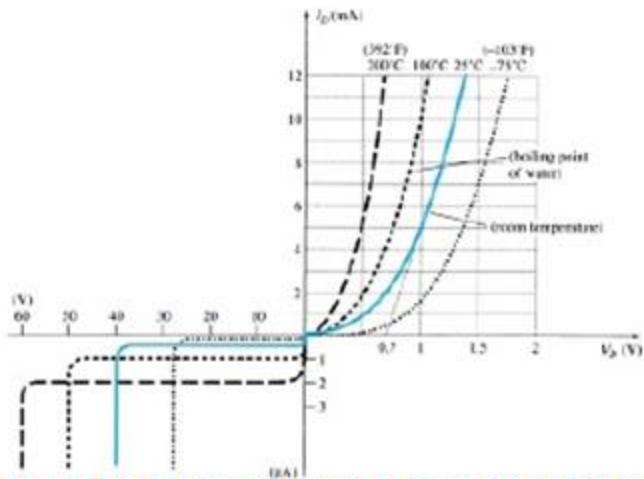


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an I_o in the order of 1 or 2 A at 25°C to have a leakage current of $100 \text{ A} \sim 0.1 \text{ mA}$ at a temperature of 100°C . Typical values of I_o for silicon are much lower than that of germanium for similar power and current levels. The result is that even at high temperatures the levels of I_o for silicon diodes do not reach the same high levels obtained for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of I_o with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of I_o in and not rise in diode current. Of course, the level of T_K also will be increase, but the increasing level of I_o will overpower the smaller percent change in T_K . As the temperature increases the forward characteristics are actually becoming more “ideal.”

1.3 IDEAL VERSUS PRACTICAL RESISTANCE LEVELS

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1.25 and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-

current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

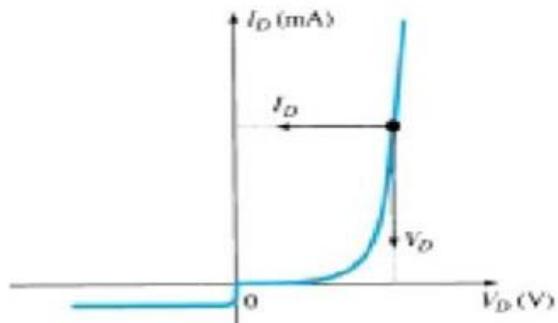


Figure 1.25 determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

It is obvious from Eq. 1.5 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.27. With no applied varying signal, the point of operation would be the Q-point appearing on Fig. 1.27 determined by the applied dc levels. The designation Q-point is derived from the word quiescent, which means “still or unvarying.” A straight-line drawn tangent to the curve through the Q-point as shown in Fig. 1.28 will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

where Δ signifies a finite change in the quantity.

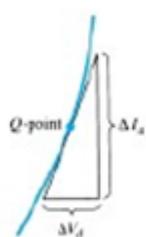


Figure 1.28 determining the ac resistance at a Q-point.

1.4 DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In

other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behaviour of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open-circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.31), a battery V_T opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established, the resistance of the diode will be the specified value of r_{av} .

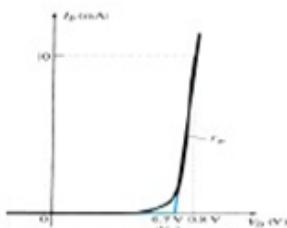


Figure 1.31 Defining the piecewise-linear equivalent circuit using straight-line segments to

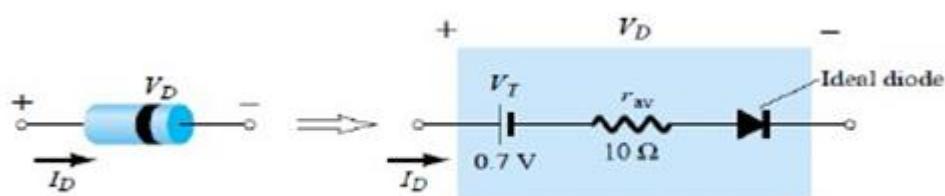


Figure 1.32 Components of the piecewise-linear equivalent circuit.

The approximate level of r_{av} can usually be determined from a specified operating point on the

specification sheet. For instance, for a silicon semiconductor diode, if $I_F = 10 \text{ mA}$ (a forward conduction current for the diode) at $V_D = 0.8 \text{ V}$, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

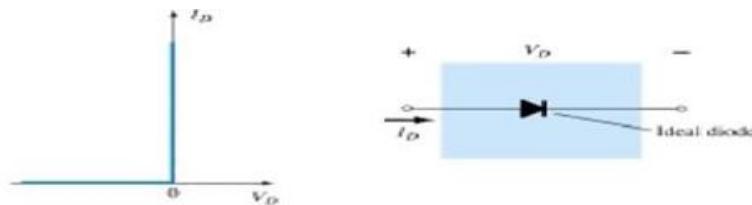


Figure 1.3-4 Ideal diode and its characteristics.

TABLE 1.3 Diode Equivalent Circuits (Models)

Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{\text{network}} \gg r_{sv}$		
Ideal device	$R_{\text{network}} \gg r_{sv}$ $E_{\text{network}} \gg V_T$		

1.5 TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance $X_C = 1/2\pi f C$ is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. X_C will become sufficiently small due to the high value of f to introduce a low-reactance

"shorting" path. In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance. Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by $C = \epsilon A/d$, where ϵ is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-, bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is over shadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

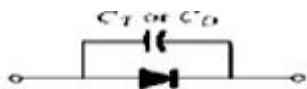


Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

Diode capacitances: The diode exhibits two types of capacitances transition capacitance and diffusion capacitance.

- Transition capacitance: The capacitance which appears between positive ion layer in n-region and negative ion layer in p-region.
- Diffusion capacitance: This capacitance originates due to diffusion of charge carriers in the opposite regions.

The transition capacitance is very small as compared to the diffusion capacitance.

In reverse bias transition, the capacitance is the dominant and is given by:

$$C_T = \epsilon A/W$$

where C_T - transition capacitance

A - diode cross sectional area

W - depletion region width

In forward bias, the diffusion capacitance is the dominant and is given by:

$$C_D = dQ/dV = \tau^* dI/dV = \tau^* g = \tau/r \text{ (general)}$$

where C_D - diffusion capacitance

dQ - change in charge stored in depletion region

V - change in applied voltage

τ - time interval for change in voltage

g - diode conductance

r - diode resistance

The diffusion capacitance at low frequencies is given by the formula:

$$C_D = \tau^* g / 2 \text{ (low frequency)}$$

The diffusion capacitance at high frequencies is inversely proportional

to the frequency and is given by the formula:

$$C_D = g(\tau/2\omega)^{1/2}$$

Note: The variation of diffusion capacitance with applied voltage is used in the design of varactor.

1.6 BREAK DOWN MECHANISMS

When an ordinary P-N junction diode is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the *breakdown diode* many useful applications as a *voltage reference source*.

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs is called the *breakdown voltage*. The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction :

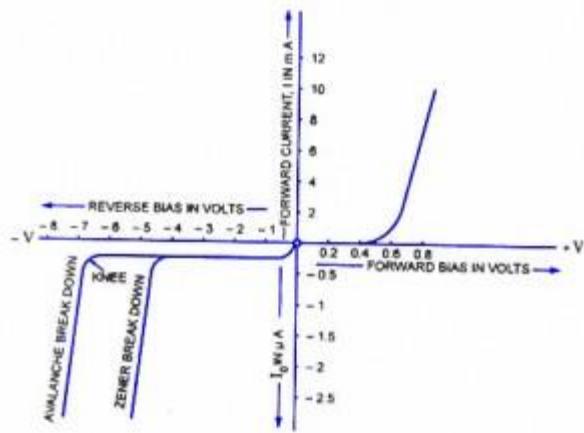
1. **avalanche breakdown and**
2. **Zener breakdown.**

Avalanche breakdown and

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. *The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.*

Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3×10^7 V/m.



Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5 V are caused by Zener effect. Junctions that experience breakdown above 5 V are caused by avalanche effect. Junctions that

breakdown around 5 V are usually caused by combination of two effects. The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce narrow depletion layers. The avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers. With the increase in junction temperature Zener breakdown voltage is reduced while the avalanche breakdown voltage increases. The Zener diodes have a negative temperature coefficient while avalanche diodes have a positive temperature coefficient. Diodes that have breakdown voltages around 5 V have zero temperature coefficient. The breakdown phenomenon is reversible and harmless so long as the safe operating temperature is maintained.

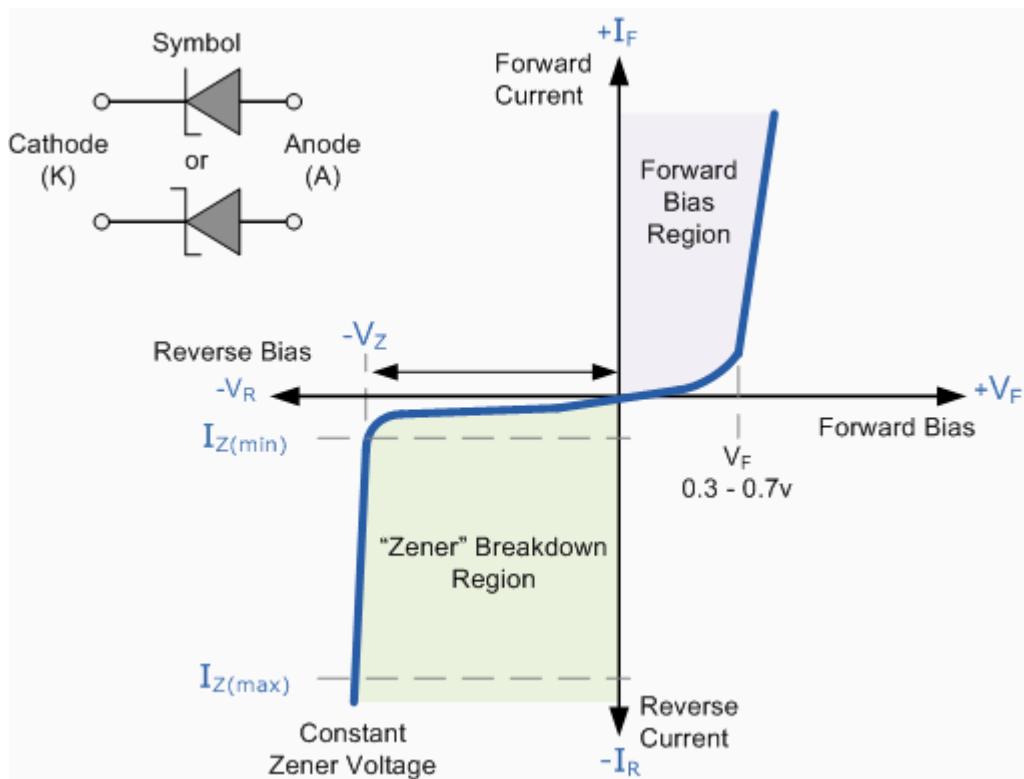
1.7 ZENER DIODES

The **Zener diode** is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage V_B is reached at which point a process called *Avalanche Breakdown* occurs in the semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.

The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achieved this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, V_B is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific *zener breakdown voltage*, (V_z) for example, 4.3V or 7.5V. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener Diode I-V Characteristics



The **Zener Diode** is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$ and the maximum current rating $I_{Z(max)}$.

This ability to control itself can be used to great effect to regulate or stabilise a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator. The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_{Z(min)}$ value in the reverse breakdown region.

UNIT III RECTIFIERS & FILTERS:

3.0 INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c.voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the fig 1 below.

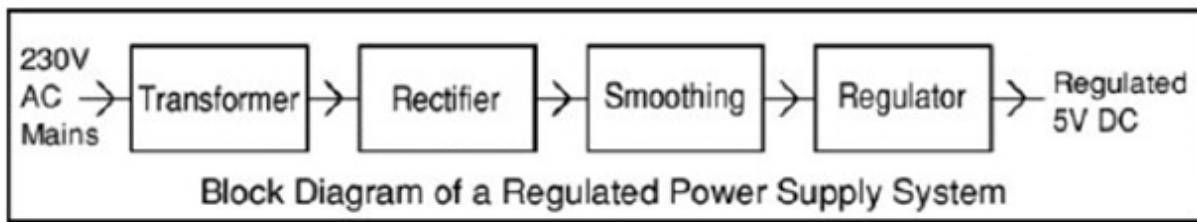


fig1 . Block diagram of Regulated D.C. Power Supply

- ✓ Transformer – steps down 230V AC mains to low voltage AC.
- ✓ Rectifier – converts AC to DC, but the DC output is varying.
- ✓ Smoothing – smooth the DC from varying greatly to a small ripple.
- ✓ Regulator – eliminates ripple by setting DC output to a fixed voltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage V_o which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

3.1 RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a non-zero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Unidirectional).

Characteristics of a Rectifier Circuit:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c.. Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

It is expressed mathematically as

i) Average value/dc value/mean value = $\frac{\text{Area over one period}}{\text{Total time period}}$

$$V_{dc} = \frac{1}{T} \int_0^T V d(wt)$$

ii) Effective (or) R.M.S current:

The effective (or) R.M.S. current squared of a periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2 d(wt)}$$

iii) Peak factor:

It is the ratio of peak value to Rms value

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

iv) Form factor:

It is the ratio of Rms value to average value

$$\text{Form factor} = \frac{\text{Rms value}}{\text{average value}}$$

v) Ripple Factor (Γ) : It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as “Ripple Factor”.

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

vi) Efficiency (η):

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o/p \text{ power}}{i/p \text{ power}}$$

vii) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

viii) Transformer Utilization Factor (UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

ix) % Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

For an ideal power supply, % Regulation is zero.

3.2 CLASSIFICATION OF RECTIFIERS:

Using one or more diodes in the circuit, following rectifier circuits can be designed.

- 1) Half - Wave Rectifier
- 2) Full – Wave Rectifier
- 3) Bridge Rectifier

3.2.1) HALF-WAVE RECTIFIER:

A Half – wave rectifier as shown in **fig 2** is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

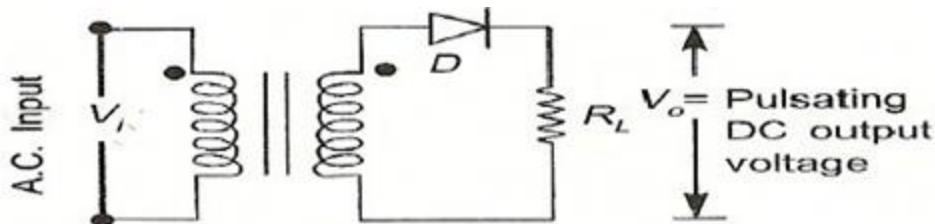


fig 2 Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element

i.e., p-n junction diode and the source of a.c. voltage, all connected in series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

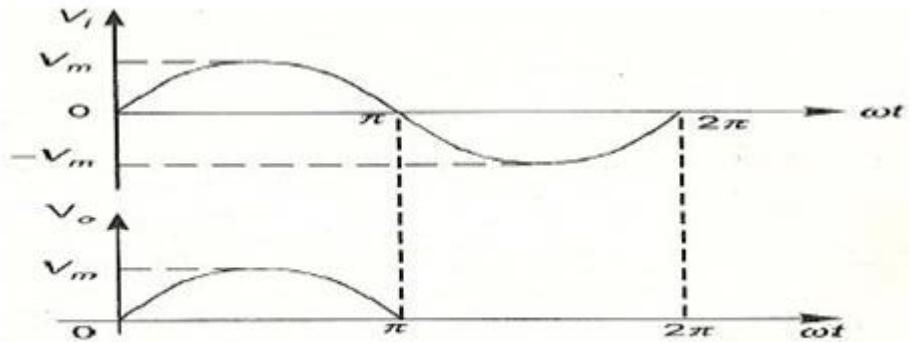


fig 3 Input and output waveforms of a Half wave rectifier

$$V = V_m \sin(\omega t)$$

The input to the rectifier circuit, Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across RL. The waveform of the diode current (or) load current is shown in **fig 3**.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., $i=0$ and $V_o=0$. Thus for the negative half-cycle no power is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage
5. Rectifier Efficiency (η)

6. Ripple factor (γ)
7. Peak Factor
8. % Regulation
9. Transformer Utilization Factor (TUF)
10. form factor
11. o/p frequency

Let a sinusoidal voltage V_i be applied to the input of the rectifier.

Then $V = V_m \sin(wt)$ Where V_m is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance R_f in the forward direction i.e., in the ON state and $R_r (\infty)$ in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance RL is given by $V = V_m \sin(wt)$

i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T} \int_0^T V d(wt)$$

$$V_{dc} = \frac{1}{T} \int_0^{2\pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\pi} \int_{-\pi}^{\pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin(wt) d(wt)$$

$$V_{dc} = \frac{V_m}{\pi}$$

ii).AVERAGE CURRENT:

$$I_{dc} = \frac{I_m}{\pi}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (V_m \sin(wt))^2 d(wt)}$$

$$V_{rms} = \frac{V_m}{2}$$

IV) RMS CURRENT

V) PEAK FACTOR

$$I_{rms} = \frac{I_m}{\Pi}$$

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m / 2)}$$

$$\text{Peak Factor} = 2$$

vi) FORM FACTOR

$$\text{Form factor} = \frac{\text{Rms value}}{\text{average value}}$$

$$\text{Form factor} = \frac{(V_m / 2)}{V_m / \Pi}$$

$$\text{Form Factor} = 1.57$$

vii) Ripple Factor:

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{ac}}$$

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$\Gamma = 1.21$$

viii) Efficiency (η):

$$\eta = \frac{o/power}{i/power} * 100$$

$$\eta = \frac{P_{ac}}{P_{dc}} * 100$$

$$\eta = 40.8$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

$$TUF = 0.286.$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.

If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver
 $1000 \times 0.287 = 287$ watts to resistance load.

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-wave rectifier, PIV is V_m .

DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

3.2.2) FULL WAVE RECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the **fig 4** below

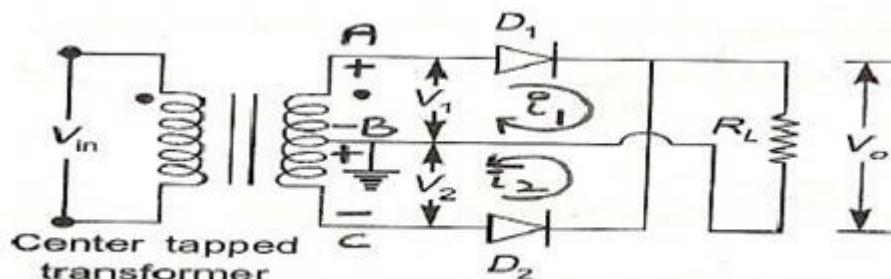


fig 4 Full-Wave Rectifier

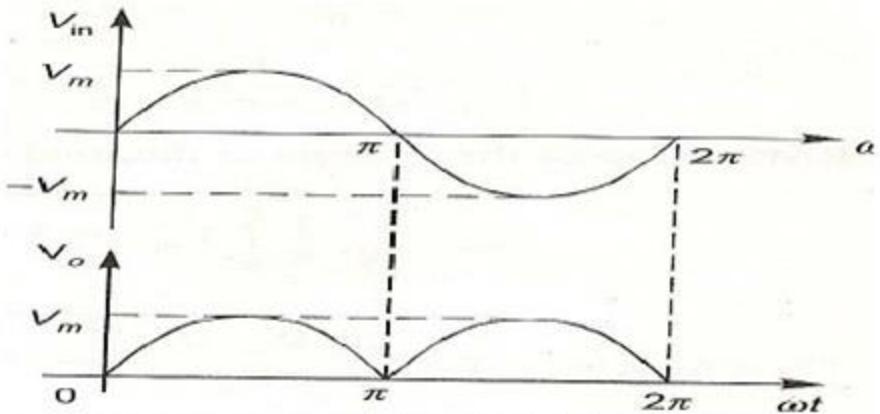


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D1 becomes positive and at the same time the anode of diode D2 becomes negative. Hence D1 conducts and D2 does not conduct. The load current flows through D1 and the voltage drop across RL will be equal to the input voltage.

During the negative half cycle of the input, the anode of D1 becomes negative and the anode of D2 becomes positive. Hence, D1 does not conduct and D2 conducts. The load current flows through D2 and the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

i) AVERAGEVOLTAGE

$$V_{dc} = I_{dc} \cdot R_L = \frac{2I_m}{\pi} \cdot R_L \quad \text{We know } I_m = \frac{V_m}{R_s + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2V_m R_L}{\pi(R_s + R_f + R_L)}$$

If $(R_s + R_f) \ll R_L$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637 V_m$$

ii) _AVERAGE CURRENT

$$\begin{aligned}
\frac{1}{2\pi} \int_0^{2\pi} id\theta &= \frac{1}{2\pi} \int_0^{2\pi} I_m \sin \theta dt \\
I_{dc} &= \frac{I_m}{2\pi} \left[\int_0^{\pi} \sin \theta d\theta - \int_{\pi}^{2\pi} \sin \theta d\theta \right] \\
&= \frac{I_m}{2\pi} [(-2)(-2)] \\
&= \frac{I_m}{2\pi} \cdot 4 = \frac{2I_m}{\pi} = 0.637 I_m. \\
\boxed{I_{dc} = 0.637 I_m.} \\
\therefore I_{DC \text{ FWR}} &= 2 I_{DC \text{ HWR}}.
\end{aligned}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (V_m \sin(wt))^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{2I_m}{\pi}}$$

V) PEAK FACTOR

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m / 2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{\text{Rms value}}{\text{average value}}$$

$$\text{Form factor} = \frac{(V_m / \sqrt{2})}{2V_m / \Pi}$$

$$\text{Form Factor} = 1.11$$

vii) Ripple Factor:

$$\mathcal{V} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\begin{aligned}\therefore \mathcal{V}_{FWR} &= \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1} \\ &= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} \\ &= \sqrt{\left(\frac{3.1416}{2 \times 1.414}\right)^2 - 1} = 0.483\end{aligned}$$

viii) Efficiency (η):

$$\eta = \frac{o / ppower}{i / ppower} * 100$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

For FWR, $P_{dc} = I_{dc}^2 \cdot R_L = \left(\frac{2}{\pi} \cdot I_m \right)^2 \cdot R_L$

$$P_{ac} = I_{rms}^2 (R_f + R_s + R_L)$$

$$\left(\frac{I_m}{\sqrt{2}} \right)^2 (R_f + R_s + R_L)$$

$$\eta = \frac{\frac{I_m^2}{\pi^2} \cdot 4 \cdot R_L}{\frac{I_m^2 m^2}{2} \cdot (R_f + R_s + R_L)}$$

If $(R_f + R_s) \ll R_L$

$$\eta = \frac{4}{\pi^2} \cdot \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

- a) TUF (Secondary) = $\frac{P_{dc} \text{ delivered to load}}{AC \text{ power rating of transformer secondary}}$
- b) Since both the windings are used $TUF_{FWR} = 2 TUF_{HWR}$
 $= 2 \times 0.287 = 0.574$
- c) TUF primary = Rated efficiency = $\frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$
- d) Average = $\frac{0.812 + 0.574}{2} = 0.693$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-wave rectifier, PIV is $2V_m$

xi) % Regulation

$$\begin{aligned}\text{Voltage regulation} &= \\ &= \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_s)}\end{aligned}$$

Advantages

- 1) Ripple factor = 0.482 (against 1.21 for HWR)
- 2) Rectification efficiency is 0.812 (against 0.405 for HWR)
- 3) Better TUF (secondary) is 0.574 (0.287 for HWR)
- 4) No core saturation problem

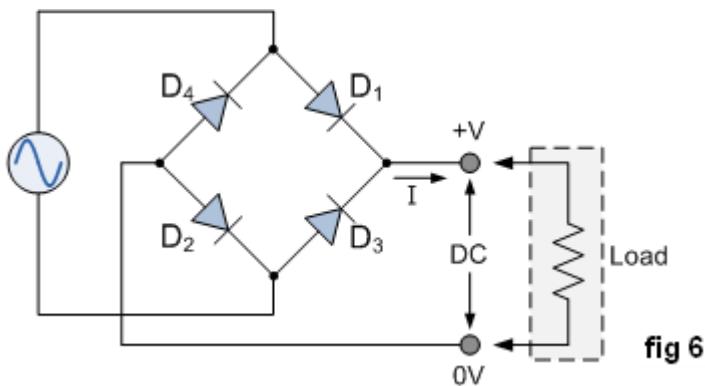
Disadvantages:

- 1) Requires center tapped transformer.

3.2.3) BRIDGE RECTIFIER.

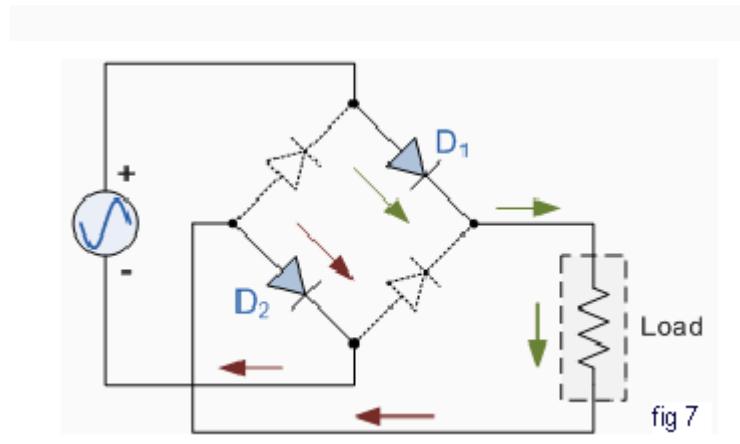
Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the **Full Wave Bridge Rectifier**. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier



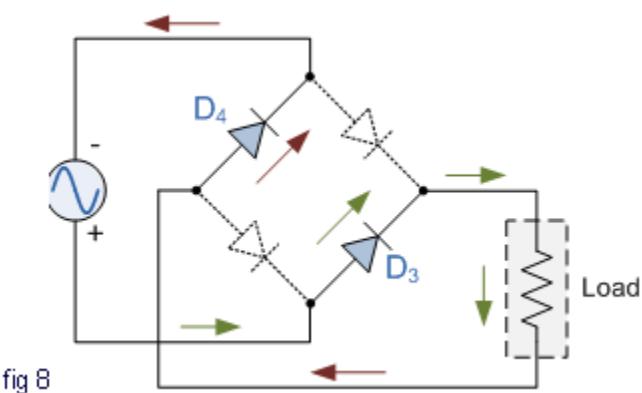
The four diodes labelled D₁ to D₄ are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D₁ and D₂ conduct in series while diodes D₃ and D₄ are reverse biased and the current flows through the load as shown below (fig 7).

The Positive Half-cycle



The Negative Half-cycle

During the negative half cycle of the supply, diodes D₃ and D₄ conduct in series (fig 8), but diodes D₁ and D₂ switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.



As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is $0.637V_{\max}$. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is

two voltage drops ($2 \times 0.7 = 1.4V$) less than the input V_{MAX} amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Therefore, the following expressions are same as that of full wave rectifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no.load) $V_{DC} = \frac{2V_m}{\pi}$

d) Ripple factor $\gamma = 0.482$

e) Rectification efficiency $\eta = 0.812$

f) DC output voltage full load.

$$= V_{DCFL} = \frac{2V_m}{\pi} - I_{dc}(R_s + 2R_f); \quad \text{i.e., less by one diode loss.}$$

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

Comparison:

SL No.	Parameter	HWR	FWR	BR
1	No. of diodes	1	2	4
2	PIV of diodes	V_m	$2V_m$	V_m
3	Secondary voltage (rms)	V	$V-0-V$	V
4	DC output voltage at no load	$\frac{V_m}{\pi} = 0.318V_m$	$\frac{2V_m}{\pi} = 0.636V_m$	$\frac{2V_m}{\pi} = 0.636V_m$
5	Ripple factor γ	1.21	0.482	0.482
6	Ripple frequency	f	$2f$	$2f$
7	Rectification efficiency η	0.406	0.812	0.812
8	TUF	0.287	0.693	0.812

3.3 FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimize the undesirable ac i.e., ripple leaving only the dc component to appear at the output.

Some important filters are:

1. Inductor filter
2. Capacitor filter

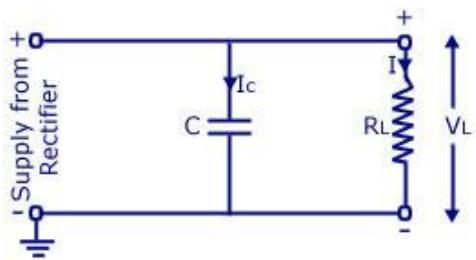
3. LC or L section filter
4. CLC or Π -type filter

2.3.1 CAPACITOR FILTER

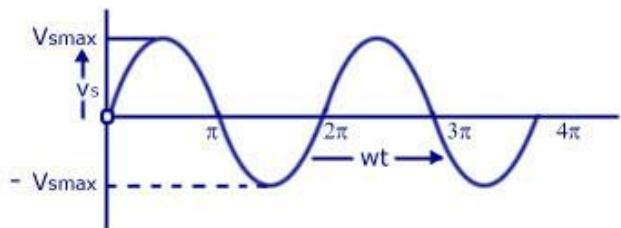
This is the most simple form of the **filter circuit** and in this arrangement a high value capacitor C is placed directly across the output terminals, as shown in figure. During the conduction period it gets charged and stores up energy to it during non-conduction period. Through this process, the time duration during which F_t is to be noted here that the capacitor C gets charged to the peak because there is no resistance (except the negligible forward resistance of diode) in the charging path. But the discharging time is quite large (roughly 100 times more than the charging time depending upon the value of R_L) because it discharges through load resistance R_L.

The function of the capacitor filter may be viewed in terms of impedances. The large value capacitor C offers a low impedance shunt path to the ac components or ripples but offers high impedance to the dc component. Thus ripples get bypassed through capacitor C and only dc component flows through the load resistance R_L

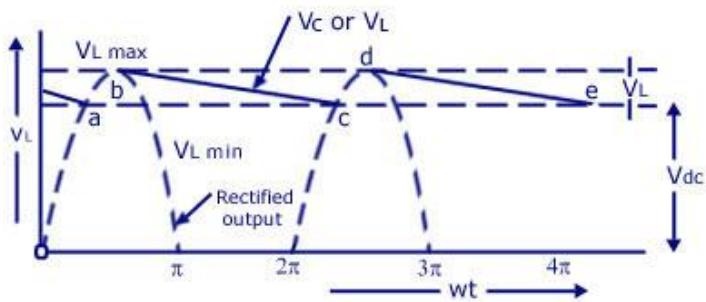
Capacitor filter is very popular because of its low cost, small size, light weight and good characteristics.



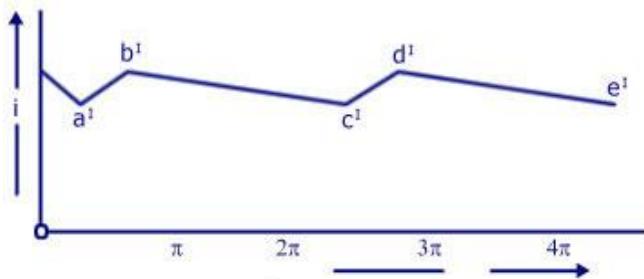
Circuit Diagram



Input voltage Waveform to Rectifier



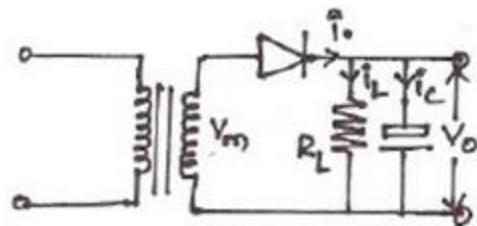
Rectified and filtered Output Voltage Waveform



Load Current Waveform
Half-wave Rectifier With Shunt Capacitor Filter

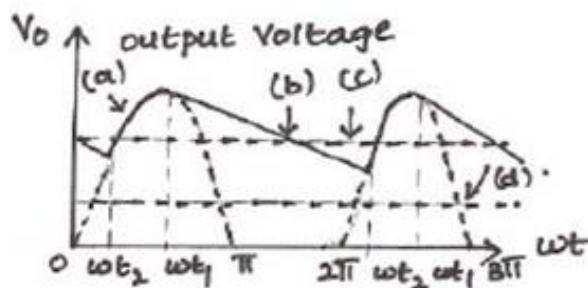
www.CircuitsToday.com

CAPACITOR FILTER WITH HWR



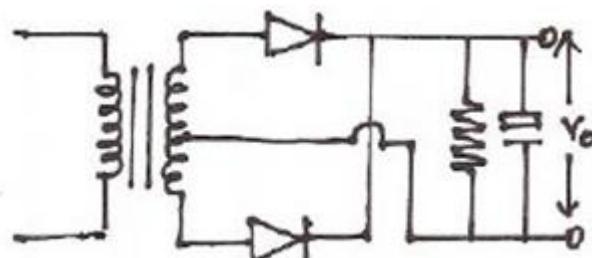
Cut In angle – ωt_2

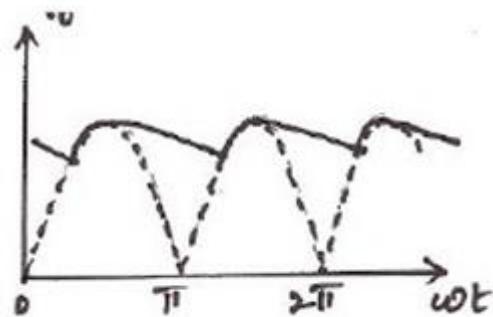
Cut out angle = Wt_1
 $Wt_1 = \pi - \tan^{-1} WCR_L$



- (a) Capacitor charging through diode
 $(Wt_2 - Wt_1)$
- (b) Capacitor discharging through R_L
 $(Wt_1 \text{ to } Wt_2)$
- (c) Average (DC) voltage with filter
- (d) Average (DC) voltage without filter.

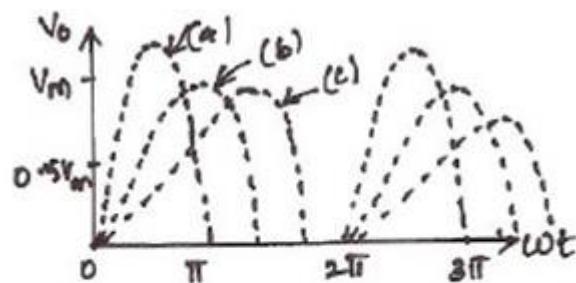
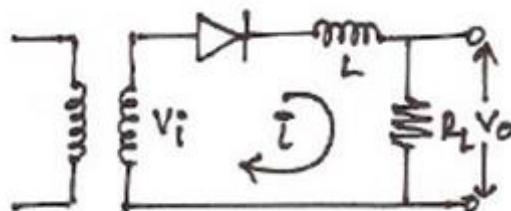
CAPACITOR FILTER WITH FWR





$$\text{Ripple factor } r = \frac{1}{4\sqrt{3}fCR_L}$$

Ripple freq FWR = 2 ripple freq HWR.

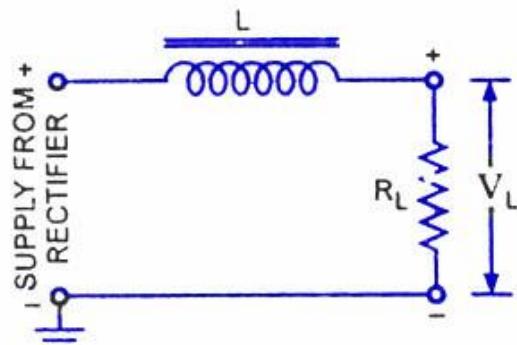


$$(a) \frac{w_L}{R_L} = 0 \quad (b) \frac{w_L}{R_L} = 1 \quad (c) \frac{w_L}{R_L} = 5.$$

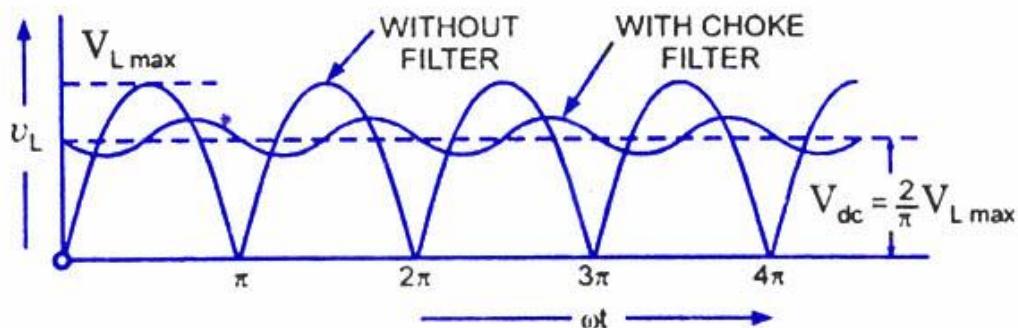
The worth noting points about shunt capacitor filter are:

1. For a fixed-value filter capacitance larger the load resistance RL larger will be the discharge time constant CRL and therefore, lower the ripples and more the output voltage. On the other hand lower the load resistance (or more the load current), lower will be the output voltage.
2. Similarly smaller the filter capacitor, the less charge it can hold and more it will discharge. Thus the peak-to-peak value of the ripple will increase, and the average dc level will decrease. Larger the filter capacitor, the more charge it can hold and the less it will discharge. Hence the peak-to-peak value of the ripple will be less, and the average dc level will increase. But, the maximum value of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be handled by a diode is limited by the figure quoted by the manufacturer. Thus the maximum value of the capacitance, that can be used in the shunt filter capacitor is limited.

2.3.2 Series Inductor Filter.



Circuit Diagram



*Output Voltage Waveforms
Full-Wave Rectifier With Series Inductor Filter*

In this arrangement a high value inductor or choke L is connected in series with the rectifier element and the load, as illustrated in figure. The filtering action of an inductor filter depends upon its property of opposing any change in the current flowing through it. When the output current of the rectifier increases above a certain value, energy is stored in it in the form of magnetic field and this energy is given up when the output current falls below the average value. Thus by placing a choke coil in series with the rectifier output and load, any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor L.

The function of the inductor filter may be viewed in terms of impedances. The choke offers high impedance to the ac components but offers almost zero resistance to the desired dc components. Thus ripples are removed to a large extent. Nature of the output voltage without filter and with choke filter is shown in figure.

For dc (zero frequency), the choke resistance R_c in series with the load resistance R_L forms a voltage divider and dc voltage across the load is given as

where V_{dc} is dc voltage output from a full-wave rectifier. Usually choke coil resistance R_c , is much small than R_L and, therefore, almost entire of the dc voltage is available across the load resistance R_L .

Since the reactance of inductor increases with the increase in frequency, better filtering of the higher harmonic components takes place, so effect of third and higher harmonic voltages can be neglected.

As obvious from equation , if choke coil resistance R_c is negligible in comparison to load resistance R_L , then the entire dc component of rectifier output is available across $2 R_L$ and is equal to $-V_{L \max}$. The ac voltage partly drops across X_L and partly over R_L .

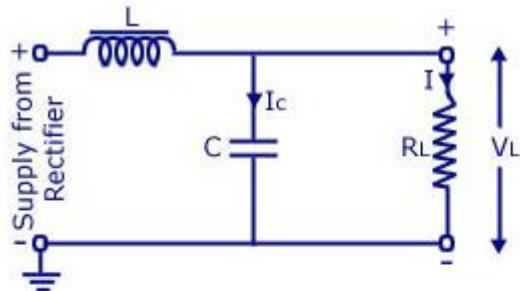
2.3.3 L-SECTION FILTER:

A simple series inductor reduces both the peakand effective values of the output current and output voltage. On the other hand a simple **shunt capacitor filter** reduces the ripple voltage but increases the diode current. The diode may get damaged due to large current and at the same time it causes greater heating of supply transformer resulting in reduced efficiency.

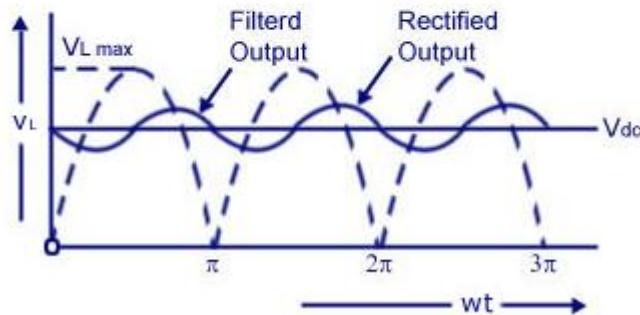
In an inductor filter, ripple factor increases with the increase in load resistance R_L while in a capacitor filter it varies inversely with load resistance R_L .

From economical point of view also, neither series inductor nor shunt capacitor type filters are suitable.

Practical **filter-circuits** are derived by combining the voltage stabilizing action of shunt capacitor with the current smoothing action of series choke coil. By using combination of inductor and capacitor ripple factor can be lowered, diode current can be restricted and simultaneously ripple factor can be made almost independent of load resistance (or load current). Two types of most commonly used combinations are choke-input or L-section filter-and capacitor-input or Pi-Filter.



Circuit Diagram

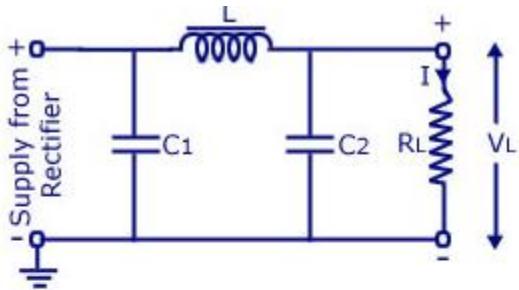


Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With Choke-Input Filter

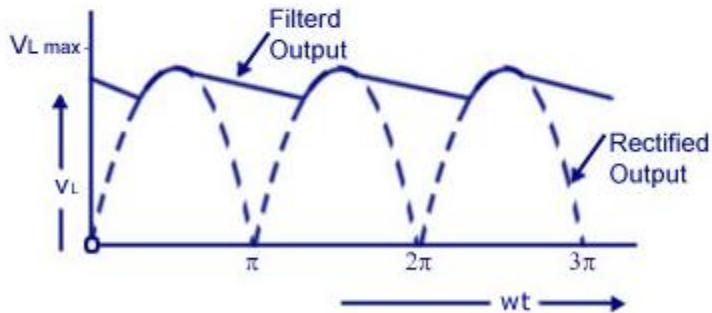
Choke-input filter is explained below:

Choke-input filter consists of a choke L connected in series with the rectifier and a capacitor C connected across the load . This is also sometimes called the L-section filter because in this arrangement inductor and capacitor are connected, as an inverted L. In figure only one filter section is shown. But several identical sections are often employed to improve the smoothing action. (The choke L on the input side of the filter readily allows dc to pass but opposes the flow of ac components because its dc resistance is negligibly small but ac impedance is large. Any fluctuation that remains in the current even after passing through the choke are largely by-passed around the load by the shunt capacitor because X_C is much smaller than R_L . Ripples can be reduced effectively by making X_L greater than X_C at ripple frequency. However, a small ripple still remains in the filtered output and this is considered negligible if it is less than 1%. The rectified and filtered output voltage waveforms from a full-wave rectifier with choke-input filter are shown in figure.

2.3.4 Π-SECTION FILTER:



Circuit Diagram



Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With capacitor Input Filter

Capacitor-Input or Pi-Filter.

Such a filter consists of a shunt capacitor C_1 at the input followed by an L-section filter formed by series inductor L and shunt capacitor C_2 . This is also called the *n-filter* because the shape of the circuit diagram for this filter appears like Greek letter *n* (*pi*). Since the rectifier feeds directly into the capacitor so it is also called *capacitor input filter*.

As the rectified output is fed directly into a capacitor C_1 . Such a filter can be used with a half-wave rectifier (series inductor and L-section filters cannot be used with half-wave rectifiers). Usually electrolytic capacitors are used even though their capacitances are large but they occupy minimum space. Usually both capacitors C_1 and C_2 are enclosed in one metal container. The metal container serves as, the common ground for the two capacitors.

A capacitor-input or *pi*-filter is characterized by a high voltage output at low current drains. Such a filter is used, if, for a given transformer, higher voltage than that can be obtained from an L-section filter is required and if low ripple than that can be obtained from a shunt capacitor filter or L-section filter is desired. In this filter, the input capacitor C_1 is selected to offer very low reactance to the ripple frequency. Hence major part of filtering is accomplished by the input capacitor C_1 . Most of the remaining ripple is removed by the L-section filter consisting of a choke L and capacitor C_2 .)

The action of this filter can *best* be understood by considering the action of L-section filter, formed by L and C_2 , upon the triangular output voltage wave from the input capacitor C_1 . The charging and discharging action of input capacitor C_1 has already been discussed. The output

voltage is roughly the same as across input capacitor C1 less the dc voltage drop in inductor. The ripples contained in this output are reduced further by L-section filter. The output voltage of pi-filter falls off rapidly with the increase in load-current and, therefore, the voltage regulation with this filter is very poor.

SALIENT FEATURES OF L-SECTION AND PI-FILTERS.

1. In pi-filter the dc output voltage is much larger than that can be had from an L-section filter with the same input voltage.
2. In pi-filter ripples are less in comparison to those in shunt capacitor or L-section filter. So smaller valued choke is required in a pi-filter in comparison to that required in L-section filter.
3. In pi-filter, the capacitor is to be charged to the peak value hence the rms current in supply transformer is larger as compared in case of L-section filter.
4. Voltage regulation in case of pi-filter is very poor, as already mentioned. So n-filters are suitable for fixed loads whereas L-section filters can work satisfactorily with varying loads provided a minimum current is maintained.
5. In case of a pi-filter PIV is larger than that in case of an L-section filter.

COMPARISON OF FILTERS

- 1) A capacitor filter provides V_m volts at less load current. But regulation is poor.
- 2) An Inductor filter gives high ripple voltage for low load currents. It is used for high load currents
- 3) L – Section filter gives a ripple factor independent of load current. Voltage Regulation can be improved by use of bleeder resistance
- 4) Multiple L – Section filter or π filters give much less ripple than the single L – Section Filter.

UNIT III

BIPOLAR JUNCTION TRANSISTOR

3.1 INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogous to vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

3.2 CONSTRUCTION OF BJT AND ITS SYMBOLS

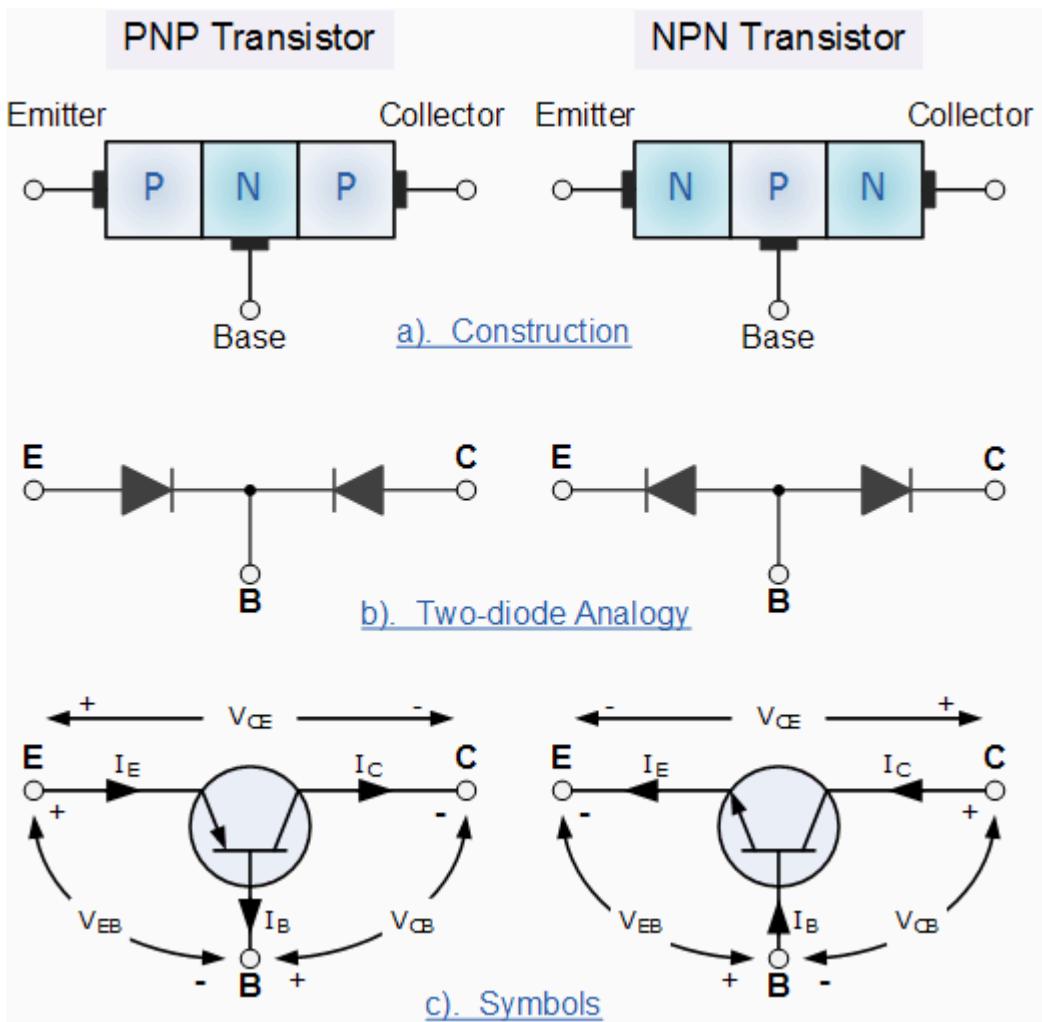
The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the **Emitter (E)**, the **Base (B)** and the **Collector (C)** respectively. There are two basic types of bipolar transistor construction, **PNP** and **NPN**, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. **Active Region** - the transistor operates as an amplifier and $I_c = \beta \cdot I_b$
- 2. **Saturation** - the transistor is "fully-ON" operating as a switch and $I_c = I_{(saturation)}$
- 3. **Cut-off** - the transistor is "fully-OFF" operating as a switch and $I_c = 0$

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types **PNP** and **NPN**, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type(fig 1).

Bipolar Transistor Construction



- **Fig:1**
The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

3.3 TRANSISTOR CURRENT COMPONENTS:

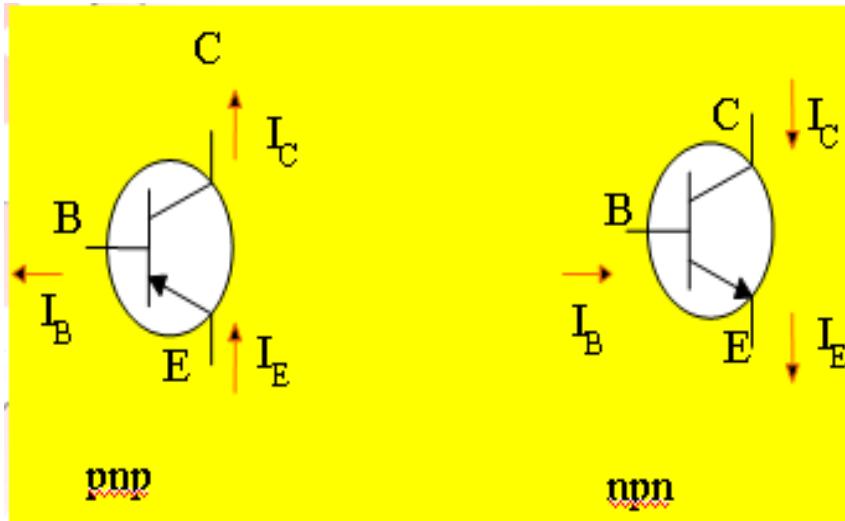


FIG 2

The above fig 2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{pE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter).The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter does not contribute carriers, which can reach the collector.

Not all the holes crossing the emitter junction J_E reach the the collector junction J_C

Because some of them combine with the electrons in n-type base. If I_{pC} is hole current at junction J_C there must be a bulk recombination current ($I_{pE} - I_{pC}$) leaving the base.

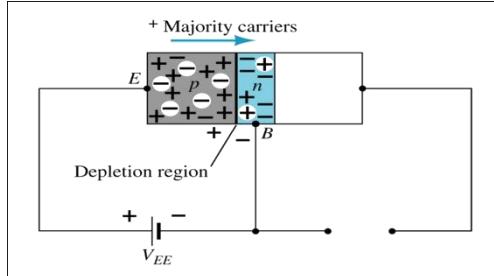
Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across J_E . If the emitter were open circuited so that $I_E=0$ then I_{pC} would be zero. Under these circumstances, the base and collector current I_C would equal the reverse saturation current I_{CO} . If $I_E \neq 0$ then

$$I_C = I_{CO} - I_{pC}$$

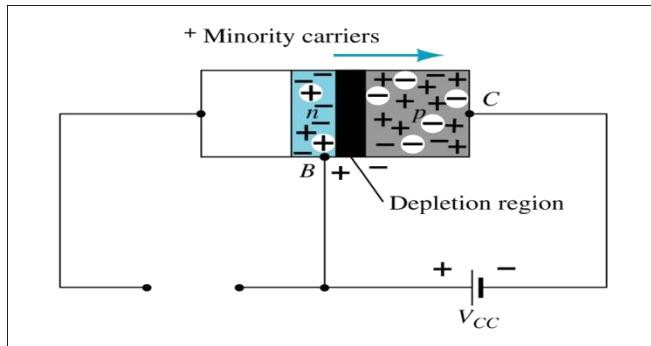
For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left,

then for a p-n-p transistor, I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive. The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

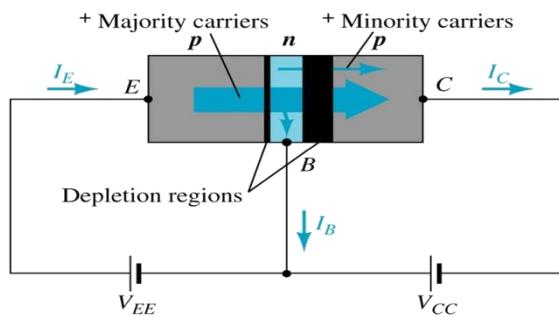
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



Forward-biased junction of a pnp transistor



Reverse-biased junction of a pnp transistor



Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will pass through n-type material to the base terminal. Resulting I_B is typically in the order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{C\text{majority}} + I_{C\text{minority}}$$

$I_{CO} - I_C$ current with emitter terminal open and is called leakage current

Various parameters which relate the current components is given below

Emitter efficiency:

$$\gamma = \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}}$$

$$\gamma = \frac{I_{pE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\beta^* = \frac{\text{injected carrier current reaching } J_C}{\text{injected carrier current at } J_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off)to I_E the large signal current gain of a common base transistor.

$$\alpha = \frac{-(I_C - I_{CO})}{I_E}$$

Since I_C and I_E have opposite signs, then α , as defined, is always positive. Typically numerical values of α lies in the range of 0.90 to 0.995

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \quad \alpha = \beta^* \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio α^* is unity. α^* is the ratio of total current crossing J_C to hole arriving at the junction.

3.4 Bipolar Transistor Configurations

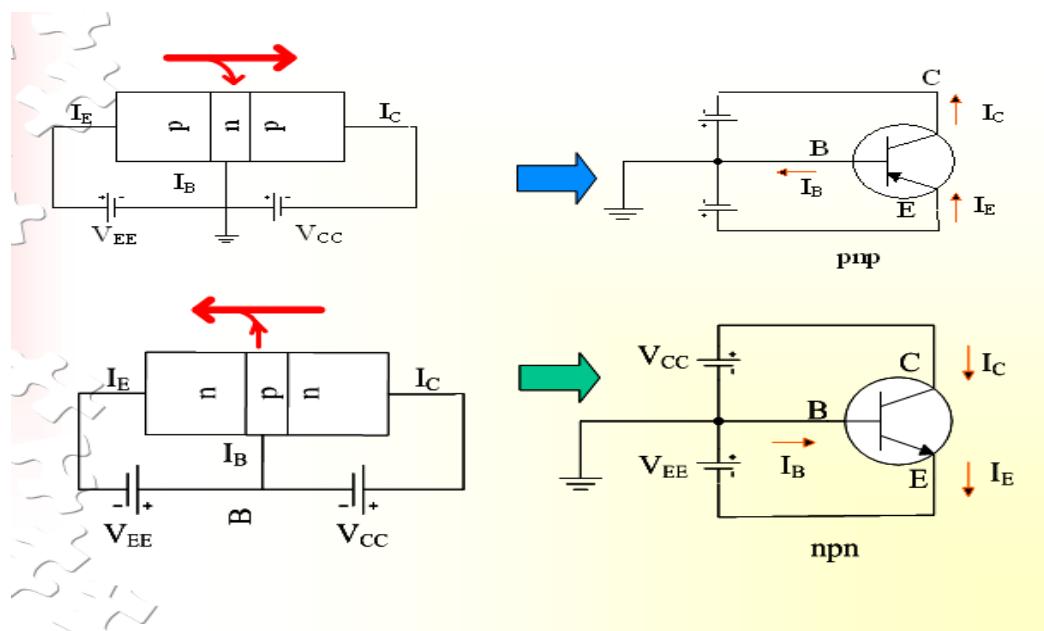
As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

3.5 COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and output of t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

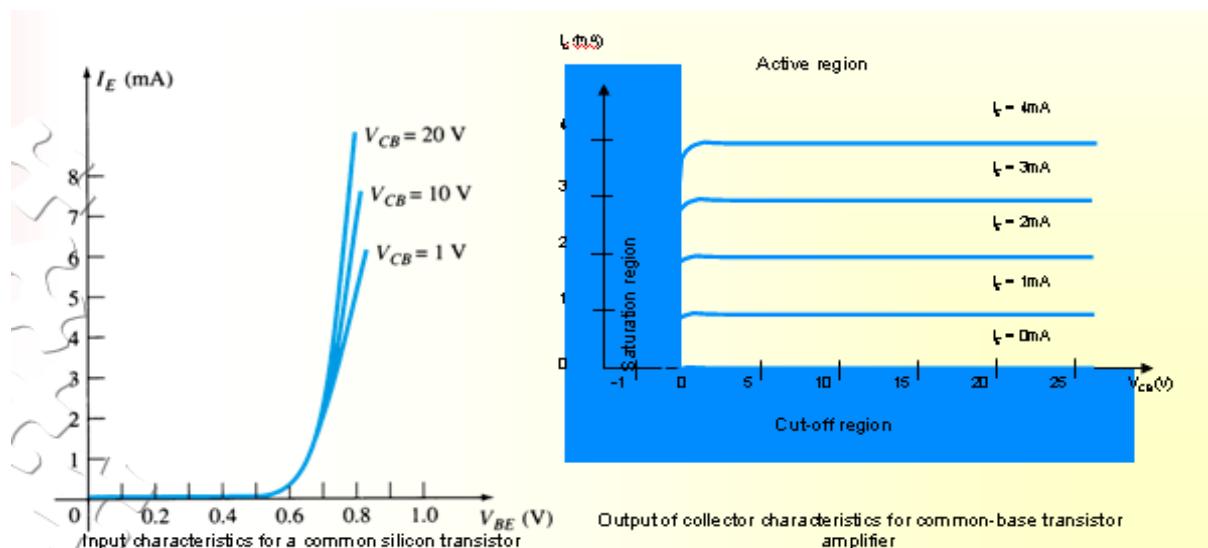


To describe the behavior of common-base amplifiers requires two set of characteristics:

1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of $V_{CB} = 0V$

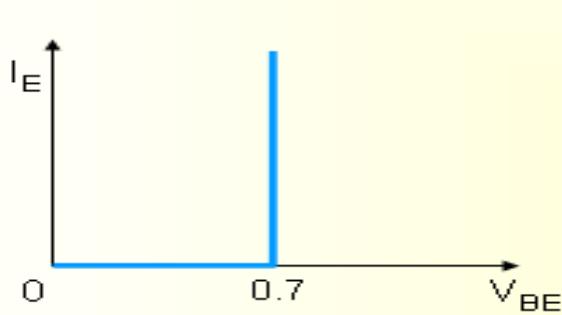


Active region	Saturation region	Cut-off region
<ul style="list-style-type: none"> • I_E increased, I_C increased • BE junction forward bias and CB junction reverse bias • Refer to the <u>graf</u>, $I_C \approx I_E$ • I_C not depends on V_{CB} • Suitable region for the transistor working as amplifier 	<ul style="list-style-type: none"> • BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to I_C • The allocation for this region is to the left of $V_{CB} = 0\text{ V}$. 	<ul style="list-style-type: none"> • Region below the line of $I_E = 0\text{ A}$ • BE and CB is reverse bias • no current flow at collector, only leakage current

The curves (output characteristics) clearly indicate that a first approximation to the relationship between I_E and I_C in the active region is given by

$$I_C \approx I_E$$

Once a transistor is in the ‘on’ state, the base-emitter voltage will be assumed to be $V_{BE} = 0.7V$



In the dc mode the level of I_C and I_E due to the majority carriers are related by a quantity called alpha
 $\alpha = \alpha_{dc}$

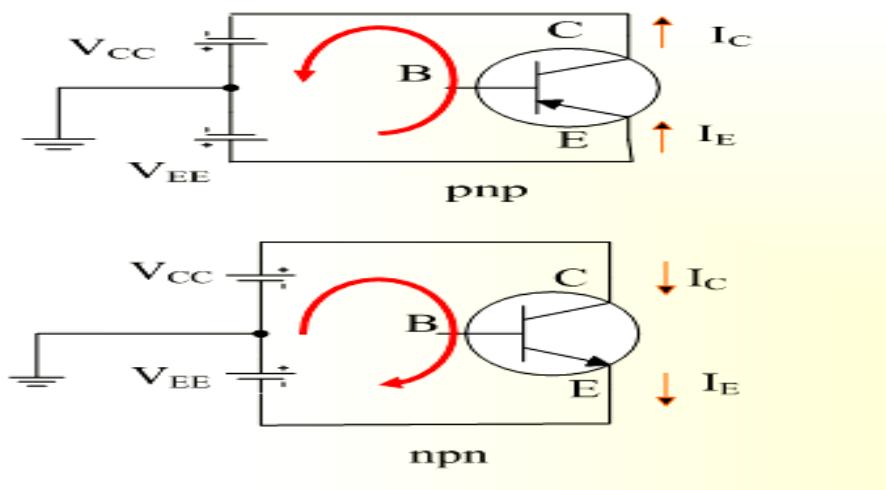
$$I_C = \alpha I_E + I_{CBO}$$

It can then be summarize to $I_C = \alpha I_E$ (ignore I_{CBO} due to small value)

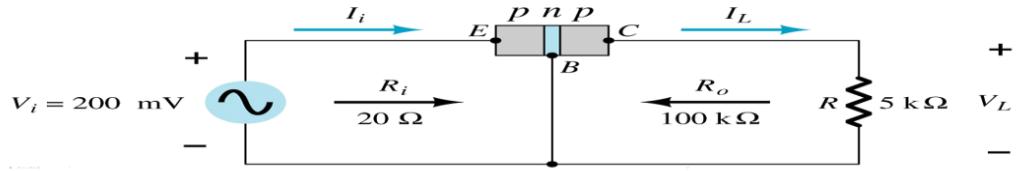
For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by α_{ac}

Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of α is typical from $0.9 \sim 0.998$.

Biassing: Proper biassing CB configuration in active region by approximation $I_C \approx I_E$ ($I_B \approx 0 \mu A$)



3.6 TRANSISTOR AS AN AMPLIFIER



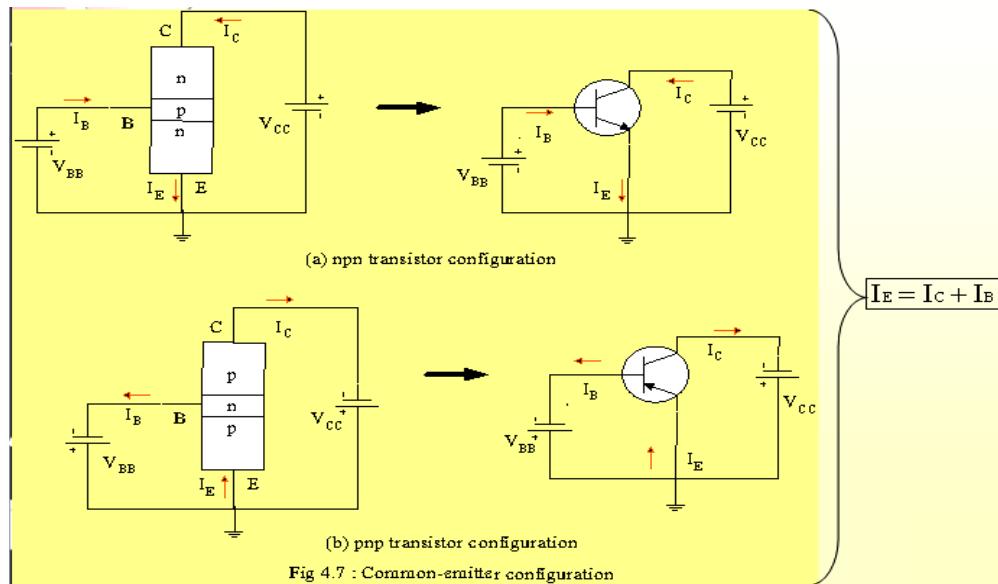
Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals.emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

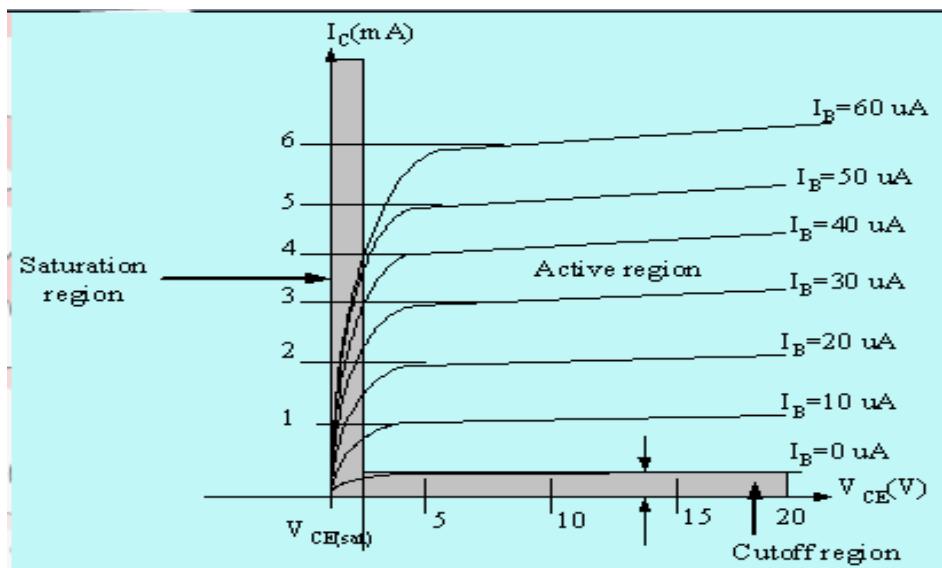
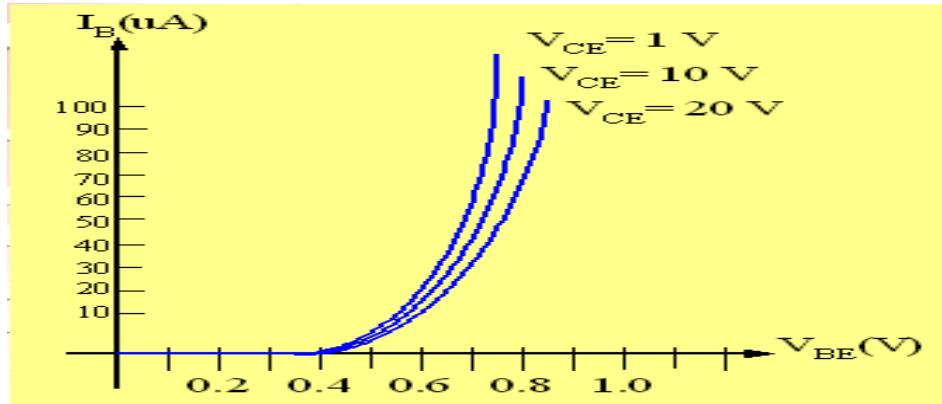


I_B is microamperes compared to miliamperes of I_C .

I_B will flow when $V_{BE} > 0.7V$ for silicon and $0.3V$ for germanium

Before this value I_B is very small and no I_B .

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.



Output characteristics for a common-emitter npn transistor

For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of V_{CE}

$V_{CE} > V_{CESAT}$ I_C not totally depends on $V_{CE} \rightarrow$ constant I_C

$I_B(uA)$ is very small compare to $I_C (mA)$. Small increase in I_B cause big increase in I_C

$I_B=0 A \rightarrow I_{CEO}$ occur.

Noticing the value when $I_C=0A$. There is still some value of current flows.

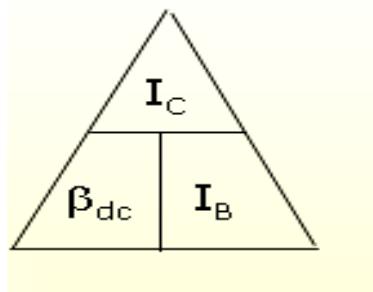
Active region	Saturation region	Cut-off region
<ul style="list-style-type: none"> B-E junction is forward bias C-B junction is reverse bias can be employed for voltage, current and power amplification 	<ul style="list-style-type: none"> B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. The value of V_{CE} is so small. Suitable region when the transistor as a logic switch. NOT and avoid this region when the transistor as an amplifier. 	<ul style="list-style-type: none"> region below $I_B=0\mu A$ is to be avoided if an undistorted o/p signal is required B-E junction and C-B junction is reverse bias $I_B=0$, I_C not zero, during this condition $I_C=I_{CEO}$ where is this current flow when B-E is reverse bias.

Beta (β) or amplification factor

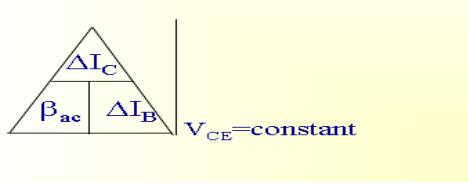
The ratio of dc collector current (I_C) to the dc base current (I_B) is dc beta (β_{dc}) which is dc current gain where I_C and I_B are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$$30 < \beta_{dc} < 300 \rightarrow 2N3904$$

On data sheet, $\beta_{dc}=hfe$ with h is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.



For ac conditions, an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point. On data sheet, $\beta_{ac}=hfe$ It can defined by the following equation:

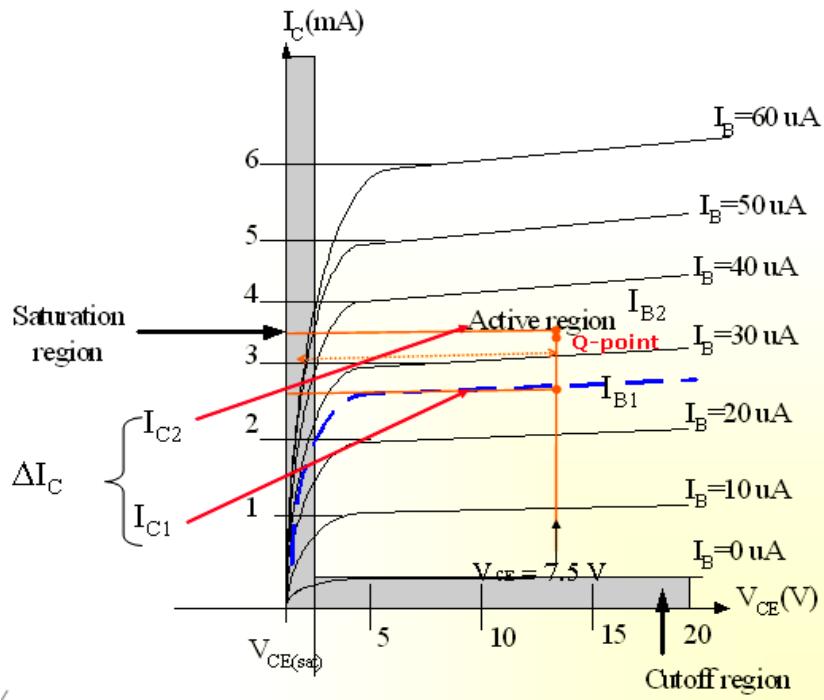


From output characteristics of commonemitter configuration, find β_{ac} and β_{dc} with an

Operating point at $I_B=25 \mu A$ and $V_{CE}=7.5V$

$$\begin{aligned}
 \beta_{ac} &= \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{CE} = \text{constant}} \\
 &= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2 \text{ mA} - 2.2 \text{ mA}}{30 \mu - 20 \mu} \\
 &= \frac{1 \text{ mA}}{10 \mu} = 100
 \end{aligned}$$

$$\begin{aligned}
 \beta_{dc} &= \frac{I_C}{I_B} \\
 &= \frac{2.7 \text{ mA}}{25 \mu} \\
 &= \underline{\underline{108}}
 \end{aligned}$$



Relationship analysis between α and β

CASE 1

$$I_E = I_C + I_B \quad (1)$$

substitute equ. $I_C = \beta I_B$ into (1) we get

$$\underline{\underline{I_E = (\beta + 1)I_B}}$$

CASE 2

$$\text{known} : \alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha} \quad (2)$$

$$\text{known} : \beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta} \quad (3)$$

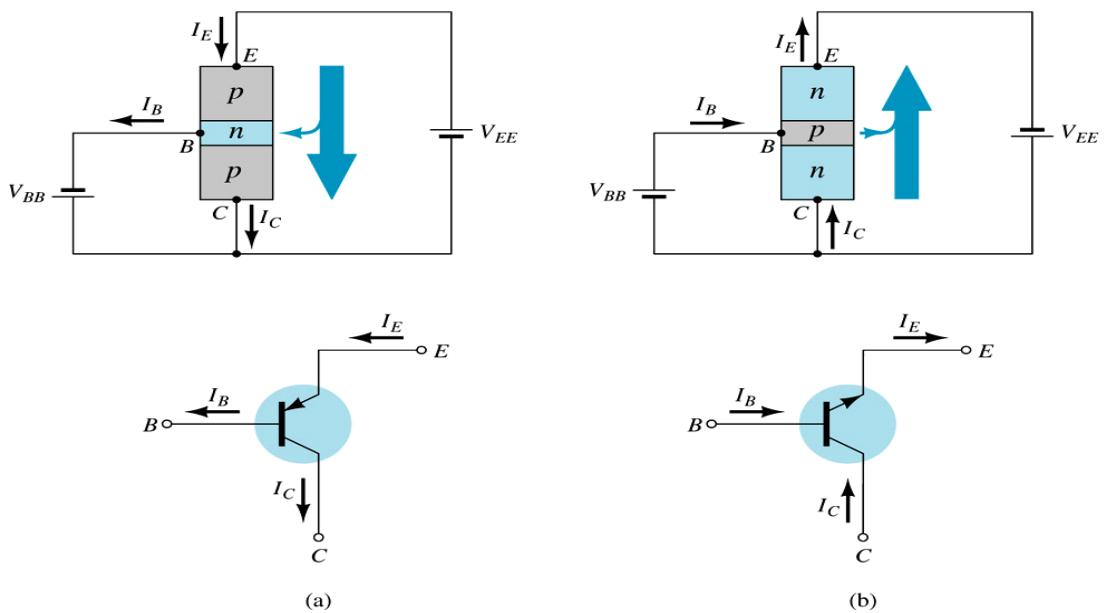
substitute (2) and (3) into (1) we get,

$$\underline{\underline{\alpha = \frac{\beta}{\beta + 1}}} \quad \text{and} \quad \underline{\underline{\beta = \frac{\alpha}{1 - \alpha}}}$$

3.7 COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal

source and the load share the collector terminal as a common connection point. The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is similar with common-emitter configuration. Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.



For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B .

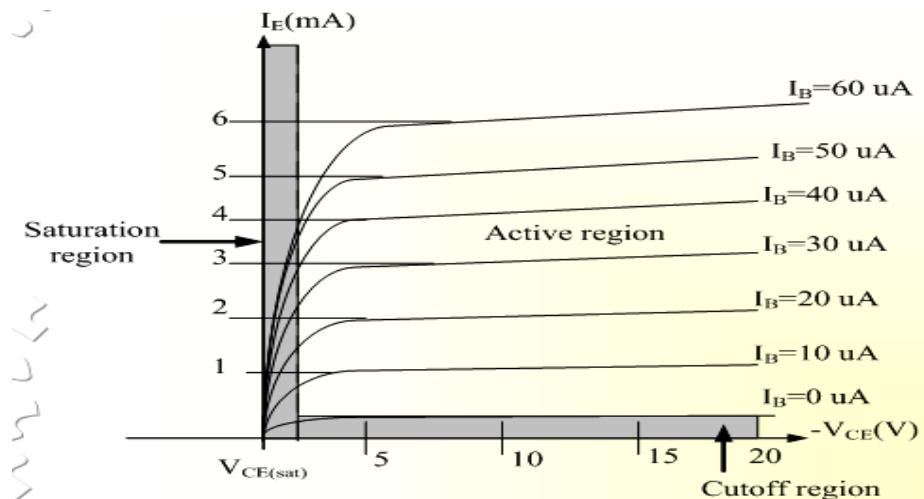


Fig 4.9 : Output characteristic in CC configuration for npn transistor

Limits of operation

Many BJT transistors are used as amplifiers. Thus it is important to notice the limits of operations. At least 3 maximum values are mentioned in data sheet.

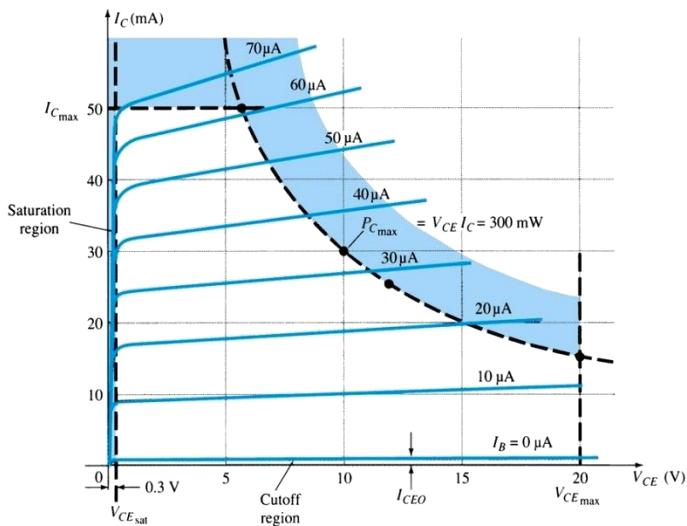
There are:

- Maximum power dissipation at collector: P_{Cmax} or P_D
- Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$ or V_{CEO} .
- Maximum collector current: I_{Cmax}

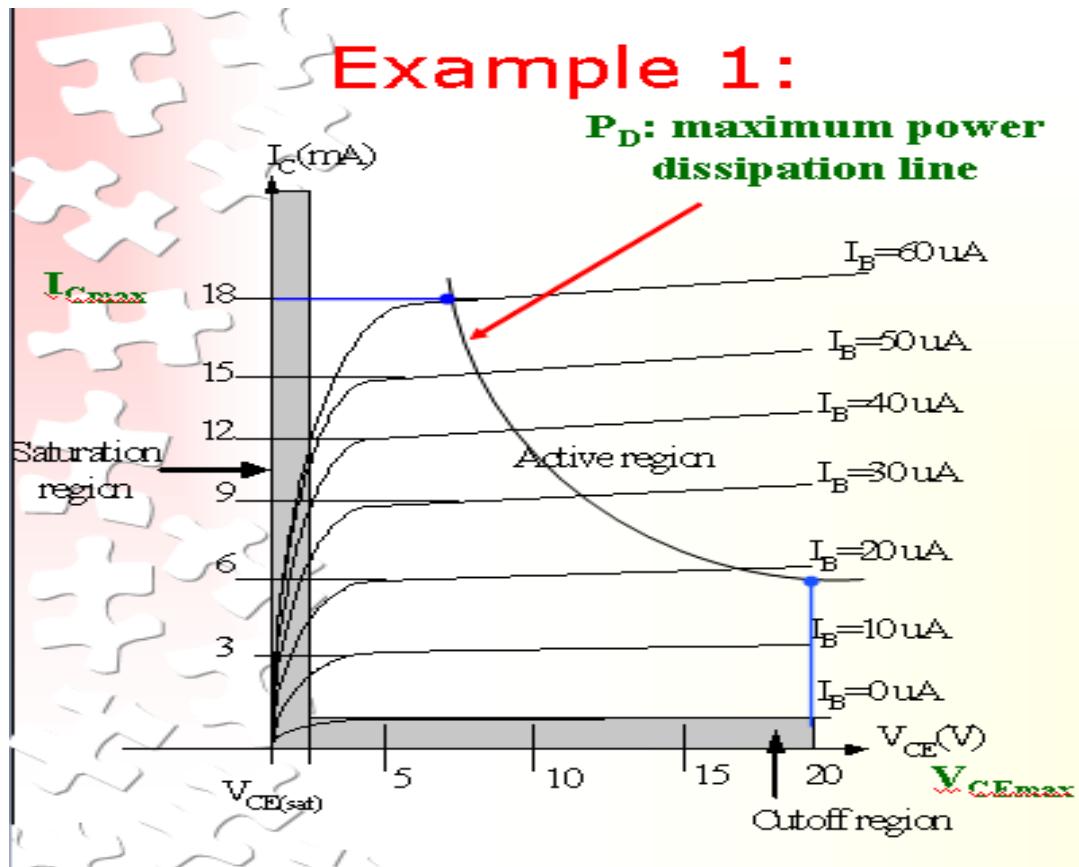
There are few rules that need to be followed for BJT transistors used as amplifiers. The rules are: transistor needs to operate in active region!

$$I_C < I_{Cmax}$$

$$P_C < P_{Cmax}$$



Note: V_{CE} is at maximum and I_C is at minimum ($I_{C\max}=I_{CEO}$) in the cutoff region. I_C is at maximum and V_{CE} is at minimum ($V_{CE\max}=V_{cesat}=V_{CEO}$) in the saturation region. The transistor operates in the active region between saturation and cutoff.



Refer to the fig. Example; A derating factor of $2\text{mW}/^\circ\text{C}$ indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Step 1:

The maximum collector power dissipation,

$$P_D = I_{C\text{MAX}} \times V_{CE\text{max}} = 18\text{mA} \times 20\text{V} = 360\text{mW}$$

Step 2:

At any point on the characteristics the product of and must be equal to 360mW .

Ex. 1. If choose $I_{C\text{max}} = 5\text{mA}$, substitute into the (1), we get

$$V_{CE\text{max}}I_{C\text{max}} = 360\text{mW}$$

$$V_{CE\text{max}}(5\text{mA}) = 360/5 = 7.2\text{V}$$

Ex.2. If choose $V_{CE\text{max}} = 18\text{V}$, substitute into (1), we get

$$V_{CE\text{max}}I_{C\text{max}} = 360\text{mW}$$

$$(10) I_{C\text{MAX}} = 360\text{mW} / 18\text{V} = 20\text{mA}$$

Derating $P_{D\text{max}}$

$P_{D\text{MAX}}$ is usually specified at 25°C .

The higher temperature goes, the less is $P_{D\text{MAX}}$

Example; A derating factor of $2\text{mW}/^\circ\text{C}$ indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

IV TRANSISTOR BIASING AND STABILIZATION

4.1 NEED FOR TRANSISTOR BIASING:

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

- 1) Emitter base junction must be forward biased ($V_{BE}=0.7V$ for Si, $0.2V$ for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
- 2) V_{ce} voltage should not fall below $V_{CE(sat)}$ ($0.3V$ for Si, $0.1V$ for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE(sat)}$ the collector base junction is not probably reverse biased.
- 3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current due to signal alone.
- 4) Max. rating of the transistor $I_{c(max)}$, $V_{CE(max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, $I_c=0$, $V_{CE} =0$. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

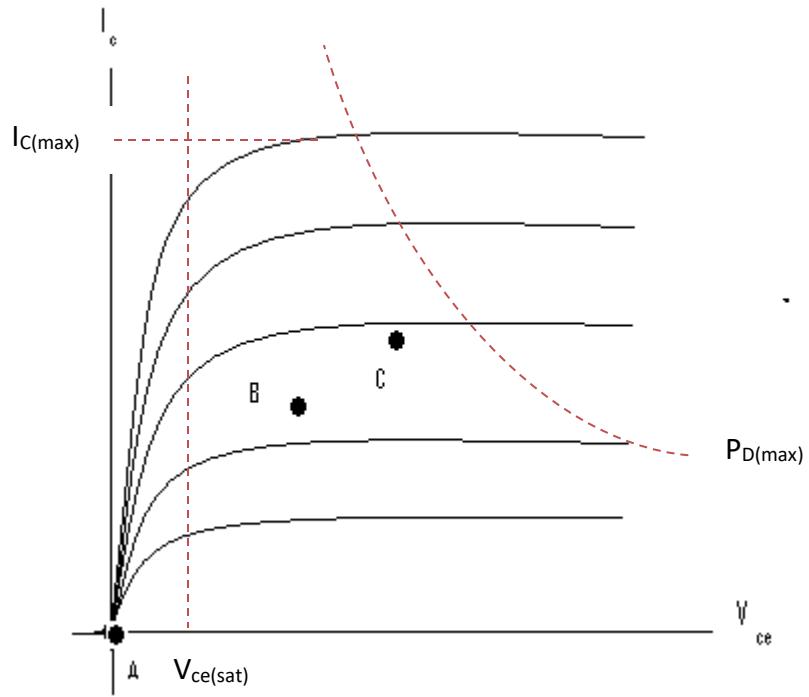


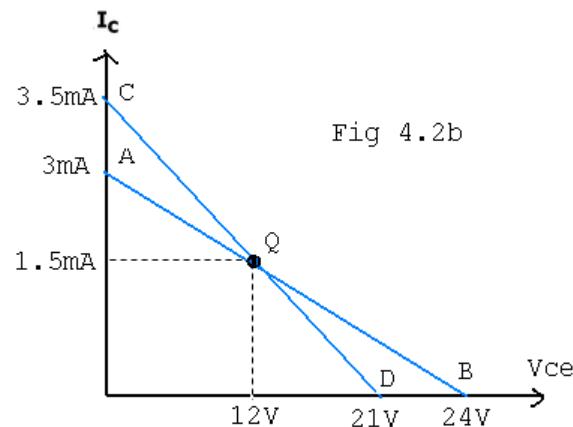
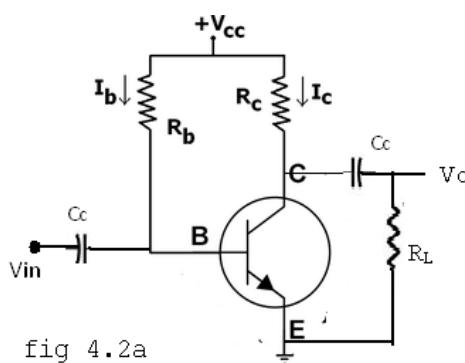
fig1

4.2 DC LOAD LINE:

Referring to the biasing circuit of fig 4.2a, the values of V_{CC} and R_C are fixed and I_C and V_{CE} are dependent on R_B .

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$V_{CC} = I_C R_C + V_{CE}$$



The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting $V_{CE} = 0$ in the above equation. Then $I_C = \frac{V_{CC}}{R_C}$.

Therefore The coordinates of A are $V_{CE} = 0$ and $I_C = \frac{V_{CC}}{R_C}$.

The coordinates of B are obtained by substituting $I_C = 0$ in the above equation. Then $V_{CE} = V_{CC}$. Therefore the coordinates of B are $V_{CE} = V_{CC}$ and $I_C = 0$. Thus the dc load line AB can be drawn if the values of R_C and V_{CC} are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

- 1) Reverse saturation current, I_{CO} , which doubles for every $10^\circ C$ raise in temperature
- 2) Base emitter Voltage , V_{BE} , which decreases by 2.5 mV per $^\circ C$
- 3) Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to V_{CC}/R_B . If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current I_C for a given I_B . Hence , in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

4.3 AC LOAD LINE:

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pass through the operating point Q. The effective ac load resistance R_{ac} , is a combination of R_C parallel to R_L i.e. $R_{ac} = R_L || R_C$. So the slope of the ac load line CQD will be $(\frac{-1}{R_{ac}})$. To draw the ac load line, two end points, i.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

$V_{CE(\max)} = V_{CEQ} + I_{CQ}R_{ac}$, which locates point D on the Vce axis.

$I_{c(\max)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the Ic axis.

By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than ac load line.

4.4 STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current I_{CO} . So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant}$$

$$\text{For CE configuration } I_C = \beta I_B + (1 + \beta) I_{CO}$$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{CO}}{dI_C}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C} \right) = \frac{(\beta + 1)}{S}$$

$$\therefore S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE} , keeping I_C and V_{BE} constant.

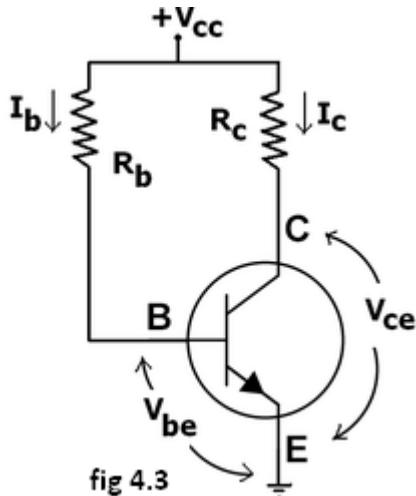
$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β , keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta}$$

4.5 METHODS OF TRANSISTOR BIASING:

1) Fixed bias (base bias)



This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$$V_{cc} = I_B R_B + V_{be}$$

$$\text{Therefore, } I_B = (V_{cc} - V_{be})/R_B$$

Since the equation is independent of current $I_C R$, $dI_B/dI_C R = 0$ and the stability factor is given by the equation..... reduces to

$$S=1+\beta$$

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used for biasing.

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_B , the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

Also for given circuit, $V_{cc} = I_C R_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_C R_C$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

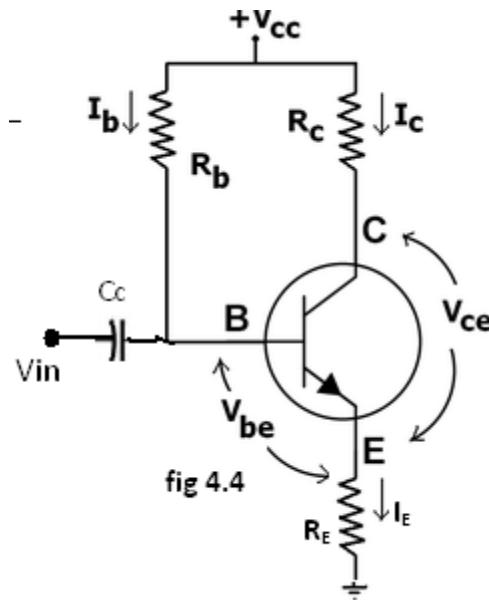
Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

2) Emitter-Feedback Bias:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$$V_{RB} = V_{CC} - I_E R_E - V_{be}$$



From Ohm's law, the base current is

$$I_b = V_{Rb} / R_b.$$

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_e R_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = \beta I_b$. Collector current and emitter current are related by $I_c = \alpha I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_c (corresponding to change in β -value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$$I_B = (V_{CC} - V_{be}) / (R_B + (\beta+1)R_E).$$

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β -value.

Demerits:

- In this circuit, to keep I_c independent of β the following condition must be met:

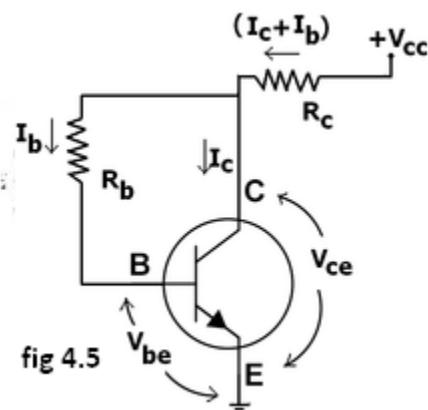
$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if $(\beta + 1)R_E \gg R_B$.

- As β -value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.

- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

3) COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:



This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{CC} . So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b} across the base resistor R_b is

$$V_{R_b} = V_{CC} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b + I_b}^{I_c}) R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b} across the base resistor R_b . A lower base-resistor voltage drop reduces the base current I_b , which results in less collector current I_c . Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β , the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

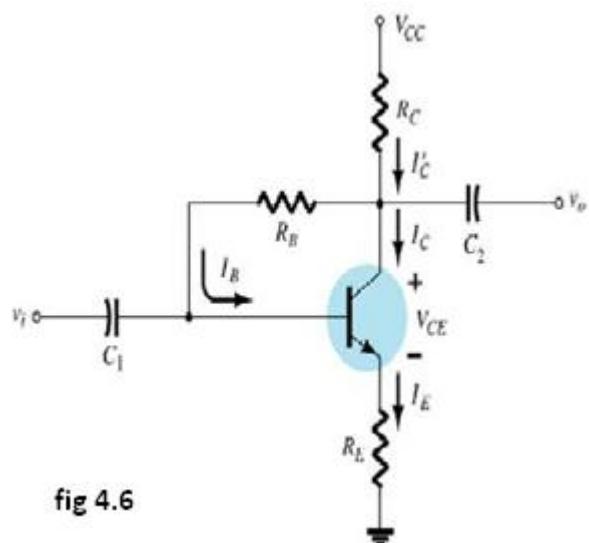
$$\beta R_c \gg R_b.$$

- As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
- If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.

- If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

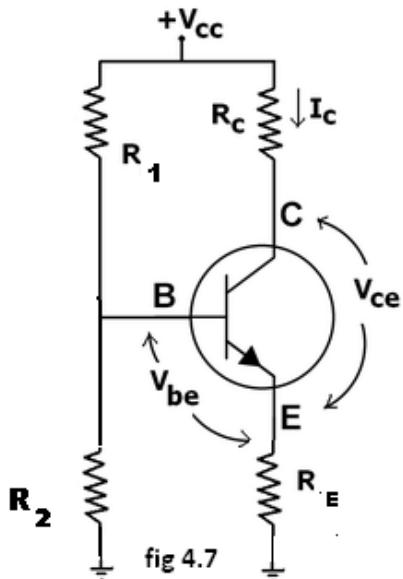
4) COLLECTOR –EMITTER FEEDBACK BIAS:



The above fig4.6 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

5) VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS:

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2 . The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2 , the operating point of the transistor can be made independent of β . In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.



In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc} \frac{R_2}{(R_1 + R_2)} - I_B \frac{R_1 R_2}{(R_1 + R_2)}$$

$$\approx V_{cc} \frac{R_2}{(R_1 + R_2)} \text{ provided } I_B \ll I_2 = V_B / R_2.$$

$$\text{Also } V_B = V_{be} + I_E R_E$$

For the given circuit,

$$I_B = \frac{\frac{V_{cc}}{1+R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R_1 is I_1 and this is divided into two parts – current through base and resistor R_2 . Since the base current is very small so for all practical purpose it is assumed that I_1 also flows through R_2 , so we have

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{V_2 - V_{BE}}{R_R} \quad \because I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of V_{BE} thus the stability is excellent. In all practical cases the value of V_{BE} is quite small in comparison to the V_2 , so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\therefore I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor R_E provides stability to the circuit. If the current through the collector rises, the voltage across the resistor R_E also rises. This will cause V_{CE} to increase as the voltage V_2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1 + \beta)(R_{eq} + R_E)}{R_{eq} + R_E(1 + \beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1 + \beta) \left(1 + \frac{R_{eq}}{R_E} \right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If R_{eq}/R_E is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1 + \beta}{1 + \beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since R_{eq}/R_E cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta + 1)R_E \gg R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β -value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \parallel R_2$ very low.
 - If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
 - If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C , reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be} , reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_E , which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

4.6 BIAS COMPENSATION USING DIODE AND TRANSISTOR:

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for variations in current.

DIODE COMPENSATION:

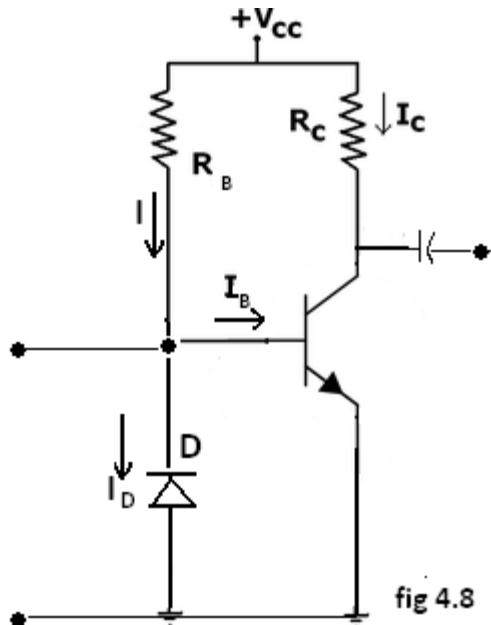


fig 4.8

The following fig4.8 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current I_{CO} . The diode is of the same material as the transistor and it is reverse biased by the emitter-base junction voltage V_{BE} , allowing the diode reverse saturation current I_0 to flow through diode D. The base current $I_B=I-I_0$.

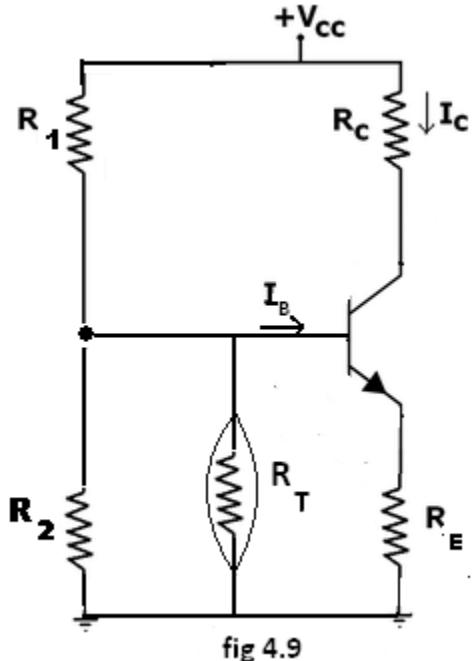
As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_0 through D to increase and thereby decrease the base current I_B . This is the required action to keep I_c constant.

This type of bias compensation does not need a change in I_c to effect the change in I_c , as both I_0 and I_{CO} can track almost equally according to the change in temperature.

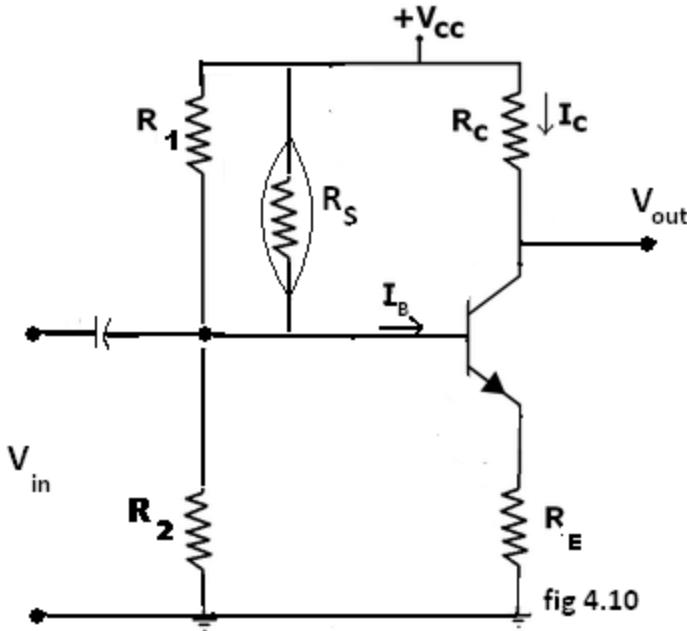
THERMISTOR COMPENSATION:

The following fig4.9 a thermistor R_T , having a negative temperature coefficient is connected in parallel with R_2 . The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage V_{BE} , reducing I_B and I_C .



SENSISTOR COMPENSATION:

In the following fig4.10 shown a sensistor R_s having a positive temperature coefficient is connected across R_1 or R_E . R_s increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R_1 and R_s also increases and hence V_{BE} decreases, reducing I_B and I_c . This reduced I_c compensates for increased I_c caused by the increase in V_{BE} , I_{CO} and β due to temperature.



4.7 THERMAL RUNAWAY AND THERMAL STABILITY:

THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_c = \beta I_B + (1 + \beta)I_{CO}$. The three variables in the equation, β , I_B , and I_{CO} increases with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature. Specifically it doubles for every 10°C rise in temperature. The collector current I_c causes the collector base junction temperature to rise which in turn, increase I_{CO} , as a result I_c will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to “*thermal runaway*”. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the $(1 + \beta)I_{CO}$, keeping I_c almost constant.

THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is T_A °C and the temperature of the collector-base junction of the transistor is T_J °C.

Due to heating within the transistor T_J is higher than T_A . As the temperature difference $T_J - T_A$ is greater, the power dissipated in the transistor, P_D will be greater, i.e., $T_J - T_A \propto P_D$

The equation can be written as $T_J - T_A = \Theta P_D$, where Θ is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation $\Theta = (T_J - T_A) / P_D$. Hence Θ is measured in °C/W which may be as small as 0.2 °C/W for a high power transistor that has an efficient heat sink or up to 1000°C/W for small signal, low power transistor which have no cooling provision.

As Θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as Θ_{J-A} . However, for power transistors, thermal resistance is given from junction to case, Θ_{J-C} .

The amount resistance from junction to ambience is considered to consist of 2 parts.

$$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A}$$

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence the power dissipated.

$$\begin{aligned} P_D &= (T_J - T_A) / \Theta_{J-A} \\ &= (T_J - T_A) / (\Theta_{J-C} + \Theta_{C-A}) \end{aligned}$$

Θ_{J-C} is determined by the type of manufacture of the transistor and how it is located in the case, but Θ_{C-A} is determined by the surface area of the case or flange and its contact with air. If the effective surface area of the transistor case could be increased, the resistance to heat flows, or could be increased Θ_{C-A} , could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance Θ_{HS-A} .

This thermal resistance is not added to Θ_{C-A} in series, but is instead in parallel with it and if

Θ_{HS-A} is much less than Θ_{C-A} , then Θ_{C-A} will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

$$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \parallel \Theta_{HS-A}$$

4.8 CONDITION FOR THERMAL STABILITY:

For preventing thermal runaway, the required condition is the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$$P_C = I_C V_{CB} \approx I_C V_{CE}$$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$$P_C = I_C V_{CC} - I_C^2 (R_E + R_C) \dots \dots \dots (1)$$

The condition to prevent thermal runaway can be written as

As Θ and $\frac{\partial I_{Cj}}{\partial T_j}$ are positive, $\frac{\partial P_{Cj}}{\partial I_{Cj}}$ should be negative in order to satisfy the above condition.

Differentiating equation (1) w.r.t I_C we get

Hence to avoid thermal runaway it is necessary that

Since $VCE = VCC - IC(R_E + RC)$ then eq(4) implies that $VCE < VCC/2$. IF the inequality of eq(4) is not satisfied and $VCE < VCC/2$, then from eq(3), $\frac{\partial P_C}{\partial I_C}$ is positive., and the corresponding eq(2) should be satisfied. Other wise thermal runaway will occur.

UNIT I

SINGLE STAGE AMPLIFIERS

1.1 Introduction

V-I characteristics of an active device such as BJT are non-linear. The analysis of a non- linear device is complex. Thus to simplify the analysis of the BJT, its operation is restricted to the linear V-I characteristics around the Q-point i.e. in the active region. This approximation is possible only with small input signals. With small input signals transistor can be replaced with small signal linear model. This model is also called small signal equivalent circuit.

1.2 Two -Port Devices and Network Parameters

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

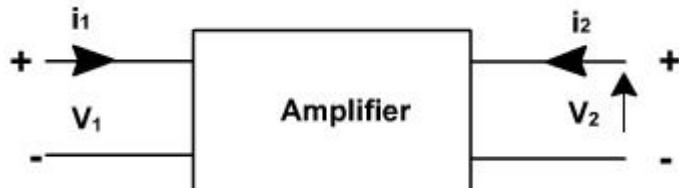


Fig. 1

A two-port network is represented by four external variables: voltage V_1 and current I_1 at the input port, and voltage V_2 and current I_2 at the output port, so that the two-port network can be treated as a black box modeled by the relationships between the four variables, V_1, V_2, I_1, I_2 . Out of four variables two can be selected as independent variables and two are dependent variables. The dependent variables can be expressed in terms of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters (h-parameters)
- 4.

1.1.1 z-parameters

A two-port network can be described by z-parameters as

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

$$z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0}$$

Input impedance with output port open circuited

$$z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0}$$

Output impedance with input port open circuited

1.1.2 Y-parameters

A two-port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}$$

Input admittance with output port short circuited

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}$$

Reverse transfer admittance with input port short circuited

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}$$

Forward transfer admittance with output port short circuited

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

Output admittance with input port short circuited

1.1.3 Hybrid parameters (h-parameters)

If the input current I_1 and output voltage V_2 are taken as independent variables, the dependent variables V_1 and I_2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where $h_{11}, h_{12}, h_{21}, h_{22}$ are called as hybrid parameters.

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$$

Input impedance with o/p port short circuited

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

output impedance with i/p port open circuited

1.2 THE HYBRID MODEL FOR TWO PORT NETWORK:

Based on the definition of hybrid parameters the mathematical model for two port networks known as h-parameter model can be developed. The hybrid equations can be written as:

$$V_1 = h_i I_1 + h_r V_2$$

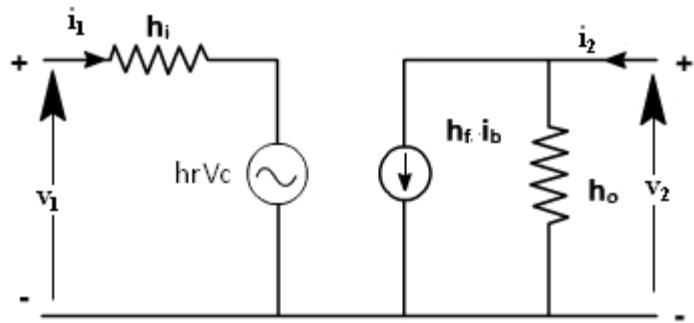
$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended by the IEEE Standards:

i=11= input o = 22 = output

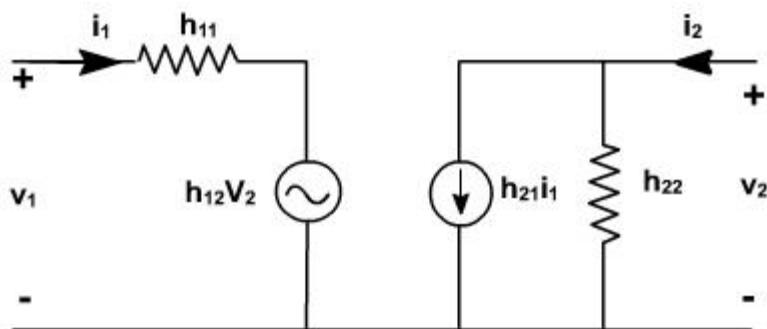
f=21 = forward transfer r = 12 = reverse transfer)

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff's voltage and current laws for input and output ports.



If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} , h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in [fig. 2](#).



[Fig. 2](#)

1.2.1 TRANSISTOR HYBRID MODEL:

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in [fig. 3](#). The variables, i_B , i_C , v_C , and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B , I_C as dependent variables.

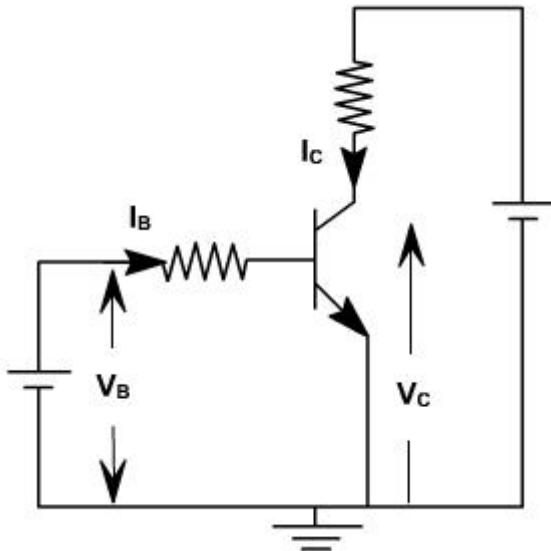


Fig. 3

$$V_B = f_1(i_B, v_C)$$

$$I_C = f_2(i_B, v_C).$$

Using Taylor's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \frac{\partial f_1}{\partial i_B} \Big|_{v_C} \Delta i_B + \frac{\partial f_1}{\partial v_C} \Big|_{i_B} \Delta v_C$$

$$\Delta i_C = \frac{\partial f_2}{\partial i_B} \Big|_{v_C} \Delta i_B + \frac{\partial f_2}{\partial v_C} \Big|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B , Δv_C , Δi_B , Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as v_B , i_C , i_B , v_C

$$\therefore v_B = h_{ie} i_B + h_{re} v_C$$

$$i_C = h_{fe} i_B + h_{oe} v_B$$

where

$$h_{ie} = \frac{\partial f_1}{\partial i_B} \Big|_{v_C} = \frac{\partial v_B}{\partial i_B} \Big|_{v_C}; \quad h_{re} = \frac{\partial f_1}{\partial v_C} \Big|_{i_B} = \frac{\partial v_B}{\partial v_C} \Big|_{i_B}$$

$$h_{fe} = \frac{\partial f_2}{\partial i_B} \Big|_{v_C} = \frac{\partial i_C}{\partial i_B} \Big|_{v_C}; \quad h_{oe} = \frac{\partial f_2}{\partial v_C} \Big|_{i_B} = \frac{\partial i_C}{\partial v_C} \Big|_{i_B}$$

The model for CE configuration is shown in fig. 4.

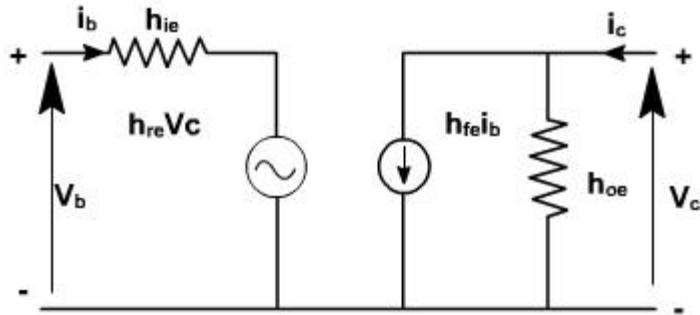


Fig. 4

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. [Fig. 5](#), shows the output characteristics of CE amplifier.

$$h_{re} = \left. \frac{\partial i_c}{\partial i_b} \right|_{V_C} = \frac{i_{c2} - i_{c1}}{i_{b2} - i_{b1}}$$

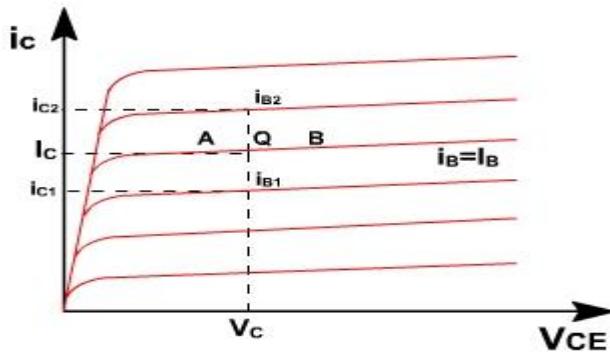


Fig. 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left. \frac{\partial i_c}{\partial V_C} \right|_{i_b}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \left. \frac{\partial V_B}{\partial i_b} \right|_{V_C} \approx \left. \frac{\Delta V_B}{\Delta i_b} \right|_{V_C}$$

h_{ie} is the slope of the appropriate input on [fig. 6](#), at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left. \frac{\Delta V_B}{\Delta V_C} \right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

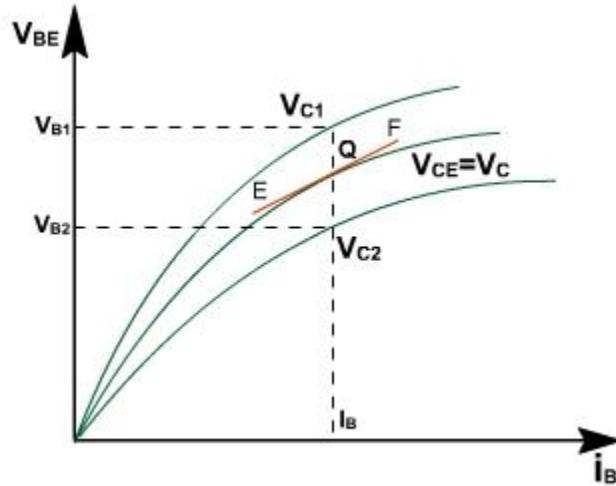


Fig. 6

A vertical line on the input characteristic represents constant base current. The parameter h_{re} can be obtained from the ratio $(V_{B2} - V_{B1})$ and $(V_{C2} - V_{C1})$ for at Q.

Typical CE h-parameters of transistor 2N1573 are given below:

$$h_{ie} = 1000 \text{ ohm.}$$

$$h_{re} = 2.5 * 10^{-4}$$

$$h_{fe} = 50$$

$$h_{oe} = 25 \text{ mA/V}$$

1.3 ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in [fig. 1](#) and to bias the transistor properly.

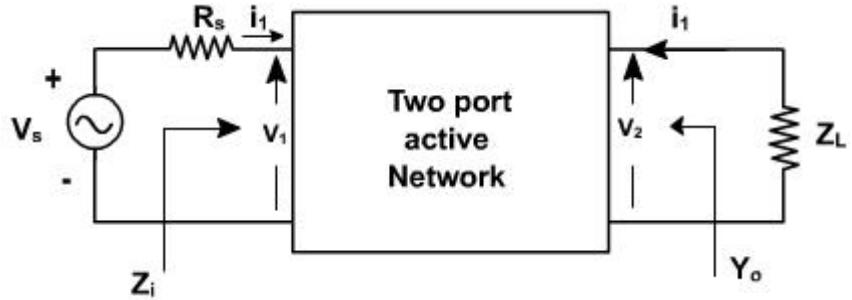


Fig. 1

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedance h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in [fig. 2](#). (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedance, voltage gain, and output impedance.

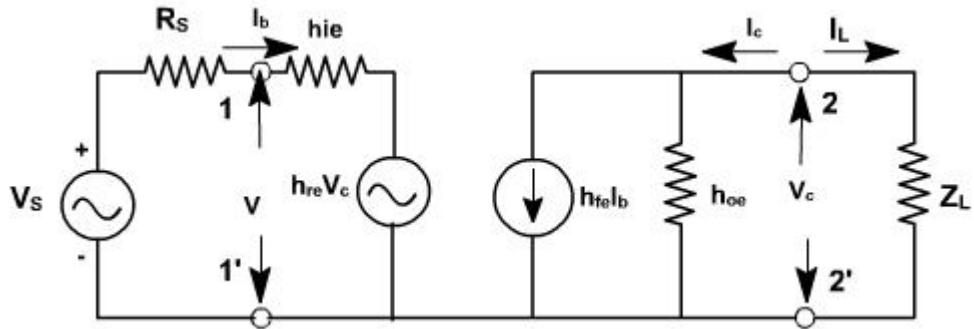


Fig. 2

1.3.1 Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

1.3.2 Input impedance:

The impedance looking into the amplifier input terminals (1,1') is the input impedance Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_i Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \quad (\text{since } Y_L = \frac{1}{Z_L})$$

1.3.3 Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_c}{V_b} = -\frac{I_c Z_L}{V_b}$$

$$\therefore A_v = \frac{I_b A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

1.3.4 Output Admittance:

It is defined as

$$Y_0 = \frac{I_o}{V_c} \Big|_{V_s} = 0$$

$$I_o = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_o}{V_c} = h_{fe} \frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $R_s \cdot I_b + h_{ie} \cdot I_b + h_{re} V_c = 0$.

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_s) is given by

$$\begin{aligned} A_{Vs} &= \frac{V_o}{V_s} = \frac{V_o}{V_b} + \frac{V_b}{V_s} \quad \left(V_b = \frac{V_s}{R_s + Z_i} \cdot Z_i \right) \\ &= A_v \cdot \frac{Z_i}{Z_i + R_s} \\ &= \frac{A_v Z_L}{Z_i + R_s} \end{aligned}$$

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_s in parallel with a resistance R_s as shown in [fig. 3](#).

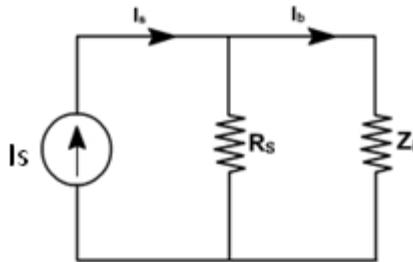


Fig. 3

In this case, overall current gain A_{Is} is defined as

$$\begin{aligned} A_{Is} &= \frac{I_L}{I_s} \\ &= -\frac{I_o}{I_s} \\ &= -\frac{I_o}{I_b} \cdot \frac{I_b}{I_s} \quad \left(I_b = \frac{I_s \cdot R_s}{R_s + Z_i} \right) \\ &= A_I \cdot \frac{R_s}{R_s + Z_i} \end{aligned}$$

If $R_s \rightarrow \infty$, $A_{Is} \rightarrow A_I$

h-parameters

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example fig. 4 hrc in terms of CE parameter can be obtained as follows.

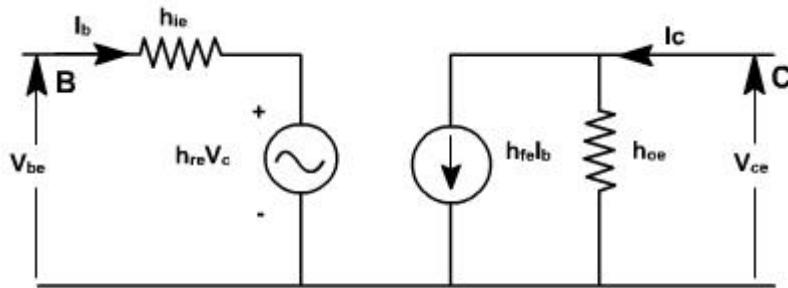


Fig. 4

For CE transistor configuration

$$V_{be} = h_{ie} I_b + h_{re} V_{ce}$$

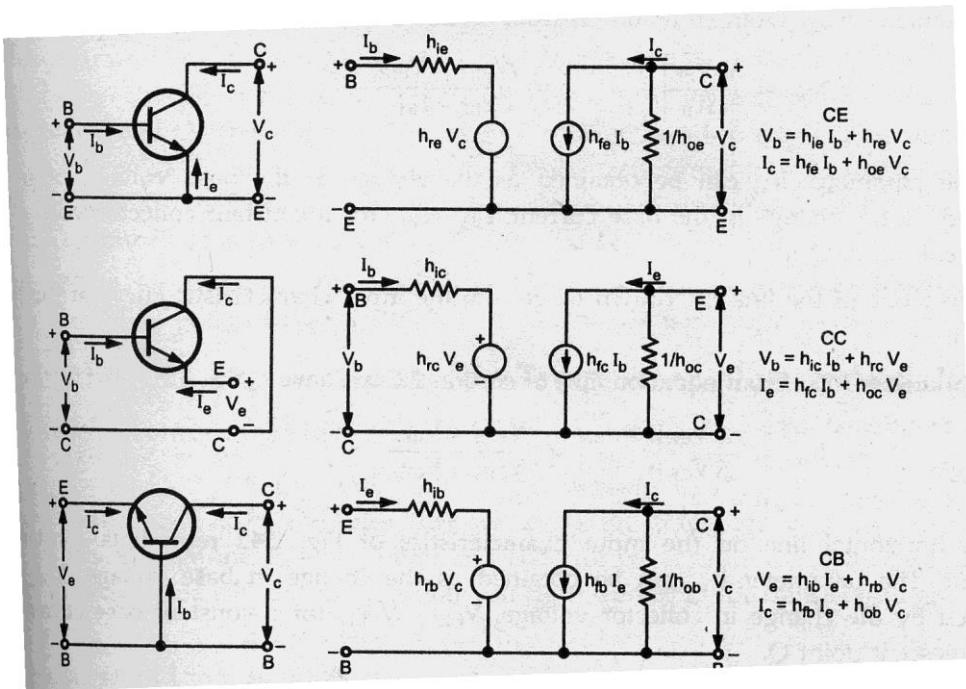
$$I_c = h_{fe} I_b + h_{oe} V_{ce}$$

The circuit can be redrawn like CC transistor configuration as shown in fig. 5.

$$V_{bc} = h_{ie} I_b + h_{rc} V_{ce}$$

$$I_c = h_{fe} I_b + h_{oc} V_{ce}$$

hybrid model for transistor in three different configurations



Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100Ω	1100Ω	22Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	$25 \mu\text{A/V}$	$25 \mu\text{A/V}$	$0.49 \mu\text{A/V}$

Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

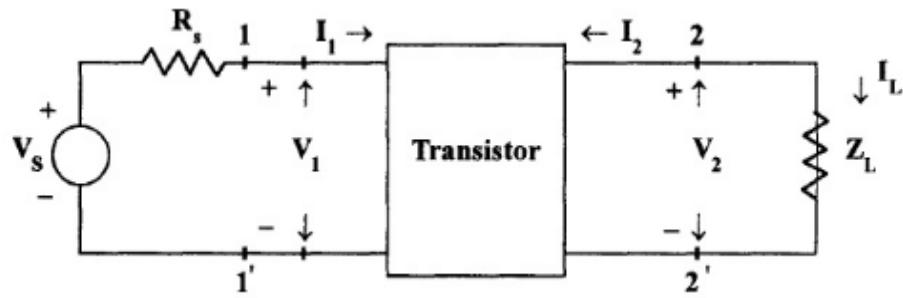


Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range. The input is sinusoidal and I_1, V_1, I_2 and V_2 are phase quantities

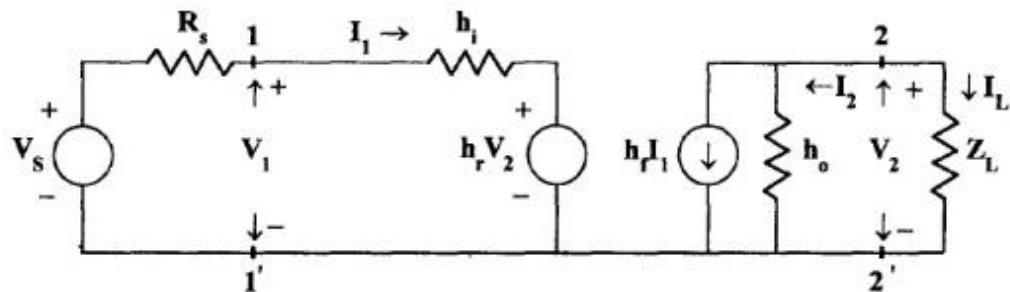


Fig. 1.5 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current, i.e.,

$$A_i = I_L / I_1 = -I_2 / I_1$$

From the circuit of Fig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1 + Z_L h_o) = h_f I_1$$

$$A_i = -I_2 / I_1 = -h_f / (1 + Z_L h_o)$$

Therefore,

$$A_i = -h_f / (1 + Z_L h_o)$$

Input Impedance (Z_i)

In the circuit of Fig , R_s is the signal source resistance .The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance Z_i ,

$$Z_i = V_1 / I_1$$

From the input circuit of Fig $V_1 = h_i I_1 + h_r V_2$

$$Z_i = (h_i I_1 + h_r V_2) / I_1$$

$$= h_i + h_r V_2 / I_1$$

Substituting

$$V_2 = -I_2 Z_L = A_i I_1 Z_L$$

$$Z_i = h_i + h_r A_i I_1 Z_L / I_1$$

$$= h_i + h_r A_i Z_L$$

Substituting for A_i

$$Z_i = h_i - h_f h_r Z_L / (1 + h_o Z_L)$$

$$= h_i - h_f h_r Z_L / Z_L (1/Z_L + h_o)$$

Taking the Load admittance as $Y_L = 1/Z_L$

$$Z_i = h_i - h_f h_r / (Y_L + h_o)$$

Voltage Gain or Voltage Gain Amplification Factor(A_v)

The ratio of output voltage V_2 to input voltage V_1 give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_1 Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_s to zero, Z_L to infinity and by driving the output terminals from a generator V_2 . If the current V_2 is I_2 then $Y_o = I_2/V_2$ with $V_s=0$ and $R_L=\infty$.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2 ,

$$I_2 / V_2 = h_f I_1 / V_2 + h_o$$

With $V_2=0$, by KVL in input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$(R_s + h_i) I_1 + h_r V_2 = 0$$

$$\text{Hence, } I_2 / V_2 = -h_r / (R_s + h_i)$$

$$= h_f (-h_r / (R_s + h_i)) + h_o$$

$$Y_o = h_o - h_f h_r / (R_s + h_i)$$

The output admittance is a function of source resistance. If the source impedance is resistive then Y_o is real.

Voltage Amplification Factor(A_{vs}) taking into account the resistance (R_s) of the source

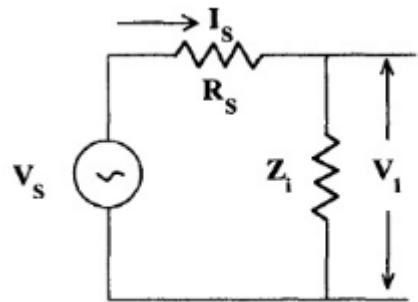


Fig. 5.6 Thevenin's Equivalent Input Circuit

This overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_s = V_2 V_1 / V_1 V_s = A_v V_1 / V_s$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$$V_1 = V_s Z_i / (Z_i + R_s)$$

$$V_1 / V_s = Z_i / (Z_i + R_s)$$

$$\text{Then, } A_{vs} = A_v Z_i / (Z_i + R_s)$$

$$\text{Substituting } A_v = A_i Z_L / Z_i$$

$$A_{vs} = A_i Z_L / (Z_i + R_s)$$

$$A_{vs} = A_i Z_L R_s / (Z_i + R_s) R_s$$

$$A_{vs} = A_{is} Z_L / R_s$$

Current Amplification (A_{is}) taking into account the source Resistance(R_s)

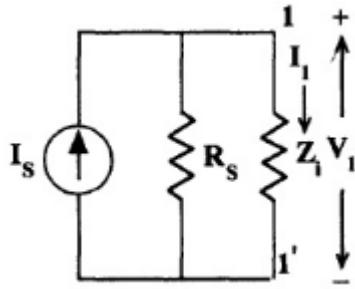


Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7

$$\text{Overall Current Gain, } A_{is} = -I_2 / I_s = -I_2 I_1 / I_1 I_s = A_i I_1 / I_s$$

$$\text{From Fig. 1.7 } I_1 = I_s R_s / (R_s + Z_i)$$

$$I_1 / I_s = R_s / (R_s + Z_i)$$

$$\text{and hence, } A_{is} = A_i R_s / (R_s + Z_i)$$

Operating Power Gain (A_p)

The operating power gain A_p of the transistor is defined as

$$A_p = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$$

$$A_p = A_i^2 (Z_L / Z_i)$$

Small Signal analysis of a transistor amplifier

$A_i = -h_f / (1 + Z_L h_o)$	$A_v = A_i Z_L / Z_i$
$Z_i = h_i + h_r$ $A_i Z_L = h_i - h_f h_r / (Y_L + h_o)$	$A_{vs} = A_v Z_i / (Z_i + R_s) = A_i Z_L / (Z_i + R_s)$ $= A_{is} Z_L / R_s$
$Y_o = h_o - h_f h_r / (R_s + h_i) = 1 / Z_o$	$A_{is} = A_i R_s / (R_s + Z_i) = A_{vs} = A_{is} R_s / Z_L$

Simplified common emitter hybrid model:

In most practical cases it is appropriate to obtain approximate values of A_V , A_i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig. 4** shows the CE amplifier equivalent circuit in terms of h-parameters. Since $1/h_{oe}$ in parallel with R_L is approximately equal to R_L if $1/h_{oe} \gg R_L$ then h_{oe} may be neglected. Under these conditions.

$$I_c = h_{fe} I_B .$$

$$h_{re} V_c = h_{re} I_c R_L = h_{re} h_{fe} I_B R_L .$$

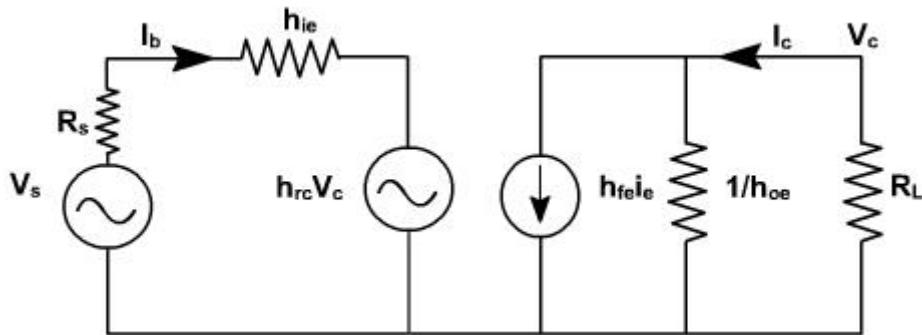


Fig. 4

Since $h_{fe} \cdot h_{re} = 0.01$ (approximately), this voltage may be neglected in comparison with $h_{ic} I_b$ drop across h_{ie} provided R_L is not very large. If load resistance R_L is small than h_{oe} and h_{re} can be neglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe} R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedance seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we find $I_b = 0$, $I_c = 0$. True value depends upon R_s and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

CE amplifier with an emitter resistor:

The voltage gain of a CE stage depends upon h_{fe} . This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_v of each stage, it should be

independent of h_{fe} . A simple and effective way is to connect an emitter resistor R_e as shown in [fig. 5](#). The resistor provides negative feedback and provide stabilization.

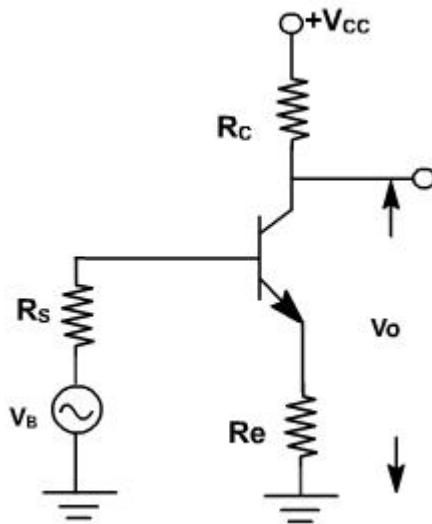


Fig. 5

An approximate analysis of the circuit can be made using the simplified model.

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe} I_b}{I_b} = -h_{fe}$$

It is unaffected by the addition of R_C .

Input resistance is given by

$$\begin{aligned} R_i &= \frac{V_i}{I_b} \\ &= \frac{h_{ie} I_b + (1+h_{fe}) I_b R_e}{I_b} \\ &= h_{ie} + (1+h_{fe}) R_e \end{aligned}$$

The input resistance increases by $(1+h_{fe}) R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe} R_L}{h_{ie} + (1+h_{fe}) R_e}$$

Clearly, the addition of R_e reduces the voltage gain.

If $(1+h_{fe}) R_e \gg h_{ie}$ and $h_{fe} \gg 1$

then

$$A_v = \frac{-h_{fe} R_L}{(1+h_{fe}) R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation A_v is completely stable. The output resistance is infinite for the approximate model.

Comparison of Transistor Amplifier Configuration

The characteristics of three configurations are summarized in Table .Here the quantities A_i, A_v, R_i, R_o and A_p are calculated for a typical transistor whose h-parameters are given in table .The values of R_L and R_s are taken as $3\text{K}\Omega$.

Table: Performance schedule of three transistor configurations

Quantity	CB	CC	CE
A_i	0.98	47.5	-46.5
A_v	131	0.989	-131
A_p	128.38	46.98	6091.5
R_i	22.6Ω	$144 \text{ k}\Omega$	1065Ω
R_o	$1.72 \text{ M}\Omega$	80.5Ω	$45.5 \text{ k}\Omega$

The values of current gain, voltage gain, input impedance and output impedance calculated as a function of load and source impedances

Characteristics of Common Base Amplifier

- (i) Current gain is less than unity and its magnitude decreases with the increase of load resistance R_L ,
- (ii) Voltage gain A_v is high for normal values of R_L ,
- (iii) The input resistance R_i is the lowest of all the three configurations, and
- (iv) The output resistance R_o is the highest of all the three configurations.

Applications The CB amplifier is not commonly used for amplification purpose. It is used for

- (i) Matching a very low impedance source
- (ii) As a non inverting amplifier to voltage gain exceeding unity.
- (iii) For driving a high impedance load.

(iv) As a constant current source.

Characteristics of Common Collector Amplifier

- (i) For low R_L ($< 10 \text{ k}\Omega$), the current gain A_i is high and almost equal to that of a CE amplifier.
- (ii) The voltage gain A_v is less than unity.
- (iii) The input resistance is the highest of all the three configurations.
- (iv) The output resistance is the lowest of all the three configurations.

Applications: The CC amplifier is widely used as a buffer stage between a high impedance source and a low impedance load.

Characteristics of Common Emitter Amplifier

- (i) The current gain A_i is high for $R_L < 10 \text{ k}\Omega$.
- (ii) The voltage gain is high for normal values of load resistance R_L .
- (iii) The input resistance R_i is medium.
- (iv) The output resistance R_o is moderately high.

Applications: CE amplifier is widely used for amplification.

Simplified common emitter hybrid model:

In most practical cases it is appropriate to obtain approximate values of A_v , A_i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig 1. 8** shows the CE amplifier equivalent circuit in terms of h-parameters. Since $1/h_{oe}$ is parallel with R_L is approximately equal to R_L if $1/h_{oe} \gg R_L$ then h_{oe} may be neglected. Under these conditions.

$$I_c = h_{fe} I_B .$$

$$h_{re} v_c = h_{re} I_c R_L = h_{re} h_{fe} I_b R_L .$$

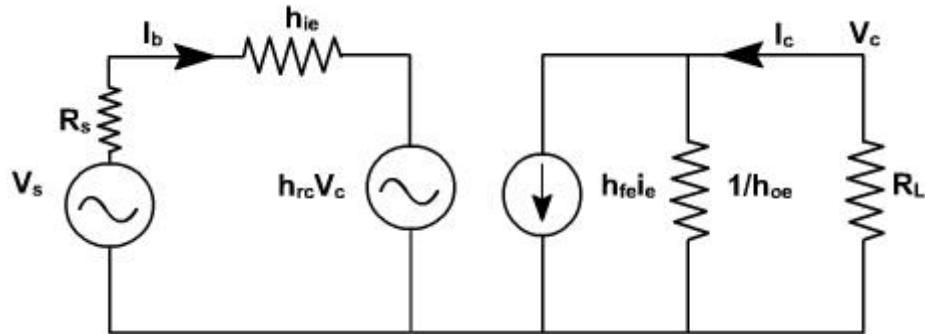


Fig 1.8

Since $h_{fe} \cdot h_{re} \gg 0.01$, this voltage may be neglected in comparison with $h_{ic} I_b$ drop across h_{ie} provided R_L is not very large. If load resistance R_L is small than h_{oe} and h_{re} can be neglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe} R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedance seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we find $I_b = 0$, $I_c = 0$. True value depends upon R_s and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

CE amplifier with an emitter resistor:

The voltage gain of a CE stage depends upon h_{fe} . This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_v of each stage, it should be independent of h_{fe} . A simple and effective way is to connect an emitter resistor R_e as shown in fig.1.9. The resistor provides negative feedback and provide stabilization.

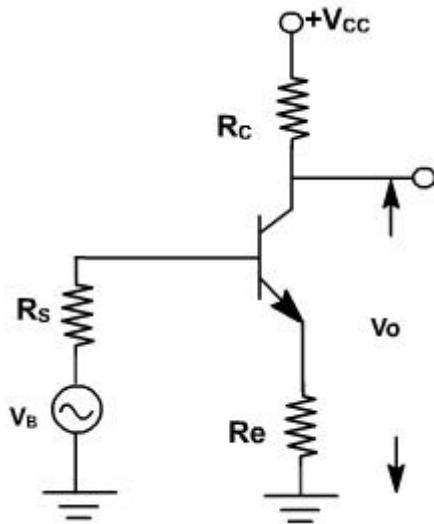


Fig.1.9

An approximate analysis of the circuit can be made using the simplified model.

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe} I_b}{I_b} = -h_{fe}$$

It is unaffected by the addition of R_C .

Input resistance is given by

$$\begin{aligned} R_i &= \frac{V_i}{I_b} \\ &= \frac{h_{ie} I_b + (1+h_{fe}) I_b R_e}{I_b} \\ &= h_{ie} + (1+h_{fe}) R_e \end{aligned}$$

The input resistance increases by $(1+h_{fe}) R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe} R_L}{h_{ie} + (1+h_{fe}) R_e}$$

Clearly, the addition of R_e reduces the voltage gain.

If $(1+h_{fe}) R_e \gg h_{ie}$ and $h_{fe} \gg 1$

then

$$A_v = \frac{-h_{fe} R_L}{(1+h_{fe}) R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation A_v is completely stable. The output resistance is infinite for the approximate model.

Common Base Amplifier:

The common base amplifier circuit is shown in [Fig. 1](#). The V_{EE} source forward biases the emitter diode and V_{CC} source reverse biased collector diode. The ac source v_{in} is connected to emitter through a coupling capacitor so that it blocks dc. This ac voltage produces small fluctuation in currents and voltages. The load resistance R_L is also connected to collector through coupling capacitor so the fluctuation in collector base voltage will be observed across R_L .

The dc equivalent circuit is obtained by reducing all ac sources to zero and opening all capacitors. The dc collector current is same as I_E and V_{CB} is given by

$$V_{CB} = V_{CC} - I_C R_C.$$

These current and voltage fix the Q point. The ac equivalent circuit is obtained by reducing all dc sources to zero and shorting all coupling capacitors. r'_e represents the ac resistance of the diode as shown in [Fig. 2](#).

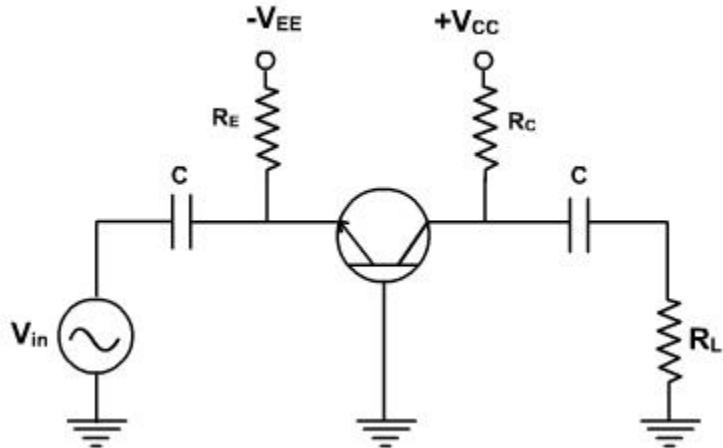


Fig. 1

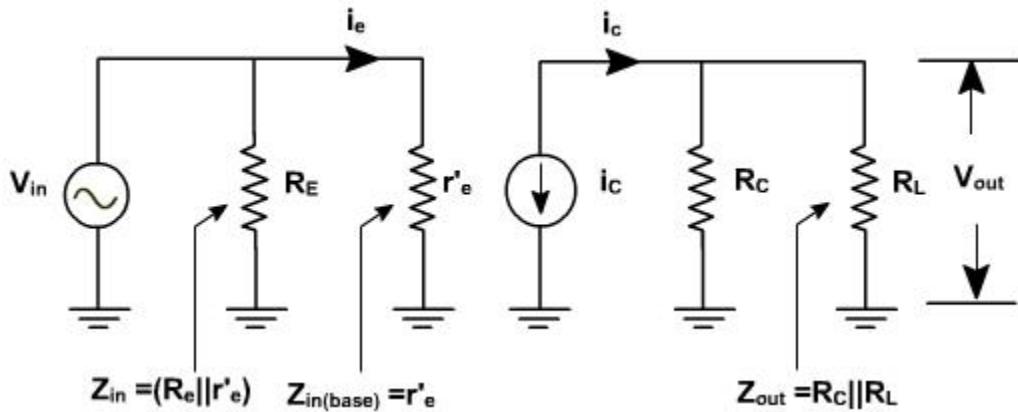


Fig. 2

[Fig. 3](#), shows the diode curve relating I_E and V_{BE} . In the absence of ac signal, the transistor operates at Q point (point of intersection of load line and input characteristic). When the ac signal is applied, the emitter current and voltage also change. If the signal is small, the operating point swings sinusoidally about Q point (A to B).

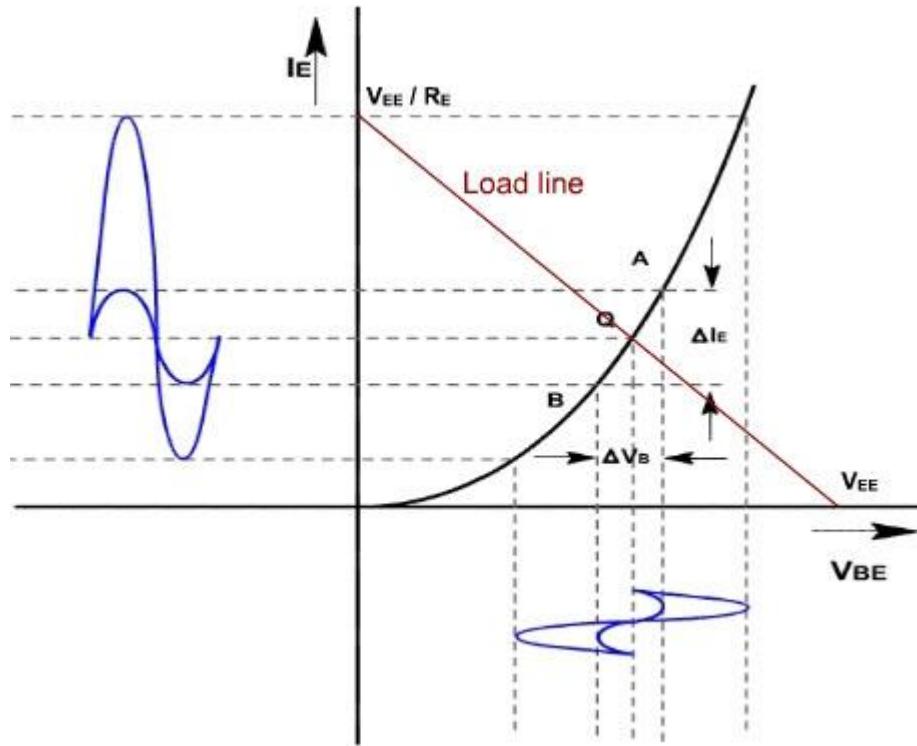


Fig .3

If the ac signal is small, the points A and B are close to Q, and arc A B can be approximated by a straight line and diode appears to be a resistance given by

$$r'_e = \left. \frac{\Delta V_{BE}}{\Delta I_E} \right|_{\text{small change}}$$

$$= \frac{V_{be}}{i_e} = \frac{\text{ac voltage across base and emitter}}{\text{ac current through emitter}}$$

If the input signal is small, input voltage and current will be sinusoidal but if the input voltage is large then current will no longer be sinusoidal because of the non linearity of diode curve. The emitter current is elongated on the positive half cycle and compressed on negative half cycle. Therefore the output will also be distorted.

r'_e is the ratio of ΔV_{BE} and ΔI_E and its value depends upon the location of Q. Higher up the Q point small will be the value of r'_e because the same change in V_{BE} produces large change in I_E . The slope of the curve at Q determines the value of r'_e . From calculation it can be proved that.

$$r'_e = 25 \text{mV} / I_E$$

Common Base Amplifier

Proof:

In general, the current through a diode is given by

$$I = I_{co} (e^{\frac{qV}{KT}} - 1)$$

Where q is the charge on electron, V is the drop across diode, T is the temperature and K is a constant.

On differentiating w.r.t V , we get,

$$\frac{dI}{dV} = I_{co} * e^{\frac{qV}{KT}} * \frac{q}{KT}$$

The value of (q / KT) at 25°C is approximately 40.

$$\frac{dI}{dV} = 40 * I_{co} * e^{\frac{qV}{KT}}$$

Therefore, $\frac{dV}{dI} = 40 * (I + I_{co})$

$$\text{or, } \frac{dV}{dI} = \frac{1}{40 * (I + I_{co})} \approx \frac{1}{40 * I}$$

$$\text{Therefore, ac resistance of the emitter diode} = \frac{dV}{dI} = \frac{25mV}{I} \text{ Ohms}$$

To a close approximation the small changes in collector current equal the small changes in emitter current. In the ac equivalent circuit, the current ' i_c ' is shown upward because if ' i_e ' increases, then ' i_c ' also increases in the same direction.

Voltage gain:

Since the ac input voltage source is connected across r'_e . Therefore, the ac emitter current is given by

$$i_e = V_{in} / r'_e$$

$$\text{or, } V_{in} = i_e r'_e$$

The output voltage is given by $V_{out} = i_c (R_C \parallel R_L)$

$$\text{Therefore, voltage gain } A_V = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{(R_C \parallel R_L)}{r'_e}$$

$$= \frac{r_C}{r}$$

Under open circuit condition $v_{\text{out}} = i_c R_C$

$$\text{Therefore, voltage gain in open circuit condition} = A_V = \frac{R_C}{r'_e}$$

Example-1

Find the voltage gain and output of the amplifier shown in [fig. 4](#), if input voltage is 1.5mV.

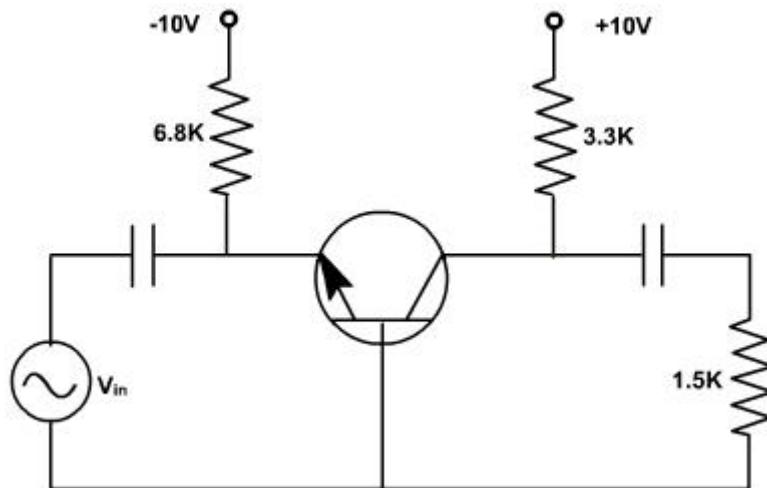


Fig. 4

Solution:

$$I_E = \frac{10 - 0.7}{6.8k} = 1.37mA$$

The emitter dc current I_E is given by

$$A_V = \frac{r_e}{r'_e} = \frac{3.3k \parallel 1.5k}{18.2\Omega}$$

Therefore, emitter ac resistance =

$$\text{or, } A_V = 56.6$$

$$\text{and, } V_{\text{out}} = 1.5 \times 56.6 = 84.9 \text{ mV}$$

Example-2

Repeat example-1 if ac source has resistance $R_s = 100 \Omega$.

Solution:

The ac equivalent circuit with ac source resistance is shown in fig. 5.

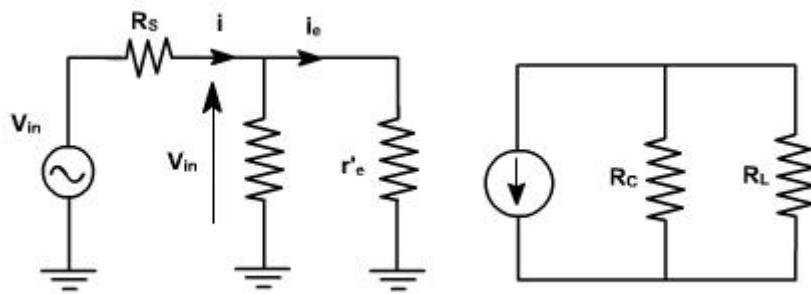


Fig. 5

$$i_e = \frac{V_{in}}{R_s + (R_E \parallel r'_e)} \times \frac{R_E}{R_E + r'_e}$$

The emitter ac current is given by

$$\text{or, } i_e = \frac{V_{in}}{(R_s + r'_e)R_E + R_s r'_e} \times R_E ; \frac{V_{in}}{R_s + r'_e}$$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{i_e r_c}{i_e (R_s + r'_e)} = \frac{r_c}{R_s + r'_e}$$

Therefore, voltage gain of the amplifier =

$$A_V = \frac{3.3k \parallel 1.5k}{100\Omega + 18.2\Omega} = 8.71$$

and,

$$V_{out} = 1.5 \times 8.71 = 13.1 \text{ mV}$$

Small Signal CE Amplifiers:

CE amplifiers are very popular to amplify the small signal ac. After a transistor has been biased with a Q point near the middle of a dc load line, ac source can be coupled to the base. This produces fluctuations in the base current and hence in the collector current of the same shape and frequency. The output will be enlarged sine wave of same frequency.

The amplifier is called linear if it does not change the wave shape of the signal. As long as the input signal is small, the transistor will use only a small part of the load line and the operation will be linear.

On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear.

The CE amplifier configuration is shown in [fig. 1](#).

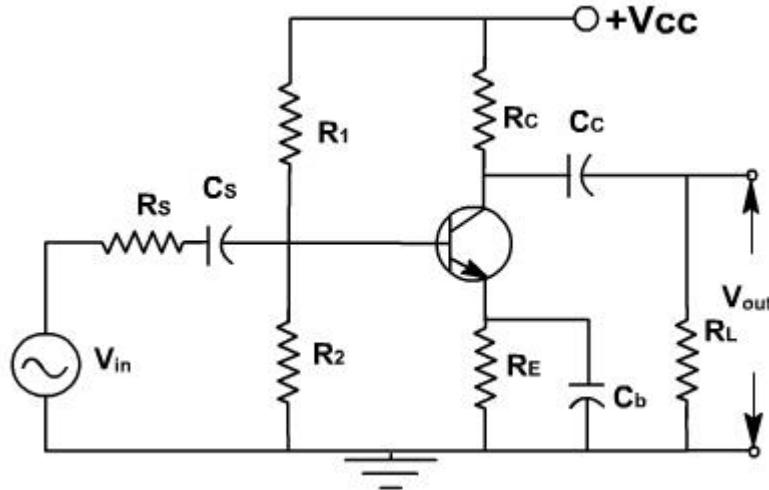


Fig. 1

The coupling capacitor (C_c) passes an ac signal from one point to another. At the same time it does not allow the dc to pass through it. Hence it is also called blocking capacitor.

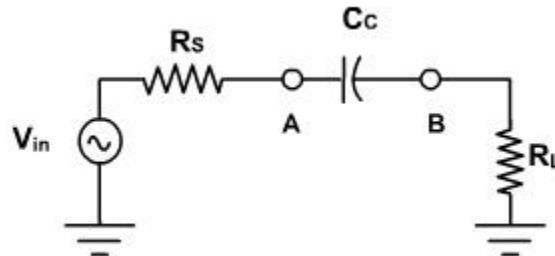


Fig. 2

For example in [fig. 2](#), the ac voltage at point A is transmitted to point B. For this series reactance X_C should be very small compared to series resistance R_s . The circuit to the left of A may be a source and a series resistor or may be the Thevenin equivalent of a complex circuit. Similarly R_L may be the load resistance or equivalent resistance of a complex network. The current in the loop is given by

$$\begin{aligned} i &= \frac{V_{in}}{\sqrt{(R_s + R_L)^2 + X_C^2}} \\ &= \frac{V_{in}}{\sqrt{R^2 + X^2}} \end{aligned}$$

$X_C = \frac{1}{2\pi f C}$

As frequency increases, X_C decreases, and current increases until it reaches its maximum value V_{in} / R . Therefore the capacitor couples the signal properly from A to B when $X_C \ll R$. The size of the coupling capacitor depends upon the lowest frequency to be coupled. Normally, for lowest frequency $X_C \approx 0.1R$ is taken as design rule.

The coupling capacitor acts like a switch, which is open to dc and shorted for ac.

The bypass capacitor C_b is similar to a coupling capacitor, except that it couples an ungrounded point to a grounded point. The C_b capacitor looks like a short to an ac signal and therefore emitter is said ac grounded. A bypass capacitor does not disturb the dc voltage at emitter because it looks open to dc current. As a design rule $X_{Cb} \approx 0.1R_E$ at Analysis of CE amplifier:

In a transistor amplifier, the dc source sets up quiescent current and voltages. The ac source then produces fluctuations in these current and voltages. The simplest way to analyze this circuit is to split the analysis in two parts: dc analysis and ac analysis. One can use superposition theorem for analysis .

AC & DC Equivalent Circuits:

For dc equivalent circuit, reduce all ac voltage sources to zero and open all ac current sources and open all capacitors. With this reduced circuit shown in [fig. 3](#) dc current and voltages can be calculated.

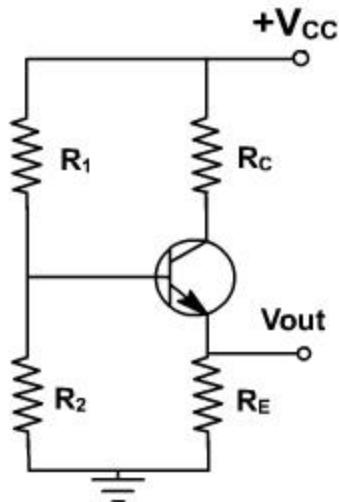


Fig. 3

For ac equivalent circuits reduce dc voltage sources to zero and open current sources and short all capacitors. This circuit is used to calculate ac currents and voltage as shown in [fig. 4](#).

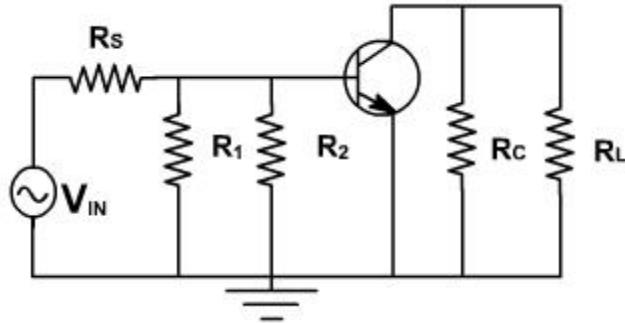


Fig. 4

The total current in any branch is the sum of dc and ac currents through that branch. The total voltage across any branch is the sum of the dc voltage and ac voltage across that branch.

Phase Inversion:

Because of the fluctuation in base current; collector current and collector voltage also swing above and below the quiescent voltage. The ac output voltage is inverted with respect to the ac input voltage, meaning it is 180° out of phase with input.

During the positive half cycle base current increases, causing the collector current to increase. This produces a large voltage drop across the collector resistor; therefore, the voltage output decreases and negative half cycle of output voltage is obtained. Conversely, on the negative half cycle of input voltage less collector current flows and the voltage drop across the collector resistor decreases, and hence collector voltage increases we get the positive half cycle of output voltage as shown in [fig. 5](#).

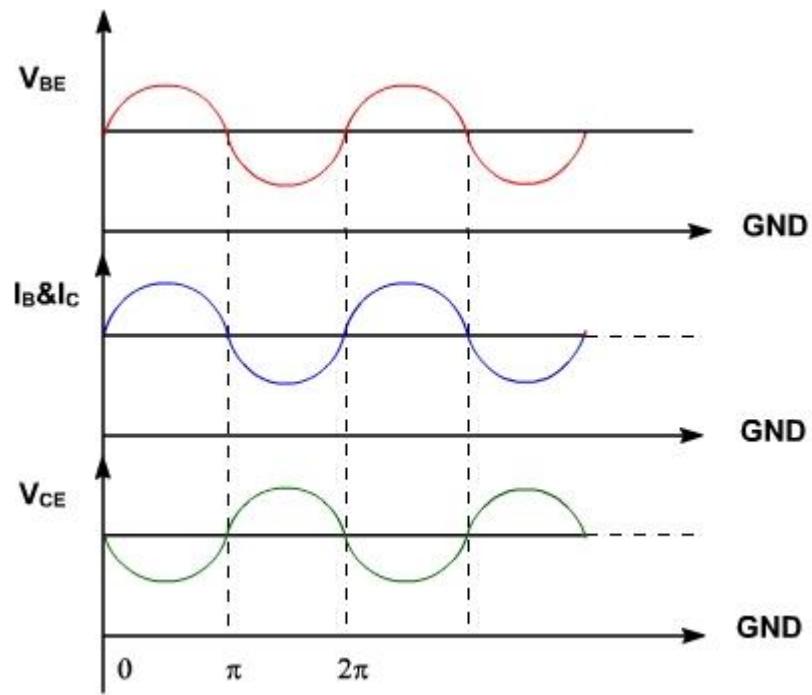


Fig. 5

lowest frequency.

AC Load line:

Consider the dc equivalent circuit [fig. 1](#).

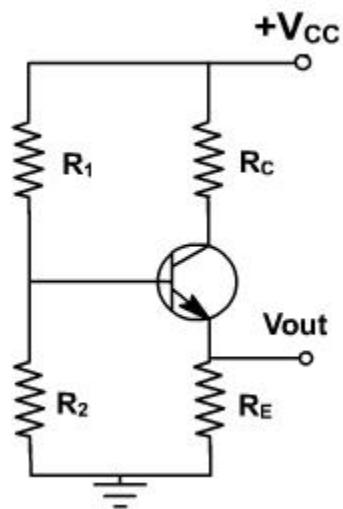


Fig. 1

Assuming $I_C = I_C(\text{approx})$, the output circuit voltage equation can be written as

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$\text{and } I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E}$$

$$\text{and } I_C = 0, \quad V_{CE} = V_{CC}$$

The slope of the d.c load line is $-\frac{1}{R_C + R_E}$.

When considering the ac equivalent circuit, the output impedance becomes $R_C \parallel R_L$ which is less than $(R_C + R_E)$.

In the absence of ac signal, this load line passes through Q point. Therefore ac load line is a line of slope $(-1 / (R_C \parallel R_L))$ passing through Q point. Therefore, the output voltage fluctuations will now be corresponding to ac load line as shown in [fig. 2](#). Under this condition, Q-point is not in the middle of load line, therefore Q-point is selected slightly upward, means slightly shifted to saturation side.

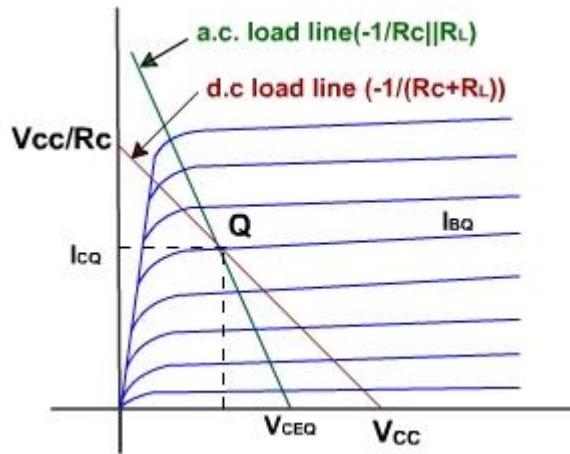


Fig. 2

Analysis of CE amplifier

Voltage gain:

To find the voltage gain, consider an unloaded CE amplifier. The ac equivalent circuit is shown in [fig. 3](#). The transistor can be replaced by its collector equivalent model i.e. a current source and emitter diode which offers ac resistance r'_e .

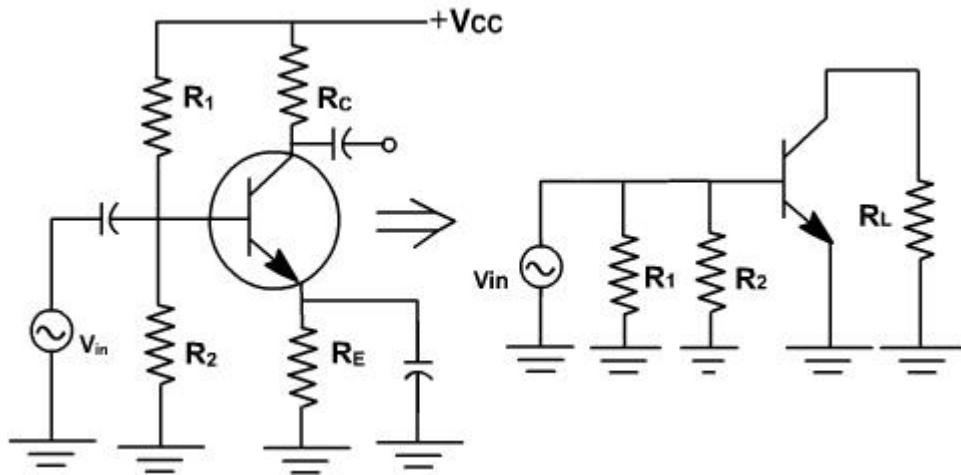


Fig. 3

The input voltage appears directly across the emitter diode.

Therefore emitter current $i_e = V_{in} / r'_e$.

Since, collector current approximately equals emitter current and $i_c = i_e$ and $v_{out} = -i_e R_C$ (The minus sign is used here to indicate phase inversion)

Further $v_{out} = - (V_{in} R_C) / r'_e$

Therefore voltage gain $A = v_{out} / v_{in} = -R_C / r'_e$

The ac source driving an amplifier has to supply alternating current to the amplifier. The input impedance of an amplifier determines how much current the amplifier takes from the ac source.

In a normal frequency range of an amplifier, where all capacitors look like ac shorts and other reactance are negligible, the ac input impedance is defined as

$$Z_{in} = V_{in} / i_{in}$$

Where v_{in} , i_{in} are peak to peak values or rms values

The impedance looking directly into the base is symbolized $Z_{in(base)}$ and is given by

$$Z_{in(base)} = V_{in} / i_b ,$$

Since, $v_{in} = i_e r'_e$

$$Z_{in(base)} = r'_e .$$

From the ac equivalent circuit, the input impedance z_{in} is the parallel combination of R_1 , R_2 and

r'_e .

$$Z_{in} = R_1 \parallel R_2 \parallel r'_e$$

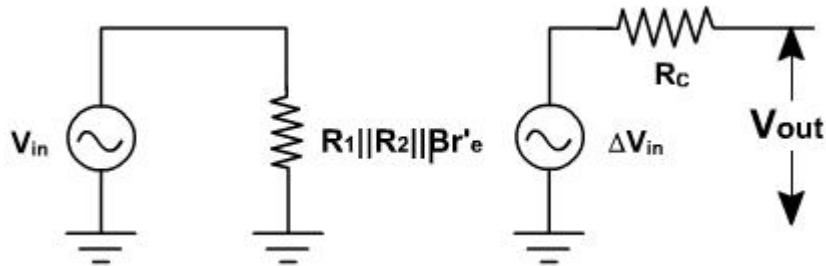
The Thevenin voltage appearing at the output is

$$V_{out} = A V_{in}$$

The Thevenin impedance is the parallel combination of R_C and the internal impedance of the current source. The collector current source is an ideal source, therefore it has an infinite internal impedance.

$$Z_{out} = R_C$$

The simplified ac equivalent circuit is shown in [fig. 4](#).



Analysis of CE amplifier

Example-1:

Select R_1 and R_2 for maximum output voltage swing in the circuit shown in [fig. 5](#).

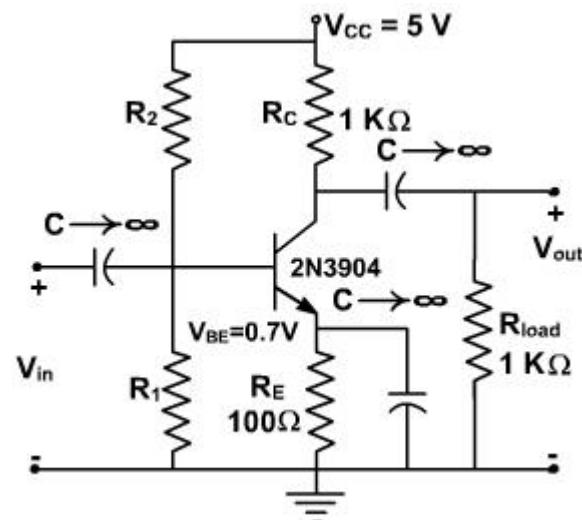


Fig. 5

Solution:

We first determine ICQ for the circuit

$$R_{ac} = R_C \parallel R_{load} = 500$$

$$R_{dc} = R_E + R_C = 1100$$

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{5}{500 + 1100} = 3.13 \text{ mA}$$

For maximum swing,

$$V'CC = 2 VCEQ$$

The quiescent value for VCE is given by

$$VCEQ = (3.13 \text{ mA}) (500 \text{ W}) = 1.56 \text{ V}$$

The intersection of the ac load line on the vCE axis is $V'CC = 3.13 \text{ V}$. From the manufacturer's specification, β for the 2N3904 is 180. R_B is set equal to $0.1 \beta R_E$. So,

$$R_B = 0.1(180)(100) = 1.8 \text{ K W}$$

$$V_{BB} = (3.13 \times 10^{-3})(1.1 \times 100) + 0.7 = 1.044 \text{ V}$$

Since we know V_{BB} and R_B , we find R_1 and R_2 ,

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{1800}{1 - 1.044/5} = 2.28 \text{ K}\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{1800 \times 5}{1.044} = 8.62 \text{ K}\Omega$$

The maximum output voltage swing, ignoring the non-linearity's at saturation and cutoff, would then be

$$\begin{aligned} \text{Max collector current swing} &= 2 I_{CQ} (R_C \parallel R_{load}) \\ &= 2 (3.13 \text{ mA}) (500 \Omega) = 3.13 \text{ V} \end{aligned}$$

The load lines are shown on the characteristics of fig. 6.

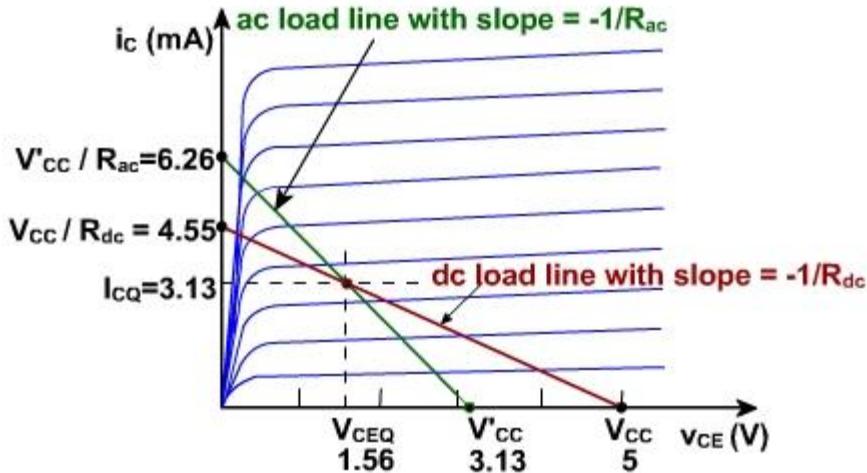


Fig. 6

The maximum power dissipated by the transistor is calculated to assure that it does not exceed the specifications. The maximum average power dissipated in the transistor is

$$P(\text{transistor}) = V_{CEQ} I_{CQ} = (1.56 \text{ (V)}) (3.13 \text{ mA}) = 4.87 \text{ mW}$$

This is well within the 350 mW maximum given on the specification sheet. The maximum conversion efficiency is

$$\eta = \frac{P_{out}(\text{ac})}{P_{VCC}(\text{dc})} = \frac{\left(3.13 \times 10^{-3} / 2\right)^2 \times 1000 / 2 \times 100}{5 \times 3.13 \times 10^{-3} + 5^2 / 10.9 \times 10^3} = 6.84\%$$

The swamped Amplifier:

The ac resistance of the emitter diode r'e equals 25mV / IE and depends on the temperature. Any change in r'e will change the voltage gain in CE amplifier. In some applications, a change in voltage is acceptable. But in many applications we need a stable voltage gain is required.

To make it stable, a resistance rE is inserted in series with the emitter and therefore emitter is no longer ac grounded. fig .7.

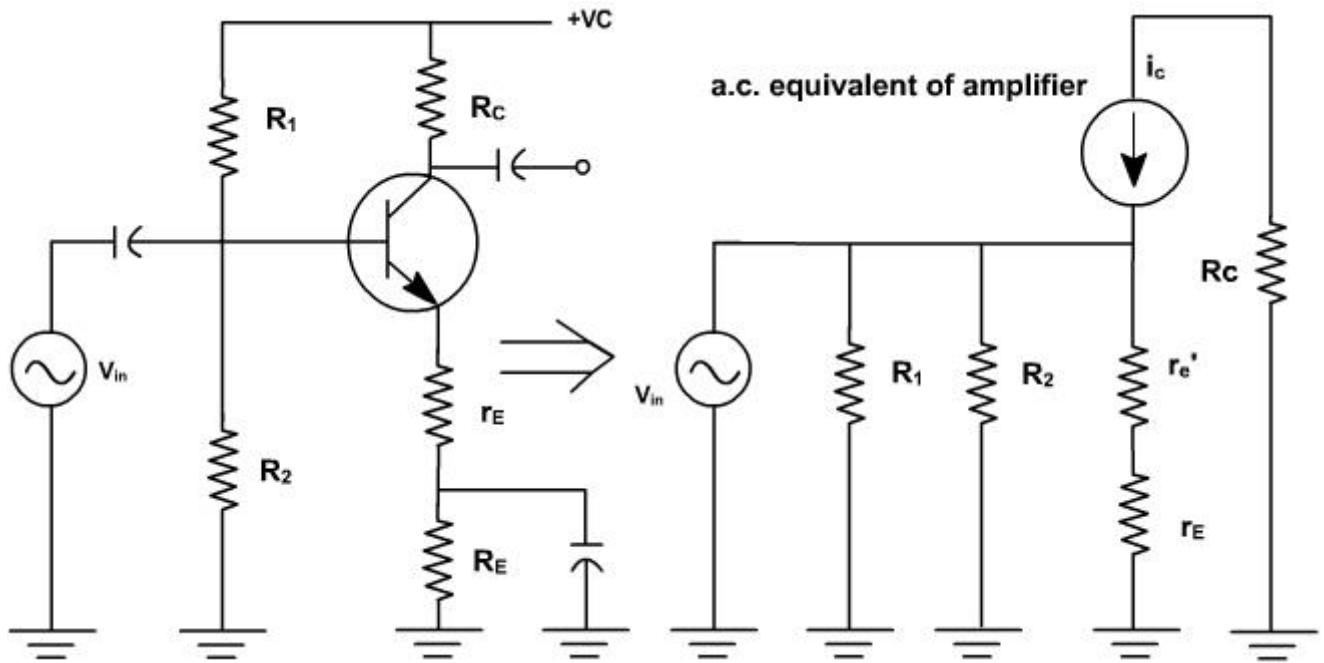


Fig. 7

Because of this the ac emitter current flows through r'_e and produces an ac voltage at the emitter. If r'_e is much greater than r'_e almost all of the ac input signal appears at the emitter, and the emitter is bootstrapped to the base for ac as well as for dc.

In this case, the collector circuit is given by

$$i_C = \frac{V_{in}}{r'_e + r_E}$$

$$\text{and } V_{out} = -i_C R_C$$

Therefore,

$$\begin{aligned} A &= \frac{V_{out}}{V_{in}} = -\frac{i_C R_C}{i_C (r'_e + r_E)} \\ &= -\frac{R_C}{(r'_e + r_E)} \end{aligned}$$

Now r'_e has a less effect on voltage gain, swamping means $r'_e \gg r'_e$. If swamping is less, voltage gain varies with temperature. If swamping is heavy, then gain reduces very much.

Design of Amplifier :

Example -1 (Common Emitter Amplifier Design)

Design a common-emitter amplifier with a transistor having a $\beta = 200$ and $V_{BE} = 0.7$ V. Obtain an overall gain of $|A_V| \geq 100$ and maximum output voltage swing. Use the CE configuration shown in [fig. 1](#) with two power supplies. R_{source} is the resistance associated with the source, v_{source} . Let $R_{source} = 100$ Ohms. The output load is $2K\Omega$. Determine the resistor values of the bias circuitry, the maximum undistorted output voltage swing, and the stage voltage gain.

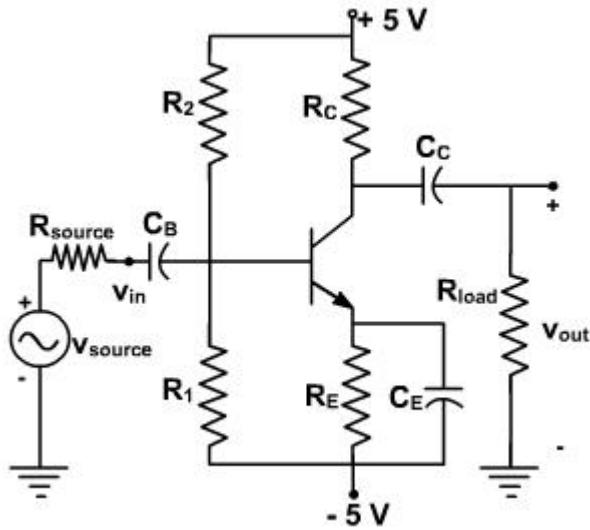


Fig. 1

Solution:

The maximum voltage across the amplifier is 10 V since the power supply can be visualized as a 10V power supply with a ground in the center. In this case, the ground has no significance to the operation of the amplifier since the input and output are isolated from the power supplies by capacitors.

We will have to select the value for R_C and we are really not given enough information to do so. Let choose $R_C = R_{load}$.

We don't have enough information to solve for R_B – we can't use the bias stability criterion since we don't have the value of R_E either. We will have to (arbitrarily) select a value of R_B or R_E . If this leads to a contradiction, or “bad” component values (e.g., unobtainable resistor values), we can come back and modify our choice. Let us select a value for R_E that is large enough to obtain a reasonable value of V_{BB} . Selecting R_E as 400Ω will not appreciably reduce the collector current yet it will help in maintaining a reasonable value of V_{BB} . Thus,

$$R_B = 0.1 \beta R_E = 0.1 (200)(400) = 8 K\Omega$$

To insure that we have the maximum voltage swing at the output, we will use

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{10}{1000 + 2400} = 2.94 \text{ mA}$$

$$V_{BB} = V_{BE} + I_{CQ} (R_B / \beta + R_E) = 0.7 + 2.9 \times 10^{-3} \left(\frac{8000}{200} + 400 \right) = 1.99 \text{ V}$$

Note that we are carrying out our calculations to four places so that we can get accuracy to three places. The bias resistors are determined by

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{8000}{1 - 1.99/10} = 9.99 \text{ k}\Omega$$

$$R_2 = R_B \frac{V_{CC}}{V_{BB}} = 8000 \left(\frac{10}{1.99} \right) = 40.2 \text{ k}\Omega$$

Since we designed the bias circuit to place the quiescent point in the middle of the ac load line, we can use

$$V_{out}(\text{undistorted p-p}) = 1.8 (2.94 \times 10^{-3}) (2 \text{ k}\Omega \parallel 2 \text{ k}\Omega) = 5.29 \text{ V}$$

Now we can determine the gain of the amplifier itself.

$$|A_v| = g_m (R_C \parallel R_{load}) = \frac{2.94 \times 10^{-3} \times 1000}{26 \times 10^{-3}}$$

Using voltage division, we can determine the gain of the overall circuit.

The value of R_{in} can be obtained as

$$R_{in} = r_s \parallel R_B = 1.77 \text{ k}\Omega \parallel 8 \text{ k}\Omega = 1.45 \text{ k}\Omega$$

Thus the overall gain of the amplifier is

$$|A_v|_{\text{overall}} = \left| \frac{V_{out}}{V_{in}} \right| = 113 \times \frac{R_{in}}{R_{in} + R_{source}} = 106$$

This shows that the common-emitter amplifier provides high voltage gain. However, it is very noisy, it has a low input impedance, and it does not have the stability of the emitter resistor common emitter a

Design of Amplifier

Example-2 (Emitter-Resistor Amplifier Design)

Design an emitter-resistor amplifier as shown in fig. 2 to drive a $2 \text{ k}\Omega$ load using a pnp silicon transistor, $V_{CC} = -24 \text{ V}$, $\beta = 200$, $A_v = -10$, and $V_{BE} = -0.7 \text{ V}$. Determine all element values and calculate A_i , R_{in} , I_{CQ} and the maximum undistorted symmetrical output voltage swing for three

values of R_C as given below:

1. $R_C = R_{\text{load}}$
2. $R_C = 0.1 R_{\text{load}}$
3. $R_C = 10 R_{\text{load}}$

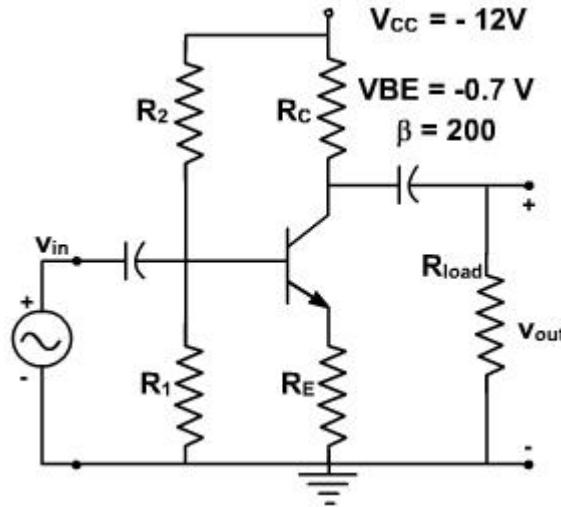


Fig. 2

Solution:

$$(a) R_C = R_{\text{load}}$$

We use the various equations derived in previous lecture in order to derive the parameters of the circuit.

From the voltage gain, we can solve for R'_E .

$$A_v = -10 = - \frac{R_{\text{load}} || R_C}{r_e + R_E} = - \frac{2K\Omega || 2K\Omega}{r_e + R_E}$$

$$\text{So } R'_E = r_e + R_E = 100 \Omega$$

We can find the quiescent value of the collector current I_C from the collector-emitter loop using the equation for the condition of maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{dc} + R_{ac}} = -7.5 \text{ mA}$$

$$\text{Therefore, } r'_E = \frac{25 \times 10^{-3}}{7.5 \times 10^{-3}} = 3.33 \Omega$$

This is small enough that we shall ignore it to find that $R_E = 100 \Omega$. Since we now know β and R_E . We can use the design guideline.

$$R_B = 0.1 \beta R_E = 2 \text{ k } \Omega$$

As designed earlier, the biasing circuitry can be designed in the same manner and given by

$$V_{BB} = -1.52 \text{ V}$$

$$R_1 = 2.14 \text{ K } \Omega$$

$$R_2 = 3.6 \text{ K } \Omega$$

The maximum undistorted symmetrical peak to peak output swing is then

$$V_{out} (\text{P-P}) = 1.8 I_{CQ} (R_{load} \parallel R_C) = 13.5 \text{ V}$$

Thus current gain $A_i = -9.1$

and input impedance $R_{in} = 1.82 \text{ K } \Omega$

$$(b) \quad R_C = 0.1 R_{load}$$

we repeat the steps of parts (a) to find

$$R_C = 200 \Omega \quad R_i = 390 \Omega$$

$$I_{CQ} = -57.4 \text{ mA} \quad R_2 = 4.7 \text{ K } \Omega$$

$$r'_e = 0.45 \Omega \quad v_{out}(\text{p-p}) = 18.7 \text{ V}$$

$$R_B = 360 \Omega \quad A_i = -1.64$$

$$V_{BB} = -1.84 \text{ V} \quad R_{in} = 327 \Omega$$

$$(C) \quad R_C = 10 R_{load}$$

Once again, we follow the steps of part (a) to find

$$R_C = 20 \text{ K } \Omega \quad R_i = 3.28 \text{ K } \Omega$$

$$I_{CQ} = -1.07 \text{ mA} \quad R_2 = 85.6 \text{ K } \Omega$$

$$r'_e = 24.2 \Omega \quad v_{out}(\text{p-p}) = 3.9 \text{ V}$$

$$R_B = 3.64K \Omega \quad A_i = -14.5$$

$$V_{BB} = -0.886 V \quad R_{in} = 2.91K W$$

We now compare the results obtained Table-I for the purpose of making the best choice for R_C .

	I_{CQ}	A_i	R_{in}	$V_{out}(p-p)$
$R_C = R_{load}$	-7.5 mA	-9.1	1.82K W	13.5 V
$R_C = 0.1 R_{load}$	-57.4 mA	-1.64	327 W	20.8 V
$R_C = 10 R_{load}$	-1.07mA	-14.5	2.91W	3.9 V

Table - 1 Comparsion for the three selections of R_C

It indicates that of the three given ratios of R_C to R_{load} , $R_C = R_{load}$ has the most desirable performance in the CE amplifier stage.

It can be used as a guide to develop a reasonable designs. In most cases, this choice will provide performance that meets specifications. In some applications, it may be necessary to do additional analysis to find the optimum ratio of R_C to R_{load} .

mplifier.

Design of Amplifier

Example-2 (Emitter-Resistor Amplifier Design)

Design an emitter-resistor amplifier as shown in fig. 2 to drive a $2 K\Omega$ load using a pnp silicon transistor, $V_{CC} = -24V$, $\beta = 200$, $A_v = -10$, and $V_{BE} = -0.7 V$. Determine all element values and calculate A_i , R_{in} , I_{CQ} and the maximum undistorted symmetrical output voltage swing for three values of R_C as given below:

1. $R_C = R_{load}$
2. $R_C = 0.1 R_{load}$
3. $R_C = 10 R_{load}$

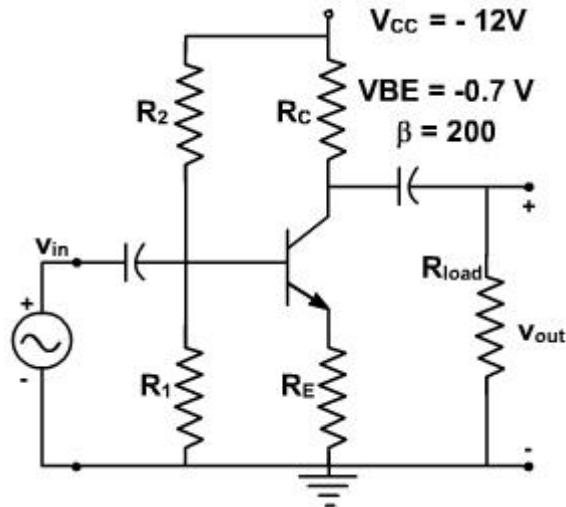


Fig. 2

Solution:

$$(a) R_C = R_{load}$$

We use the various equations derived in previous lecture in order to derive the parameters of the circuit.

From the voltage gain, we can solve for R'_E .

$$A_v = -10 = -\frac{R_{load} \parallel R_C}{r_e + R_E} = -\frac{2k\Omega \parallel 2k\Omega}{r_e + R_E}$$

$$\text{So } R'_E = r_e + R_E = 100 \Omega$$

We can find the quiescent value of the collector current I_C from the collector-emitter loop using the equation for the condition of maximum output swing.

$$I_{cq} = \frac{V_{cc}}{R_{dc} + R_{ac}} = -7.5 \text{ mA}$$

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$$R_i = 390 \text{ } \Omega$$

$$I_{CQ} = -57.4 \text{ mA}$$

$$R_2 = 4.7 \text{ K } \Omega$$

$$r'_e = 0.45 \text{ } \Omega$$

$$v_{out}(\text{p-p}) = 18.7 \text{ V}$$

$$R_B = 360 \text{ } \Omega$$

$$A_i = -1.64$$

$$V_{BB} = -1.84 \text{ V}$$

$$R_{in} = 327 \text{ } \Omega$$

$$(C) \quad R_C = 10 R_{load}$$

Once again, we follow the steps of part (a) to find

$$R_C = 20 \text{ K } \Omega$$

$$R_1 = 3.28 \text{ K } \Omega$$

$$I_{CQ} = -1.07 \text{ mA}$$

$$R_2 = 85.6 \text{ K } \Omega$$

$$r'_e = 24.2 \text{ } \Omega$$

$$v_{out}(\text{p-p}) = 3.9 \text{ V}$$

$$R_B = 3.64 \text{ K } \Omega$$

$$A_i = -14.5$$

$$V_{BB} = -0.886 \text{ V}$$

$$R_{in} = 2.91 \text{ K W}$$

We now compare the results obtained Table-I for the purpose of making the best choice for R_C .

	I_{CQ}	A_i	R_{in}	$V_{out}(p-p)$
$R_C = R_{load}$	-7.5 mA	-9.1	1.82K W	13.5 V
$R_C = 0.1 R_{load}$	-57.4 mA	-1.64	327 W	20.8 V
$R_C = 10 R_{load}$	-1.07mA	-14.5	2.91W	3.9 V

Table - 1 Comparsion for the three selections of R_C

It indicates that of the three given ratios of R_C to R_{load} , $R_C = R_{load}$ has the most desirable performance in the CE amplifier stage.

It can be used as a guide to develop a reasonable designs. In most cases, this choice will provide performance that meets specifications. In some applications, it may be necessary to do additional analysis to find the optimum ratio of R_C to R_{load} .

Design of Amplifier

Example- 3 (Capacitor-Coupled Emitter-Resistor Amplifier Design)

Design an emitter-resistor amplifier as shown in fig. 3 with $A_v = -10$, $\beta = 200$ and $R_{load} = 1K \Omega$. A pnp transistor is used and maximum symmetrical output swing is required.

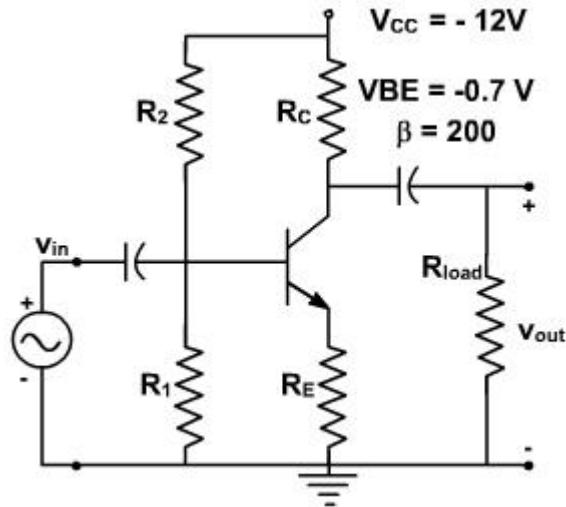


Fig. 3

Solution:

As designed earlier, we shall chose $R_C = R_{load} = 10 k\Omega$.

$$A_v = \frac{R_{load} || R_C}{R'_E}$$

The voltage gain is given by

where $R'_E = R_E + r'_e$.

Substituting A_v , R_{load} and R_C in this equation, we find $R'_E = 50 \Omega$.

We need to know the value of r'_e to fine R_E . We first find R_{ac} and R_{dc} , and then calculate the Q point as follows (we assume r'_e is small, so $R_E = R'_E$)

$$R_{ac} = R_E + R_C || R_{load} = 550 \Omega$$

$$R_{dc} = R_E + R_C = 1050 \Omega$$

Now, the first step is to calculate the quiescent collector current needed to place the Q-point into the center of the ac load line (i.e., maximum swing). The equation is

$$I_{cq} = \frac{V_{cc}}{R_{ac} + R_{dc}} = -7.5 \text{ mA}$$

The quantity, r'_e , is found as follows

$$r'_e = \frac{25(\text{mV})}{|I_{cq}|} = \frac{25(\text{mV})}{7.5(\text{mA})} = 3.33 \Omega$$

Then

$$R_E = 50 - r_e = 46.67 \Omega$$

If there were a current gain or input resistance specification for this design, we would use it to solve for the value of R_B . Since is no such specification, we use the expression

$$R_B = 0.1 \beta R_E = 0.1 (200) (46.6) = 932 \Omega$$

Then continuing with the design steps,

$$A_i = \frac{-R_B}{R_B + r'_e + R_B} \cdot \frac{R_C}{R_C + R_{load}} = -8.50$$

$$V_{CEO} = V_{cc} - (R_C + R'_E) I_{cq} = -4.125 \text{ V}$$

and

$$V_{BB} = I_{CQ} \left(R_E + \frac{R_E}{\beta} \right) + V_{BE} = -1.08 \text{ V}$$

$$R_1 = \frac{R_B}{1 - \frac{V_{BB}}{V_{CC}}} = 1.02 \text{ k}\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = 10.3 \text{ k}\Omega$$

$$R_{in} = \frac{R_B(r_e + R_E)}{\frac{R_B}{\beta} + r_e + R_E} = 8.51\Omega$$

$$R_o = R_C = 1 \text{ k}\Omega$$

The last equality assumes that r_o is large compared to R_C .

The maximum undistorted peak to peak output swing is given by

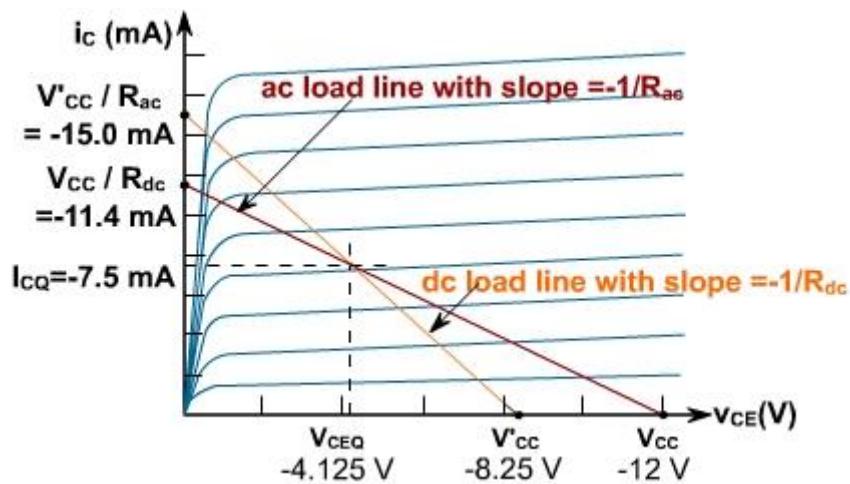
$$1.8 |I_{CQ}| (R_C \parallel R_{load}) = 1.8 (0.0075) (500) = 6.75 \text{ V}$$

The power delivered into the load and the maximum power dissipated by the transistor are found as

$$P_{Load} = \frac{1}{2} \left(I_{CQ} \frac{R_C}{R_C + R_{load}} \right)^2 R_{load} = \frac{I_{CQ}^2 R_{load}}{8} = 7 \text{ mW}$$

$$P_{transistor} = V_{CEO} I_{CQ} = (-4.125 \text{ V})(-7.5 \text{ mA}) = 31 \text{ mW}$$

The load lines for this circuit are shown in fig. 4.



Common Collector Amplifier:

If a high impedance source is connected to low impedance amplifier then most of the signal is dropped across the internal impedance of the source. To avoid this problem common collector amplifier is used in between source and CE amplifier. It increases the input impedance of the CE

amplifier without significant change in input voltage.

Fig. 1, shows a common collector (CC) amplifier. Since there is no resistance in collector circuit, therefore collector is ac grounded. It is also called grounded collector amplifier. When input source drives the base, output appears across emitter resistor. A CC amplifier is like a heavily swamped CE amplifier with a collector resistor shorted and output taken across emitter resistor.

$$V_{out} = V_{in} - V_{BE}$$

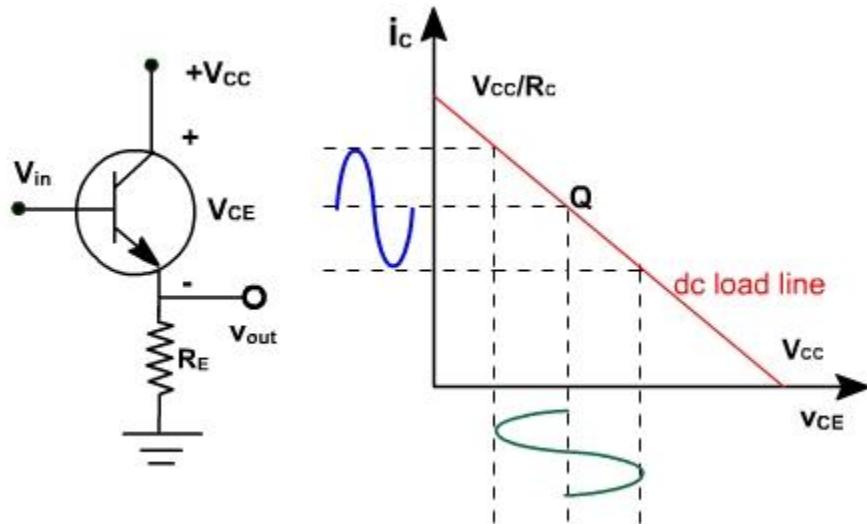


Fig. 1

Therefore, this circuit is also called emitter follower, because \$V_{BE}\$ is very small. As \$v_{in}\$ increases, \$v_{out}\$ increases.

If \$v_{in}\$ is 2V, \$v_{out} = 1.3\$V

If \$v_{in}\$ is 3V, \$v_{out} = 2.3\$V.

Since \$v_{out}\$ follows exactly the \$v_{in}\$ therefore, there is no phase inversion between input and output.

The output circuit voltage equation is given by

$$V_{CE} = V_{CC} - I_E R_E$$

Since \$I_E = \beta I_C\$

$$I_C = (V_{CC} - V_{CE}) / R_E$$

This is the equation of dc load line. The dc load line is shown in Fig. 1.

Common Collector Amplifier:

Voltage gain:

Fig. 2, shows an emitter follower driven by a small ac voltage. The input is applied at the base of transistor and output is taken across the emitter resistor. Fig. 3, shows the ac equivalent circuit of the amplifier. The emitter is replaced by ac resistance r'_e .

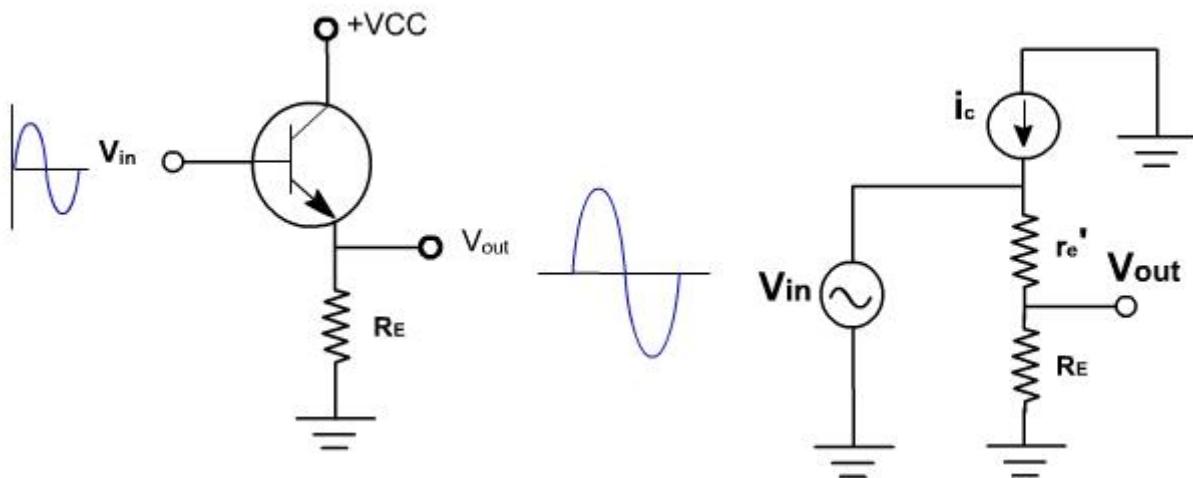


Fig. 2

The ac output voltage is given by

$$V_{out} = R_E i_e$$

$$\text{and, } V_{in} = i_e (R_E + r'_e)$$

$$\text{Therefore, } A = R_E / (R_E + r'_e)$$

Since $r'_e \ll R_E$

$$\boxed{A_v} = \boxed{1.} \text{ (approx)}$$

Therefore, it is a unity gain amplifier. The practical emitter follower circuit is shown in Fig. 4.

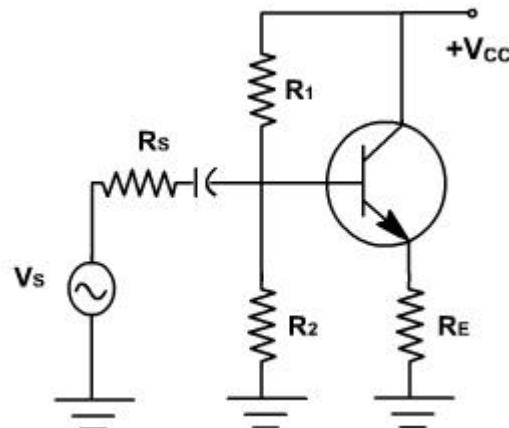


Fig. 4

The ac source (V_s) with a series resistance R_s drives the transistor base. Because of the biasing resistor and input impedance of the base, some of the ac signal is lost across the source resistor. The ac equivalent circuit is shown in Fig. 5.

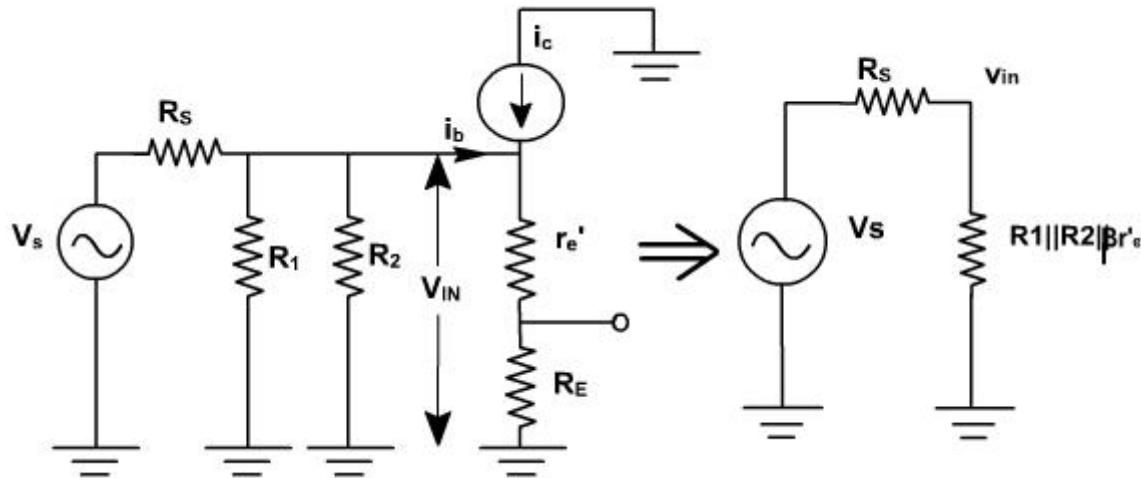


Fig. 5

The input impedance at the base is given by

$$\begin{aligned}
 Z_{\text{in(base)}} &= \frac{V_{\text{in}}}{i_b} \\
 &= \frac{i_e(r'_e + R_E)}{i_b} \\
 &= \frac{\beta i_b(r'_e + R_E)}{i_b} \\
 &= \beta(r'_e + R_E)
 \end{aligned}$$

Since r'_e is very small in comparison with R_E

$$\therefore Z_{\text{in(base)}} \approx \beta R_E$$

The total input impedance of an emitter follower includes biasing resistors in parallel with input impedance of the base.

$$Z_{\text{in}} = R_1 \parallel R_2 \parallel (r'_e + R_E)$$

Since R_E is very large as compared to R_1 and R_2 .

$$\text{Thus, } Z_{\text{in}} \approx R_1 \parallel R_2$$

Therefore input impedance is very high.

Applying Thevenin's theorem to the base circuit of Fig. 5, it becomes a source v_{in} and a series resistance ($R_1 \parallel R_2 \parallel R_S$) as shown in Fig. 6.

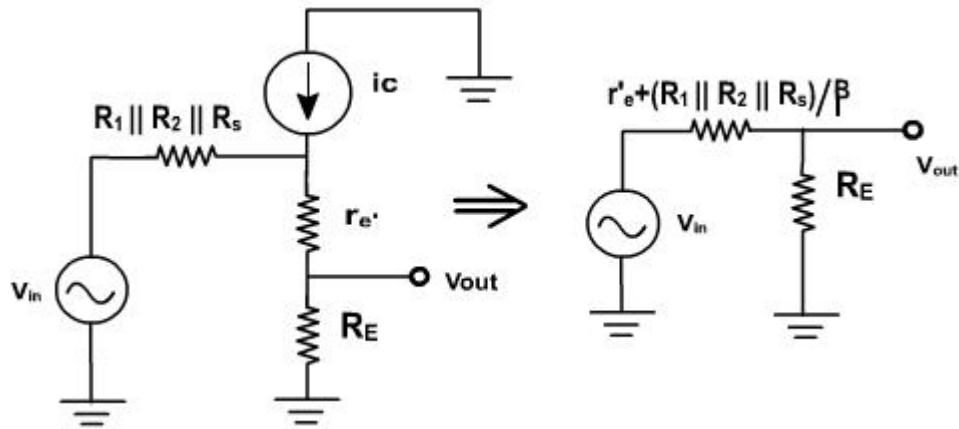


Fig. 6

$$V_{in} = (R_1 \parallel R_2 \parallel R_s) + i_e (r'_e + R_E)$$

$$\text{or, } i_e = \frac{V_{in}}{R_E + r'_e + \frac{R_1 \parallel R_2 \parallel R_s}{\beta}}$$

The emitter resistor R_E is driven by an ac source with output impedance of

$$Z_{out} = r'_e + \frac{R_1 \parallel R_2 \parallel R_s}{\beta}$$

The impedance of the amplifier seen from the output terminal is given by

$$Z = R_E \parallel r'_e + \frac{R_1 \parallel R_2 \parallel R_s}{\beta}$$

The output voltage is given by

$$\begin{aligned} V_{out} &= A V_{in} \\ &= \frac{R_E}{R_E + r'_e + \frac{R_1 \parallel R_2 \parallel R_s}{\beta}} V_{in} \\ &\approx V_{in} \quad (\text{if } R_E \text{ is very large}) \end{aligned}$$

Common Collector Amplifier

Example 1:

Find the Q-point of the emitter follower circuit of [fig. 7](#) with $R_1 = 10 \text{ k}\Omega$ and $R_2 = 20 \text{ k}\Omega$. Assume the transistor has a β of 100 and input capacitor C is very-very large.

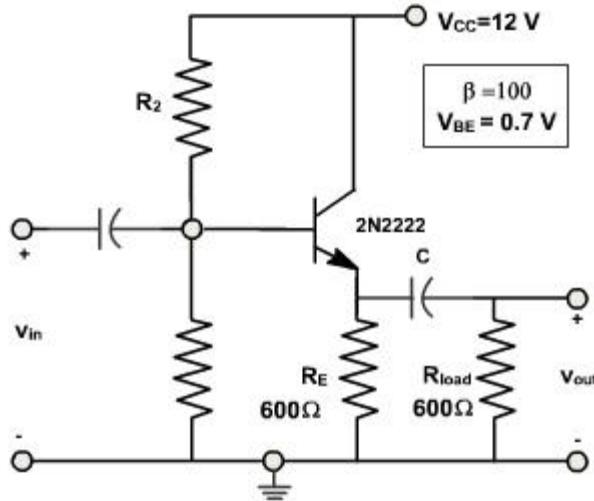


Fig. 7

Solution:

We first find the Thevenin's equivalent of the base bias circuitry.

$$R_B = R_1 \parallel R_2 = 6.67 \text{ k}\Omega$$

$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2} = \frac{12(10^4)}{30 \times 10^3} = 4 \text{ V}$$

From the bias equation we have

$$I_C = I_{CQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta} + R_E} = \frac{4 - 0.7}{\frac{6670}{100} + 600} = 4.95 \text{ mA}$$

Example - 2

Find the output voltage swing of the circuit of **fig. 7**.

Solution:

The Q-Point location has already been calculated in **Example-1**. We found that the quiescent collector current is 4.95 mA.

$$\text{The Output voltage swing} = 2 \cdot I_C \text{ peak} \cdot (R_E \parallel R_{\text{Load}}) = 2(4.95 \times 10^{-3})(300) = 2.97 \text{ V}$$

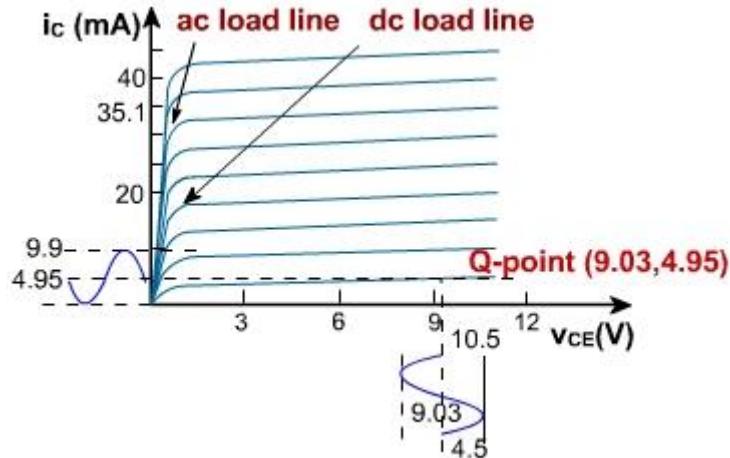
This is less than the maximum possible output swing. Continuing the analysis,

$$V_{CEQ} = V_{CC} - I_{CQ} R_E = 9.03 \text{ V}$$

$$V'_{CC} = V_{CEQ} + I_{CQ} (R_E \parallel R_{Load}) = 10.5 \text{ V}$$

$$I'_{CC} = \frac{10.5}{300} = 35.1 \text{ mA}$$

The load lines for this problem are shown in **Fig. 8.**



CLASSIFICATION OF AMPLIFIERS:

A circuit that increases the amplitude of the given input signal is an amplifier. A small ac signal fed to the amplifier is obtained as a larger ac signal of the same frequency at the output. Amplifiers constitute an essential part of radio, television and other communication circuits. Depending on the nature and level of amplification and the impedance matching requirements different types of amplifiers can be considered and they are discussed in this chapter.

Amplifiers can be classified as follows:

1. Based on the transistor configuration

(a) Common emitter amplifier

(b) Common base amplifier

(c) Common collector amplifier

2.Based on the active devices

(a) BJT amplifier

(b) FET amplifier

3.Based on the Q-point(operating condition)

(a) Class A amplifier

(b) Class B amplifier

(c) Class C amplifier

(d) Class AB amplifier

4.Based on the number of stages

(a) Single stage amplifiers

(b) Multistage amplifiers

5.Based on the output

(a)Voltage amplifiers

(b)Power amplifiers

6.Based on the frequency response

(a)Audio frequency(AF) amplifier

(b)Intermediate Frequency amplifier(IF)

(c)Radio Frequency amplifier(RF)

7.Based on the bandwidth

(a)Narrow band amplifier(normally RF amplifier)

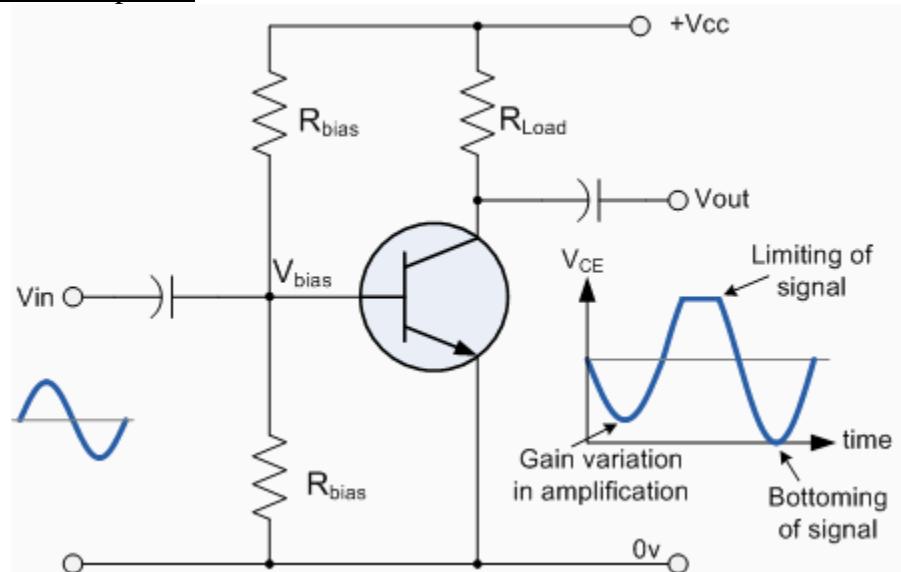
(b)Wide band amplifier(normally video amplifier)

Distortion in amplifiers:

Amplifier Distortion

From the previous tutorials we learnt that for a signal amplifier to work correctly it requires some form of DC Bias on its Base or Gate terminal so that it amplifies the input signal over its entire cycle with the bias "Q-point" set as near to the middle of the load line as possible. This then gave us a "Class-A" type amplification with the most common configuration being Common Emitter for Bipolar transistors and Common Source for unipolar transistors. We also saw that the Power, Voltage or Current Gain, (amplification) provided by the amplifier is the ratio of the peak input value to its peak output value. However, if we incorrectly design our amplifier circuit and set the biasing Q-point at the wrong position on the load line or apply too large an input signal, the resultant output signal may not be an exact reproduction of the original input signal waveform. In other words the amplifier will suffer from distortion. Consider the common emitter amplifier circuit below.

Common Emitter Amplifier



Distortion of the signal waveform may take place because:

1. Amplification may not be taking place over the whole signal cycle due to incorrect biasing.
2. The input signal may be too large, causing the amplifier to limit.
3. The amplification may not be linear over the entire frequency range of inputs.

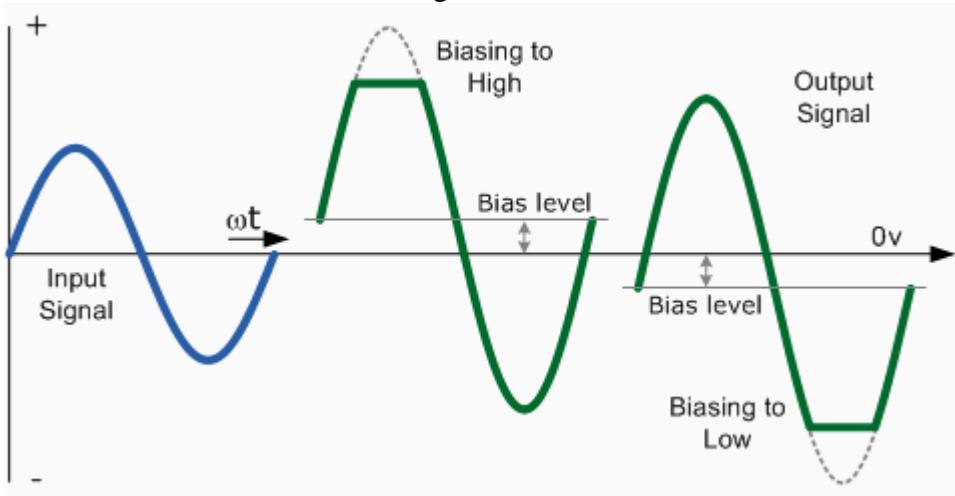
This means then that during the amplification process of the signal waveform, some form of Amplifier Distortion has occurred.

Amplifiers are basically designed to amplify small voltage input signals into much larger output signals and this means that the output signal is constantly changing by some factor or value times the input signal for all input frequencies. We saw previously that this multiplication factor is called the Beta, β value of the transistor. Common emitter or even common source type transistor circuits work fine for small AC input signals but suffer from one major disadvantage, the bias Q-point of a bipolar amplifier depends on the same Beta value which may vary from transistors of the same type, ie. the Q-point for one transistor is not necessarily the same as the Q-point for another transistor of the same type due to the inherent manufacturing tolerances. If this occurs the amplifier may not be linear and Amplitude Distortion will result but careful choice of the transistor and biasing components can minimise the effect of amplifier distortion.

Amplitude Distortion

Amplitude distortion occurs when the peak values of the frequency waveform are attenuated causing distortion due to a shift in the Q-point and amplification may not take place over the whole signal cycle. This non-linearity of the output waveform is shown below.

Amplitude Distortion due to Incorrect Biasing



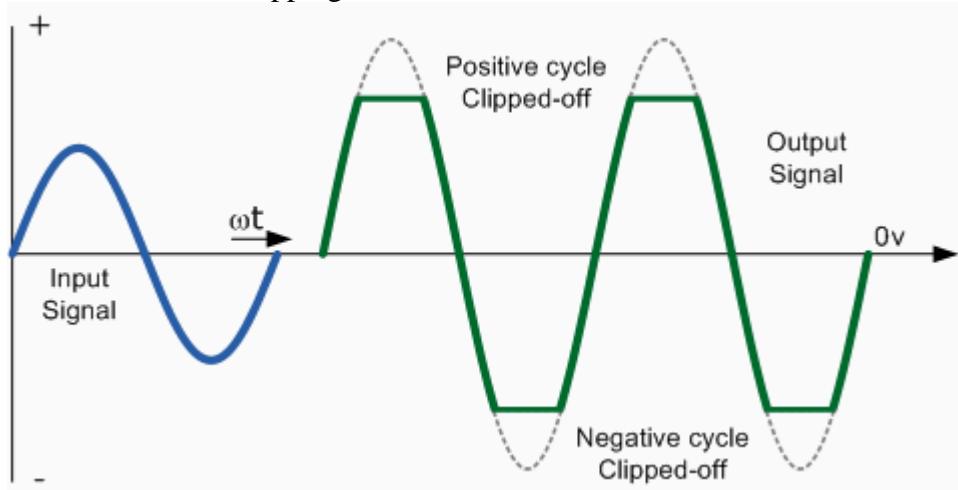
If the bias is correct the output waveform should look like that of the input waveform only bigger, (amplified). If there is insufficient bias the output waveform will look like the one on the right with the negative part of the output waveform "cut-off". If there is too much bias the output waveform will look like the one on the left with the positive part "cut-off". When the bias voltage is too small, during the negative part of the cycle the transistor does not conduct fully so

the output is set by the supply voltage. When the bias is too great the positive part of the cycle saturates the transistor and the output drops almost to zero.

Even with the correct biasing voltage level set, it is still possible for the output waveform to become distorted due to a large input signal being amplified by the circuit's gain. The output voltage signal becomes clipped in both the positive and negative parts of the waveform and no longer resembles a sine wave, even when the bias is correct. This type of amplitude distortion is called Clipping and is the result of "Over-driving" the input of the amplifier.

When the input amplitude becomes too large, the clipping becomes substantial and forces the output waveform signal to exceed the power supply voltage rails with the peak (+ve half) and the trough (-ve half) parts of the waveform signal becoming flattened or "Clipped-off". To avoid this the maximum value of the input signal must be limited to a level that will prevent this clipping effect as shown above.

Amplitude Distortion due to Clipping



Amplitude Distortion greatly reduces the efficiency of an amplifier circuit. These "flat tops" of the distorted output waveform either due to incorrect biasing or over driving the input do not contribute anything to the strength of the output signal at the desired frequency. Having said all that, some well known guitarists and rock bands actually prefer that their distinctive sound is highly distorted or "overdriven" by heavily clipping the output waveform to both the +ve and -ve power supply rails. Also, excessive amounts of clipping can also produce an output which resembles a "square wave" shape which can then be used in electronic or digital circuits.

We have seen that with a DC signal the level of gain of the amplifier can vary with signal amplitude, but as well as Amplitude Distortion, other types of distortion can occur with AC signals in amplifier circuits, such as Frequency Distortion and Phase Distortion.

Frequency Distortion

Frequency Distortion occurs in a transistor amplifier when the level of amplification varies with frequency. Many of the input signals that a practical amplifier will amplify consist of the required signal waveform called the "Fundamental Frequency" plus a number of different frequencies called "Harmonics" superimposed onto it. Normally, the amplitude of these harmonics are a fraction of the fundamental amplitude and therefore have very little or no effect on the output waveform. However, the output waveform can become distorted if these harmonic frequencies increase in amplitude with regards to the fundamental frequency. For example, consider the waveform below:

Frequency Distortion due to Harmonics

In the example above, the input waveform consists of the fundamental frequency plus a second harmonic signal. The resultant output waveform is shown on the right hand side. The frequency distortion occurs when the fundamental frequency combines with the second harmonic to distort the output signal. Harmonics are therefore multiples of the fundamental frequency and in our simple example a second harmonic was used. Therefore, the frequency of the harmonic is 2 times the fundamental, $2 \times f$ or $2f$. Then a third harmonic would be $3f$, a fourth, $4f$, and so on. Frequency distortion due to harmonics is always a possibility in amplifier circuits containing reactive elements such as capacitance or inductance.

Phase Distortion

Phase Distortion or Delay Distortion occurs in a non-linear transistor amplifier when there is a time delay between the input signal and its appearance at the output. If we call the phase change between the input and the output zero at the fundamental frequency, the resultant phase angle delay will be the difference between the harmonic and the fundamental. This time delay will depend on the construction of the amplifier and will increase progressively with frequency within the bandwidth of the amplifier. For example, consider the waveform below:

Phase Distortion due to Delay

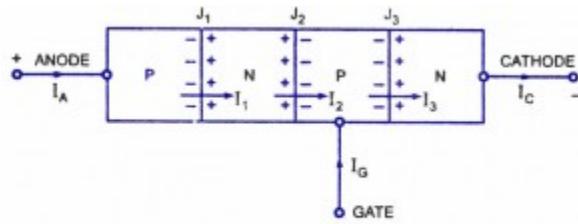
Any practical amplifier will have a combination of both "Frequency" and "Phase" distortion together with amplitude distortion but in most applications such as in audio amplifiers or power amplifiers, unless the distortion is excessive or severe it will not generally affect the operation of the system.

UNIT-V

Power semiconductor devices

TYRISTORS

Principle of Operation



Diagrammatic Representation Showing Current Flow and Voltage Bias in An SCR

SCR Working Principle

The **SCR** is a four-layer, three-junction and a three-terminal device and is shown in fig.a. The end P-region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. Ideally it remains off (voltage blocking state), or appears to have an infinite impedance until both the anode and gate terminals have suitable positive voltages with respect to the cathode terminal. The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero impedance in conduction state. For switching off or reverting to the blocking state, there must be no gate signal and the anode current must be reduced to zero. Current can flow only in one direction.

In absence of external bias voltages, the majority carrier in each layer diffuses until there is a built-in voltage that retards further diffusion. Some majority carriers have enough energy to cross the barrier caused by the retarding electric field at each junction. These carriers then become minority carriers and can recombine with majority carriers. Minority carriers in each layer can be accelerated across each junction by the fixed field, but because of absence of external circuit in this case the sum of majority and minority carrier currents must be zero.

A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which include the following terms:

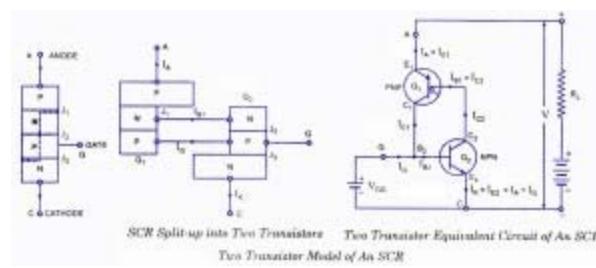
The current I_x is due to

- Majority carriers (holes) crossing junction J₁
- Minority carriers crossing junction J₁
- Holes injected at junction J₂ diffusing through the N-region and crossing junction J₁ and
- Minority carriers from junction J₂ diffusing through the N-region and crossing junction J₁.

Similarly I₂ is due to six terms and I₃ is due to four terms.

The two simple analogues to explain the basic action for the thyristor are those of the diode and the two transistor models.

1. **1. Diode Model.** The thyristor is similar to three diodes in series as there are three P-N junctions. Without gate bias, there is always at least one reverse biased junction to prevent conduction irrespective of the polarity of an applied voltage between anode and cathode. If the anode is made positive and the gate is also biased positively with respect to cathode, the P-layer at the gate is flooded by the electrons from the cathode and loses its identity as a P-layer. Accordingly the thyristor becomes equivalent to a conducting diode.



Scr working

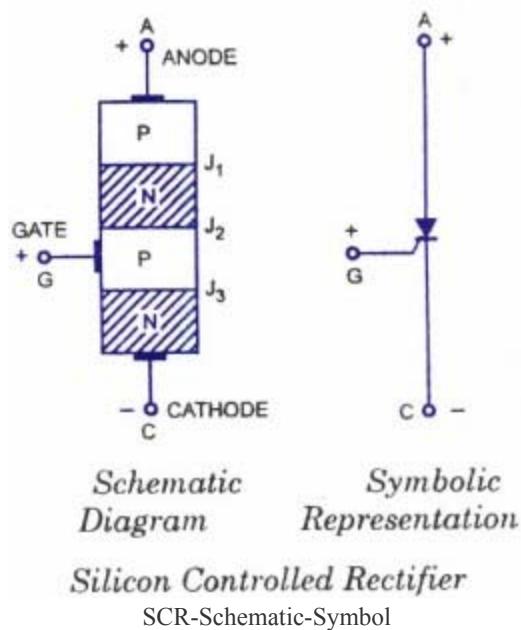
2. **2. Two Transistor Model.** Imagine the SCR cut along the dotted line, as shown in fig. a. Then we can have two devices, as shown in fig.b. These two devices can be recognized as two transistors. The upper left one is P-N-P transistor and the lower right N-P-N type. Further it can be recognized that the base of the P-N-P transistor is joined to the collector of the N-P-N transistor while the collector of P-N-P is joined to the base of N-P-N transistor, as illustrated in fig. c. The gate terminal is brought out from the base of the N-P-N material. This construction has been conceived merely to explain the working of SCR, otherwise in physical shape the SCR has four solid layers of P-N-P-N type only.

Now we can see that the two transistors are connected in such a manner that the collector of Q₁ is connected to the base of Q₂ i.e. the output collector current of Q₁ becomes the base current for Q₂. In the similar way the collector of Q₂ is joined to the base of Q₁ which shows that the output collector current of Q₂ is fed to Q₁ as input base current. These are back to back connections of transistors in such a way that the output of one goes into as input of other transistor and vice-versa. This gives net gain of loop circuit as $\beta_1 \times \beta_2$ where β_1 and β_2 are current gains of two transistors respectively.

When the gate current is zero or the gate terminal is open, the only current in circulation is the leakage current, which is very small in case of silicon device specially and the total current is a little higher than sum of individual leakage currents. Under these conditions P-N-P-N device is said to be in its forward blocking or high impedance ‘off state. As soon as a small amount of gate

current is given to the base of transistor Q_2 by applying forward bias to its base-emitter junction, it generates the collector current as β_2 times the base current. This collector current of Q_2 is fed as input base current to Q_1 which is further multiplied by β_1 times as I_{C1} which forms input base current of Q_2 and undergoes further amplification. In this way both transistors feedback each other and the collector current of each goes on multiplying. This process is very quick and soon both the transistors drive each other to saturation. Now the device is said to be in on-state. The current through the on-state SCR is controlled by external impedance only.

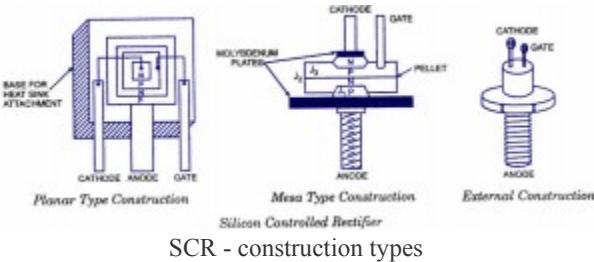
Silicon Controlled Rectifier



As the terminology indicates, the **SCR** is a controlled rectifier constructed of a silicon semiconductor material with a third terminal for control purposes. Silicon was chosen because of its high temperature and power capabilities. The basic operation of the SCR is different from that of an ordinary two-layer semiconductor diode in that a third terminal called a gate, determines when the rectifier switches from the open-circuit to short-circuit state. It is not enough simply to forward-bias the anode-to-cathode region of the device. In the conduction state the dynamic resistance of the SCR is typically 0.01 to 0.1 ohm and reverse resistance is typically 100 kilo ohm or more. It is widely used as a switching device in power control applications. It can control loads by switching on and off upto many thousand times a second. It can switch on for a variable lengths of time duration, thereby delivering desired amount of power to the load. Thus, it possesses the advantage of a rheostat as well as a switch with none of their drawback. A schematic diagram and symbolic representation of an SCR are shown in figures a & b respectively. As illustrated in fig-a, SCR is a three-terminal four-layer semiconductor device, the layers being alternately of P-type and N-type. The junctions are marked J_1 , J_2 and J_3 (junctions J_1 and J_3 operate in forward direction while middle junction J_2 operates in the reverse direction) whereas the three terminals are anode (A), cathode (C) and gate (G) which is connected to the inner P-type layer. The function of the

gate is to control the firing of SCR. In normal operating conditions, anode is positive with respect to cathode.

Construction of an SCR



From fig a it is clear that SCR is essentially an ordinary rectifier (PN) and a junction transistor (N-P-N) combined in one unit to form PNPN device. Three terminals are taken: one from the outer P-type material, known as anode, second from the outer N-type material, known as cathode and the third from the base of transistor section known as the gate.

The basic material used for fabrication of an SCR is N-type silicon. It has a specific resistance of about 6 ohm-mm. Silicon is the natural choice as base material because of the following advantages

- (i) ability to withstand high junction temperature of the order of 150° C
- (ii) high thermal conductivity;
- (iii) less variations in characteristics with temperature; and
- (iv) less leakage current in P-N junction.

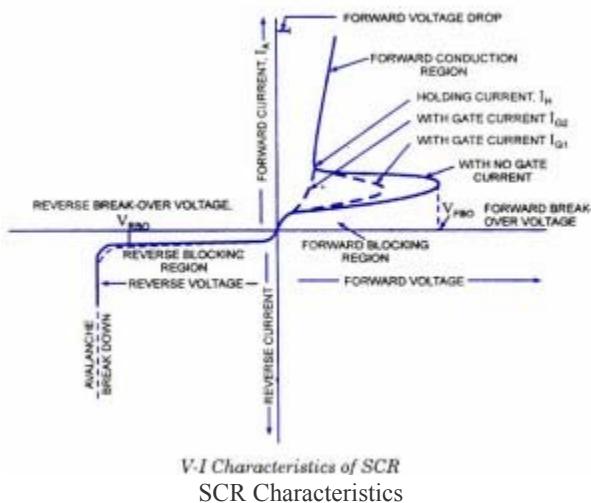
It consists, essentially, of a four layer pellet of P and N type silicon semiconductor materials. The junctions are diffused or alloyed. The material which may be used for P diffusion is aluminium and for N diffusion is phosphorous. The contact with anode can be made with an aluminium foil and through cathode and gate by metal sheet. Diffusion must be carried out at a proper temperature and for necessary duration to provide correct concentration because this decides the properties of the device. Low power SCRs employ the planar construction shown in fig a. Planar construction is useful for making a number of units from a silicon wafer. Here, all the junctions are diffused. The other technique is the mesa construction shown in fig.b. This technique is used for high power SCRs. In this technique, the inner junction J₂ is obtained by diffusion, and then the outer two layers are alloyed to it. The PNPN pellet is properly braced with tungsten or molybdenum plates to provide greater mechanical strength and make it capable of handling large currents. One of these plates is hard soldered to a copper or an aluminium stud, which is threaded for attachment to a heat sink. This provides an efficient thermal path for conducting the internal losses to the surrounding medium. The uses of hard solder between the pellet and back-up plates minimises thermal fatigue, when the SCRs are subjected to temperature induced stresses. For medium and low power SCRs, the pellet is mounted directly on the copper stud or casing, using a soft solder which absorbs the thermal stresses set up by differential expansion and provides a good thermal path for heat transfer.

For a larger cooling arrangement, which is required for high power SCRs, the press-pack or hockey-puck construction is employed, which provides for double-sided air for cooling.

The salient features to be considered, while designing an SCR, are the diameter and thickness of wafer, composition of the base material, type and amount of the material to be diffused into the wafer, shape, position and contact area of the gate, shape and size of the SCR, type of heat sink etc.

Fabrication technology determines various properties of the device. The voltage rating of a device can be increased by lightly doping the inner two layers and increasing their thickness. But due to this increased resistance, forward voltage drop increases and large triggering currents are required causing greater power dissipation accompanied by smaller current ratings. The heat dissipation of silicon falls from 1.5 W/cm^2 at 25° C to 1.25 W/cm^2 at 125° C . A high voltage power device can seldom be used beyond 125° C .

The current carrying capacity and voltage rating of the device can be increased by irradiating silicon with neutrons. The current rating of the device can also be increased by reducing the current density at the junction but this result in a bulky device with large turn-on time.



As already mentioned, the **SCR** is a four-layer device with three terminals, namely, the anode, the cathode and the gate. When the anode is made positive with respect to the cathode, junctions J_1 and J_3 are forward biased and junction J_2 is reverse-biased and only the leakage current will flow through the device. The SCR is then said to be in the forward blocking state or in the forward mode or off state. But when the cathode is made positive with respect to the anode, junctions J_1 and J_3 are reverse-biased, a small reverse leakage current will flow through the SCR and the SGR is said to be in the reverse blocking state or in reverse mode.

When the anode is positive with respect to cathode i.e. when the SCR is in forward mode, the SCR does not conduct unless the forward voltage exceeds certain value, called the forward breakover voltage, V_{FB0} . In non-conducting state, the current through the SCR is the leakage current which is very small and is negligible. If a positive gate current is supplied, the SCR can become

conducting at a voltage much lesser than forward break-over voltage. The larger the gate current, lower the break-over voltage. With sufficiently large gate current, the SCR behaves identical to PN rectifier. Once the SCR is switched on, the forward voltage drop across it is suddenly reduced to very small value, say about 1 volt. In the conducting or on-state, the current through the SCR is limited by the external impedance.

When the anode is negative with respect to cathode, that is when the SCR is in reverse mode or in blocking state no current flows through the SCR except very small leakage current of the order of few micro-amperes. But if the reverse voltage is increased beyond a certain value, called the reverse break-over voltage, V_{RBO} avalanche break down takes place. Forward break-over voltage V_{FB0} is usually higher than reverse breakdown voltage, V_{RBO} .

From the foregoing discussion, it can be seen that the SCR has two stable and reversible operating states. The change over from off-state to on-state, called turn-on, can be achieved by increasing the forward voltage beyond V_{FB0} . A more convenient and useful method of turn-on the device employs the gate drive. If the forward voltage is less than the forward break-over voltage, V_{FB0} , it can be turned-on by applying a positive voltage between the gate and the cathode. This method is called the gate control. Another very important feature of the gate is that once the SCR is triggered to on-state the gate loses its control.

Insulated Gate Bipolar Transistor (IGBT) Basics

Operation Modes

Forward-Blocking and Conduction Modes

When a positive voltage is applied across the collector-to-emitter terminal with gate shorted to emitter shown in Figure 1, the device enters into forward blocking mode with junctions J1 and J3 are forward-biased and junction J2 is reverse-biased. A depletion layer extends on both-sides of junction J2 partly into P-base and N-drift region.

An IGBT in the forward-blocking state can be transferred to the forward conducting state by removing the gate-emitter shorting and applying a positive voltage of sufficient level to invert the Si below gate in the P base region. This forms a conducting channel which connects the N⁺ emitter to the N⁻-drift region. Through this channel, electrons are transported from the N⁺ emitter to the N⁻-drift. This flow of electrons into the N⁻-drift lowers the potential of the N⁻-drift region whereby the P⁺ collector/ N⁻-drift becomes forward-biased. Under this forward-biased condition, a high density of minority carrier holes is injected into the N⁻-drift from the P⁺ collector. When the injected carrier concentration is very much larger the background concentration, a condition defined as a plasma of holes builds up in the N⁻-drift region. This plasma of holes attracts electrons from the emitter contact to maintain local charge neutrality. In this manner, approximately equal excess concentrations of holes and electrons are gathered in the N⁻-drift region. This excess electron and hole concentrations drastically enhance the conductivity of N⁻-drift region. This mechanism in rise in conductivity is referred to as the conductivity modulation of the N⁻-drift region.

Reverse-Blocking Mode

When a negative voltage is applied across the collector-to-emitter terminal shown in Figure 1, the junction J1 becomes reverse-biased and its depletion layer extends into the N⁻-drift region. The break down voltage during the reverse-blocking is determined by an open-base BJT formed by the P⁺ collector/ N⁻-drift/P-base regions. The device is prone to punch-through if the N⁻-drift region is very lightly-doped. The desired reverse voltage capability can be obtained by optimizing the resistivity and thickness of the N⁻-drift region.

The width of the N⁻-drift region that determines the reverse voltage capability and the forward voltage drop which increases with increasing width can be determined by

$$d_1 = \sqrt{\frac{2\epsilon_o\epsilon_s V_m}{qN_D}} + L_p \quad (1)$$

Where,

L_P = Minority carrier diffusion length

V_m = Maximum blocking voltage

ε_o = Permittivity of free space

ϵ_s = Dielectric constant of Si

q = Electronic charge

N_D = Doping concentration of N-drift region

Note: Reverse blocking IGBT is rare and in most applications, an anti-parallel diode (FRED) is used.

Output Characteristics

The plot for forward output characteristics of an NPT-IGBT is shown in Figure 5. It has a family of curves, each of which corresponds to a different gate-to-emitter voltage (V_{GE}). The collector current (I_C) is measured as a function of collector-emitter voltage (V_{CE}) with the gate-emitter voltage (V_{GE}) constant.

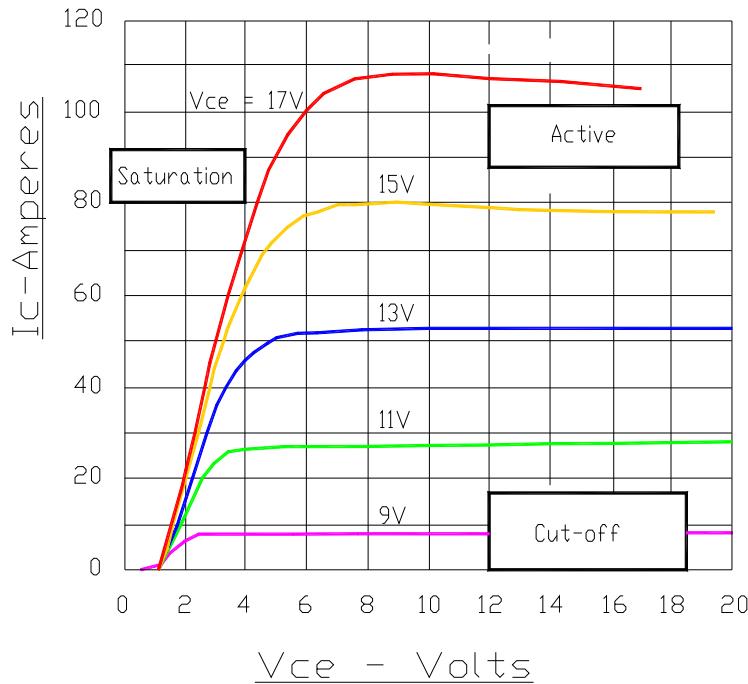


Figure 5: Output I-V characteristics of an NPT-IGBT [IXSH 30N60B2D1] [3]

A distinguishing feature of the characteristics is the 0.7V offset from the origin. The entire family of curves is translated from the origin by this voltage magnitude. It may be recalled that with a P⁺ collector, an extra P-N junction has been incorporated in the IGBT structure. This P-N junction makes its function fundamentally different from the power MOSFET.

Transfer Characteristics

The transfer characteristic is defined as the variation of I_{CE} with V_{GE} values at different temperatures, namely, 25°C, 125°C, and -40°C. A typical transfer characteristic is shown in Figure 6. The gradient of transfer characteristic at a given temperature is a measure of the transconductance (g_{fs}) of the device at that temperature.

$$g_{fs} = \frac{\partial I_C}{\partial V_{GE}} \Big|_{V_{CE}=\text{Constant}} \quad (2)$$

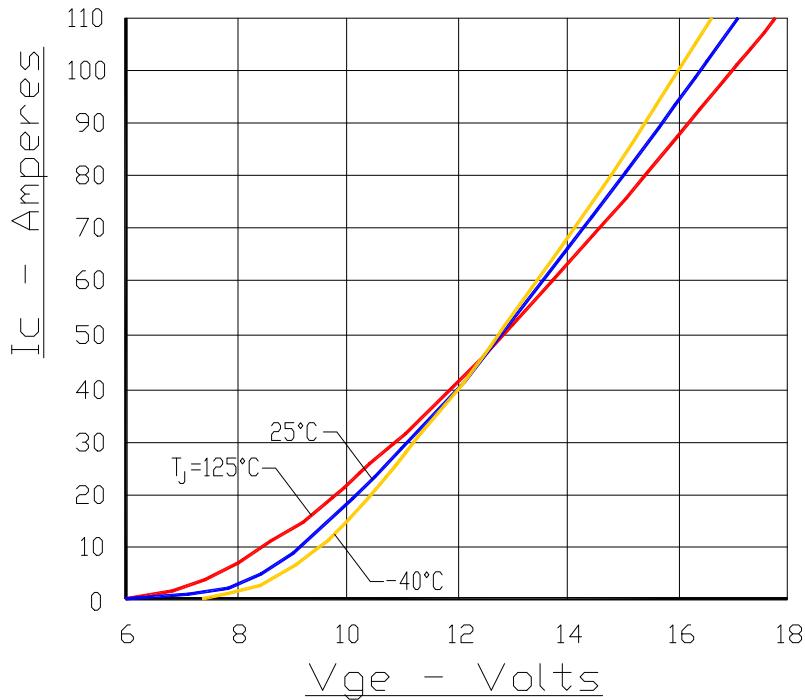


Figure 6: IGBT Transfer Characteristics [IXSH30N60B2]

A large g_{fs} is desirable to obtain a high current handling capability with low gate drive voltage. The channel and gate structures dictate the g_{fs} value. Both g_{fs} and $R_{DS(on)}$ (on-resistance of IGBT) are controlled by the channel length which is determined by the difference in diffusion depths of the P base and N⁺ emitter. The point of intersection of the tangent to the transfer characteristic determines the threshold voltage ($V_{GE(th)}$) of the device.

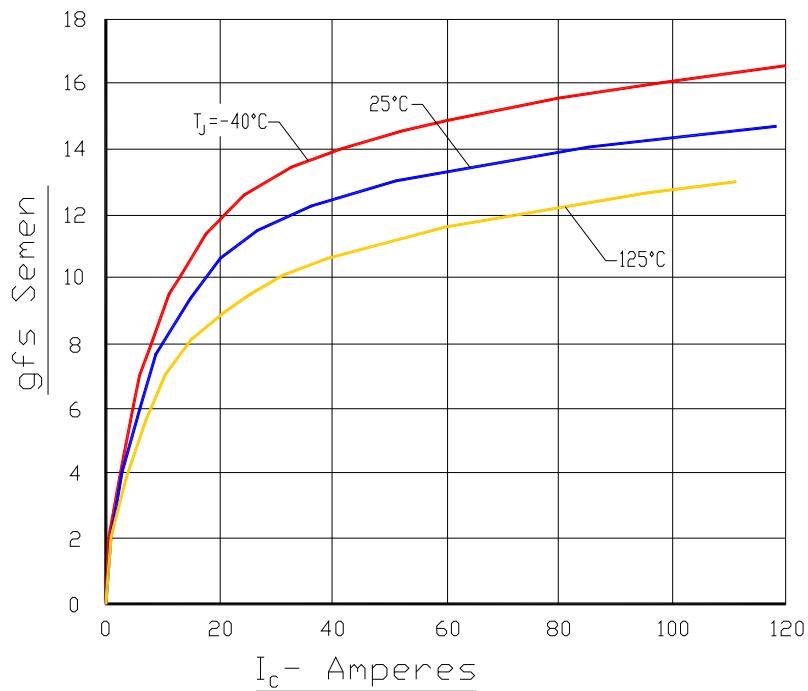
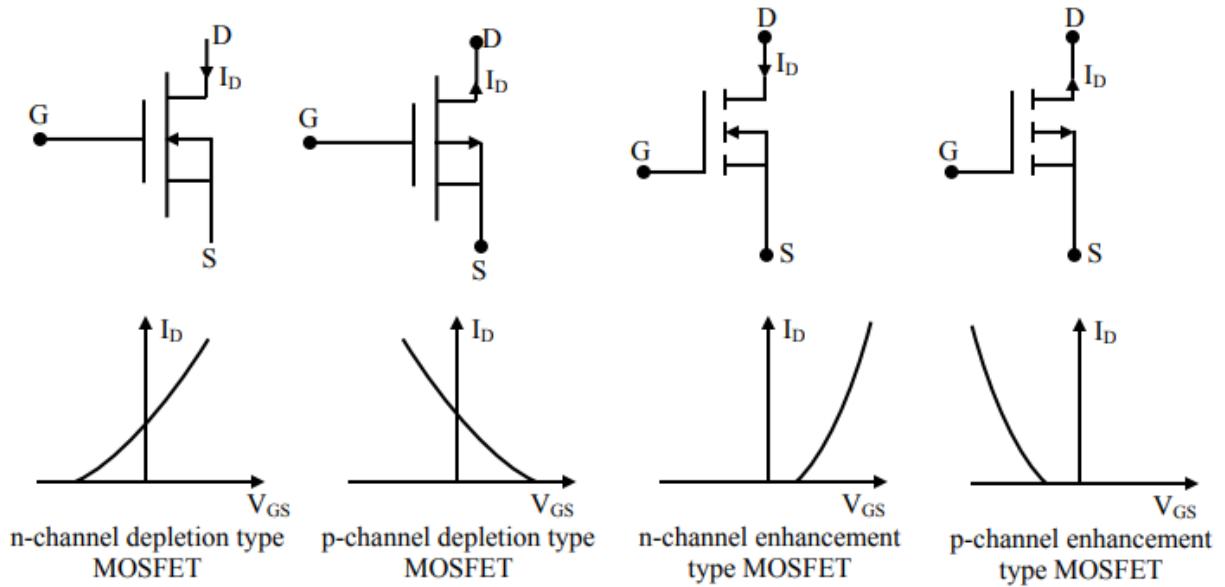


Figure 7: Transconductance Characteristics of an IGBT [IXSH30N60B2]

A typical transconductance (g_{fs}) vs collector current (I_C) is shown in Figure 7. The g_{fs} increases with collector current, flattening out at a peak level slowly for a range of collector currents. The g_{fs} flattens out because the saturation phenomenon in the parasitic MOSFET decreases the base current drive of the PNP transistor.

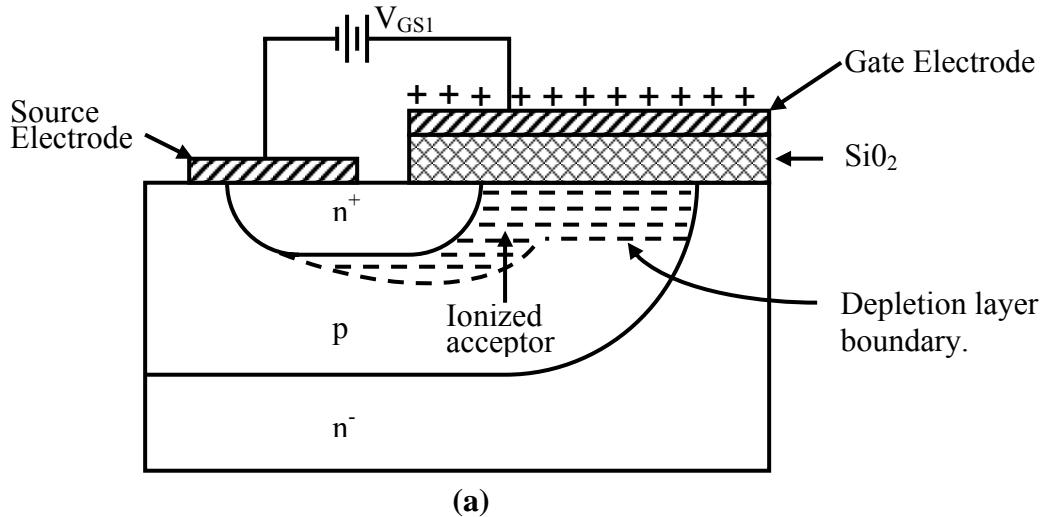
POWER MOSFET



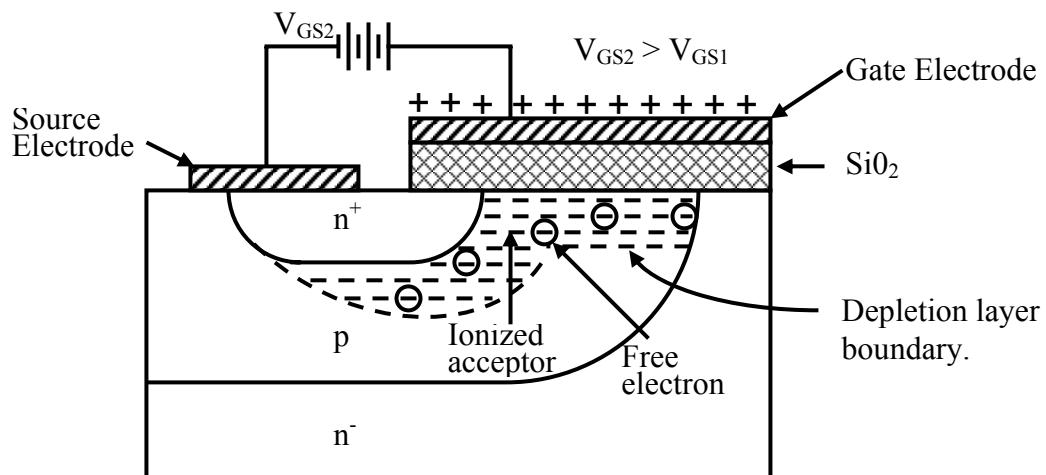
6.3 Operating principle of a MOSFET

At first glance it would appear that there is no path for any current to flow between the source and the drain terminals since at least one of the **p-n** junctions (source – body and body-Drain) will be reverse biased for either polarity of the applied voltage between the source and the drain. There is no possibility of current injection from the gate terminal either since the gate oxide is a very good insulator. However, application of a positive voltage at the gate terminal with respect to the source will convert the silicon surface beneath the gate oxide into an **n** type layer or “channel”, thus connecting the Source to the Drain as explained next.

The gate region of a MOSFET which is composed of the gate metallization, the gate (silicon) oxide layer and the p-body silicon forms a high quality capacitor. When a small voltage is application to this capacitor structure with gate terminal positive with respect to the source (note that body and source are shorted) a depletion region forms at the interface between the SiO_2 and the silicon as shown in Fig. 6.4 (a).



(a)



(b)

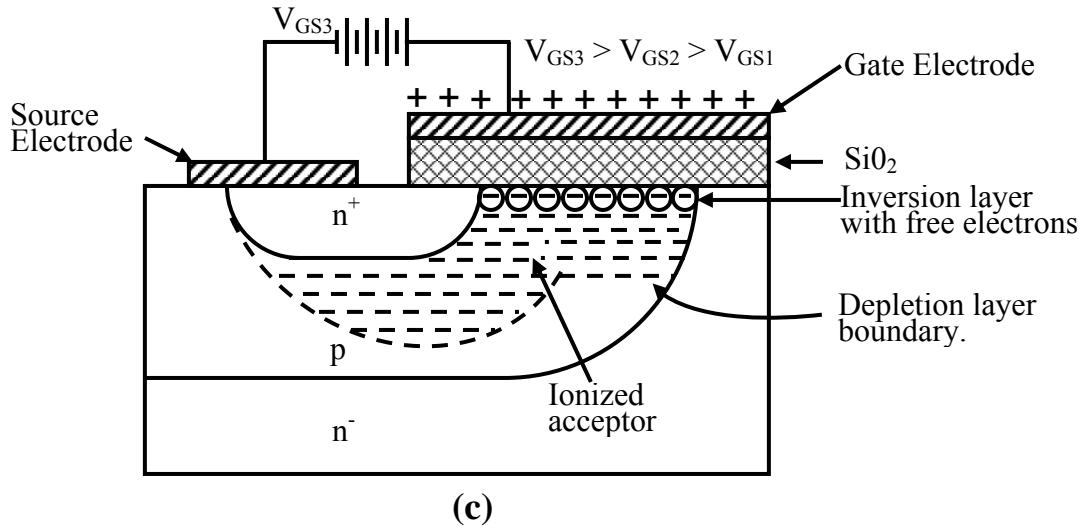


Fig. 6.4: Gate control of MOSFET conduction.

- (a) **Depletion layer formation;**
- (b) **Free electron accumulation;**
- (c) **Formation of inversion layer.**

The positive charge induced on the gate metallization repels the majority hole carriers from the interface region between the gate oxide and the **p** type body. This exposes the negatively charged acceptors and a depletion region is created.

Further increase in V_{GS} causes the depletion layer to grow in thickness. At the same time the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as shown in Fig 6.4 (b). The immediate source of electron is electron-hole generation by thermal ionization. The holes are repelled into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons from the source.

As V_{GS} increases further the density of free electrons at the interface becomes equal to the free hole density in the bulk of the body region beyond the depletion layer. The layer of free electrons at the interface is called the inversion layer and is shown in Fig 6.4 (c). The inversion layer has all the properties of an **n** type semiconductor and is a conductive path or “channel” between the drain and the source which permits flow of current between the drain and the source. Since current conduction in this device takes place through an **n**- type “channel” created by the electric field due to gate source voltage it is called “Enhancement type n-channel MOSFET”.

The value of V_{GS} at which the inversion layer is considered to have formed is called the “Gate – Source threshold voltage $V_{GS}(th)$ ”. As V_{GS} is increased beyond $V_{GS}(th)$ the inversion layer gets some what thicker and more conductive, since the density of free electrons increases further with increase in V_{GS} . The inversion layer screens the depletion layer adjacent to it from increasing V_{GS} . The depletion layer thickness now remains constant.

Exercise 6.1 (after section 6.3)

1. Fill in the blank(s) with the appropriate word(s)
 - i. A MOSFET is a _____ controlled _____ carrier device.
 - ii. Enhancement type MOSFETs are normally _____ devices while depletion type MOSFETs are normally _____ devices.
 - iii. The Gate terminal of a MOSFET is isolated from the semiconductor by a thin layer of _____.
 - iv. The MOSFET cell embeds a parasitic _____ in its structure.
 - v. The gate-source voltage at which the _____ layer in a MOSFET is formed is called the _____ voltage.
 - vi. The thickness of the _____ layer remains constant as gate source voltage is increased beyond the _____ voltage.

Answer: (i) voltage, majority; (ii) off, on; (iii) SiO_2 , (iv) BJT, (v) inversion, threshold; (vi) depletion, threshold.

2. What are the main constructional differences between a MOSFET and a BJT? What effect do they have on the current conduction mechanism of a MOSFET?

Answer: A MOSFET like a BJT has alternating layers of **p** and **n** type semiconductors. However, unlike BJT the **p** type body region of a MOSFET does not have an external electrical connection. The gate terminal is insulated from the semiconductor by a thin layer of SiO_2 . The body itself is shorted with **n⁺** type source by the source metallization. Thus minority carrier injection across the source-body interface is prevented. Conduction in a MOSFET occurs due to formation of a high density **n** type channel in the **p** type body region due to the electric field produced by the gate-source voltage. This **n** type channel connects **n⁺** type source and drain regions. Current conduction takes place between the drain and the source through this channel due to flow of electrons only (majority carriers). Whereas in a BJT, current conduction occurs due to minority carrier injection across the Base-Emitter junction. Thus a MOSFET is a voltage controlled majority carrier device while a BJT is a minority carrier bipolar device.

6.4 Steady state output i-v characteristics of a MOSFET

The MOSFET, like the BJT is a three terminal device where the voltage on the gate terminal controls the flow of current between the output terminals, Source and Drain. The source terminal is common between the input and the output of a MOSFET. The output characteristics of a MOSFET is then a plot of drain current (i_D) as a function of the Drain – Source voltage (v_{DS}) with gate source voltage (v_{GS}) as a parameter. Fig 6.5 (a) shows such a characteristics.

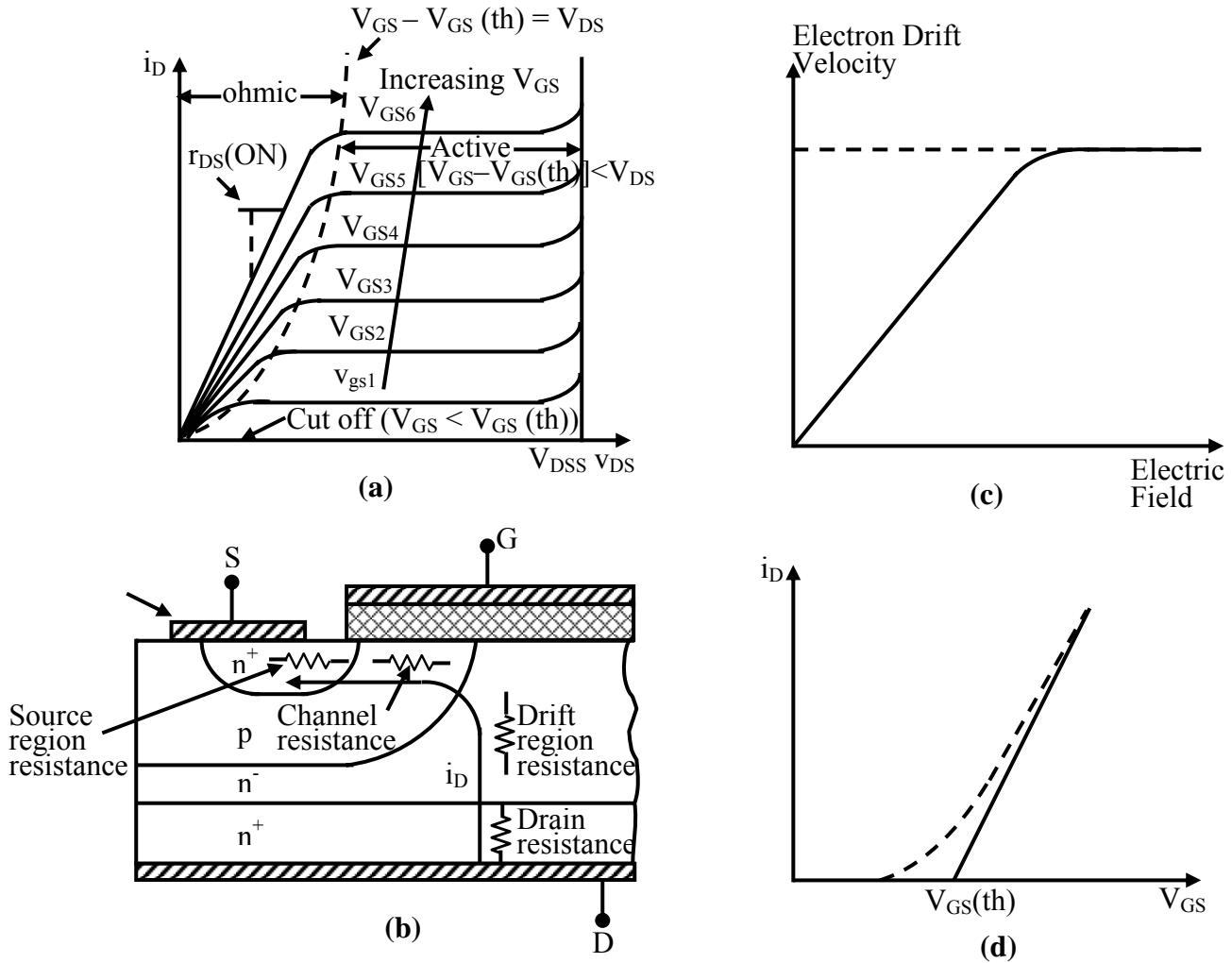


Fig. 6.5: Output i-v characteristics of a Power MOSFET

- (a) **i-v characteristics;**
- (b) **Components of ON-state resistance;**
- (c) **Electron drift velocity vs Electric field;**
- (d) **Transfer**

With gate-source voltage (V_{GS}) below the threshold voltage ($v_{GS}(th)$) the MOSFET operates in the cut-off mode. No drain current flows in this mode and the applied drain-source voltage (v_{DS}) is supported by the body-collector p-n junction. Therefore, the maximum applied voltage should be below the avalanche break down voltage of this junction (V_{DSS}) to avoid destruction of the device.

When V_{GS} is increased beyond $v_{GS}(th)$ drain current starts flowing. For small values of v_{DS} ($v_{DS} < (V_{GS} - v_{GS}(th))$) i_D is almost proportional to v_{DS} . Consequently this mode of operation is called “ohmic mode” of operation. In power electronic applications a MOSFET is operated either in the cut off or in the ohmic mode. The slope of the $v_{DS} - i_D$ characteristics in this mode is called the ON state resistance of the MOSFET ($r_{DS}(\text{ON})$). Several physical resistances as shown in Fig 6.5 (b) contribute to $r_{DS}(\text{ON})$. Note that $r_{DS}(\text{ON})$ reduces with increase in v_{GS} . This is mainly due to reduction of the channel resistance at higher value of

v_{GS} . Hence, it is desirable in power electronic applications, to use as large a gate-source voltage as possible subject to the dielectric break down limit of the gate-oxide layer.

At still higher value of v_{DS} ($v_{DS} > (v_{GS} - v_{GS(\text{th})})$) the $i_D - v_{DS}$ characteristics deviates from the linear relationship of the ohmic region and for a given v_{GS} , i_D tends to saturate with increase in v_{DS} . The exact mechanism behind this is rather complex. It will suffice to state that, at higher drain current the voltage drop across the channel resistance tends to decrease the channel width at the drain drift layer end. In addition, at large value of the electric field, produced by the large Drain – Source voltage, the drift velocity of free electrons in the channel tends to saturate as shown in Fig 6.5 (c). As a result the drain current becomes independent of V_{DS} and determined solely by the gate – source voltage v_{GS} . This is the active mode of operation of a MOSFET. Simple, first order theory predicts that in the active region the drain current is given approximately by

$$i_D = K(v_{GS} - v_{GS(\text{th})})^2 \quad (6.1)$$

Where K is a constant determined by the device geometry.

At the boundary between the ohmic and the active region

$$v_{DS} = v_{GS} - v_{GS(\text{th})} \quad (6.2)$$

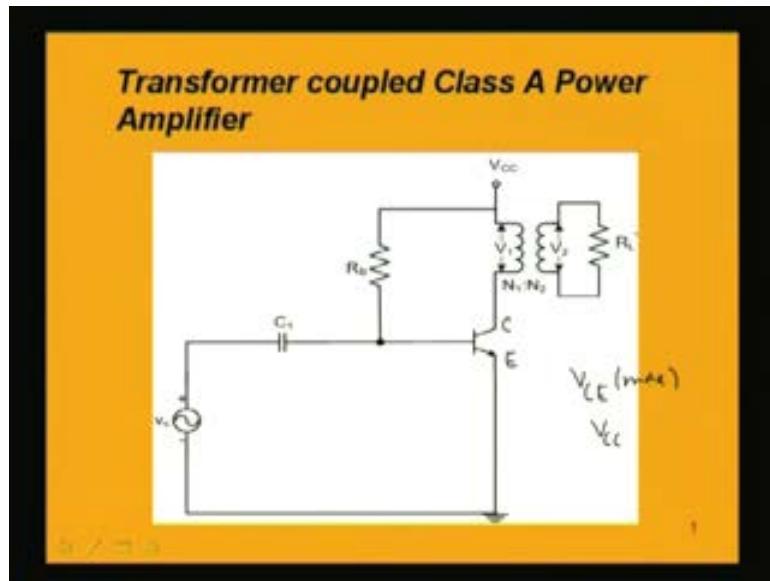
$$\text{Therefore, } i_D = Kv_{DS}^2 \quad (6.3)$$

Module -5
Power Circuits and System
Lecture - 2
Transformer Couple Power Amplifier

Today we will discuss about other type of class A power amplifier which is transformer couple class A power amplifier. In the last class we discussed about one type of class A power amplifier which is series fed and today we will discuss transformer couple large signal power amplifier. The transformer coupling, as the name suggests, there will be a transformer which will be used for coupling the load to the amplifier. Here let us consider a resistive load; for example when we have to use an audio power amplifier we have to drive a loudspeaker. We have to transfer power to a load having resistance around 5 to 15 ohm. This resistance is very small but here we are transferring power from the large signal amplifier using a transistor and we know that the output resistance of a transistor is quite high. So, here to transfer power from a device having high resistance to a load having very low resistance that mismatching of the impedance causes lesser transfer of power because the load is having a very small resistance and the device that is a transistor amplifier is having a high resistance.

It cannot transfer the whole amount of power because of mismatch in the impedances. We know from maximum power transfer theorem that if the load resistance as well as the resistance of the device from where we are transferring the power, these two impedances match. That is ideally when they are equal that is source resistance and load resistance are equal, then maximum power can be transferred. Here in view of that we are going to use a transformer at the output side. That is we are going to couple the load to the device or the amplifier through a transformer.

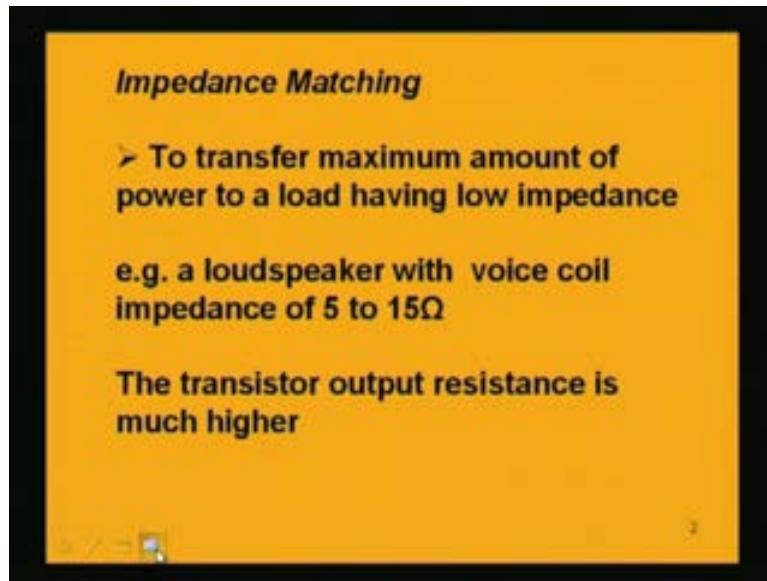
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That type of circuit is shown here where we are having a transformer having the turns ratio between the primary winding and the secondary winding; N_1 is to N_2 . A transformer, as we know, has two windings. One is the primary winding, other is the secondary winding and the primary winding is where we connect the supply and by induction we get an induced voltage in the secondary side. Here we are showing a transformer having number of turns in the primary N_1 and number of turns in the secondary N_2 . So, N_1 is to N_2 is the turns ratio.

The resistance R_L is a load resistance which is connected across the secondary of the transformer and we are using a fixed bias scheme given by this resistance R_B ; similar to that we discussed earlier in series fed class A power amplifier. Here the primary is having voltage V_1 and the secondary of the transformer is having the voltage V_2 .

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As I have mentioned this is to transfer maximum amount of power to the load having low impedance; for example in a loudspeaker where the voice coil impedance is only around 5 to 15 ohm. But the transistor output resistance used in the large signal amplifier is quite high; that is much higher than the loudspeaker voice coil impedance. So, we have to go through a transformer coupling.

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$$\frac{N_1}{N_2} = n = \frac{V_1}{V_2} = \frac{I}{k} = \frac{I_2}{I_1}$$

n = turns ratio

K = transformation ratio

$$V_1 I_1 = V_2 I_2 \rightarrow \frac{V_1}{V_2} = \frac{I_2}{I_1} = n \quad I_1 = \frac{I_2}{n}$$
$$K = \frac{V_2}{V_1} = \frac{I_1}{I_2}$$
$$\frac{V_1}{I_1} = \frac{V_2 I_2}{I_1^2} = \frac{V_2 I_2}{I_2^2 / n^2} = n^2 \frac{V_2}{I_2}$$

or, $R_L' = n^2 R_L$

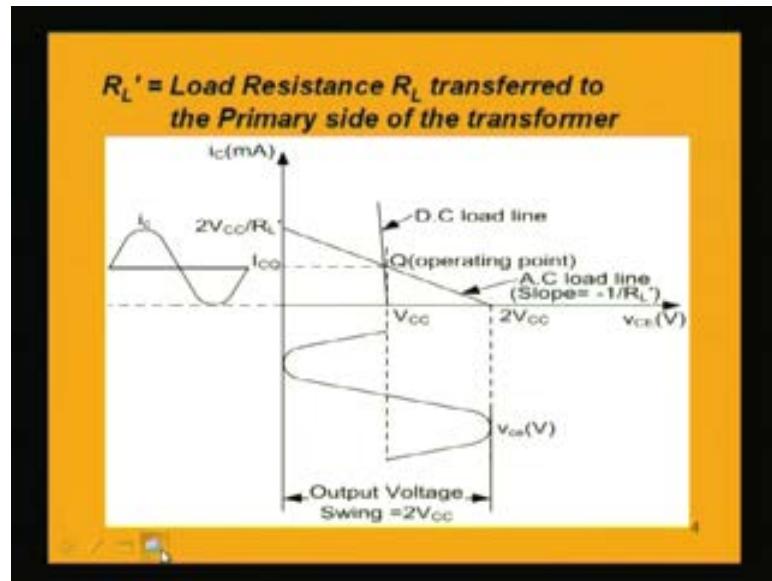
In this transformer as I have noted N_1 is the number of turns in the primary winding and N_2 is the number of turns in the secondary winding. The ratio between N_1 and N_2 is given by turns ratio and it is denoted by a small letter n and that is equal to V_1 by V_2 . That is the ratio between the windings of the primary and secondary determines at what ratio the supply voltage will be transferred to the secondary winding side. So, V_1 is to V_2 is given by the turns ratio n and that turns ratio n is actually 1 by K where K is the transformation ratio. That K which is transformation ratio is a term that is used in transformer to denote the ratio between V_2 and V_1 . So, actually K , the transformation ratio is V_2 by V_1 . It is equal to 1 by n .

Transformation ratio is 1 by turns ratio and assuming ideal transformer where the input power and output power are equal, $V_1 I_1$ is equal to $V_2 I_2$. That is the assumption we will use for ideal transformer and from that we can get that V_1 by I_1 is equal to, right side also if we divide by I_1 square that means both left hand side and right hand side if we divide by I_1 square what we get is V_1 by I_1 equal to $V_2 I_2$ by I_1 square. That can be written as $V_2 I_2$ by I_2 square by n square because from $V_1 I_1$ is equal to $V_2 I_2$ we get that V_1 by V_2 equal to I_2 by I_1 . As V_1 by V_2 is equal to n that is equal to I_2 by I_1 is equal to n . So, we can write I_1 as I_2 by n . Using that relation, here in place of I_1 we are substituting I_2 by n and as it is square, we get I_2 square by n square. This n square will come to the numerator. If we simplify it will be equal to n square into, one I_2 will cancel with one I_2 . So, what will remain is n square into V_2 by I_2 .

If we look into this expression that V_1 by I_1 equal to n square into V_2 by I_2 . Now V_1 by I_1 means, the resistance in the primary side if we look, the resistance which will be obtained in the primary side is nothing but the resistance R_L transferred to the primary side. The resistance which is actually in the secondary winding that is R_L , if we transfer this resistance from the secondary to the primary side then, we get the value as R_L dash which is equal to n square into R_L . The value of the resistance in the secondary winding that has to be multiplied by square of the turns ratio so that we can transfer that secondary winding load resistance R_L to the primary side and that value is denoted by R_L dash.

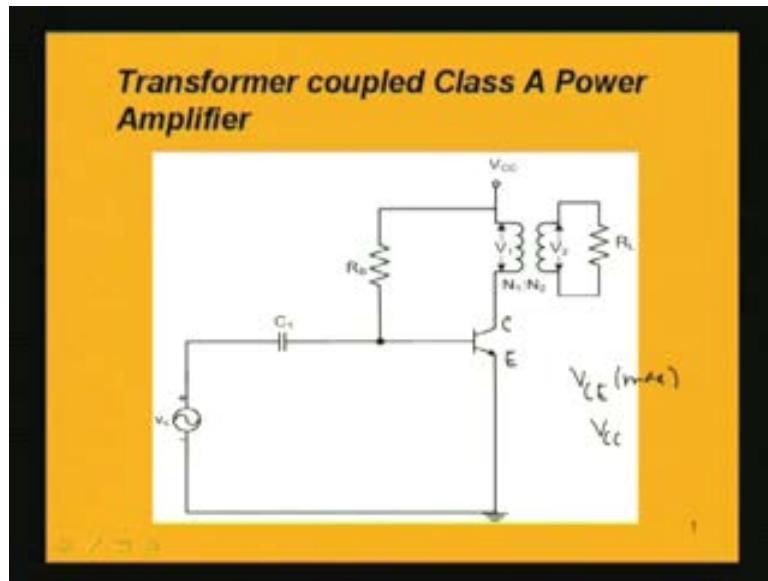
It is equivalently expressing that. We are having in the transformer primary resistance R_L dash which is nothing but the secondary resistance or load resistance transferred to the primary side. This is done in order to easily draw the load line which will be required in further analysis. Because it is a transistor which is being employed for this power amplifier or large signal amplifier, we will find out the efficiency that means the ratio between the output AC power to the input DC power and that requires the currents and voltages in the AC as well as the DC conditions and we have to draw load line for the transistor to see how the signal changes.

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If we now consider the load line for this transistor, then we have two load lines. One is the DC load line which is the load line for the prevailing DC conditions and under DC condition we will not have the R_L dash because the R_L dash that is the load resistance transferred from the secondary to the primary side will be only effective when we consider AC power because the load R_L dash or R_L is getting AC power. We are concerned about the AC power being transferred to the transformer secondary side load. If we consider the DC load line, we can draw the DC load line by noting down the maximum value of the DC collector current and the maximum value of the DC voltage.

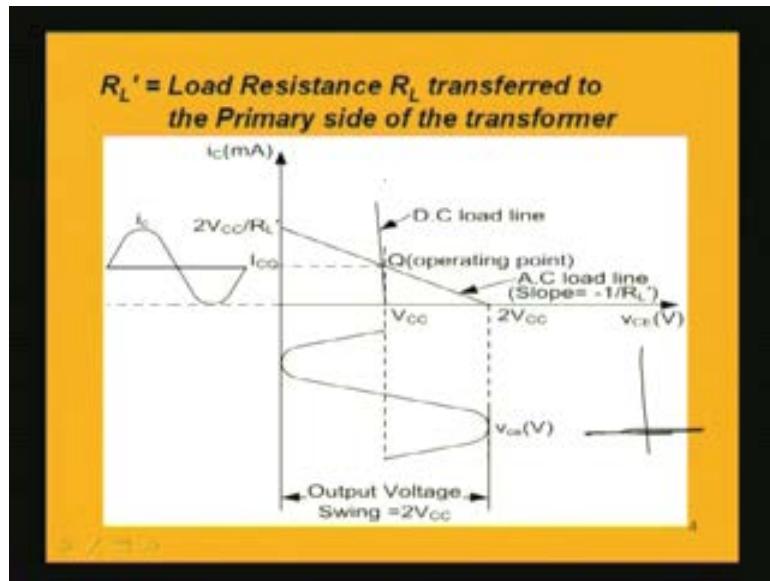
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If we look into the circuit again, when the DC condition prevails, if we are only interested in the DC condition then in this circuit if we consider from V_{CC} to ground this transformer primary is having very negligible resistance. It can be assumed to be almost zero. That is the transformer primary winding is having almost zero resistance. That is why in this part, the DC current which will flow will have no resistance and the current which will flow is almost infinite. The current which will flow, almost it will be like a short circuit current. If we consider this collector current then as there is no resistance, the current will be almost infinite and the voltage is V_{CC} .

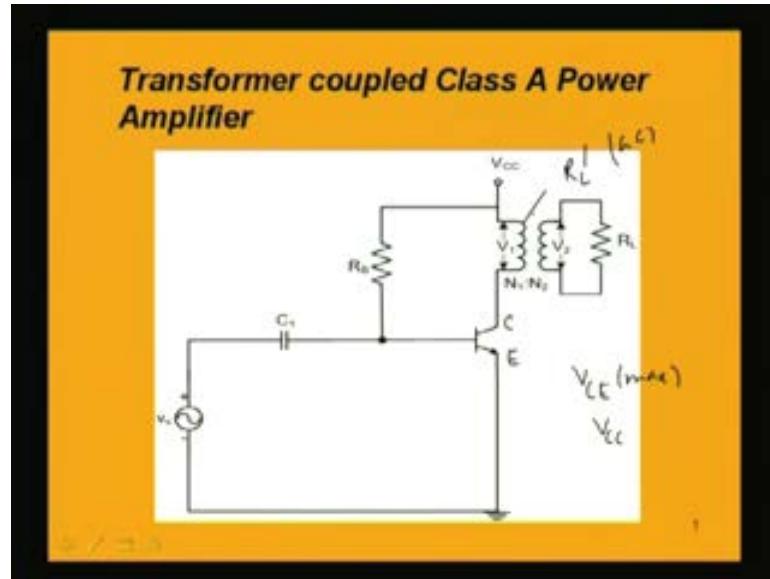
Collector to emitter we consider because, we have to know the maximum values of the collector to emitter voltage and the maximum value of the collector current to draw the DC load line. If we now consider this circuit in the collector side of the transistor, V_{CE} maximum value can be the value which is the supply voltage V_{CC} . So, under DC conditions the maximum collector to emitter voltage will be V_{CC} and maximum collector current will be infinite. It is infinitely large.

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The DC load line if we draw it is almost like a vertical line because current is reaching around infinite value and the collector to emitter voltage under DC is V_{CC} . Joining two points actually we get a vertical line and there is a very small resistance in the primary winding. Considering that exactly it will be not vertical but it will have a little slope; very small slope. This is the DC load line. To draw the AC load line, we consider the AC conditions prevailing and we have already seen that the primary of the transformer will have this R_L transferred to it by the value $R_{L'}$.

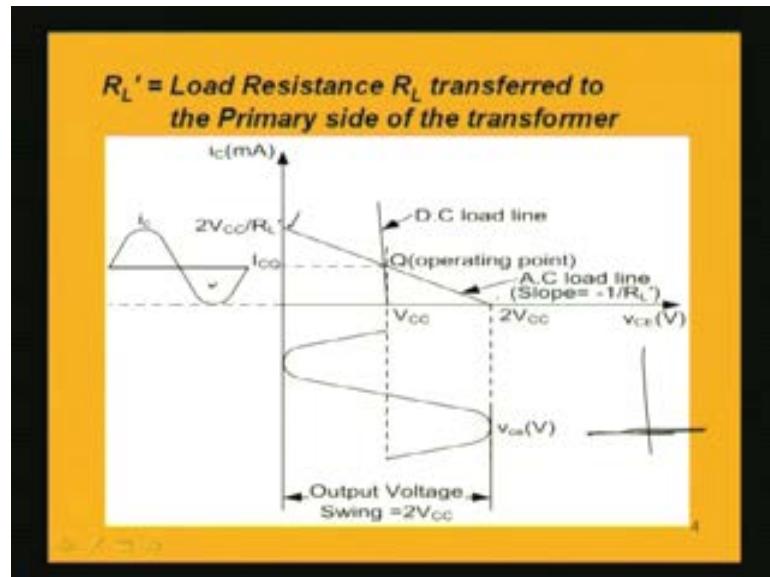
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That is in the primary winding we will have a resistance R_L dash. So, here will be a resistance R_L dash in the AC condition. As this transformer primary winding is having R_L dash which is equal to n^2 into R_L and the load line if we want to draw for AC, when there is no signal then, the voltage of the collector to emitter will be simply V_{CC} . That is the DC source V_{CC} .

When you apply the signal, this is the signal V_s which we are applying and we are applying a sinusoidal voltage, the current in the collector will be sinusoidally increasing and decreasing; it will be a sinusoidal wave. Starting from DC value it will increase and decrease. So, that point is Q point which is the DC point or quiescent point. We know that at that point the value of the collector to emitter voltage was V_{CC} and the collector current was say I_{CQ} . If we now apply the signal then the collector current will increase and decrease like this and when the collector current increases the collector to emitter voltage will decrease from V_{CC} and it will go down and the maximum collector current that can flow is at this point where the collector to emitter voltage will be zero.

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Then it will again increase and in this half cycle, when the collector current goes down to the negative half, the AC collector current goes to the negative half, then the collector to emitter voltage will increase beyond V_{CC} and the increment will be to this point. That is the maximum point on the load line and that point has the voltage of 2 times V_{CC} . When this maximum voltage between collector to emitter becomes 2 times V_{CC} , to understand that we have to see about the circuit; what is it having in the circuit? We are having a transformer. Transformer winding carries a current. When this current is in the negative half cycle, if we see the circuit again (Refer Slide Time: 19:27), the collector current which is flowing in the primary of the transformer if it goes down, as soon as it starts falling or decreasing then the collector current is that factor which establishes the flux in the core. If the flux goes down, then due to the Lenz law there will be an EMF which will be opposing the very cause behind it. That means it will not let the collector current to collapse and for encountering or for over coming that it will be actually aiding the voltage by increasing it to 2 times V_{CC} . It will aid the voltage V_{CC} . It will prevent the fall or collapse of the collector current. Due to the Lenz law it will not allow the collector current to fall and it will oppose the very cause behind the fall of the current. So, it will try to over come it and it will aid it by the voltage which will make it equal to V_{CC} and

that is why total voltage at that point when the collector current goes down to the valley will be 2 times V_{CC} total.

The maximum value of the collector current if we consider the signal then this is 2 times V_{CC} by R_L dash. R_L dash is the resistance in the primary winding. This 2 times V_{CC} by R_L dash will be this peak value of the collector current and this is equal to this portion. V_{CC} by R_L dash was here and the total will be twice V_{CC} by R_L dash; the maximum or the peak of the collector current. AC load line is having a slope of 1 by R_L dash. But it is in the negative direction because you can see from the AC load line, the slope is negative. This is the load line analysis and what is the maximum swing of the output voltage or collector to emitter voltage? From one peak to the other peak the total swing is 2 times V_{CC} .

With this knowledge of the load line analysis, we can proceed to find out what will be the output AC power. The AC power if we consider we know that the AC power is equal to the voltage and current multiplied but that voltage and current is the RMS voltage and RMS current. We are finding out the average power and average AC power is given by i_c peak to peak into V_{CE} peak to peak by 8.

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$$\begin{aligned}
 P_o & (\text{A.C}) \text{ (max)} \\
 & = \frac{i_c \text{ (peak to peak)} \cdot V_{CE} \text{ (peak to peak)}}{8} \\
 & = \frac{\left(\frac{2V_{CC}}{R_L} \right) \cdot 2V_{CC}}{8} \\
 & = \frac{V_{CC}^2}{2R_L} \\
 P_i & (\text{D.C})(Q) = V_{CC} I_{CQ} = V_{CC} \frac{V_{CC}}{R_L} = \frac{V_{CC}^2}{R_L}
 \end{aligned}$$

That we have earlier found in the class A series fed power amplifier also and we have deduced that. Putting down the value of i_c peak to peak and V_{CE} peak to peak, i_c peak to peak means this point to this point is twice V_{CC} by R_L dash and V_{CE} total swing peak to peak is 2 times V_{CC} divided by 8. Simplifying this expression we get, V_{CC} square divided by R_L dash into 2. This is the expression for the AC power output, maximum. We are considering the maximum AC power output; maximum because we are considering from this point to this point. The maximum value of this current it can have is 2 times V_{CC} by R_L dash.

This is the output power and the input power, which is a DC power, is provided by the source or battery V_{CC} and we know that the DC power is equal to V_{CC} into I_{CQ} and that can be written as V_{CC} into V_{CC} by R_L dash is equal I_{CQ} . Because this current I_{CQ} at this point (Refer Slide Time: 25:16) is the DC collector current, which is the Q point collector current. Q point is the quiescent point and at that quiescent point the collector current is I_{CQ} that is the DC collector current and that value is equal V_{CC} by R_L dash. Putting down this value V_{CC} by R_L dash multiplying with V_{CC} we get V_{CC} square by R_L dash. This is the DC input.

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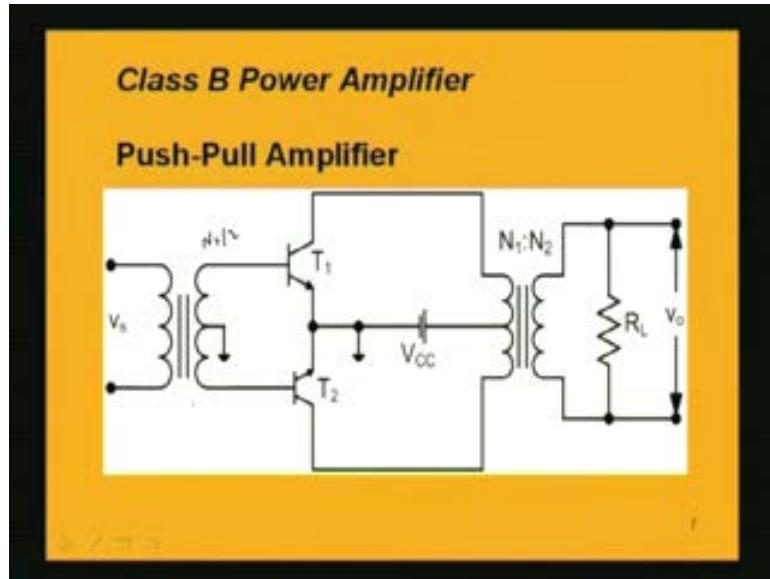
Maximum Efficiency of the amplifier

$$\begin{aligned}\eta &= \frac{P_o(\text{A.C})}{P_i(\text{D.C})} \\ &= \frac{V_{CC}^2 / 2R_L'}{V_{CC}^2 / R_L} \\ &= 50\%\end{aligned}$$

If we want to find out the maximum efficiency of this transformer couple amplifier, we have to take the ratio. We have to find the ratio between the output AC power and the DC input. Output AC power P_o AC we have found out to be V_{CC} square by twice R_L dash and V_{CC} square by R_L dash is the DC input. Putting down these values if we find out the maximum efficiency it boils down to half or 50%. So, here in the transformer couple amplifier we achieve a higher efficiency than the series fed class A power amplifier which we discussed earlier. We get 50% maximum efficiency in the transformer couple power amplifier.

The operation of this amplifier both series fed which we discussed earlier and the transformer couple power amplifier that we discussed today, they are both in class A operation. Because if we look into the output characteristic, I mean the collector current then we see that the current is flowing for whole cycle because it is not going down to either saturation or cut off. So, it is in class A operation; the conduction angle is 360 degree.

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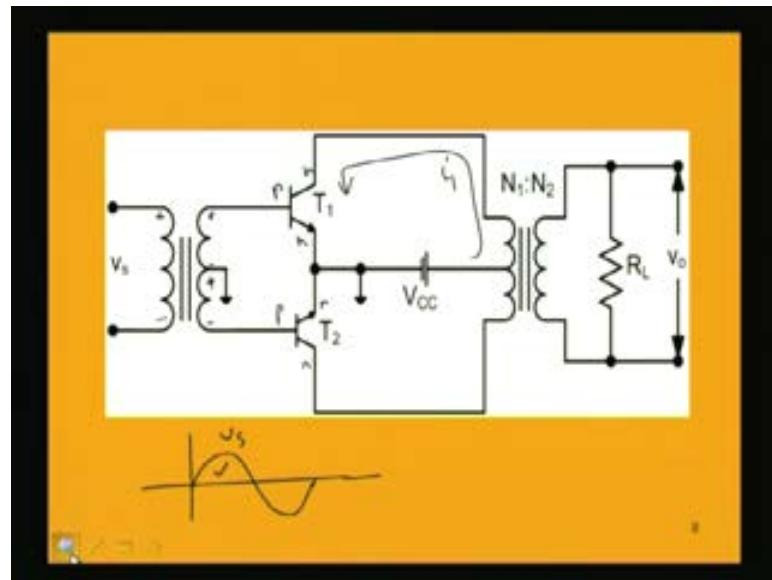
We consider another type of power amplifier. Depending upon the conduction angle we have another type of power amplifier which is class B power amplifier. In class B power amplifier, we know that the conduction angle is 180 degree. The quiescent point is located in such a way that it does not allow one half of the current cycle to flow. For example we have a push pull amplifier which is an example of a class B operation. What is there in this class B push pull type of amplifier? We have 2 transistors. They are shown as T₁ and T₂ and we are having transformer stages both at the input and the output. One example we are showing where we are having a transformer at this input stage and we are having another transformer at the output stage and the resistance R_L is connected to the secondary of the output stage transformer and the voltage across this R_L is V_o which is the output voltage we considered for driving any load and here given an AC input V_s, supply voltage at the input, this is a transformer which is having a center tap secondary.

The meaning of this center tap secondary is that actually we are having the same number of turns here from the upper half of this point and the lower half of this point. Suppose we have N₁ here, N₂ here in the secondary set then N₂ by 2 will be in this half; number of windings and N₂ by 2 will be in the lower half. That means exactly equal voltages will be induced in the two halves and we are considering N₁ is to N₂ that is the turns ratio in this

output stage transformer and here also we are using a center tap transformer. So, here if this total is N_1 , this will be N_1 by 2, this will be N_1 by 2.

We note here that we are having two transistors T_1 and T_2 , which are npn transistors. Both are similar type of transistors and V_{CC} is the source DC supply. As we are applying an input voltage which is sinusoidal what will happen in the positive half of the input? Let us consider when we have V_s in this positive half wave. Let us consider what will happen? How the operation of the transistor will proceed for the positive half of the input voltage cycle? In the positive half cycle this point is positive, this point is negative.

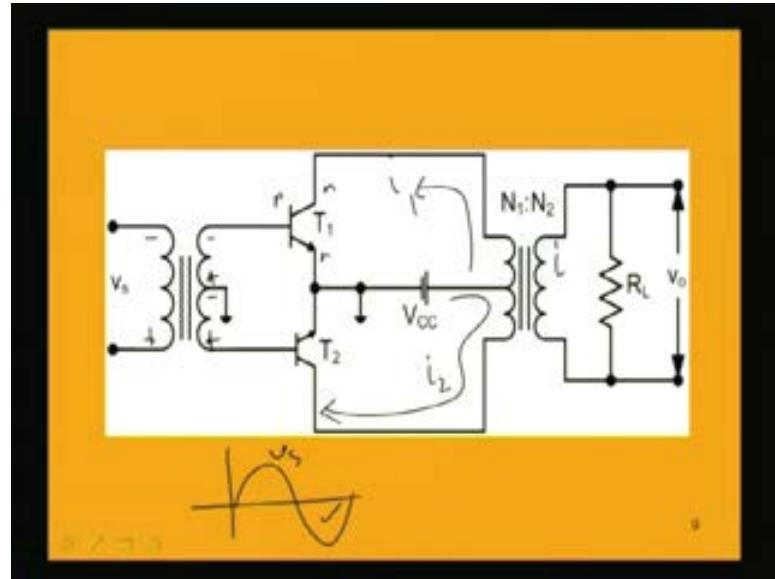
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Here also we will have induced voltage like this. That is this point, the center point is ground. With respect to ground, the upper point will be positive and with respect to ground the lower point will be negative. Equal voltages will be induced here in both the halves. This is the case of transistor T_1 ; it is forward biased. If we look into the transistor base, this is npn transistor. So, we have this forward biasing for the transistor T_1 in the emitter base junction. The transistor T_1 will now conduct and so, collector current will flow in the transistor T_1 in this direction. Let us consider this is i_1 . But what about the other transistor T_2 ? If we look into the other transistor T_2 , this is also an npn transistor,

but look at the biasing. This p is connected to negative. So, it will be reverse biased. There is no conduction taking place in the transistor T_2 . The transistor T_1 will only conduct and the current flowing in the winding will be i_1 and so there will be a current flow in the secondary of the transformer and this current as it flows, it will produce an output voltage V_o .

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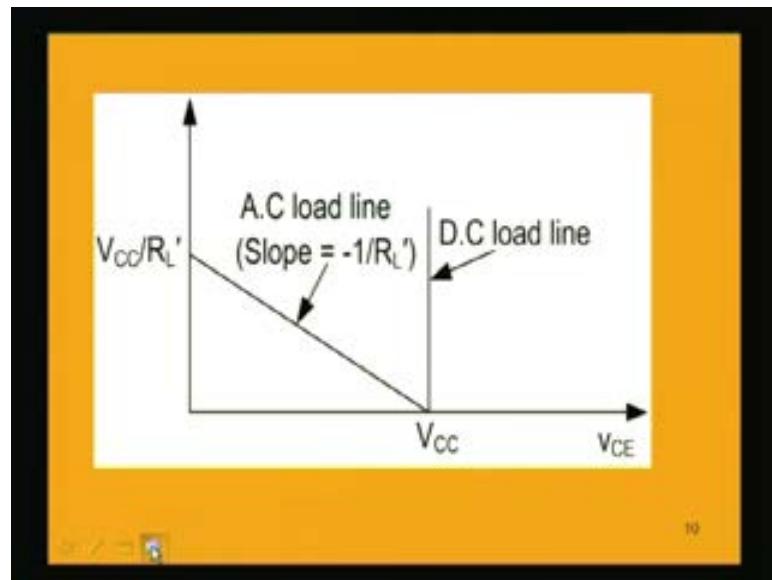


In the other half of the input cycle that is in the lower half if we consider, in the negative half cycle what will happen is that we get this point positive. The induced EMF will have these polarities so that now the transistor T_2 is forward biased in the emitter base junction. Because P is connected to positive, it will be forward biased and other transistor T_1 will be reverse biased. That is clear from this polarity of the induced EMF here in the secondary upper part. This is P at this npn transistor. P is connected to negative. So, it will be forward biased. There is no conduction in the transistor T_1 but conduction will take place in the transistor T_2 and so we will have a collector current in the transistor T_2 flowing in this direction.

So, through this transformer primary winding we see the direction of the current, i_1 and i_2 . This is i_1 and this is i_2 . Earlier i_1 was in this direction. So, one is in this direction, one is in

other direction. These two directions are opposite. The current which will flow by induction in the secondary, which is say i in the secondary of the transformer in the output stage, will be the difference between these two currents because these are opposite. It will depend upon the current directions of i_1 and i_2 . So, their difference will flow in the secondary of this transformer i . This type of push pull amplifier is named as push pull because in one half cycle the current is pushed up and in the other half cycle it is pushed down.

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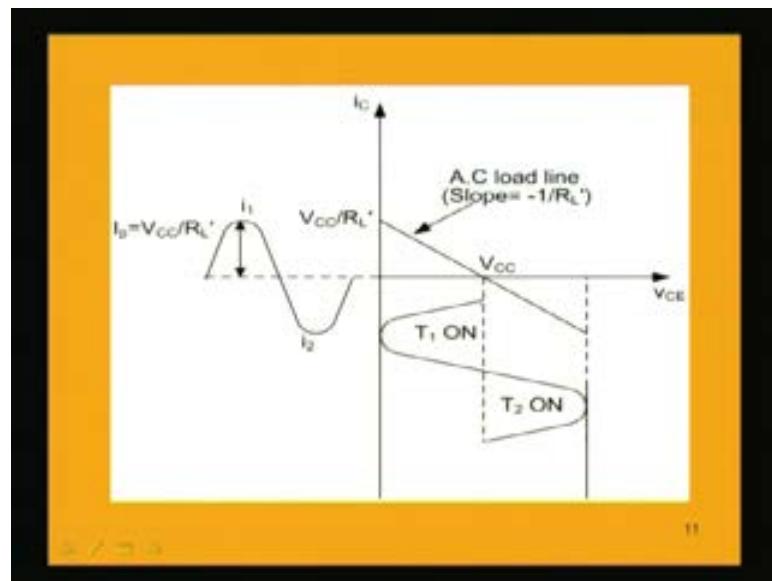


In the load line characteristics if we see, DC load line as we have earlier mentioned will be almost vertical and that is because the primary windings are assumed to be ideal having no parasitic resistance and that is why in the DC condition, the current will be infinitely high. That is why we are showing a DC load line by a vertical line and V_{CC} is the DC voltage because the source is V_{CC} source. In this type of push pull amplifier what we have seen is that one transistor is operating at a time. So, we are combining the operations of two transistors and finally we are finding out the output voltage by combining these two voltages which are induced individually by the two transistors in each half cycle. At a time only one transistor is conducting. The AC load line for one transistor if we consider, then the load line will be like this. The V_{CC} is the DC voltage.

When you do not have any signal when we do not have this V_s , suppose V_s is zero then, it will only have the V_{CC} voltage that is the DC voltage. That is why the DC voltage is here which is the voltage across collector to emitter when there is no signal.

When there is one transistor conducting say T_1 , then we will have increase of the collector current and the collector current will increase up to the maximum value V_{CC} by R_L dash. Suppose upper one transistor is conducting, so ignoring the transistor drop which is very negligible we can have only the V_{CC} voltage maximum up to which the collector current can go is V_{CC} by R_L dash. R_L transferred to this primary side will be R_L dash and will be n square into R_L ; n being the turns ratio between primary and secondary winding. If we now consider the AC load line we are having one point here and the other point, starting point is here. This AC load line will have a slope of minus 1 by R_L dash. This picture is only for one transistor, mind it.

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If we now combine both the transistors and try to draw the voltage and current swings, then for upper portion when the transistor current i_1 is increasing that means the upper transistor T_1 is conducting then current is rising. i_1 the sinusoidal current; peak value can be V_{CC} by R_L dash starting from zero. This is the AC current that we are considering and

in the other half when T_2 is conducting, the current is i_2 ; the other sinusoidal current in the other half when T_2 is ON. So, the load line will extend to this point; starting from this it will come down to here. That means we are having the T_2 ON; T_1 ON, the voltage will be reducing. This is the combination of the two transistors load lines and we now find out the DC current which is flowing.

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$I_{D.C} = I_1(D.C) + I_2(D.C) = \underline{2I_p/\pi}$

A.C Output Power

$$P_o(A.C) = I_{rms}^2 R_L$$

$$= \left(\frac{I_p}{\sqrt{2}} \right)^2 R_L = \frac{I_p^2 R_L}{2}$$

$$P_i(D.C) = V_{CC} I_{D.C} = 2V_{CC} \frac{I_p}{\pi}$$

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You have to be careful about this point because we are having a sinusoidal waveform and this is having two halves. One is this I_1 and the other is I_2 . That is why if we find out the total DC current that will be I_1 DC plus I_2 DC and we can find that out which is nothing but 2 by π into I peak. If the peak value of this current is say, I_p then the DC current that will flow, the DC value of this sinusoidal current will be 2 times I_p by π ; 2 by π into I_p , I_p being the peak value of the current. Now we find out the AC output power. We know that the AC power can be found out if we consider the average AC value. That is obtained by considering RMS, root mean square value. The output voltage is obtained across this load resistance R_L because we are interested in this voltage V_o and what is this voltage? It is a resistive load, so, it is current square multiplied by R_L . That current must be the RMS value of the AC current. Whenever we find out the power average value in AC, we take the RMS value. So I square R but that I should be the RMS value of the I .

That is why we are writing I_{rms} square into R_L dash. Here actually we are considering the R_L dash to be transferred to the primary winding. Everything we are considering in the primary side because we are going to compare the output and input; find out the efficiency.

With respect to this input circuit, we will do every thing. That is why we are transferring this R_L from secondary to the primary side. That is nothing but I_{rms} square; I root mean square value into R_L dash and root mean square value is nothing but peak value divided by root 2. That is why we are writing I_P by root 2 square into R_L dash and if we simplify that we get I_P square into R_L dash by 2. This is the AC output power. AC output power is obtained as given by this expression. It depends on the peak value of the current. If we consider the DC input that is the power you are giving as input to the amplifier, then V_{CC} into $I_{D.C}$ that is the power input and that is equal to V_{CC} into $I_{D.C}$; we have seen it is 2 times I_P by pi; so, 2 V_{CC} into I_P by pi that is the DC input.

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$$\begin{aligned}
 \text{Efficiency } \eta &= \frac{P_o(\text{A.C})}{P_i(\text{D.C})} \\
 &= \frac{I_p^2 R_L / 2}{2V_{CC} I_p / \pi} \\
 &= \frac{\pi I_p R_L}{4V_{CC}}
 \end{aligned}$$

If we find out the efficiency of this amplifier, finding out the ratio between the output and the input, output is the AC output, input is the DC input. What will be the ratio between these two? Just by substituting the values of this P_o A.C and P_i D.C, P_o A.C is this value I_P

square R_L dash by 2. So, we are replacing here I_P square R_L dash by 2 and P_i D.C we have as twice V_{CC} into I_P by π . That is why we are replacing here or substituting here 2 times $V_{CC} I_P$ by π . This calculation gives us π into, this π will go up; π into, one I_P will cancel out with one I_P and finally what will remain is π times I_P into R_L dash divided by 4; 2 will come down, 4 into V_{CC} . This is the efficiency of this push pull amplifier.

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$$\begin{aligned}
 \text{Efficiency } \eta(\max) &= \frac{P_o(\text{A.C})(\max)}{P_i(\text{D.C})} \\
 &= \frac{\pi I_p(\max) R_L'}{4V_{CC}} = \frac{\pi \left(V_{CC} / R_L' \right) R_L'}{4V_{CC}} \\
 &= \frac{\pi}{4} \\
 &= 78.54\%
 \end{aligned}$$

If we now consider the maximum efficiency, what will be the maximum efficiency that you can achieve with the push pull amplifier? We have to consider the maximum output power and find out the ratio between the maximum output power which is an AC power, the maximum value of the AC power that can be obtained with the DC input. If we look into this expression, the variable is I_P because for a particular push pull amplifier the value which is the load resistance that we are fixing; we are not going to change the load resistance and also we are having a constant DC source. So, the peak value of the current, actually this value can go upto maximum value is this one, which is V_{CC} by R_L dash. If I put this in this expression, the output power maximum which we obtained as $\pi I_P R_L$ dash, so $\pi I_P (\max) R_L$ dash by 4 V_{CC} if we put, just I am writing this again by taking I_P max which can be written down as V_{CC} by R_L dash. If we now design in such a way that this value I_P which is dependent upon these two, you get the efficiency changing.

The value of I_p if we now substitute, maximum value of the peak current that is given by V_{CC} by R_L dash. What we get is here V_{CC} and V_{CC} cancel, R_L dash and R_L dash also cancel. So, we get π by 4. π by 4 means, in percentage value we find 78.54% is the maximum efficiency that we can get for this type of push pull amplifier. We have seen earlier that we were able to get 50% maximum efficiency when we were considering a transformer couple power amplifier. Here in the class B operation an example of which is a push pull amplifier, we are getting an efficiency of 78.54% that is higher than the earlier cases.

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Power Dissipated as heat (P_D) by the transistor

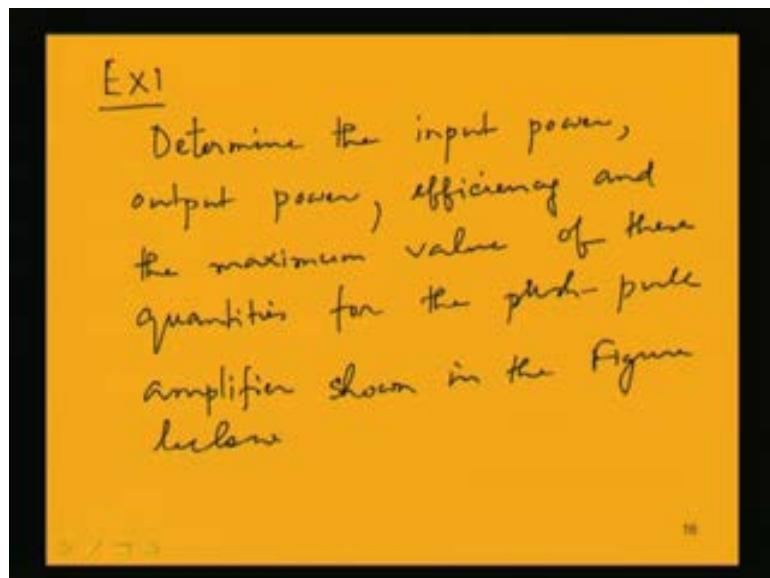
$$P_D = P_i(\text{D.C}) - P_o(\text{A.C})$$

$$P_D = 2V_{CC} \frac{I_p}{\pi} - \frac{I_p^2 R_L}{2}$$

If we want to find out the power dissipated by the transistor as heat, this power dissipation can be found out by subtracting the AC power output from the DC power input, P_i D.C minus P_o A.C. That will give the power dissipation by the transistors. That power which is dissipated as heat can be found out by just subtracting P_o A.C from P_i D.C. Putting down these values, P_i D.C is nothing but $2 V_{CC} I_p$ by π minus output AC power is I_p square into R_L dash by 2. If we substitute these values, we get the power dissipated as heat. In this type of push pull amplifier the key point is that we are having class B operation no doubt. That means for a particular transistor it is operating only in

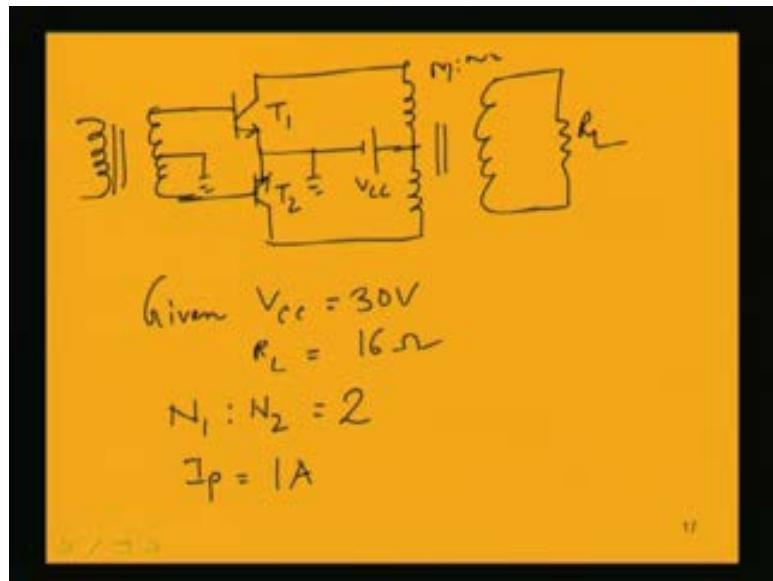
one half but we are combining these two transistors to get the overall output current and individually each of the transistor is operating in class B operation. Advantage here is that we can increase the efficiency. It is even higher than the earlier examples which we are taking, like a class A amplifier were only having 25% and 50% efficiency, but here it is more which is 78.54%. If we now compare these three amplifiers which we have discussed that is we have already discussed a class A and now we are discussing class B, then from the efficiency point of view we are having a higher value in push pull amplifier.

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Let us do one example to determine the input power, output power, efficiency and the maximum value of these quantities, for the push pull amplifier shown in the figure below. We have to find out the input and output power, efficiency and the maximum values of this input and output power for a push pull amplifier, which is shown here.

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It is a center tap transformer. Actually upper half and lower half are having same number of turns. It is having these transistors and we are having a source like this and at the output side we are having the load R_L . These are the transistors T_1 and T_2 . This is the source V_{CC} and this N_1 is to N_2 , transformer turns ratio. You are given that the voltage V_{CC} is equal to 30 volt, this R_L is equal to 16 ohm and the turns ratio between N_1 and N_2 , N_1 being the primary winding and N_2 being the secondary winding, is 2 and the peak value of the current is 1 ampere. This is the data given to you.

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Input Power

$$= P_i (\text{D.C.}) = \frac{2V_{CC} I_P}{\pi}$$

$$= \frac{2 \times 30 \times 1}{\pi}$$

$$= \frac{60}{\pi} = \frac{60}{3.1416}$$

$$= 19.1 \text{ W}$$

28

Now if we want to find out what is the input power, we know that input power, say P_i D.C is equal to 2 times V_{CC} into I_P by π . We substitute these values V_{CC} is equal to 30 volt; peak value of the current which flows in the circuit is given as 1 ampere. This denominator is only having π . So we get 60 by π , this much watts and if we calculate 60 by 3.1416 that value will be equal to 19.1 watts.

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$$P_i (\text{D.C.})_{\text{max}} = \frac{2V_{CC} (V_{CC}/R_L')}{\pi}$$

$$R_L' = n^2 R_L = R_L = 16 \Omega$$

$$N_1 : N_2 \Rightarrow \frac{N_1/2}{N_2} = \frac{N_1}{N_2} \cdot \frac{1}{2}$$

$$2 \cdot \frac{1}{2} = 1$$

$$P_i (\text{D.C.}) = \frac{2 \times 30^2}{\pi \times R_L'} = \frac{2 \times (30)^2}{\pi \times 16} = 35.8 \text{ W}$$

29

This is the DC input power. If we want to find out what is the DC input maximum then we will put down the I_P maximum value that it can have which is V_{CC} by R_L dash. R_L

dash is the resistance in the secondary; that is the load resistance transferred to the primary side which is given by n square into R_L . Here we are given N_1 is to N_2 . This N_1 and N_2 is the ratio between the total primary winding and secondary winding. We have to see this. This N_1 is total primary winding and this is secondary. N_1 is to N_2 for a particular transistor or for a particular conduction we will have to find out. So, that is N_1 by 2 by N_2 . That will be N_1 by 2 means N_1 is to N_2 we are given. But we will have to find out N_1 by 2 is to N_2 and if we want to find out, it will be N_1 is to N_2 into half and N_1 is to N_2 is given as 2; so, 2 into half that means 1. R_L dash and R_L are equal and what is the value of R_L ? It is 16 ohm.

Now the P_i D.C can be found out to be just by substituting this 2 into 30 square V_{CC} into V_{CC} will be V_{CC} square and divided by R_L dash into pi. So 2 into 30 square divided by pi into R_L dash is 16. If we calculate this value, it is 35.81 watts.

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The image shows handwritten calculations on a yellow background:

$$P_o(a.c) = \frac{I_p^2 R_L'}{2}$$

$$= \frac{1 \times 16}{2} = 8W$$

$$P_o(a.c)_{max} = \frac{I_p^{(max)}^2 \times R_L'}{2}$$

$$= \frac{(V_{CC}/R_L')^2 \times R_L'}{2} = \frac{V_{CC}^2}{2R_L'}$$

$$= \frac{(30)^2}{2 \times 16} = 28.125W$$

These are the DC input values and maximum value so what will be the AC output that also can be found out. Output power which is I_p square R_L dash by 2; I_p is 1, R_L dash is R_L which is 16 by 2. That means 8 watts and output power maximum can also be found out. The maximum value of this I_p can be found out which is nothing but V_{CC} by R_L dash

whole square into R_L dash by 2. It boils down to V_{CC} square by R_L dash and R_L dash - one will go; so, R_L dash into 2. Putting these values 30 square divided by 2 into R_L dash; R_L dash is 16. This gives the value of 28.125 watts.

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The image shows handwritten calculations on a yellow background. At the top, the formula for efficiency η is given as:

$$\eta = \frac{P_o(\text{A.C})}{P_i(\text{D.C})}$$

This is then simplified to:

$$= \frac{8}{19.1} = 41.89\%$$

Below this, the maximum efficiency $\eta_{(\text{max})}$ is calculated as:

$$\eta_{(\text{max})} = \frac{P_o(\text{A.C})_{\text{max}}}{P_i(\text{D.C})_{\text{max}}}$$

This is further simplified to:

$$= \frac{28.125}{35.81} = 78.54\%$$

The result 78.54% is circled.

This we have got. Now, we can find out the efficiency P_o A.C by P_i D.C. P_o A.C value is 8 watts and P_i D.C value is equal to, earlier we have found, 19.1. This value will be 8 by 19.1 and that is equal to 41.89% and maximum efficiency if we find P_o A.C maximum by P_i D.C maximum and these values are 28.125 and 35.81. So, that gives 78.54, which is the typical maximum efficiency value. It also has been verified that this value is the maximum value it can have.

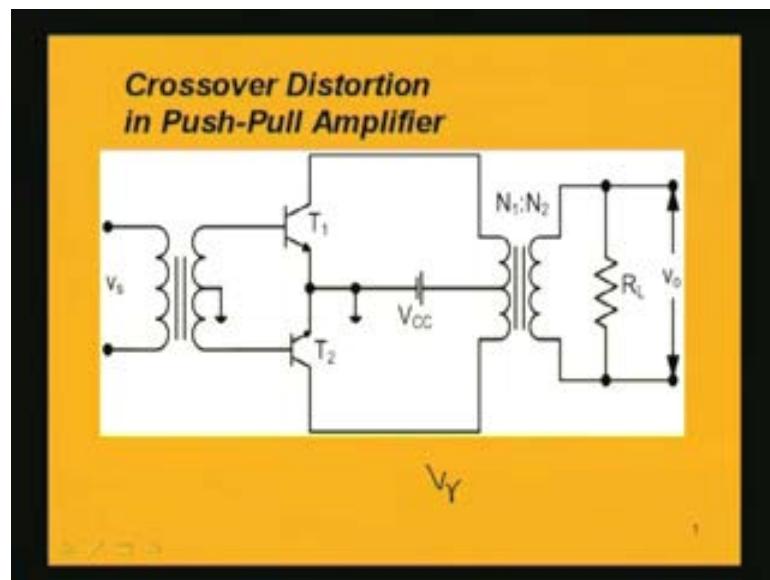
In this class today we discussed about two types of power amplifiers. One is the transformer couple power amplifiers which are generally used for audio applications which operates in class A mode of operation. But it is using a transformer to couple the load and second class of power amplifier that we discussed was a push pull amplifier which operates in class B operation and it is having a higher efficiency than class A power amplifier. It has class B operation in each of the transistor that is being operated because we are having two transistors and we are combining the operation of the two

transistors in push pull amplifier. Out of all these amplifiers which we discussed till now we have got that efficiency is highest for the last one that we discussed today which is the push pull amplifier and we will observe later other type of amplifier like class AB also we will study later.

Module -5
Power Circuits and System
Lecture - 3
Class AB Operations of Power Amplifier

In the last classes we discussed about some types of power amplifiers and these were class A and class B power amplifiers. Depending upon the conduction cycle, the class A or class B power amplifiers were named. We have seen that in class A power amplifier the conduction is for the full 360 degree and in class B amplifier the conduction angle was 180 degree. In the push pull amplifier that we discussed which is an example of class B type of power amplifier, there is one inherent disadvantage which is known as crossover distortion. This distortion is a result of the portion of the input cycle for which the transistors are not forward biased enough to let the base current flow.

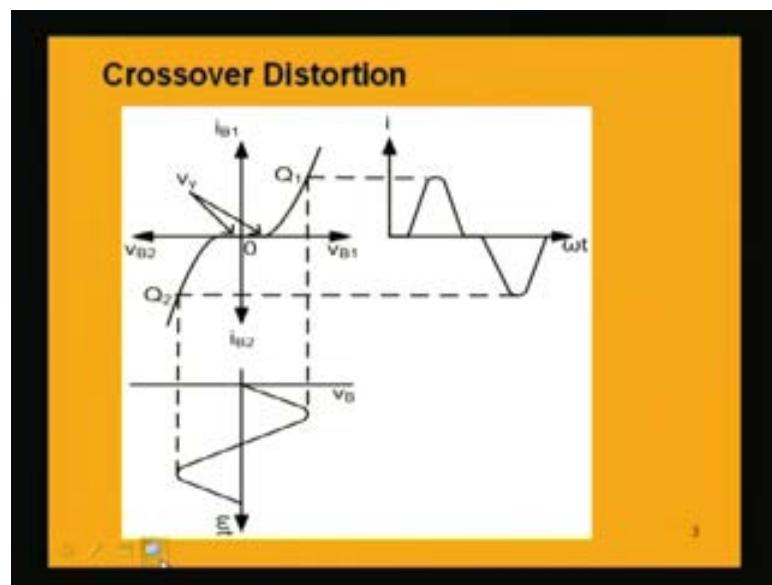
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The input signal which is applied to the primary of this transformer is V_s . In this input cycle for the portion when the input voltage is small and less than the threshold voltage for the transistors which is known as V_{gamma} and this value is 0.7 volt for silicon, we know. In order that the transistor should conduct, the input voltage which is given between emitter and base, we are taking a common emitter transistor here, so this voltage between emitter and base junction should be more than 0.7 for silicon. Otherwise what will happen is that for the portion when the input voltage is less than 0.7 volt the transistors will not conduct and so there will not be any collector current.

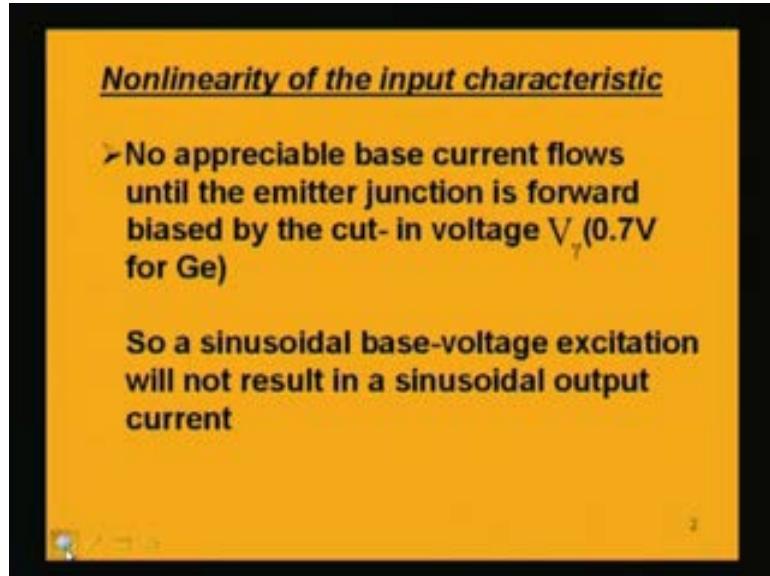
In the load side also there will not be current flowing for this portion and as we have seen that in each of the half cycle of the input voltage one of the transistors either T_1 or T_2 operates. In both the half cycles whether it is positive half cycle or negative half cycle of the input, the corresponding transistor will not conduct for that portion for which the input voltage is less than V threshold. That leads to distortion of the output current because for a portion of this input voltage being less than 0.7 volt we will not get any current in the output side. So that current will be zero.

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That is why we will be getting the output current, i like this. For this portion of the input voltage being less than 0.7 volt, we are not having any current and this is in the transistor T_1 . Similarly in the transistor T_2 , it will not be forward biased enough initially so the current will be zero.

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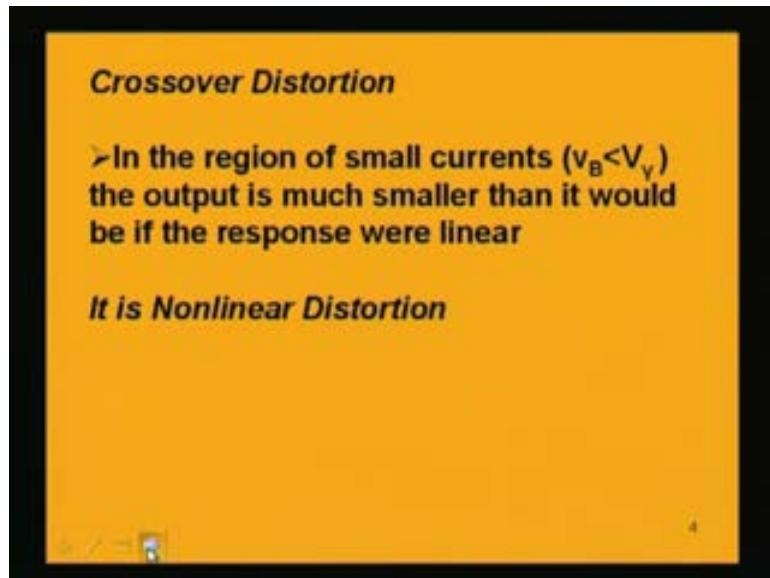
This distortion, which is occurring because of this inherent transistor property, is causing distortion in the output current and that is why we are getting nonlinear output. This nonlinearity causes the output voltage also a wave form which is not linear. So, we have to think about ways to overcome this crossover distortion which is occurring in the push pull amplifier that we discussed earlier.

If we revisit the input characteristic (Refer Slide Time: 6:24) between the base current and the base to emitter voltage of a transistor, here this plot is the input characteristics. For transistor T_1 , this is the input characteristic and for the other transistor T_2 it will be operating in the other half cycle or negative half cycle; so, up to this point it will be zero current and then it will increase. The portion where the base current is zero for the transistors is having the voltage less than V_{gamma} . So, V_{gamma} is 0.7 volt here for silicon. The input voltage V_{B1} is named to denote the voltage in the emitter base junction for the

transistor T_1 . We have the base currents zero and similarly for the other transistor T_2 , the portion up to this point this will have the current zero, base current i_{B2} zero because V_{B2} that is the voltage in the emitter base junction for the transistor T_2 is not large enough to overcome the threshold voltage. So, we are having this type of input characteristic in the two transistors T_1 and T_2 .

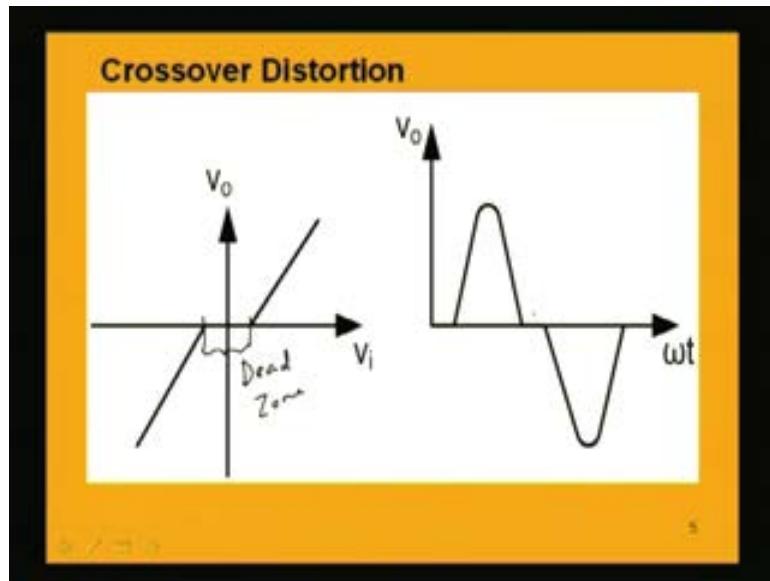
The Q_1 and Q_2 points are denoting the saturating or maximum value of the current. Corresponding to that Q_1 and Q_2 we are having the collector current maximum value and this is denoted by this point. i, current is having this peak value and for this portion you see that there is no current flow. It is zero current and for the other transistor, current that is also having a zero portion; so, that is causing an output voltage in the load which will be also having a very less or almost zero value for this portions and this is called the crossover distortion.

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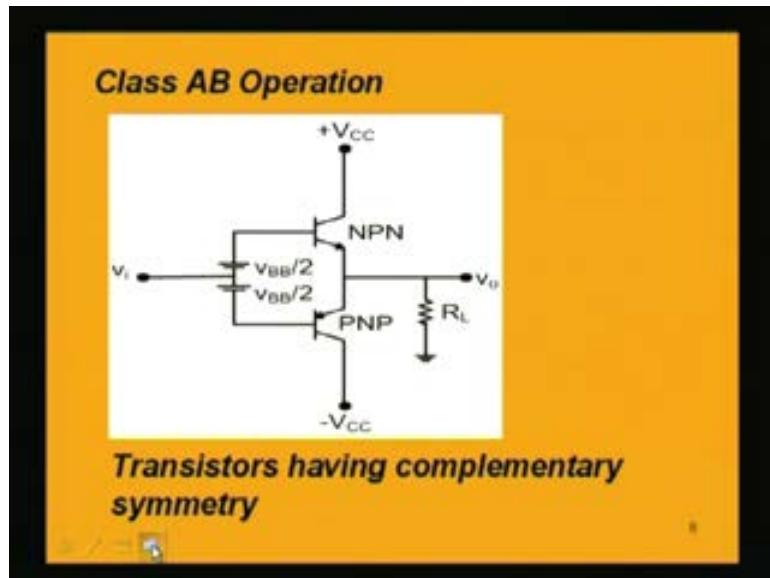
The output is smaller in this portion than it should have been if the response would have been linear. This nonlinear distortion has to be now overcome by some method and due to this crossover distortion what we are getting actually is a dead zone.

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If we consider the transfer characteristic between V_o and V_i , output voltage and input voltage given to the push pull amplifier, we see that there is a zero voltage from this portion to this portion; this point to this point within this portion the output voltage is zero. That is actually called a dead zone and then only it is rising linearly with respect to input voltage V_i . The dead zone which is occurring in the output voltage is causing nonlinearity in the output voltage and that is reflected here. We are not getting a linear characteristic of the output voltage we are having a nonlinear characteristic because of the dead zone introduced by this crossover distortion.

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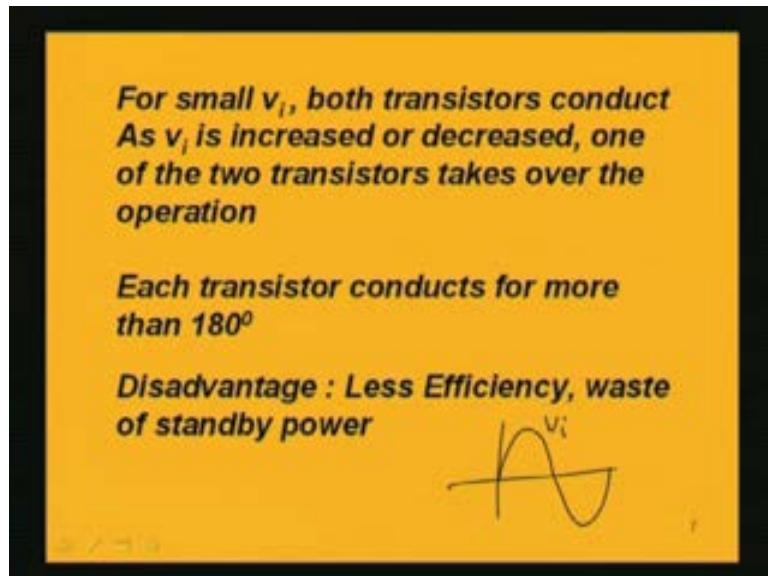
In order to overcome this crossover distortion we consider now a circuit having a class AB operation and class AB operation means the conduction angle is greater than 180 degree but less than 360 degree. An improvement or a modification of the earlier circuit of push pull amplifier is shown here. Here the transformer part is absent. What is used here is a complementary symmetry of the transistors; we are using NPN and PNP transistor, both are not of the same type. Earlier in push pull amplifier we were using the same type of transistor. (Refer Slide Time: 11:53) NPN transistors were only used, if we look back into the push pull amplifier circuit; T_1 and T_2 were both NPN types. But we can use complimentary symmetry transistor and get rid of the transformer part; so, that is being done. This is one example. Here we are using two transistors having complementary symmetry. That means one is NPN and PNP and also we are using a biasing for the emitter base.

If we look into this V_{BB} by 2 there are two sources which are connected to the two transistors and this is basically to offer biasing for overcoming the threshold voltage. Earlier we did not have any DC biasing. Only we were having in the push pull amplifier the signal. The portion of the signal for which the emitter base junction has a voltage greater than threshold voltage, conducts and that was introducing the crossover distortion.

That is why here a DC source having value of V_{BB} by 2 for each of this transistor is used for overcoming the crossover distortion and apart from that this is the input signal V_i which is there and which will have the positive and negative half cycle.

Now what happens is because of the presence of this DC source, both the transistors are already biased for overcoming the V_{gamma} or the threshold voltage. If we consider this emitter base junction it is having a voltage V_{BB} by 2 which is greater than the threshold voltage. The transistor is already conducting. There is a base current even when the input signal is zero. So, there is a current which is already flowing even when the input voltage is zero. Practically what will happen is the current will flow for an angle greater than 180 degree because even if the input voltage is smaller than the threshold voltage V_{gamma} , then also both the transistors will operate or conduct.

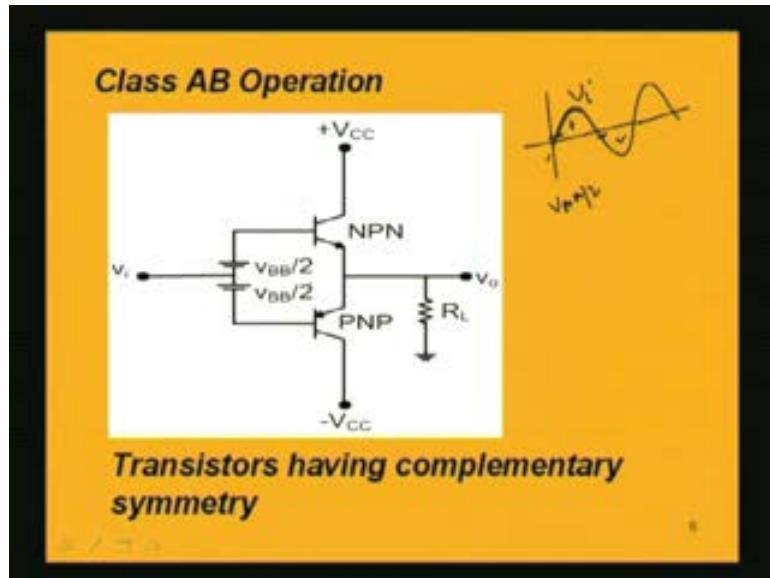
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Now as V_i is an AC signal like this, it is increasing. V_i is increasing and as V_i is increased, the NPN transistor here will take over and it will conduct but for the portion when the input voltage, even when it is smaller than V_{gamma} still the transistor was conducting and now when V_i is increased or decreased one of the transistors will take

over conduction. So only one will conduct because you can see that V_i is a sinusoidal signal for example we are taking.

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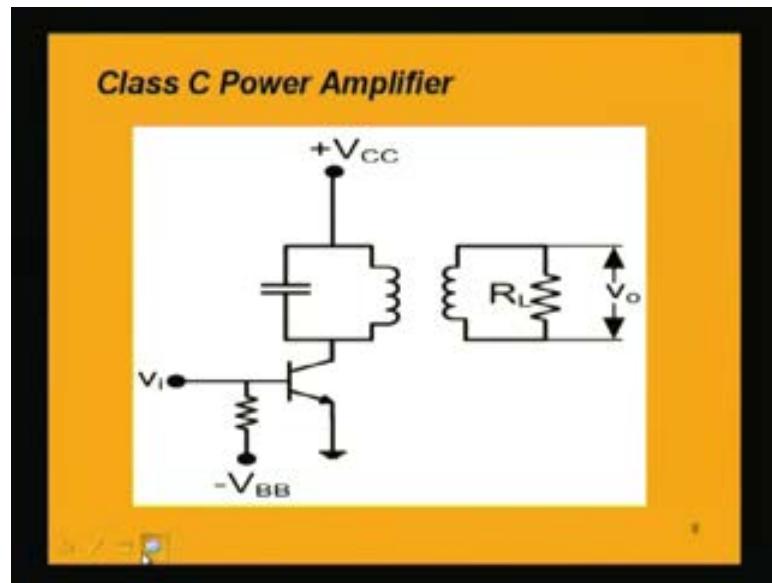


If you consider the positive half cycle, this V_{BB} by 2 is a small voltage. So, V_i will increase and then it will be greater with respect to V_{BB} by 2 considerably. This transistor NPN will conduct now because it is forward biased and then this PNP will be off because our signal is like this that the PNP transistor will be reverse biased for that portion. But in the negative half, as V_i is going on increasing in the negative half then the transistor which will be taking over for conduction will be the other one that is the PNP transistor. This transistor, lower one transistor will conduct when V_i goes on decreasing and decreasing and that means it is in the negative half because you can see that then it will be in the forward bias. But for the portion when V_i was, say, very small nearing zero even then the transistors were carrying or having a current because of this source V_{BB} by 2.

Effectively if we consider a single transistor at a time then we see that it is having a conduction angle greater than 180 degree. Because for the portion of the signal, before it was zero, that means for this portion suppose also it was having conduction the upper one was having conduction as well as the lower one. Even if it is going down, then we can see

that the lower one will take over. This one will take over but already it was having a current conducting due to the source V_{BB} by 2. Here we observe that the conduction angle of each of the transistor is more than 180 degree but it is less than 360 degree. There is a disadvantage as far as efficiency is concerned because we can see that there is a stand by current. So there will be power wastage. Efficiency will be less since we have a stand by current flowing even when the V_i signal was zero. There is already wastage of power due to that current; so that leads to lesser efficiency because of this waste of the standby power. Another type of power amplifier is there, which is class C power amplifier.

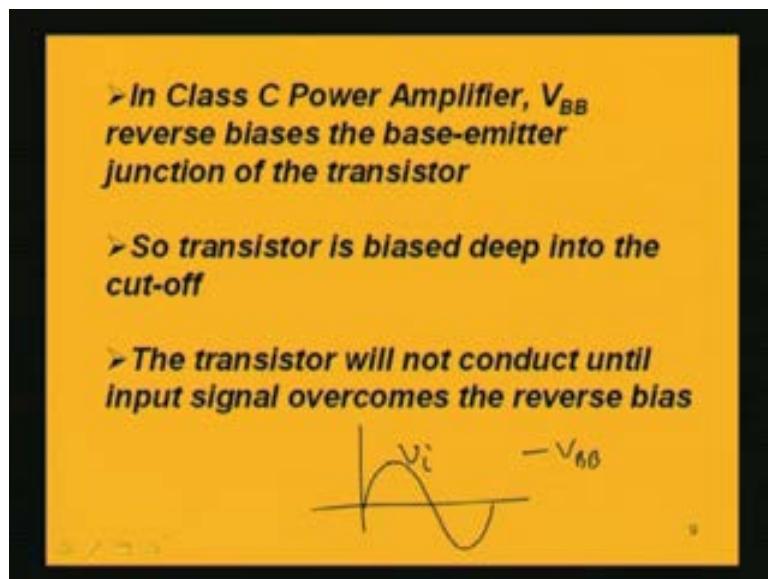
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Class C power amplifiers we have earlier already mentioned that it is having conduction angle less than 180 degree. A typical circuit for this class C power amplifier is shown here. Here one point to be noted is that it is already reverse biased, deep into cut off. If we look into the transistor, this is an NPN transistor we are taking in this circuit and there is a voltage V_{BB} negatively or reverse biasing the emitter base junction. It is already reverse biased high enough to cause the transistor deep into cut off; already having gone into the cut off region much deeper, we will have to overcome this V_{BB} reverse biasing voltage to make the transistor conduct. Whenever the input voltage, which is the signal being applied to this amplifier, will be large enough or it will be able to overcome the

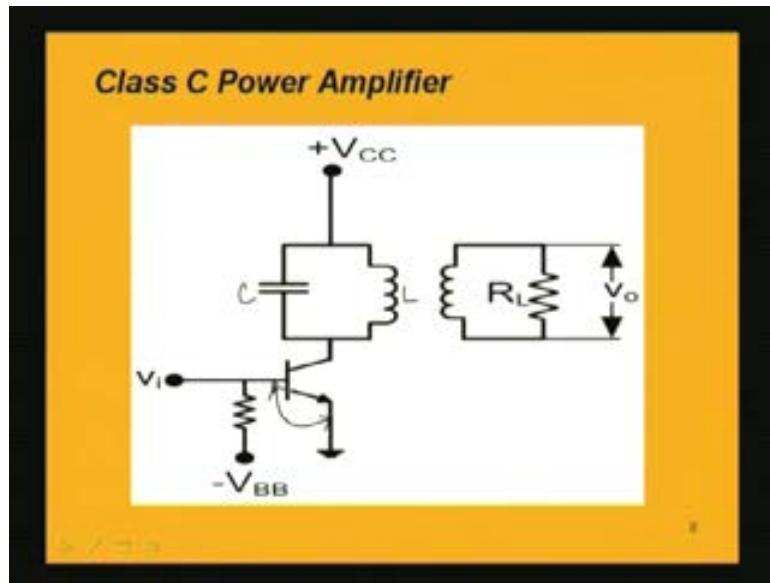
reverse biasing voltage V_{BB} , then only the transistor will start conducting and there is a tank circuit. This tank circuit which is used by this inductor L and capacitor C that is forming the tank circuit and we are having the load resistance at the output or the secondary side of this transformer; this inductively coupled portion is having this R_L . This R_L is the load resistance when we are having the voltage across this R_L .

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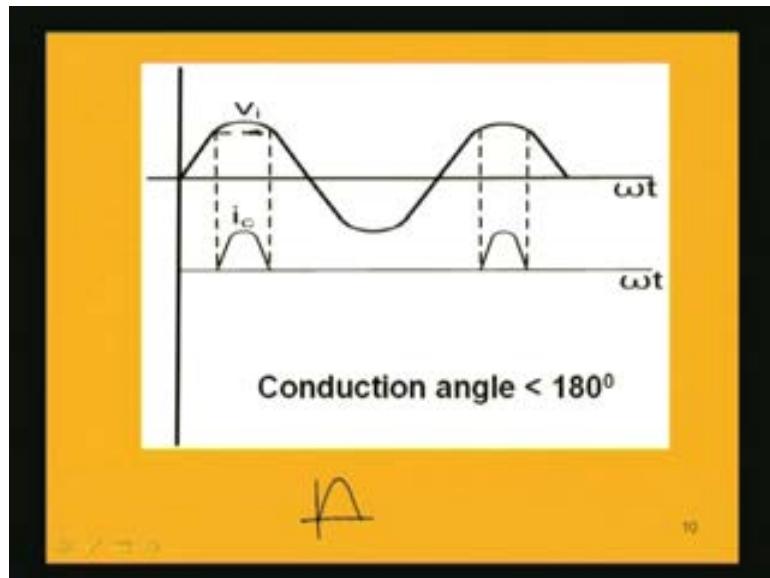
If we look into the operation of this circuit, as the transistor is already being biased deeply into the cut off, the transistor will not conduct until the input signal over comes this reverse biasing voltage. This input signal, which is a sinusoidal signal for example we are taking, is V_i ; it is increasing. Already we have a negative biasing voltage present which is reverse biasing the transistor.

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So that voltage across this emitter base junction of the transistor, this voltage must be forward biasing the emitter base junction. Only then the transistor will start conducting. So, V_i minus V_{BB} this quantity must have a value greater than the cut off voltage. It should overcome that V_{BB} .

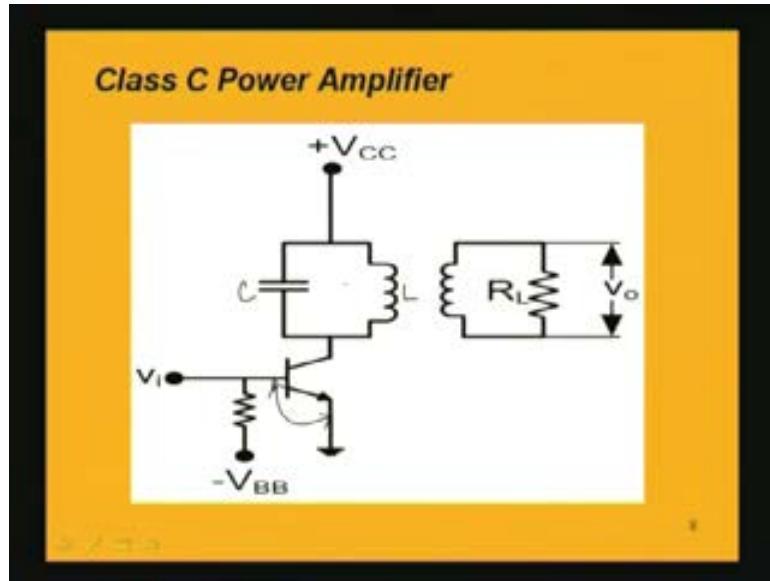
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Then it will start conducting, because of which the current which will be conducting is only for a very small portion in the positive half cycle of the signal. It is obvious that only when the emitter base junction for the transistor will have a forward biasing voltage then only it will start conducting and V_{BB} is a high voltage. It is not a small value. It will have to wait till the point when V_i is greater than V_{BB} . For example we are having here a signal shown by this V_i and practically what happens is that only for a very small portion of the input voltage cycle the transistor will conduct and it is generally even less than 90 degree. That is because only for this portion, from this point to this point, the input voltage is greater than V_{BB} . V_{BB} is sufficiently high that is why the current which flows in the transistor it is only for a very small portion of the input cycle even less than 90 degree.

The current which flows in the transistor will be like a pulse. It will be like a pulse, as shown here. It will increase and then decrease very safely. It is a very steep pulse. We will get the current in the transistor in the form of the pulse. We have to now have a method to convert that pulse into sinusoidal signal because that is the requirement. In the output side we require a sinusoidal voltage because we are amplifying a sinusoidal signal. Whatever we are giving here, we must get at the output same shape and as we are feeding an input voltage which is sinusoidal, the output voltage also must be sinusoidal but what we are getting here is a pulse like voltage. In order to convert this pulse into a sinusoidal voltage here what is done is this provision of this tank circuit.

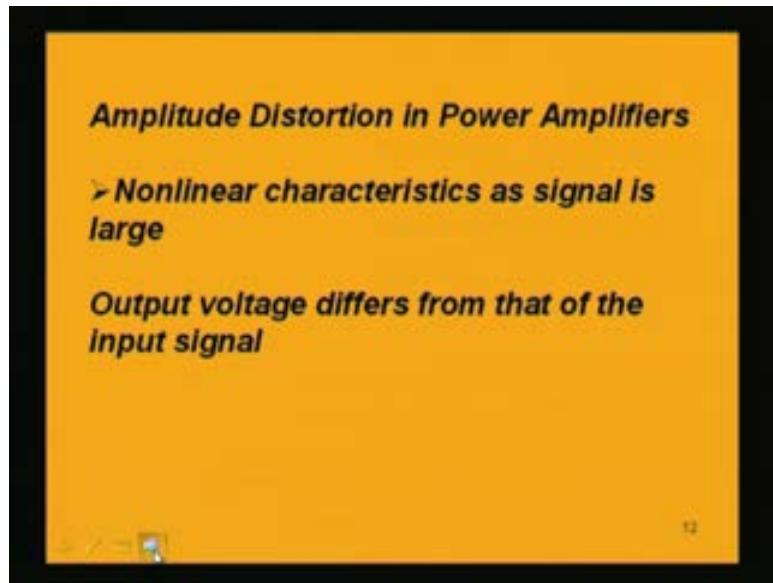
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As this tank circuit is having L and C components, it will be oscillating and that oscillation will be a high frequency oscillation. We will get a sinusoidal voltage; because of the charging and the discharging of this capacitor through this inductor and storing energy in the inductor, we will get a sinusoidal voltage no doubt but that frequency will be high. It is generally used for radio frequency operations, RF operations because frequency is quite high.

This tank circuit is there to produce sinusoidal signal from this pulse. Because the current in the transistor is in the form of pulse, the tank circuit's presence will convert this pulse type of signal into sinusoidal by charging and discharging of the capacitor as well as storing the energy in the inductor. That is the property of this tank circuit formed by this L and C. This circuit will convert the pulse to a sinusoidal signal. But it is having a radio frequency operation. Here one thing we note is that the conduction angle for the current will be less than 180 degree and almost practically the conduction angle will be around 90 degree only. This is a typical example of a class C amplifier.

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When we are considering the power amplifier, we have to always remember the fact that these signals which are being dealt with they are having high magnitude. Whether it is current or voltage it is a large magnitude; in the order of voltage or amperes we are dealing with and due to this fact the operation of the transistors in this power amplifier go into the nonlinear portion. If we remember, earlier we were discussing about the small signal amplifiers using BJT's. There we were always assuming that the transistor operation is linear and for that we have to be careful to apply the signal which is small such that the transistor is always in the linear operation.

If the input signal is high then that will drive the transistor into nonlinear portions in the characteristic curve either the saturation or cut off but here that guaranty is missing because we are dealing with signal which is large enough and that is why the transistor is driven often into the nonlinear portion like saturation. The effect is that we will have nonlinear characteristics of the signal and the output voltage which we will obtain will be often different from the input signal because of this nonlinearity being introduced by the large amplitude of the signal. There is an amplitude distortion and that causes the distortion in the output signal. We have to have a measure of how much distortion in the output signal is occurring from the input one. That distortion we are going to now discuss.

We are discussing the amplitude distortion in the output signal. To investigate into the magnitude of the amplitude distortion we have to assume the dynamic characteristics of the power amplifier transistor not as a linear one because earlier when we discussed small signal amplifiers using BJT's we were taking the output characteristics in linear way. i_c was beta times of i_b and we were only limiting the study to the linear region; that is for a small portion around the operating point only we were considering. If we consider the relation between the output and input current in a common emitter transistor then i_c is beta times of i_b . But now i_c cannot be simply taken as beta times of i_b or beta means a constant value; it is not a linear relationship. We have to now go beyond that linear study and that is why generally we can represent the current in the transistor as having a relationship of a parabola.

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To investigate the magnitude of amplitude distortion, the dynamic characteristics are Represented by a parabola

$$i_c = G_1 i_b + G_2 i_b^2$$

Let $i_b = I_{bm} \cos \omega t$

$$\begin{aligned} i_c &= G_1 I_{bm} \cos \omega t + G_2 I_{bm}^2 \cos^2 \omega t \\ &= G_1 I_{bm} \cos \omega t + G_2 I_{bm}^2 \left(\frac{1}{2} + \frac{1}{2} \cos 2\omega t \right) \\ &= B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t \end{aligned}$$

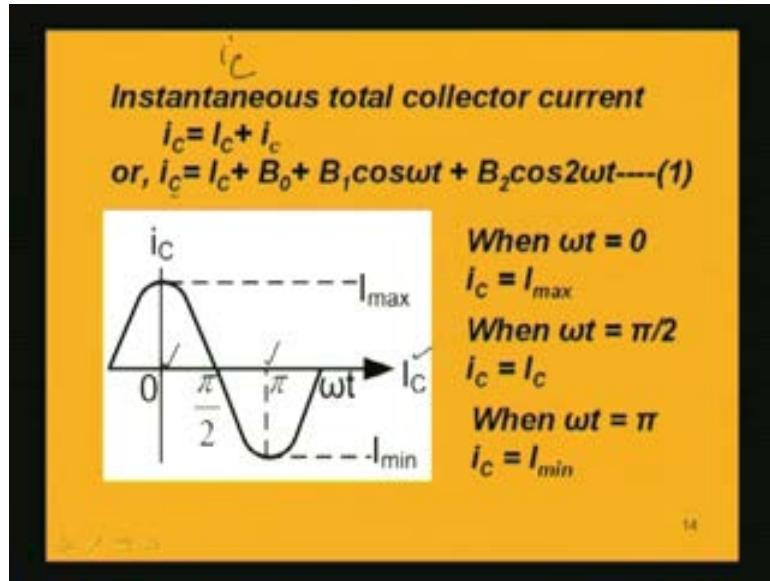
The dynamic characteristics of the transistors are represented by a parabola. We are having an expression of i_c equal to G_1 into i_b plus G_2 into i_b square. This is the equation of parabola. We are basically having the characteristics curve represented by a parabola. Let us take that assumption of taking up to only the second order and we will analyze the

relationship of the collector current and the base current by this parabolic relationship G_1 into i_b plus G_2 into i_b square where i_b is the base current, i_c is the collector current.

Let us assume that we are applying a sinusoidal signal and we can then represent i_b as $I_{bm} \cos \omega t$. This a sinusoidal signal having the peak value of I_{bm} . If we now replace i_b in this equation by this expression of $I_{bm} \cos \omega t$ what you will get is i_c equal to G_1 into $I_{bm} \cos \omega t$ plus G_2 into square of i_b means I_{bm} square $\cos^2 \omega t$. Further simplifying we get that is equal to G_1 into $I_{bm} \cos \omega t$ plus $G_2 I_{bm}$ square. The $\cos^2 \omega t$ can be broken up into having another representation because we know that $\cos^2 \omega t$ equal to $\frac{1}{2} + \frac{1}{2} \cos 2\omega t$. So, from this relationship we can find out what is $\cos^2 \omega t$? It is half of 1 plus $\cos 2\omega t$. Representing in that way just substituting for $\cos^2 \omega t$ by this expression of half of $\cos 2\omega t$ plus 1 term, then we are getting this.

Now if we look into this expression we are having actually the terms which are constant part having a $\cos \omega t$ part and the other is having a $\cos 2\omega t$. Representing that constant $G_2 I_{bm}$ square by 2 by B_o , B_o is a constant to represent this part G_2 into I_{bm} square into half plus G_1 into I_{bm} another constant we are representing by B_1 , so, we get $B_1 \cos \omega t$ plus a third term having $G_2 I_{bm}$ square by 2 representing it by B_2 and there is $\cos 2\omega t$ term. So, what you get in the current expression is the terms: one is constant B_o ; other is having a signal having the frequency of the input signal ω . We are applying the input signal which is $I_{bm} \cos \omega t$ that is the base current signal. This frequency is seen but another part or third term is having twice of that frequency. That means we are getting twice ω in the frequency.

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This is actually leading to an analysis which will deal with second harmonics; fundamental frequency and second harmonic. We are going to discuss that. But before that let us complete to find out the instantaneous total collector current because the current which we are discussing right now is the AC component. If we consider the instantaneous total collector current there is a DC part, there is an AC part. The DC part is capital I capital C and the AC part is small i small c. This total instantaneous current will be combination of this I_C and small i_c .

Now we are representing the instantaneous total current by i capital C that means we are writing i small and the subscript capital C and that is equal to capital I capital C that is the DC part plus the signal AC part which is small i small c. We have just now derived what is small i small c. That is equal to B_0 plus $B_1 \cos \omega t$ plus $B_2 \cos 2\omega t$. Now we write all this, the whole expression and we get the value of i_c equal to capital I_C plus B_0 plus $B_1 \cos \omega t$ plus $B_2 \cos 2\omega t$. This is the instantaneous total current expression and I am naming it as equation 1.

Now we look into the current i_C curve. This is the current. It has a peak value, maximum value and minimum value and these are denoted as I_{max} and I_{min} and it is symmetrical swing and we are having the DC collector current in between them which is denoted by

capital I capital C. Starting from this DC current it will go on increasing and getting the maximum value I_{max} then decreasing it will be having the minimum value I_{min} . Let us consider omega t between this point, take it as zero, and when omega t is equal to pi. Let us consider this portion of omega t; because x axis is having omega t and we are considering these points starting from zero here when it is having the magnitude I_{max} and then when it traverses an angle of pi.

What will be the value of the instantaneous total current small i capital C, as we are denoting by, when omega t is zero at this point. When omega t is zero that value is I_{max} . Because we are starting from this point, this we are assuming as zero. Because this is the whole sinusoidal wave it will be continuing; we can start with any point and we can take a portion of that signal. That is what we are doing. Where we are starting? At this point we are starting when the value of the instantaneous total current is I_{max} . Then we consider when it traverses an angular distance of pi by 2. When omega t is equal to pi by 2, the instantaneous total current is capital I capital C. This is the value which is the DC current.

When it is traversing an angle of pi, the omega t value becomes pi then, the instantaneous total current is I_{min} because here we can see this is getting the negative peak. Now these three points which we are observing in the collector current curve, we will be using to find out the constants in this equation number 1. Because we have three unknowns B_0 , B_1 and B_2 , so we require three equations to know these three unknowns. For that we will use these conditions to find out constants. This is the normal way we generally solve this equations.

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Substituting these values in Eq.(1), we get

$$I_{max} = I_C + B_0 + B_1 + B_2 \quad \dots \dots \dots (2)$$

$$I_C = I_C + B_0 - B_2 \quad \dots \dots \dots (3)$$

$$I_{min} = I_C + B_0 - B_1 + B_2 \quad \dots \dots \dots (4)$$

$$B_0, B_1, B_2$$

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If we look into this equation 1, when we put the omega t value zero what will happen is that I capital C becomes I_{max} , left side will be I_{max} ; right side will be capital I capital C plus B_0 and omega t zero means plus B_1 plus B_0 will be there, cos of omega t when omega t is equal to zero, cos zero is 1, so cos twice omega t is also 1. That will give us this equation number 2 which is I_{max} equal to I_C plus B_0 plus B_1 plus B_2 . Secondly we will apply when omega t is equal to pi by 2.

From this signal we have seen that when omega t is equal to pi by 2, the instantaneous total current is equal to the DC value capital I capital C. So, put the value omega t is equal to pi by 2. What we will get in this equation is, left side will be capital I capital C; right side will be capital I capital C plus B_0 plus B_1 into cos of pi by 2. What will be cos of pi by 2? That will be zero and then B_2 cos twice omega t. Put the value of omega t is equal to pi by 2; cos of 2 into pi by 2 means cos of pi and cos of pi is minus 1. So, it will be minus B_2 . That is what is obtained in equation 3. We get capital I capital C equal to capital I capital C plus B_0 minus B_2 . B_1 becomes zero because cos of pi by 2 is zero. Then in the next equation, equation number 4 is obtained by putting the value of omega t is equal to pi.

So, put the value of omega t is equal to pi in this equation 1. What we will get is the value of instantaneous total current, I_{min} ; this point. Left side will be I_{min} and that is equal to

right side equal to capital I capital C plus B_0 plus when you put the value of omega t is equal to pi, cos of pi is equal to minus 1; so, minus B_1 and then the next term $B_2 \cos 2 \omega t$. Omega t is 2π ; cos of 2π , cos of 2π equal to 1, so it will be plus B_2 . We have these three equations – 2, 3, 4 and we have to solve for finding out B_0 , B_1 and B_2 . These three equations are enough to know the three unknowns. The easiest one will be, if we look into the equation number 3, from this equation we see that B_0 equal to B_2 will be obtained. I_C , I_C cancels so B_0 will be equal to B_2 . These two values are equal.

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From Eq.(3), $B_0 = B_2$

Eq.(2)-Eq.(4) gives, $B_1 = (I_{max} - I_{min})/2$

Substituting these values in Eq.(2), we get,

$$B_2 = (I_{max} + I_{min} - 2I_C)/4$$

$$i_C = I_C + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t$$

- Second Harmonic Distortion

To find out the values of B_1 etc., we will subtract equation 4 from equation 2.

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Substituting these values in Eq.(1), we get

$$I_{max} = I_C + B_0 + B_1 + B_2 \quad \dots \quad (2)$$

$$I_C = I_C + B_0 - B_2 \quad \dots \quad (3)$$

$$I_{min} = I_C + B_0 - B_1 + B_2 \quad \dots \quad (4)$$

B_0, B_1, B_2

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$I_{max} = I_C + B_2$
 $+ I_{max} - I_{min}$
 $\frac{2}{2} \neq B_2$

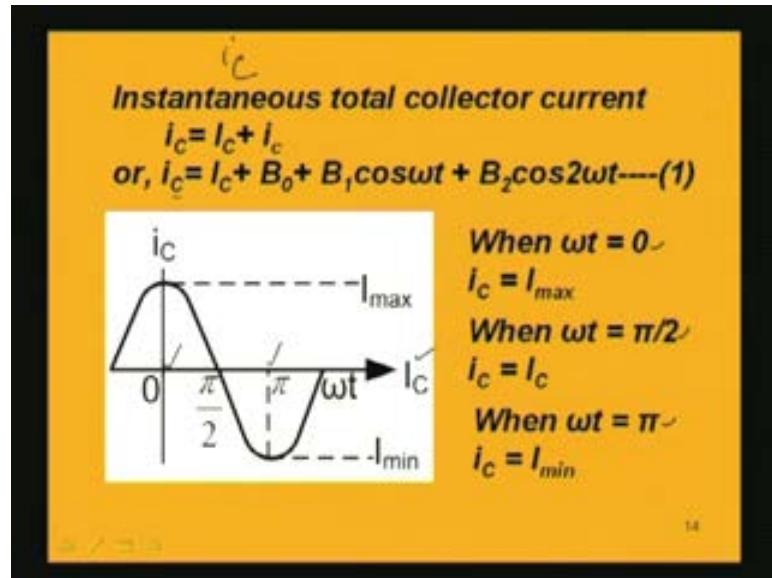
$I_{max} - I_{min} = 2B_1$
 $B_1 = \frac{I_{max} - I_{min}}{2}$

We subtract equation 4 from equation 2; equation 2 minus equation 4 that leads to what? I_{max} minus I_{min} , this left side we are subtracting equal to this equation and this equation. So, right side this two cancel; B_0 B_0 cancel we are subtracting 4 from 2. So, $2B_1$ plus $2B_2$ and that is giving you again what we have got is B_1 plus B_1 ; sorry B_2 minus B_2 cancel. That is not right; 2 minus 4 I am doing, B_1 plus B_1 it will be $2B_1$; B_2 B_2 cancel. What we are getting is B_1 that is equal to I_{max} minus I_{min} by 2. This is what we are getting for B_1 .

Now, you have to find out what is the value of B_2 ? That is equal to B_0 also. To find that you substitute these values B_0 equal to B_2 and B_1 equal to I_{max} minus I_{min} by 2 in equation 2. In Equation 2, if we substitute these values; so, what we get is that I_{max} equal to I_C plus B_0 equal to B_2 from third equation we have already got; we can simply write B_2 in place of B_0 plus B_1 we have found out. B_1 is equal to I_{max} minus I_{min} by 2. Then the rest of the terms is plus B_2 . So, this equation is the governing equation from where we will get the value of B_2 because it becomes twice B_2 plus this portion which is equal to I_{max} . Doing simplification finally we get B_2 equal to I_{max} plus I_{min} minus 2 times I_C by 4. This is obtained and now all these constants B_0 , B_1 and B_2 have been found out in terms of the maximum current, minimum current and DC current.

Putting these values of B_0 , B_1 and B_2 into the original equation number 1, what we get finally?

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In this equation we substitute these values. The total instantaneous current i capital C equal to capital I capital C plus we will be writing for say B_0 plus $B_1 \cos \omega t$ plus $B_2 \cos 2\omega t$.

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From Eq.(3), $B_0 = B_2$

Eq.(2)-Eq.(4) gives, $B_1 = (I_{max} - I_{min})/2$

Substituting these values in Eq.(2), we get,

$$B_2 = (I_{max} + I_{min} - 2I_C)/4$$

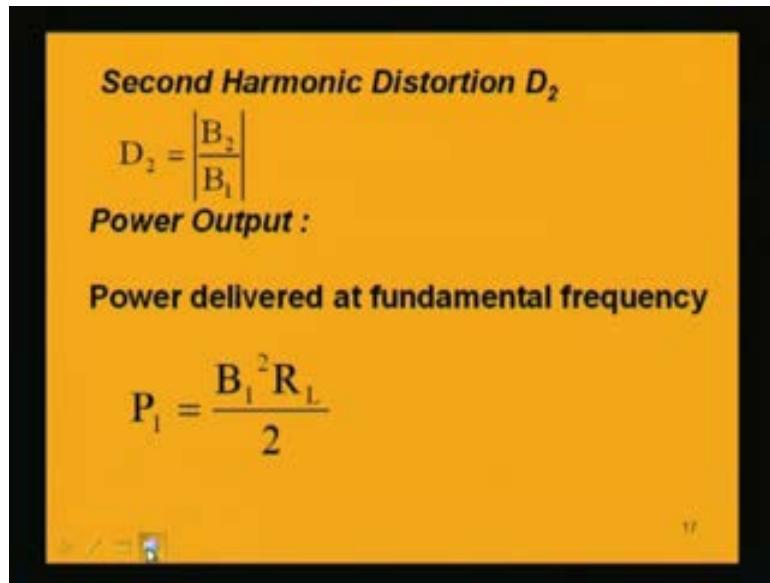
$$i_C = I_C + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t$$

- Second Harmonic Distortion

Here we can substitute all this B_0 , B_1 and B_2 values. If we observe closely the equation, this is having a fundamental frequency. This is called the frequency of the input signal is omega and this term is having the same frequency omega. This is a term having the fundamental frequency and the other term $B_2 \cos 2\omega t$ is having second harmonic component. This is a second harmonic component; this is 2 times. What is the final expression? Basically it is giving an expression which is giving you an idea about the second harmonic distortion that is occurring in the output. This second harmonic distortion we are getting because of the nonlinearity in the characteristics; the dynamic characteristic nonlinearity is giving the amplitude distortion and we are getting a second harmonic term because of that in the output.

There is a measure actually to have an idea about how much distortion is taking place. How much second harmonic distortion is taking place that distortion measure is given by term D_2 .

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This is called second harmonic distortion D_2 and it is given by the value modulus of B_2 by B_1 . The two terms B_2 and B_1 , if we take ratio between them and take the modulus value that will give the second harmonic distortion. It is basically giving you the idea about how much or second harmonic distortion is taking place. If we consider the power output, the power at the output which is delivered at the fundamental frequency is B_1 square R_L by 2 because at the fundamental frequency the term which is associated is B_1 ; $B_1 \cos \omega t$ is the term, which is relating to the fundamental frequency.

We want to find out the AC output power. We know that AC output power will be the value of peak square by 2. If we are considering the current, this is the current. I square R_L and I square means it will be peak value by root 2 square. RMS average value we will have to consider when we are considering AC. The load resistance is R_L and we have this current component at the fundamental frequency $B_1 \cos \omega t$.

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Second Harmonic Distortion D_2

$$D_2 = \left| \frac{B_2}{B_1} \right|$$

Power Output :

Power delivered at fundamental frequency

$$P_1 = \frac{B_1^2 R_L}{2}$$

So, it will be B_1 square by 2 into R_L . That will be the power delivered at the fundamental frequency and that is denoted by P_1 .

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**Total Power Output
(considering second harmonic distortion)**

$$\begin{aligned} P &= \left(B_1^2 + B_2^2 \right) \frac{R_L}{2} \\ &= \left(1 + \left(\frac{B_2}{B_1} \right)^2 \right) \frac{B_1^2 R_L}{2} \\ &= \left(1 + D_2^2 \right) P_1 \end{aligned}$$

$B_1 \cos \omega t + B_2 \cos 2\omega t$

As this is a current having second harmonic distortion term also if we want to find out the total power even considering that second harmonic distortion, the total power output at the load will be summation of the power delivered by the fundamental frequency as well

as the second harmonic term. Considering the second harmonic distortion, the total power output will be P; for example we are denoting it by P. It is equal to $B_1^2 R_L$ by 2 plus $B_2^2 R_L$ by 2. Since $B_1 \cos \omega t$ and $B_2 \cos 2\omega t$ are the terms, if we consider those two terms having fundamental frequency and second harmonic term, it is $B_1 \cos \omega t$ plus $B_2 \cos 2\omega t$. These are the terms.

If we want to find out the output power because of these two terms it will be $B_1^2 R_L$ by 2 plus $B_2^2 R_L$ by 2 and that here we are rewriting and we can write in another way taking common $B_1^2 R_L$ by 2. That is the power at the fundamental frequency then inside the bracket it will be 1 plus B_2^2 / B_1^2 because we are dividing by B_1^2 ; B_1^2 has been taken out. B_2^2 / B_1^2 that we are writing by $B_2^2 / (B_1^2)$. What is this term B_2^2 / B_1^2 ? We have just now denoted it by D_2 that is a second harmonic distortion and that is used to represent this term B_2^2 / B_1^2 . B_2^2 / B_1^2 we are writing by D_2 . So, the total power P becomes equal to 1 plus D_2^2 and this whole term we are writing by P_1 that is the power delivered at fundamental frequency. The total power P equal to 1 plus D_2^2 into P_1 .

Here whatever analysis we have been doing is using second harmonics only. We can consider the higher order terms also like up to B_2^2 we are considering but there may be B_3, B_4 , etc., considering the higher order harmonics. That will lead to the terms inside bracket $D_2^2 + D_4^2$ etc., but we are now limiting up to only second harmonics and we are not going into higher order harmonic. But if we consider those then the analysis will also involve those higher order harmonics.

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Ex.1
A transistor supplies 2W for a $5\text{k}\Omega$ load.
The zero signal D.C collector current is 35mA and it rises to 40mA when the signal is applied.
Determine the percent second-harmonic Distortion.



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Let us do one example with all the discussion that we had today. The example is that a transistor supplies 2 watt for a 5 kilo ohm load. The zero signal DC collector current is 35 milli ampere and it rises to 40 milli ampere when the signal is applied. Determine the percent second harmonic distortion. Here we are having an example of a power amplifier and the load is 5 kilo ohm and the transistor is supplying 2 watt to the 5 kilo ohm load. That means the power output is 2 watt and that power output what is actually it is considering here it is to be seen that the power 2 watt is the power output or the power consumed by the load. But we will have to also see the second harmonic distortion as is seen here, as given in this question. Determine the percent second harmonic distortion.

Another information given is that the zero signal DC collector current is 35 milli ampere but it rises to 40 milli ampere when the signal is applied. That means you have DC current, I_{DC} zero signal. When the signal is absent, no signal is applied, only the DC current is flowing. That is 35 milli ampere. 35 milli ampere is the current and it rises to 40 milli ampere when the signal is applied. We are applying a signal assuming it to be sinusoidal. When you have no signal this is the value of the current which is a DC current and it will increase and decrease like this and this is I_C max, I_C min. It increases to 40 milli ampere.

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$\frac{5\text{mA}}{\text{Total instantaneous collector current}}$
 $I_C = I_C + B_0 + B_1 C_1 \cos \omega t + B_2 C_2 \sin \omega t$
 $I_C + B_0 = 40\text{mA}$
 $B_0 = 40 - I_C$
 $= 40 - 35$
 $= 5\text{mA}$

The DC component we will have to find out because if we consider the total instantaneous collector current i_C , that is equal to this DC component plus B_0 plus $B_1 \cos \omega t$ plus $B_2 \cos 2\omega t$. It is said here that the zero signal DC collector current is 35 milli amperes and it rises to 40 milli amperes. That DC component will be what? This I_C plus B_0 will be 40 because the total DC component will be rising to 40 milli ampere from 35 milli ampere because we have seen in the earlier analysis that when we were considering this parabolic expression for the collector current we were having those terms B_0 plus $B_1 \cos \omega t$, all these things. So, that DC part if we consider, this DC component in this whole expression of this collector current we will have to see.

This is the expression; this is the total DC component (Refer Slide Time: 59:48). We will have to keep in mind that total DC component means not I_C only it will be I_C plus B_0 when the signal is applied. Without signal it will be only I_C ; that part has to be kept in mind. So now I_C plus B_0 is equal to 40 milli ampere. What is B_0 ? B_0 is equal to 40 minus I_C that is equal to 40 minus 35 is equal to 5 milli ampere.

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Power delivered to load
at fundamental freq

$$P_1 = \frac{B_1^2 R_L}{2}$$

$$2 = \frac{2}{B_1^2 \times 5 \times 10^3}$$

$$\Rightarrow B_1^2 = \frac{2}{5 \times 10^3}$$

$$B_1 = \sqrt{\frac{2}{5 \times 10^3}} = 0.0283A$$

$$= 28.3 \text{mA}$$

If this is the B_0 value, again it is given that the power delivered to load is 2 watt for a 5 kilo ohm. The power delivered to load at fundamental frequency is P_1 equal to B_1 square R_L by 2 and that power is 2 watts. So, it is B_1 square; it is a 5 kilo ohm load, so, 5 into 10 to the power 3 by 2. From this we get B_1 square equal to 4 by 5 into 10 to the power 3. So value of B_1 is equal to under root 4 by 5 into 10 to the power 3. That becomes equal to 0.0283 ampere; it is equal to 28.3 milli ampere. That much is the value of D_1 and mind it this is a having a unit 5 milli ampere because it is the current.

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$B_0 = B_2 = 5\text{mA}$
 Second Harmonic Distortion
 $D_2 = \left| \frac{B_2}{B_1} \right|$
 $= \frac{5}{28.3} \times 100\%$
 $= 17.67\%$

Again we know B_0 equal to B_2 and B_0 we have already found out 5 milli amperes. So, that is 5 milli ampere. The second harmonic distortion which we have to find out is a measure which is given by modulus B_2 by B_1 and we can simply put these values 5 by 28.3 and in percentage we will have to write. So, that gives you 17.67% which is the second harmonic distortion; that is the distortion taking place due to this nonlinearity in the output.

Today we discussed about AB type power amplifier and C type power amplifier. We have used application of complementary symmetric transistors in class AB type of power amplifier. Also we have discussed about the amplitude distortions that takes place due to the nonlinearity in the dynamic characteristics of the power amplifier because of which the second harmonic distortion is taking place and in the output current, we have seen that we got a component having fundamental frequency as well as the second harmonic component. We have also seen the second harmonic distortion measure that is given by D_2 which is an expression relating the B_2 and B_1 values. This second harmonic distortion is one effect that we get in power amplifier which is different from small signal amplifiers because in small signal amplifiers we were using the linear dynamic characteristic which is not the case in power amplifier because it deals with large amplitude of the signals.

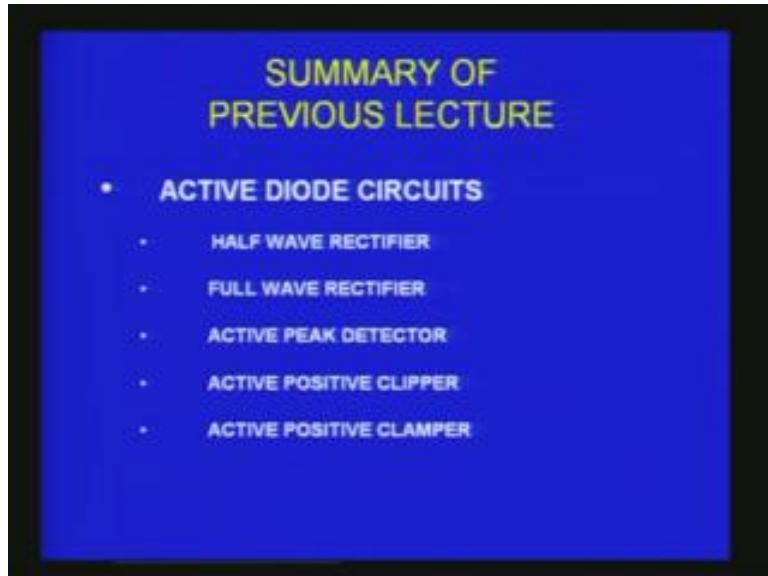
Lecture – 35

Oscillators

(Phase shift, Wein bridge,)

Hello everybody! In our series of lectures on basic electronics learning by doing let us move on to the next. Before we do that let us quickly recapitulate what we discussed in our previous lecture. You might recall that we discussed about an active diode circuit.

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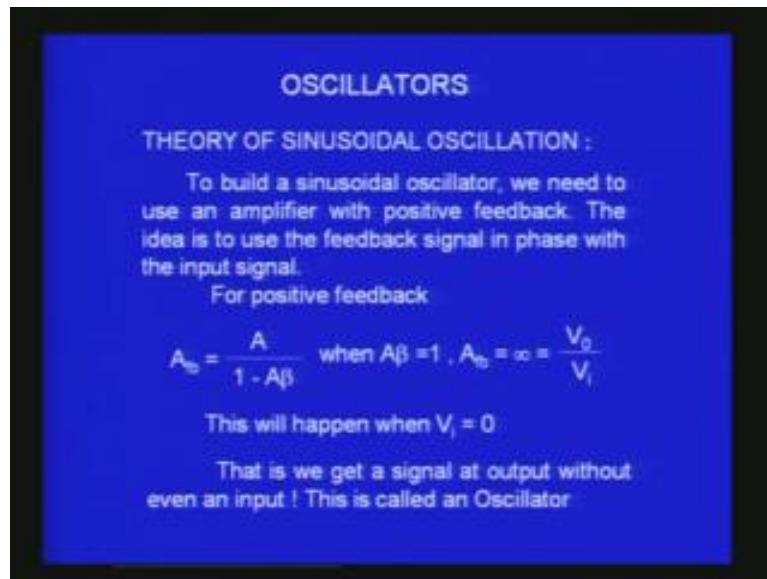


Have a normal semiconductor diode can be improved to become almost an ideal diode and making use of such an ideal diode which is actually a normal diode along with an operational amplifier. This ideal diode was used in different applications like making an half wave rectifier; then how a full wave rectifier can be implemented using such an op amp along with the diode to make an ideal diode. Then we also saw some variations of these like the peak detector and the active positive clipper and clamping circuits which are very useful in different wave shaping circuits.

Let us move on to the next important topic basically in electronics that is design of oscillators. Oscillators are basically circuits which will convert the dc voltage into a sinusoidal voltage. You know about rectifiers. Rectifiers convert an ac voltage into a dc voltage. The oscillators will do just the reverse. It takes the power supply from the dc power supply and the output of an oscillator will be sinusoidal; most of the time it will be

a sinusoidal wave form, sine wave. Oscillators are very, very useful for different applications especially in radio communications. Let us see how we can build oscillators using operational amplifiers. That is what we are going to discuss this time.

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In order to build sine wave oscillators as you can see on the screen we need to use the well known amplifier. Any amplifier can be converted to become an oscillator but you have to give the feed back. To become an oscillator an amplifier should be given a feedback. When I give negative feedback many of the characteristics of the amplifier will improve. We never discussed about the positive feedback. We only talked about negative feedback. Negative feedback means what? Take the output invert it in phase by 180 degrees with reference to the input and give. Then you get a negative feedback. The fed back voltage should be out of phase with the input voltage and this negative feedback improves several characteristics of the amplifier like input resistance, bandwidth, output resistance, distortion, etc. But if I now take the path of the output voltage and give it in phase with the input voltage then it becomes positive feedback. In an amplifier if I implement positive feedback it normally results in oscillation. When I want to use the amplifier for the amplification purposes we will not use the positive feedback. We will only use negative feedback. But when we want to convert an amplifier into an oscillator then you go in for positive feedback. We have also derived one of the earlier lectures the condition for a gain of an amplifier with feed back and that you can see in the screen.

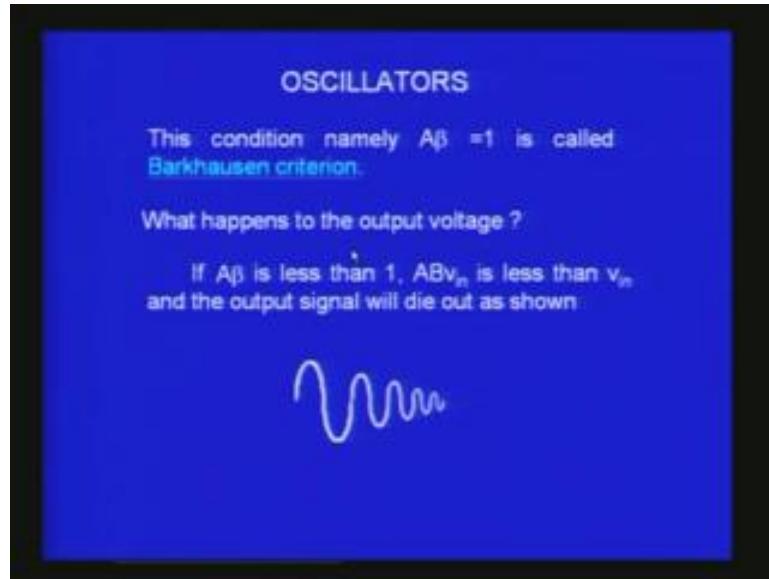
A by one plus A beta; you may remember that expression. A_{fb} which is the gain with feedback is equal to A, the gain without feedback divided by 1 minus A beta where beta is the feedback ratio, the fraction of the output which was given at the input. This minus sign is what you get for positive feedback. For negative feedback the sign in the denominator will be plus. For amplifiers you would have used the formula A_{fb} is equal to A by 1 plus A beta. But when you want positive feedback, the same derivation you can do, it will become 1 minus A beta when you impose the condition the output should be in

phase with the input which is corresponding to positive feedback. Because you have a minus sign it introduces very interesting situation here. ‘A’ generally is a large number, gain. Beta is a small fraction. Sometimes it may so happen that when A beta becomes equal to 1. That is when A is equal to 1 by beta then A beta becomes 1. When A beta becomes 1 what happens to the denominator? A by 1-1; 1-1 is zero. The denominator becomes zero. In any fraction if the denominator becomes zero it becomes infinity. The gain with the feedback is now infinity. What do you mean by that? Infinite means very large number or what is feedback in general? What is gain in general? Output voltage by input voltage; that is the voltage gain.

When will the output voltage divided by the input voltage become infinity? It will become infinity only when the denominator becomes zero. The denominator in this case is V_i , the input voltage. What it means is when I make positive feedback in an amplifier, when I provide positive feedback and make the product A beta equal to 1 it is equivalent to saying I get an output voltage with zero input voltage. That is the denominator becomes zero in this expression. When the denominator becomes zero, expression becomes infinity and you get only output voltage. That means what? Without giving any input voltage you are getting an output voltage. This is what we call oscillator. It is an amplifier in which you don’t have to give any input but you get an amplified output signal, ac signal. Where from it is coming? It is generated out of the power supply voltage that you have given. I call that as a converter of a dc into an ac. You give only a dc supply for energizing the amplifier circuits. But you have implemented a positive feedback and you have made sure the feedback ratio is in such a way that the gain into the feedback fraction is equal to 1. If you do that you get the output sine wave without any input. That means it becomes an oscillator.

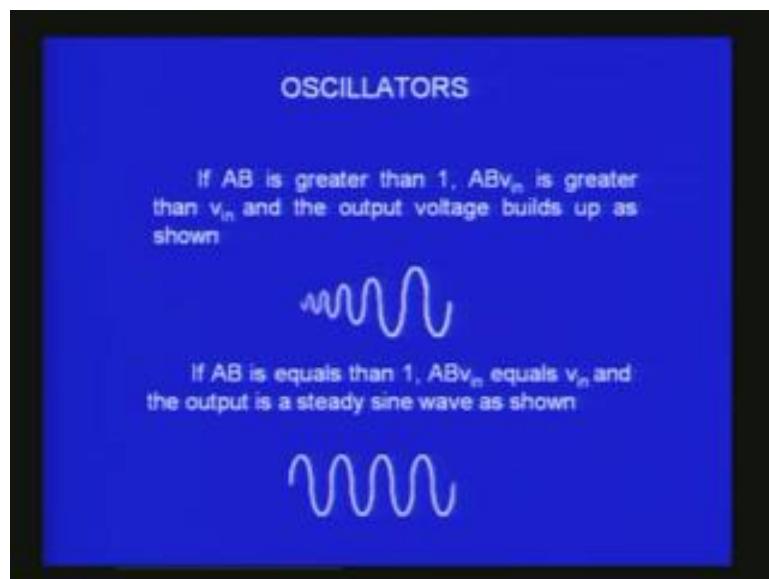
This A beta condition you will not get all the time. It has to be satisfied only at one particular frequency. This feed back will have to be given through some frequency sensitive components, reactive components and this condition will be true only for one specific value of frequency corresponding to the reactants. Only that frequency will be preferentially provided and the output will be having that frequency. If you want to vary the frequency correspondingly you have to vary the reactive components that you have in the circuit. But in principle what I have so far explained is the most important criteria or the principle of oscillators. This condition A beta should be equal to 1 in an amplifier with the positive feedback for generating oscillator is called Barkhausen criterion. What happens to the output voltage?

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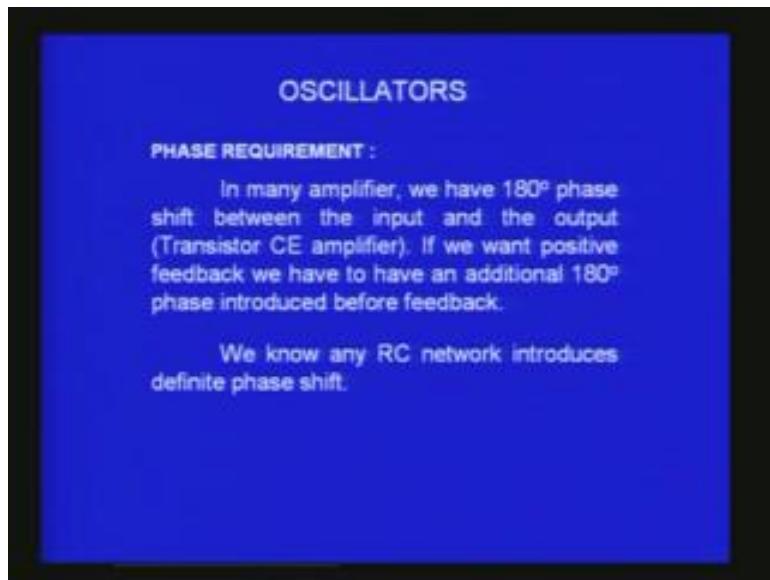
For different values of A beta if A beta is less than 1 then the gain will be increasing. ABV_{in} is less than V_{in} and the output signal will slowly die out and that is what is shown here. The initial sine wave keeps on decreasing because it is less than 1 subtracting , being subtracting. If the A beta value is greater than 1 then A beta V_{in} is greater than V_{in} and the output voltage keeps on building up. When you give feedback larger portion comes through the feedback. It increases the input voltage and the output will still further increase because it is just an amplifier. The sinusoidal voltage which starts with a small amplitude will start building up. This also is not a very desirable feature. The previous one where the amplitude decreases is not also what we want.

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What we want is something which will sustain the oscillations with constant amplitude. That happens when AB is equal to 1. Then ABV_{in} is also equal to V_{in} because A beta becomes 1. Both are V_{in} and there is no loss. There is no decrease there is no increase. It maintains the same input. You will get the same output. That means you get a steady output sine wave. That is what is shown in the picture at the bottom. This is basically the idea behind that of the oscillators. But if you actually take any amplifier for example RC coupled transistor amplifier the output is always 180 degrees out of phase with reference to the input. This is a characteristic of the RC coupled amplifier when you have common emitter configuration. This 180 degree shift is already built into the amplifier configuration due to the common emitter configuration.

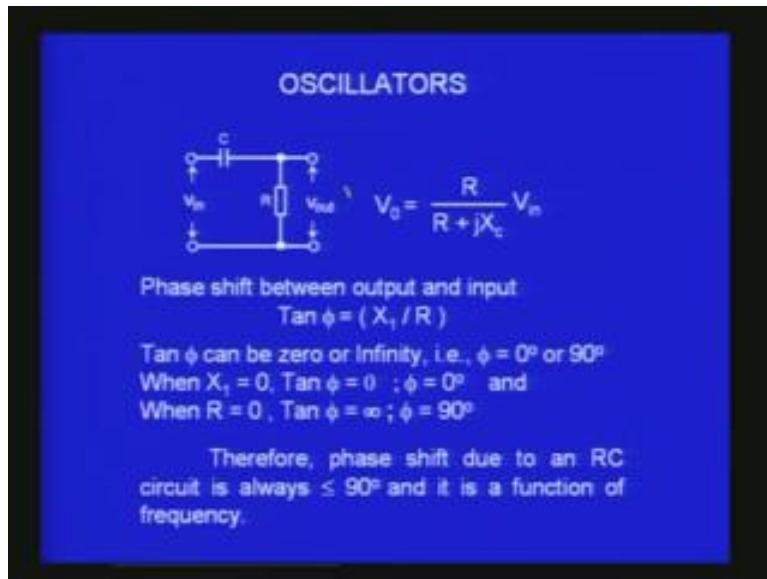
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If we want to have a feedback the feedback should be positive. That means the input voltage should be in phase with the voltage fed back from the output. If we take the output directly from this amplifier and give it at the input it is 180 degrees out of phase. It will not be positive feedback but it will only be a negative feedback. That is what we do in many amplifiers. For making positive feedback you should introduce a phase shifting network between the output and the input and then only give the feedback voltage. That phase shifting network you should make sure produces another 180 degree phase shift so that the total phase difference becomes 360 degree which is equal to zero degree phase shift. This is the idea; use a normal amplifier which has got 180 degree phase difference between the input and output, use a separate network using some combinations of reactive components so that it produces another 180 degrees in addition and together both of them will provide 360 degree phase difference and if you now give this fraction to the input and make sure that it is equivalent to the input voltage then you can slowly remove the input and this positive feedback alone will sustain the oscillations and you will get steady sine wave at the output. That is the basic principle of an oscillator.

How do we introduce that additional phase difference of 180 degrees? The simplest method is to use resistance and capacitance in combination. A RC network, which we have already discussed when we discussed about the frequency response of amplifiers, a lead network and the lag network about which we talked about you can use any one of these. Either the lead or a lag both of them introduces a phase difference. Any RC combination produces the phase. I have shown you on the screen a very simple scheme with the capacitor and R in series and you take the output across the resistor.

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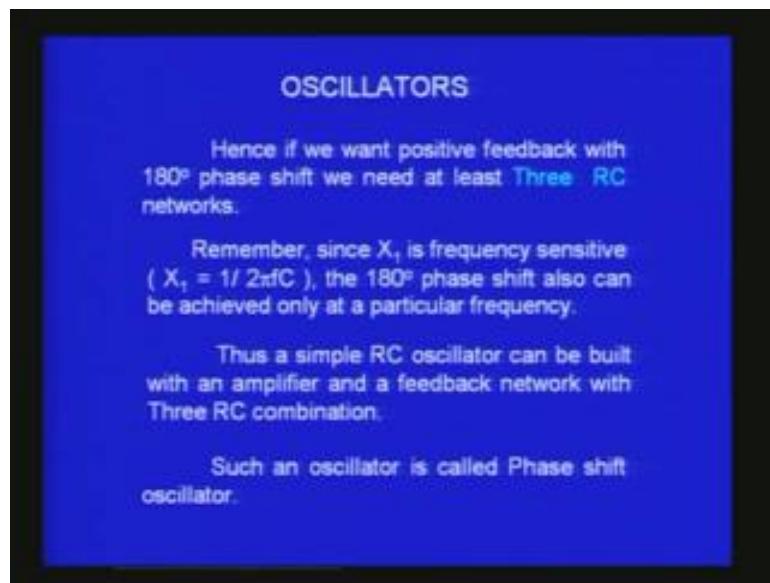


What is the output voltage? The output voltage is the output resistance R divided by R plus jX_c into V_{in} . This is a potential divider. This C and R reactive component and the resistive component form a series circuit as a potential divider and you are taking the output across the R resistance and the formula is R divided by R plus jX_c into V_{in} . The jX_c is actually the reactive impedance of the capacitance. X_c is $1/\omega C$. What is the phase shift in this case? It is X_c by R. We have written here X_1 by R. That is the phase difference phi. This simple RC network will automatically give a phase shift of X_1 by R where X_1 is $1/\omega C$ where omega is the angular frequency which is equal to $2\pi f$ where f is the frequency of the input sine wave and for a given frequency the X_1 will be different. Capacitive reactance is a function of frequency. Depending upon the frequency the reactance will change and hence the phase difference should change and in this case tan phi can be zero or infinity or any other value in between. If phi is equal to zero or 90 degree then X_1 is equal to zero. When X_1 is equal to zero, tan phi is equal to zero in this equation, in this formula and phi is equal to zero degree. When R is equal to zero in the denominator then the tan phi becomes infinity and phi becomes 90 degree. Using one RC combination you can have any phase difference between zero and 90 degrees only; not more. You can always have less than 90 degrees but you cannot have more than 90 degrees by using just one RC. Even 90 degree is an extreme case. Zero degree and 90 degree are two extreme cases. A phase shift due to an RC circuit is always less than 90

degrees and it is also a function of frequency. These two important points we should remember before we go into the design of oscillators.

If you want in an amplifier like a common emitter amplifier which produces 180 degree phase shift between the input and output and if you want another additional phase shift of 180 degrees then how many RC networks you require to have additional 180 degree? What will be the answer? One RC network can only provide at the maximum of 90 degrees. It is always going to produce a phase shift which is less than 90.

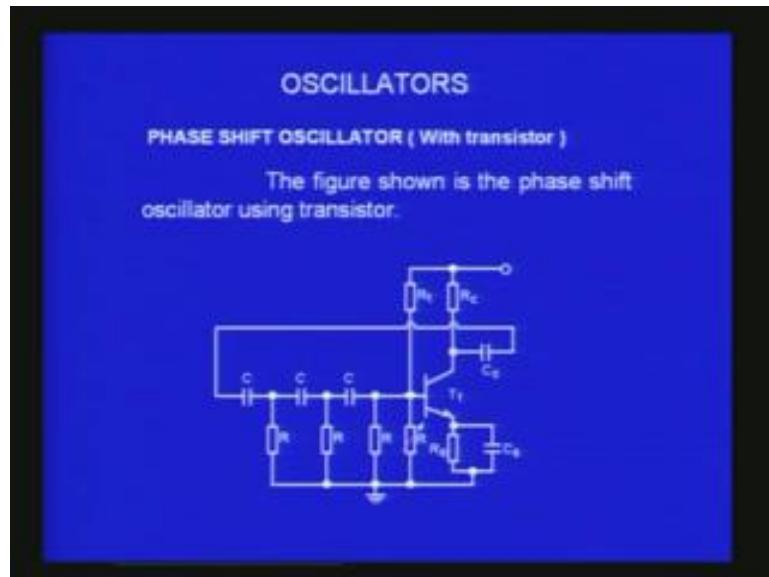
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When it is less than 90 even 2 RC networks cannot give 180 degrees and a minimum of 3 RC networks are required to produce total 180 degree phase shift for a given frequency. This is the principle of a phase shift oscillator. I will talk about it now. Let me show you the circuit of the phase shift oscillator with transistors. Then we will go on to the op amp because the principle is the same. You have here a transistor and if you look at only the first part where I show with the pointer this is nothing but an amplifier with a voltage divider bias R_1 and this variable R . R_c is the collector resistor, R_eC_e gives you the emitter bias. This is basically an amplifier, single stage RC coupled amplifier because you are coupling with the C here RC coupled amplifier.

What we are doing is we are taking the output and it is brought back through this wire to the input and at the input you are combining series of RC circuits. C R that output is taken and given to another C R. That output from the R is taken to another CR and that output is given to the input. Between this base which is the actual input of the amplifier and the collector there is 180 phase shift and that 180 degree phase shift voltage is applied here. With these three combinations of RC, RC, RC you try to produce another 180 degree so that totally it becomes 360 degrees and then this voltage which comes from the output becomes in phase with the input that you **should perhaps** have given at the beginning. You have not given anything. This happens very fast.

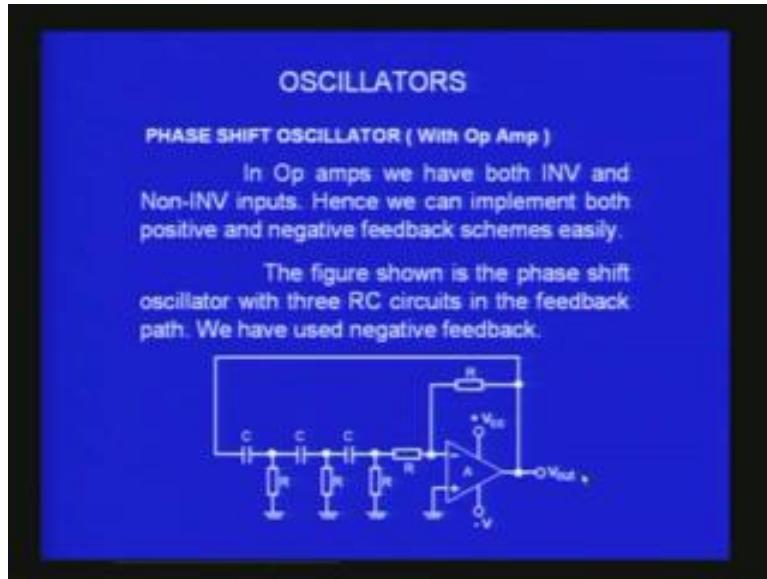
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I will explain to you how this happens? This becomes the input voltage and if the conditions are fine, ideal then this input will get amplified enough so that after passing through these three, again it becomes the same value as the initial value. You get a constant input voltage and this RC, three of them provide 180 degrees in addition to the 180 degree that is produced by the RC coupled amplifier the total **worth is** 360 degree provides the necessary positive feedback and the output you take now here from another wire and connect it to an oscilloscope it will start oscillating. If it is not oscillating, all that you have to do is in one of the bias resistors I have put variable; you vary this slightly. Then at some position of this resistance when the conditions are proper, when the gain becomes sufficient you will get a sine wave coming at the output. This is a simple RC coupled amplifier, RC phase shift oscillator constructed using a simple RC coupled common emitter amplifier.

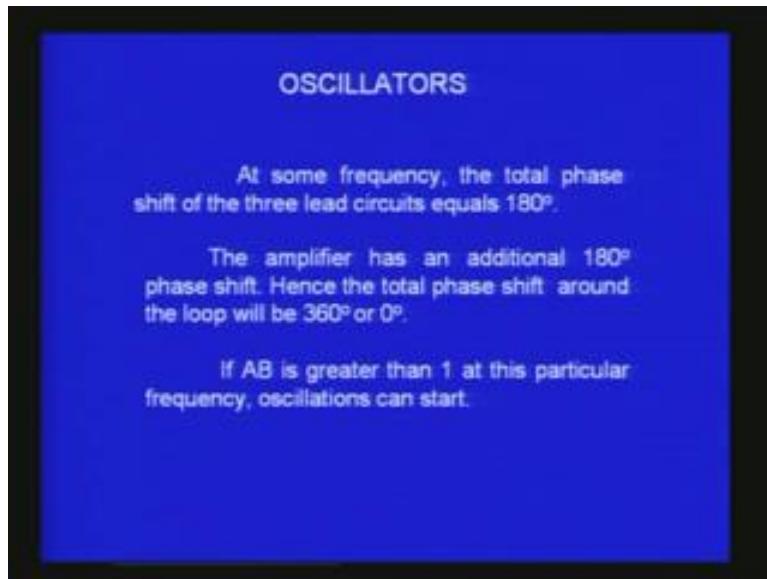
How will we do that using operational amplifier? In operational amplifier we have another advantage. The advantage is we have both the inverting and the non-inverting inputs so that whatever type of voltage feedback you want to give you can give in principle. But now what we are going to do is we are still going to use the 180 degree out of phase as we did in the phase shift oscillator I showed. There is a 180 degree phase shift. That output is now taken and given to combination of three RC networks here so that the phase here becomes 180 degrees, additional 180 degrees and it will be in phase with the input and then this will sustain oscillation and you will get the output.

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This is the circuit corresponding to a phase shift oscillator using op amp. You didn't find much difference with the transistor amplifier except that I have removed the transistor common emitter amplifier and in place of that I have introduced an inverting amplifier using op amp.

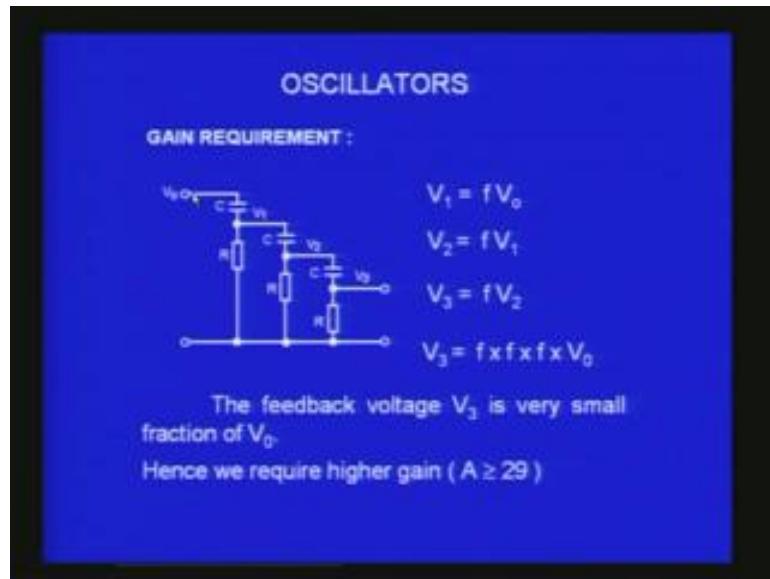
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At some definite frequency f , $2\pi f$ will be omega and that will introduce at that frequency exact 180 degree phase difference with the combination of three RC networks. Once that happens you get the oscillations and when the AB is just the right value equal to 1 corresponding to Barkhausen condition the oscillations will start and you will get the

output. You also should remember one important point in this and that is there is a minimum gain that I must ensure in this circuit, the phase shift oscillator so that the oscillations will be produced. It is not just one condition that the output should be fed back in phase there should be a positive feedback. That is one of the conditions. The second important condition is it should have sufficient gain the amplifier as such should have sufficient gain. Why is it so? To explain that I have shown you a circuit on the screen. What you are doing is you are feeding the output voltage at this network.

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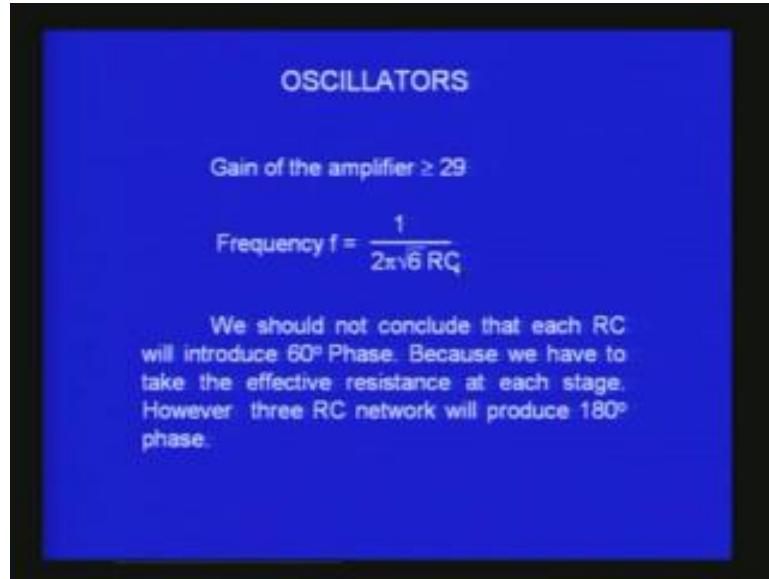


You have got a potential divider with one reactive and resistive component and take the output across the resistive component connect to one more RC. Then take the R output and again connect to one more. You have three stages of potential division. You divide it once into V_1 . Then again divide into V_2 then again divide into V_3 . What happens is for example if V_1 is 50%; if V_1 is 50% with reference to V_o output then V_2 will be half of that. That means $1/4^{\text{th}}$ of V_o . If every one of the network gives 50% let us assume then the first network will give half of the input. The second network will be $1/4^{\text{th}}$ of the input V_o and the third will be $1/8^{\text{th}}$ of this. There will be a continuous reduction and you have to amplify this to bring it to some level so that A becomes equal to 1. Whatever is the reduction that happens here you should amplify. If it is 8 times you should try to amplify by 8 so that you will get A equal to 1. That is the whole idea behind this phase shift oscillator. I call f as the fraction of the output not the frequency. V_1 is fraction of the V output. V_2 is fraction of V input, V_1 ; V_3 is fraction of V_2 and the total is f_1, f_2, f_3 times V_o . This f_1, f_2, f_3 is same like 0.5 that I mentioned and it becomes $1/8^{\text{th}}$. The V_3 that is actually applied at the input is very, very small because it has gone through three levels of potential division and when you are analyze the circuit you would get an expression where the gain of the amplifier for the phase shift oscillator to work should be greater than or equal to 29 to make the A equal to 1.

Why is it so? We will try to derive the expression also later on and we also should remember the frequency of this will be given by an

$$f = \frac{1}{2\pi\sqrt{6RC}}$$

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The root 6 is a factor which is coming in addition to the normal 1 by $2\pi RC$ term. When you use 3 RC phase shifting network the oscillator works when you maintain a gain which is larger than 29 and the frequency will be given by the expression

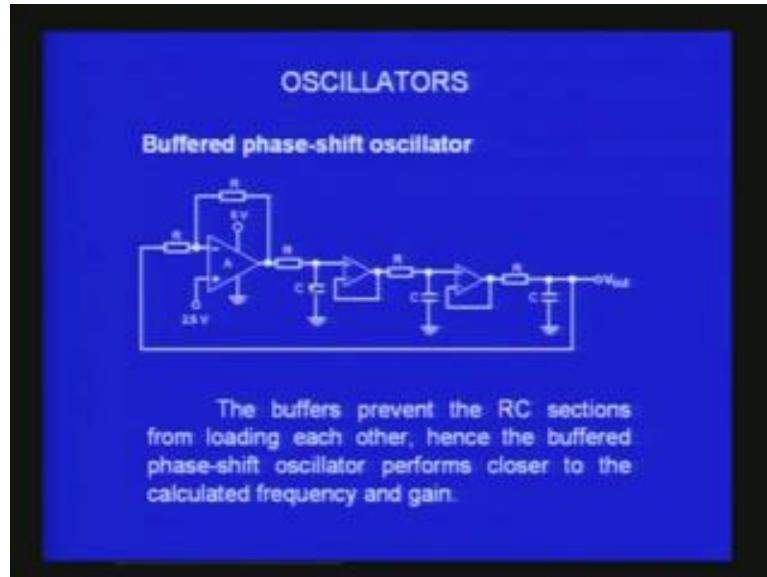
$$\frac{1}{2\pi\sqrt{6RC}}$$

where R and C I assume are equal. You can also choose $R_1 C_1$, $R_2 C_2$, $R_3 C_3$. Then this expression will be much more complicated bigger expression. So usually everybody will try to do simple equal values of R and C for all the three networks. When I give equal values for all the three networks RC each of these will produce 60 degrees phase shift. First one produce 60 degrees the second one produce another 60 degrees and the third one produce 60 degrees. That is what we all assume. In principle it should be something like that. But in practice it is not. Ideally it is like that but in actual case it is not like that because if I take this R the potential divider is between the C and this R. That is what we have assumed. That will be true only if you don't take into account the effect of the presence of this other RC network. Because they are all connected they are all connected in parallel. The value of R will be affected by these two because they are in parallel combination. Again this R is affected by this RC, etc and you would not get the same R in each of the stages because of the presence of the other components and they will be

never be equal to 60 degrees. You will get almost close to 60 degrees if you observe but it is not equal to 60 degrees.

If you really want to make them equal then what we have to do is we should isolate each of the RC networks from the other. For that I have used a buffered phase shift oscillator which you can see here. What I have done is the output voltage I connect to RC but I make sure the presence of other RC are not felt at this point.

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For that I have used a unity gain buffer which is very good circuit to produce very high input impedance and very low output impedance with a gain 1 and they only provide high input impedance here. It is so high that the reactive component due to C is the only contribution to the resistance here and the effect of all the rest of things that you have connected will not be felt here. This way I isolate segments from the other and thereby I have used two isolators here, buffers and if I measure the phase shift due to each of the RC network in this case it will exactly be 60 degrees for a given frequency. This is what is called a buffered phase shift oscillator. Let us try and see whether we can derive the expression for the phase shift oscillator.

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OSCILLATORS

Phase shift can also be produced by an R.C network. Consider a resistance R connected in series with a capacitor C . If an alternating voltage V_1 is applied to the terminals of the network. The current in the circuit

$$i = \frac{V_1}{\frac{1}{j\omega C} + R} = \frac{V_1 j\omega C}{1 + j\omega CR}$$

The voltage across R has a value

$$V_2 = iR = \frac{V_1 j\omega CR}{1 + j\omega CR}$$



I will not give too many details. I will quickly skip some of the intermediate steps. I would expect that you would try to do it on your own and learn. I will give you all the principles involved in that. I take one RC network here C and R and what is the current? The current is voltage V_1 divided by the total resistance, by Ohm's law. Total resistance is R in series with capacitance R plus 1 by $j\omega C$. 1 by $j\omega C$ is the capacitive reactance. When I simplify this it will become

$$\frac{V_1 j\omega C}{(j\omega C + 1)}$$

This is what I get. The voltage across R has a value V_2 is equal to current into resistance, again Ohm's law, i into R . Now if you multiply this i by R you get $V_1 j\omega CR$ divided by $1 + j\omega CR$. You can get the value of the output voltage with reference to the input voltage when I apply it across a simple CR network.

I am going to connect like this three such networks.

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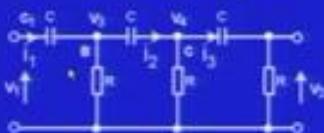
OSCILLATORS

The input voltage v_1 and the output voltage v_2 have a phase difference ϕ

$$\text{Where } \tan\phi = \frac{1}{\omega CR}$$

The phase shift depends on the frequency and the values of C and R.

Let us consider the following circuit.



This is V_1 , V_2 , V_3 etc. I am calling this V_2 and this I call V_4 . At this point it is V_3 and here I have V_1 . The phase difference due to one of them is 1 by ωCR . We have already seen that

$$\tan \phi = \frac{1}{(\omega RC)}$$

Let us try to derive the expression. What is V_4 ? V_4 is equal to V_2 plus i_3 divided by $j\omega C$. Why is it like that? V_4 is here. What is V_4 ? V_4 is the voltage across R plus the voltage across C. The voltage across the R is V_2 . The voltage across C is i_3 into reactance provided by C. Reactance provided by C is 1 by ωC . V_4 is equal to V_2 the voltage across R plus i_3 into 1 by $j\omega C$; i_3 by $j\omega C$.

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OSCILLATORS

It has three CR sections and is called a ladder network.

Let v_1 be the input voltage and v_2 the output. If v_3 and v_4 are the voltages at the points B and C we have

$$\begin{aligned}v_4 &= v_2 + \frac{i_3}{j\omega C_1} \\&= v_2 + \frac{V_2}{j\omega CR} \quad \text{as } i_3 = \frac{V_2}{R}\end{aligned}$$

What is i_3 ? i_3 is V_2 by R . This is i_3 , this current and it should be V_2 by R . If I substitute this it becomes V_2 plus V_2 by $j\omega CR$. i_3 I have replaced. This is the voltage at V_4 . I want to look at the next current i_2 in the circuit which is this current. I want this current i_2 . This current i_2 is i_3 plus the current through this. i_3 is already known; we have already derived. This current is V_4 by R . That is what I am going to use now.

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OSCILLATORS

$$i_2 = i_3 + \frac{V_4}{R} = \frac{V_2}{R} + \frac{1}{R} \left(-v_2 + \frac{V_2}{j\omega CR} \right)$$

$$= v_2 \left(\frac{2}{R} + \frac{1}{j\omega CR^2} \right)$$

$$v_3 = v_4 + \frac{i_2}{j\omega C}$$

$$= v_2 + \frac{V_2}{j\omega CR} \quad \text{as } i_3 = \frac{V_2}{R}$$

i_3 plus V_4 by R is i_2 . I now substitute for i_3 which we have already got and i_3 is V_2 by R plus 1 by R into V_2 plus V_2 by $j\omega CR$. That is V_4 . We have calculated this. When you now combine and then simplify this V_2 is common every where. V_2 into this is 1 by

R , 1 by R ; 2 by R plus 1 by $j\omega CR$ square. These two R will become R square. This is what you get. V_3 is I have to multiply this by corresponding number V_4 plus i_2 into 1 by $j\omega C$. You substitute for that again from the earlier expression for V_4 and you will get this expression and similarly you go for one more stage. i_1 is i_2 plus V_3 by R and you substitute you get this big expression and finally you can write V_1 in terms of V_2 .

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$$i_1 = i_2 + \frac{V_3}{R}$$

$$= V_2 \left(\frac{3}{R} + \frac{1}{j\omega CR^2} - \frac{1}{\omega^2 C^2 R^3} \right)$$

$$v_1 = v_3 + \frac{j i_1}{j\omega C}$$

$$= V_2 \left(1 + \frac{6}{j\omega CR} - \frac{5}{\omega^2 C^2 R^2} - \frac{1}{j\omega^3 C^3 R^3} \right)$$

If you go back and look at the circuit V_1 and V_2 are the two things that we want. When I apply V_1 what is the output? V_2 . In the final expression

$$V_1 = V_2 \left(\frac{6}{j\omega CR} - \frac{5}{\omega^2 C^2 R^2} - \frac{1}{j\omega^3 C^3 R^3} \right)$$

. That is what I get. What is the condition? The output voltage should be real and I should make sure the imaginary components in this expression become zero. The imaginary components are basically the second term 6 by $j\omega CR$ and 1 by $j\omega^3 C^3 R^3$. These two terms together should become equal to zero. That is what I have written. 6 by $j\omega CR$ minus 1 by $j\omega^3 C^3 R^3$ should be equal to zero.

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The output voltage is real at a frequency making factor

$$\left(\frac{6}{j\omega CR} - \frac{1}{j\omega^2 C^2 R^2} \right) = 0$$
$$\omega^2 = \frac{1}{6 C^2 R^2}$$
$$\omega = \frac{1}{\sqrt{6} CR}$$

If you simplify this you get omega square is equal to 1 by 6 C square R square and omega is 1 by root 6 CR and omega is 2 pi f. f is equal to 1 by 2 pi root 6 RC or CR. This is the expression for frequency. The expression for frequency comes from the condition that the network should have imaginary component zero. If you do that automatically you will get the frequency component. At this frequency what happens? This happens only for one frequency you should remember that. At this frequency I can now substitute that value in this expression and you will be taking only the real part because the imaginary part has become zero. You have

$$1 - \frac{5}{\omega^2 C^2 R^2}$$

. But what is omega square C square R square?

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OSCILLATORS

At this frequency

$$V_1 = V_2 \left(1 + \frac{6}{j\omega CR} - \frac{5}{\omega^2 C^2 R^2} - \frac{1}{j\omega^2 C^2 R^3} \right)$$

Taking only the real part

$$V_1 = V_2 \left(1 - \frac{5}{\omega^2 C^2 R^2} \right),$$

$$V_1 = V_2 (1 - 5 \times 6) = -29 V_2 \quad \left\{ \because \frac{1}{\omega^2 C^2 R^2} = 6 \right\}$$

The output voltage is $1/29$ ($= \beta$) times the input and is 180° out of phase with the input at the frequency.

From this expression $\omega^2 C^2 R^2$ is nothing but 6. When I take this $\omega^2 C^2 R^2$ to the denominator 6 comes over on to the left side and the expression becomes 5 into 6 because 1 by $\omega^2 C^2 R^2$ is equal to 6. That is 1 minus 30 is -29V₂. The output becomes V₁ is equal to -29 times V₂ or V₂ is 1 by 29 times of V₁ with a 180 degrees phase difference. Minus shows it is phase difference also. When will this become equal to 1? Only when the gain becomes 29; this is the beta factor 1 by 29. When the gain becomes 29 A beta becomes 29 into 1 by 29 which is equal to 1. It will satisfy the Barkhausen condition, you will get 180 phase also and the oscillations will be sustained. This is what we have in the RC phase shift network.

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OSCILLATORS

Hence the gain of the amplifier must be greater than 29 since $A\beta$ must be 1

$$A\beta = A \times \frac{1}{29} = 1$$

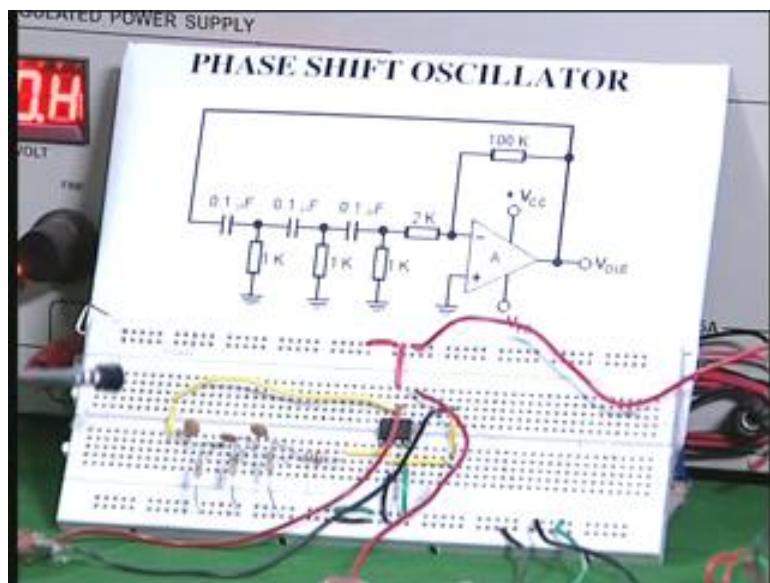
$$\therefore A = 29$$

When A is equal to 29 this product becomes 1 but has satisfied the Barkhausen condition. With this background we have now discussed how you can make the phase shift

oscillator using an operational amplifier using three RC network and it is very convenient because R, C are all very cheap components. You don't have to have very expensive gains and then you can easily vary them, change them and modify the frequency of the output waveform and it is very convenient to design, simple to design and I will show you a demonstration of the phase shift oscillator using operational amplifier.

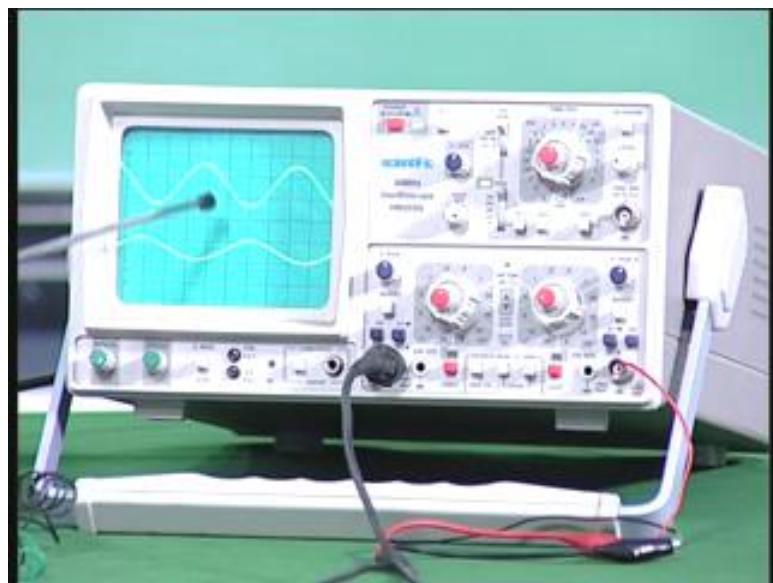
Here the circuit is the same circuit which I showed you on the screen. You have the operational amplifier in the inverting mode with R_1 R_2 . This is 2K and this is 100K. There is a gain of about 50. You can even make this as variable. I have used it as a variable potentiometer here and when I vary this I can get a gain which is larger than 29 very easily by modifying this R_2 by R_1 ratio. This is an inverting amplifier because you are connecting to the minus input. It is an inverting amplifier; there is 180 degree phase shift here. That output I take and give it to series of three RC. They are all 0.1 micro farad, 1K equal values.

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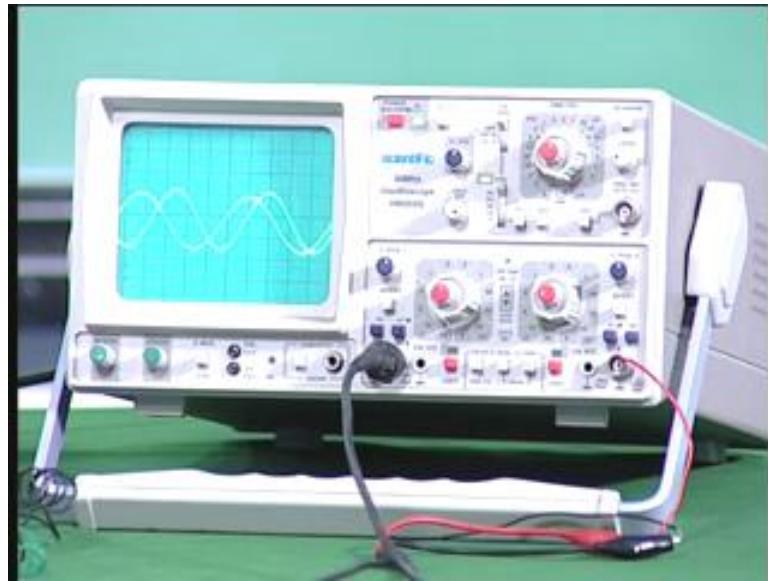
You can see in the circuit here three 1K resistors and three 0.1 micro farads here and that output is connected to the input pin number 2 of the operational amplifier that you see here and for the feedback resistor I have used a potentiometer, carbon resistor here and the output is monitored by using the oscilloscope. To determine the frequency of the oscillation I am also connecting a function generator here. You can see that this is the function generator. You can select different frequency scales here 1, 10, 100, etc and you can vary the frequency using these two knobs. One is for fast variation the other one is for slow variation; coarse and fine and you have here output voltages which is again for coarse and fine. You can vary the amplitude and the output of this I connected to another channel of the oscilloscope. In the oscilloscope you see two channels. If I change the frequency in the oscilloscope the two signals are same.

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This steady one is due to the oscillator that we have constructed. This one is from the standard oscillator that I have used. What I am trying to do is I am trying to superpose them and measure the frequency. I am using the oscilloscope to bring them together and if necessary increase the amplitude, make the amplitude equal. I have made them almost equal amplitude and then I will slowly change the frequency till you get some coincidence. This almost coincides. When it is coinciding there is a continuous phase factor which is coming. That is why it keeps on moving. If you arrest them both the frequency is almost the same.

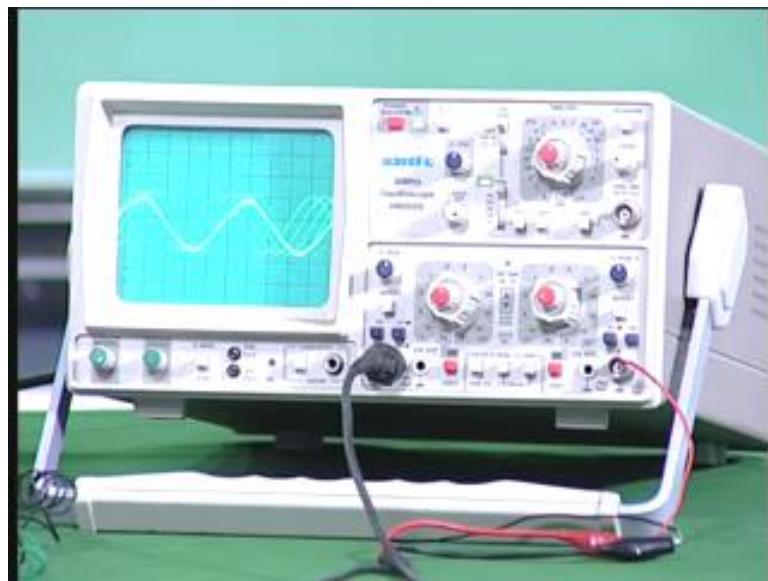
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It is around 636. That is what you see here. This is the frequency and if you actually calculate $1 \text{ by } 2 \pi \text{ RC}$ with R 1 kilo ohm and C 0.1 you will get close to 600 hertz but you may not get exact value and that is because there is also a tolerance of these resistors and the capacitors. Because of that you will not get an exact value but you should get very close value corresponding to 600 hertz.

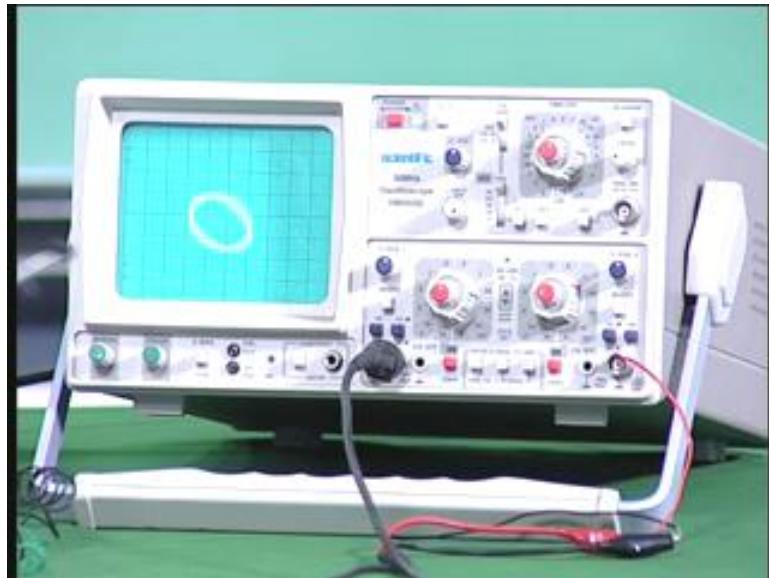
How do you know that the output wave form that I get is due to the oscillator? I am varying the gain factor here. I get very high amplitude. When I change that now I don't get any oscillation. When I change it, in the right gain of about 29 you see on the oscilloscope a building up of the sine wave.

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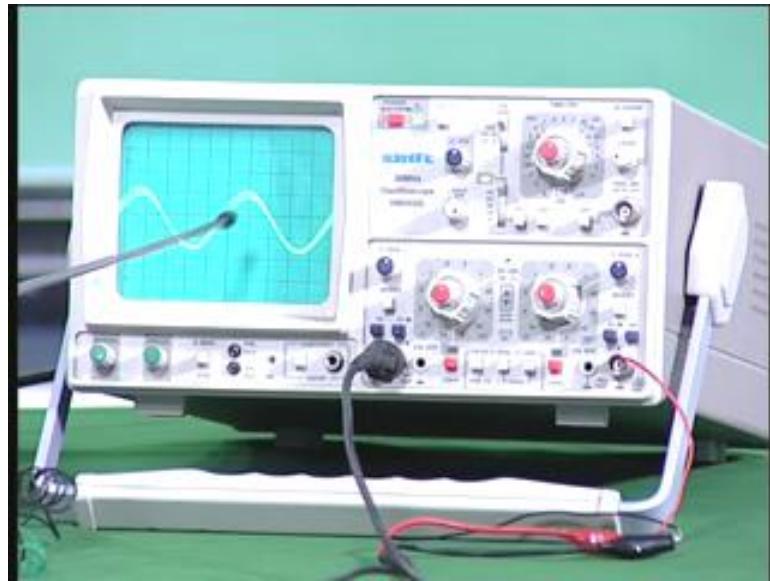
The sine wave builds up and if I now reduce it goes to zero. It is only the output from the circuit that I get on the oscilloscope. When I change it to X-Y mode then you get a straight line. We have to get the wave form back and then adjust the frequency. I am now making it X and Y and try to adjust till I get a circle. You get a circle here. When will you get? This is Lissajous pattern. When the frequency of the oscillator that we have constructed using the operational amplifier and the frequency from the function generator when both of them match I will get a circle on the screen.

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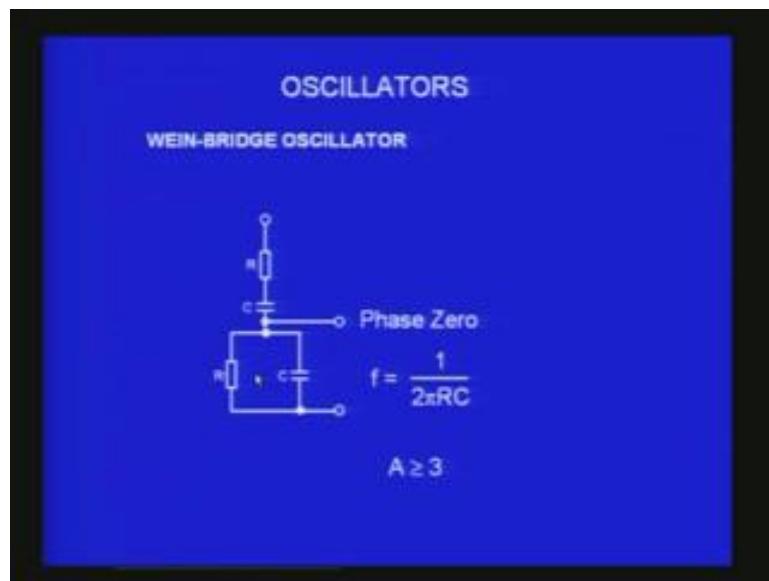
That shows the two frequencies are equal. Now if I make it into a dual slope both the sine waves are almost coinciding and the frequency is the same.

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There are two ways in which you can measure the frequency. One is by comparing with another oscillator. The other one is using the X-Y mode and trying to generate the Lissajous pattern. That is what we have just now done. You have a phase shift oscillator here using op amp and the output to be measured in the frequency also has been measured. We will go on to the next circuit which is again an oscillator and again it uses RC networks and that is called Wein's bridge oscillator. What is a Wein's bridge? You can see on the screen a combination of RC again. But one RC is in series the other RC is in parallel.

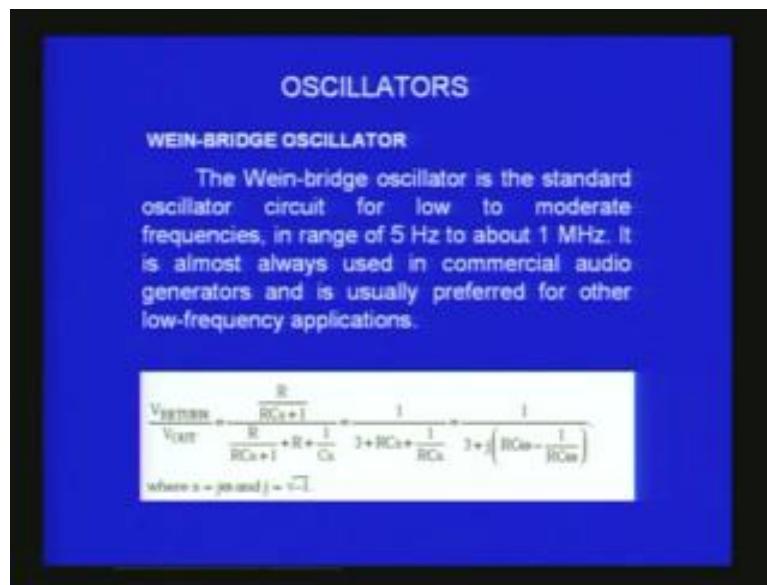
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When I have RC in series and RC in parallel this combination is what is called the Wein's network. Wein is the one who found that when I give an input here the output that

comes from this will be at zero phase for a given frequency. That is the property of this Wein's network and phase is zero and the frequency is 1 by 2 pi RC and when you do the investigation just as you did for the case of the phase shift oscillators, the gain will have to be at least 3; either equal to or greater than 3. These are the important points with reference to the Wein's bridge and one can also obtain the expression, I have given just the expression which you can test later on. This expression can be worked out on your own and this will also lead to the corresponding gain which should be greater than 3 and the phase shift will become zero. This RC Wein's bridge network can be used for generating frequencies in the range nearly 5 Hertz to 1 Mega Hertz. This is the greatest advantage of the Wein's bridge oscillator built on the Wein's network.

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Everybody wants a variable frequency oscillator. Just now you saw a function generator which I used where I was turning a knob and the frequency was changing. If you want to do that in the RC phase shift network you have got three resistors and three capacitors. You have to adjust all of them either equally or differently. It becomes very cumbersome to have too many components to vary. In the case of Wein's bridge we have only two R

and two C. Usually C is switched for decades and the resistance is varied for changing the frequency in between. It is very convenient, more convenient than RC phase shift network to use the Wein's bridge in the oscillator circuit. I have also shown a small analysis.

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OSCILLATORS

FORMULA FOR RESONANT FREQUENCY

By analyzing the figure with two complex numbers, we can derive these two equations.

$$B = \frac{1}{\sqrt{9 - (X_c/R - R/X_c)^2}}$$

and

$$\tan \phi = \frac{X_c/R - R/X_c}{3}$$

The feedback fraction given by equation has a maximum value at the resonant frequency.

If you do that the beta factor will be 1 by root 9 minus X_c by R minus R by X_c whole square. The phase factor tan phi is equal to X_c by R minus R by X_c whole value divided by 3. These two expressions can be derived by using a simple network idea. I leave it to you as an exercise and what is important is when X_c becomes R that corresponds to a condition R is equal to 1 by 2 pi f_r C where f_r is the critical frequency.

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OSCILLATORS

At this frequency, $X_C = R$

$$R = \frac{1}{2\pi f_r C}$$

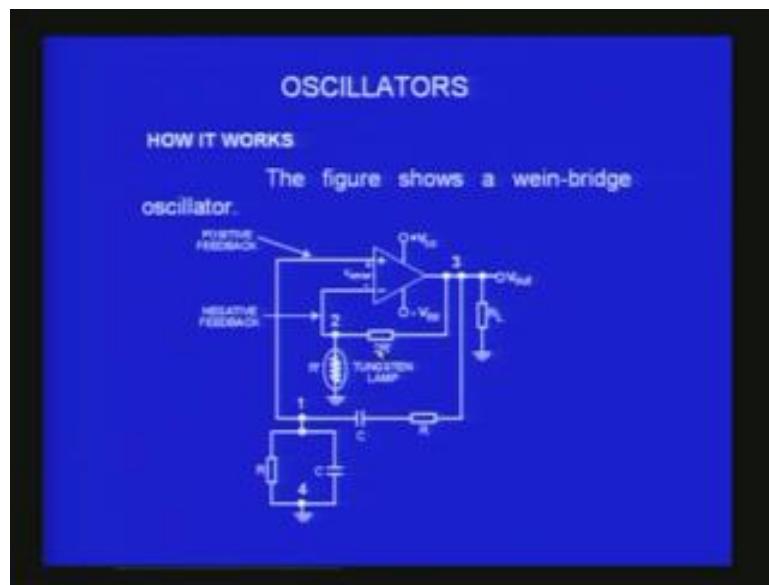
Solving for f_r gives :

$$f_r = \frac{1}{2\pi RC}$$

You get a maximum at that point, the fraction and that corresponds to 1 by 3. Beta will become 1 by 3. From this expression frequency is 1 by 2 pi RC and the phase actually goes at that frequency. X-axis is the frequency. At that frequency the phase goes to zero. Before it is +90 and beyond it is -90 and in between it crosses the zero and when it crosses the zero the corresponding factor is 1 by 3, the feedback ratio and that gives me an expression for the frequency as 1 by 2 pi RC.

I have now shown you the full circuit using op amp. This also can be constructed using transistors. When I have the Wein's bridge oscillator I have an op amp and you can see the Wein's bridge component coming here. RC in series and RC in parallel and the output at 1 with reference to 3; 3 is the output voltage of the op amp. 1 is the feedback voltage that is given. Because it is in phase the feedback is given to the plus. Already it is zero. There is no need to provide any additional feedback as in the case of the phase shift network. The output one is directly connected to the plus terminal in the picture and it becomes positive feedback. In the negative side I have used $2R'$ prime and R' prime and I don't know whether you are able to recognize the configuration. I am giving the signal to the non-inverting input and the inverting input is grounded through a resistor R' prime and $2R'$ is the feedback resistance.

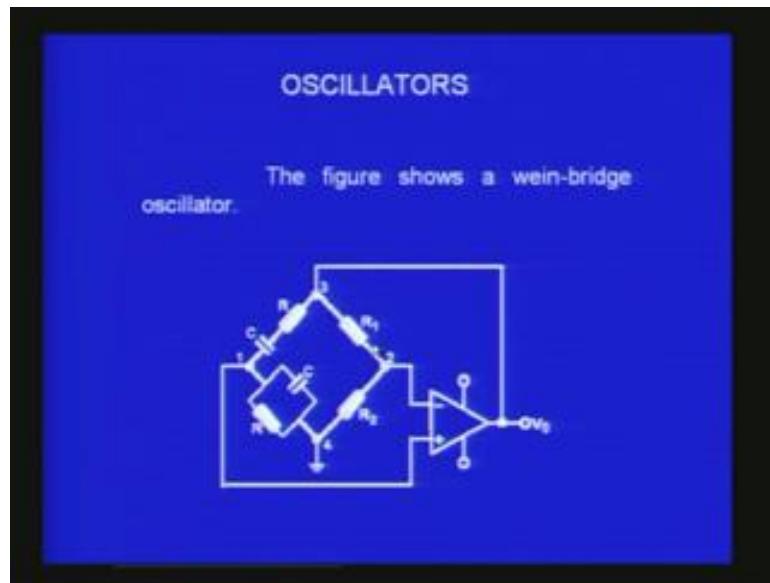
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The gain of this will be 1 plus R_2 by R_1 ; we all know that for non-inverting amplifier. R_2 is $2R'$; so $2R'$ prime by R' prime is 2. 1 + 2 is 3. The gain will be 3. That is what Wein's bridge condition says; the gain should be greater than 3. You also normally have here the resistance which is connected to the inverting input. You don't use normal resistor. You use a tungsten lamp, a small lamp you can put. Why do you put the tungsten lamp? When

the resistance is there the bulb will not glow at all. For the low current that we are going to send the bulb will not glow. But then when the current flows through that it will produce a heat. When the heat is produced the resistance becomes larger due to thermal effect and when the resistance becomes larger it will control the gain. The $2R$ by the R factor will become smaller and it will provide a negative feedback to introduce the stability in the amplifier oscillator and it is normal to use a tungsten lamp here. We will use without the tungsten lamp but one can also use the tungsten lamp and the expression becomes very simple. I have shown the same circuit. It is the same circuit but I have shown it in the form of bridge because we all know the Wheatstone's bridge; this is Wein's bridge.

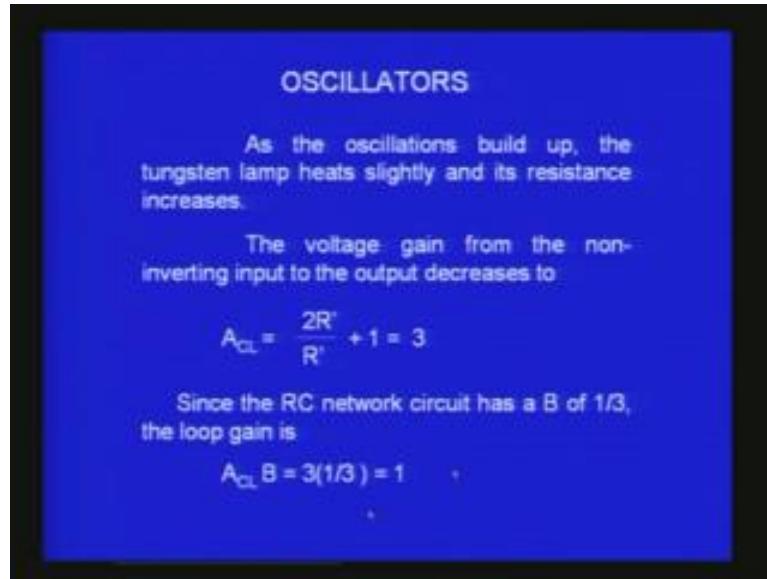
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We have $R_1 R_2$, R and C in series, R and C in parallel forming the four arms of the Wheat stone's bridge and the first two arms are given to the output **on** the ground and the other one is given to the two inputs. This is a Wein's bridge oscillator and it uses positive feedback and also negative feedback for stability and it is a very, very simple circuit to

get oscillations at the output and here again AB should be equal to 1 and that is what I have shown here.

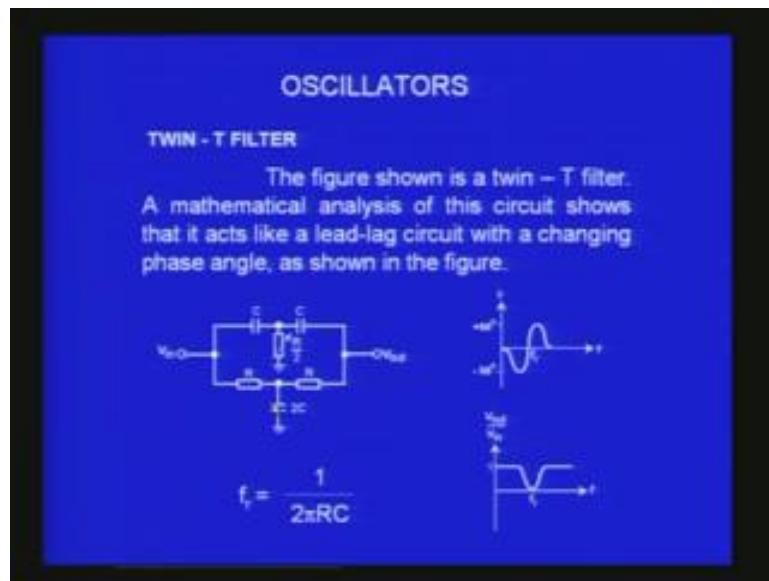
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The closed loop gain is $2R'$ prime by R' plus 1 which is equal to 3 in this case and beta is 1 by 3. 3 into 1 by 3 is 1. That corresponds to Barkhausen's condition.

Let me show you an actual working circuit of the Wein's bridge oscillator. We have seen now two different types of oscillator circuits. One is RC phase shift oscillator the other one is Wein's bridge oscillator. Both are RC oscillators. I want to show you a third type of RC oscillator which is called Twin-T oscillator. It is called Twin-T because there will be two T networks. You have got two capacitors connected in series and one resistor here in the form of a T network. We also see two resistors connected in series and a capacitor is at the stem.

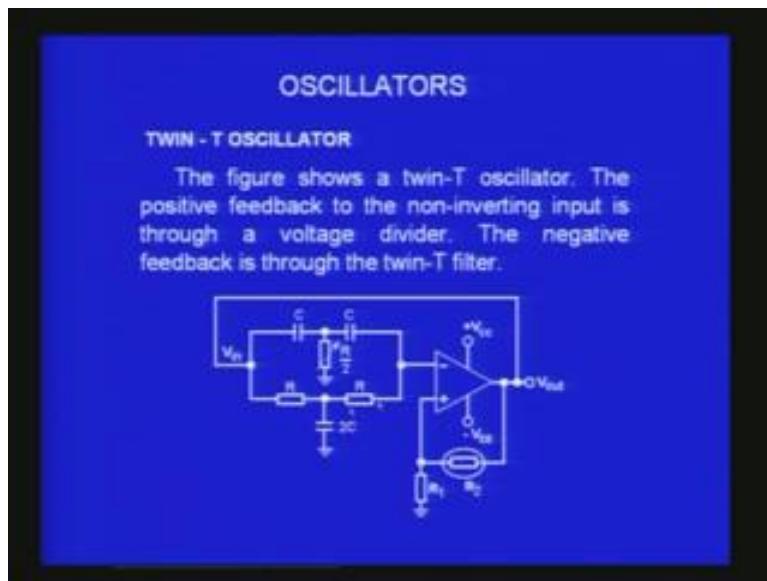
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This is one T. This is another T. Both of them are combined together to form a network. This network is called Twin-T; one T here one T here. Two T's what we called Twin-T. The Twin-T network also like the Wein's network provides zero phase shift. V_{in} is there V output is there. They are in phase for a given frequency. It is a very simple scheme and I have shown here how the phase is varying. For example from zero it goes to maximum - 90 and comes to zero again and goes to +90 and zero. This point where it crosses it gives zero output. It is actually a notch network. It will pass everything else except that frequency. It will not pass at that stage. It gives zero output at this point. V output, V_{in} gain is zero for that particular frequency. Phase is also zero output is also zero and the condition is frequency is $1 / 2\pi RC$. It is very similar to Wein's bridge very simple to construct and this is also a very useful circuit.

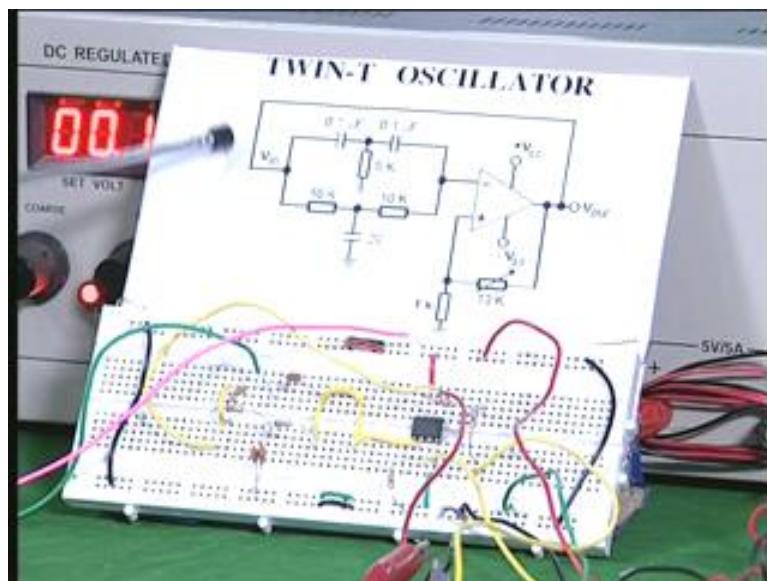
We have formed a simple Wein's bridge network here and the circuit is very similar to what we have done in the case of Wein's bridge. We take the output and give through the twin T network and connect it to the input. This is used in the feedback network with zero phase shift.

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Once you do that you get an oscillator output which is again in the form of sine wave and the values of the capacitor **C** is given here. If the value of the capacitor is C in the T network then in the other network it has to be $2C$ and the resistor R and in the other network it will be R by 2 and you have the twin T network connected having the feedback point of the operational amplifier and you get an output which is corresponding to the twin T oscillator. I will show you the demo. Here I have the circuit of the Twin-T network.

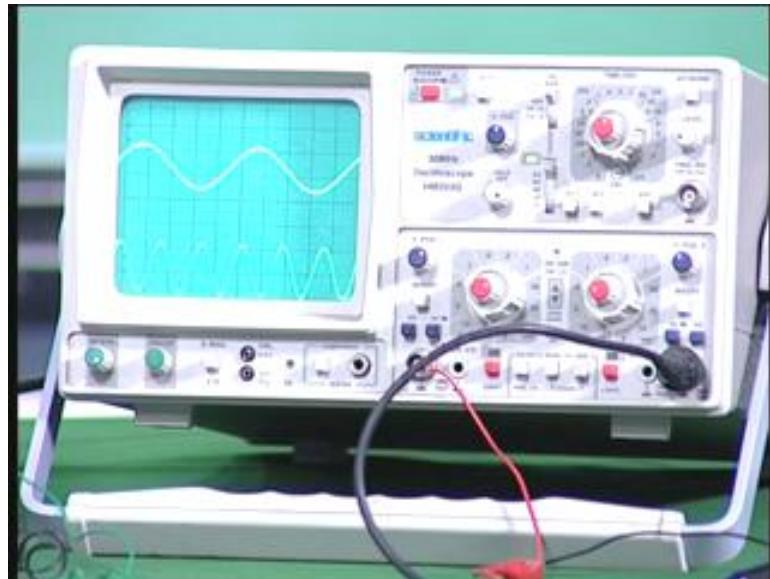
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You can see the one T here one T here. The corresponding circuit is shown with two resistors and one capacitor and the two resistors and one capacitor here. This is the Twin-T network and you have the operational amplifier and one of the resistors here is made as

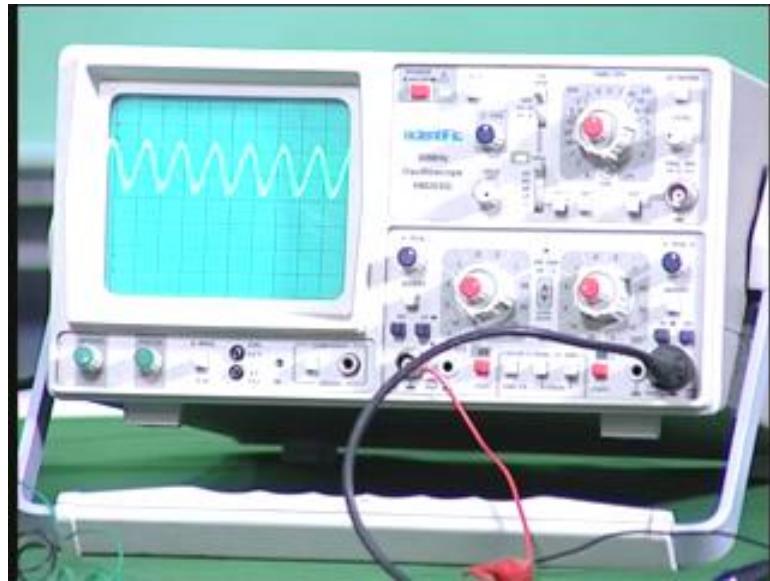
a variable resistor for adjusting the gain and you observe in the oscilloscope the sine wave generated due to the twin-twin network.

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If I vary the potentiometer I will be able to get the oscillations. I have got the two channels for the oscilloscope I have connected this is the output from the oscillator. This is the output from the standard oscillator this is from the circuit and I want to compare the frequencies. I will adjust the frequency to larger values. I keep adjusting the frequency so that they both match. If I coincide them and make them go slowly the two frequencies will almost match. The better way is to use the circle. When I get a circle, Lissajous pattern the frequencies should be matched perfectly. The frequency is about 1.84 kilo hertz for the component that I have used. The two frequencies matched very well even when I put it that way. The values of the resistors are 10K and 0.1 micro farad.

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This is 10K the two resistors and the capacitors are 0.1 microfarad and this will be 2C. That means 2 times 0.1; 0.2 micro farad. Actually parallel capacitors are put there to add and this is 5K. They have put again resistors in parallel to make these 5K or you can use 4.7K. A very simple sinusoidal oscillator can be constructed using Twin-T network.

We have seen in this lecture three different types of oscillator circuits built using op amp. One is the RC phase shift oscillator the other one is Wein's bridge oscillator and the third one is Twin-T network oscillator. All the three are very useful but the most useful among them will be the Wein's bridge because it is much easier to vary the R and C component. You can have ganged resistors and ganged capacitors and most of the oscillators that you get commercially in the low frequencies less than 1 mega hertz are based on Wein's bridge oscillator. Thank you!

UNIT 6

FIELD EFFECT TRANSISTOR

6.1 INTRODUCTION

6.2 CLASSIFICATION OF FET

6.3 CONSTRUCTION AND OPERATION OF N- CHANNEL FET

6.4 CHARACTERISTICS OF N-CHANNEL JFET

6.5 JFET PARAMETERS

6.6 THE FET SMALL SIGNAL MODEL

6.7 MOSFET

6.7.1 DEPLETION MOSFET

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6.8 APPLICATION OF MOSFET

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6.9.2 VOLTAGE DIVIDER BIAS

6.10 JFET AS A VVR OR VDR

UNIT 6

FIELD EFFECT TRANSISTOR

6.1 INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

6.2 CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

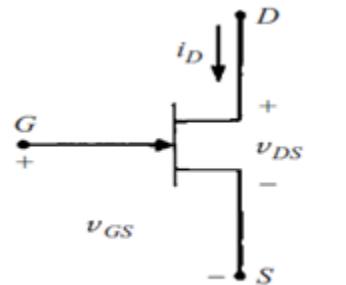
1. Junction Field Effect Transistors
2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

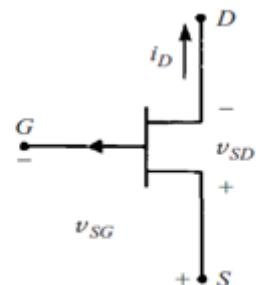
MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.



N-channel FET

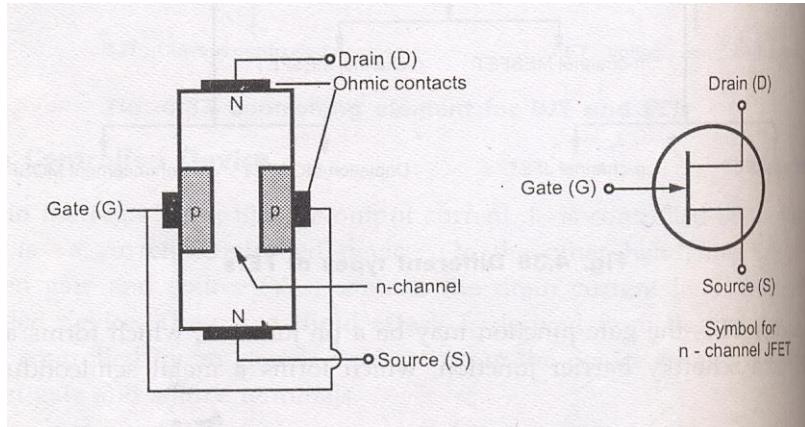


P - channel FET

6.3 CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET



A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source . And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

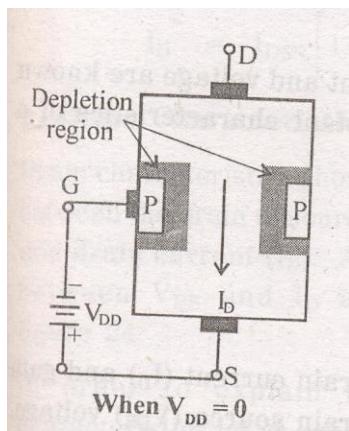
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, forming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current I_D flows. When the gate is biased negative with respect to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and I_D is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and I_D is cut off completely.

There are two ways to control the channel width

1. By varying the value of V_{GS}
2. And by Varying the value of V_{DS} holding V_{GS} constant

1 By varying the value of V_{GS} :-

We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of V_{GS} . This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage V_{GS} connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.

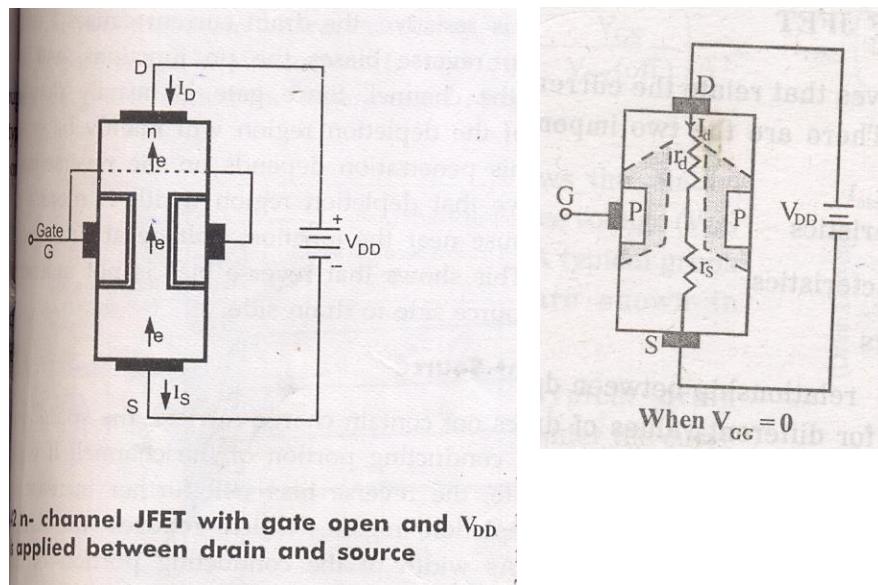


- 1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
- 2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.

- 3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
- 4) So when no V_{ds} is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
- 5) As the reverse bias voltage increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
- 6) By varying the value of V_{gs} we can vary the width of the channel.

2 Varying the value of V_{ds} holding V_{gs} constant :-

- 1) When no voltage is applied to the gate i.e. $V_{gs}=0$, V_{ds} is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current I_d .
- 2) With $V_{gs}= 0$ for $I_d= 0$ the channel between the gate junctions is entirely open .In response to a small applied voltage V_{ds} , the entire bar acts as a simple semi conductor resistor and the current I_d increases linearly with V_{ds} .
- 3) The channel resistances are represented as r_d and r_s as shown in the fig.



- 4) This increasing drain current I_d produces a voltage drop across r_d which reverse biases the gate to source junction,($r_d > r_s$) .Thus the depletion region is formed which is not symmetrical .
- 5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because $V_{rd} \gg V_{rs}$. So reverse bias is higher near drain than at source.
- 6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage V_{ds} is reached at which the channel is pinched off. This is the voltage where the current I_d begins to level off and approach a constant value.
- 7) So, by varying the value of V_{ds} we can vary the width of the channel holding V_{gs} constant.

When both V_{GS} and V_{DS} is applied:-

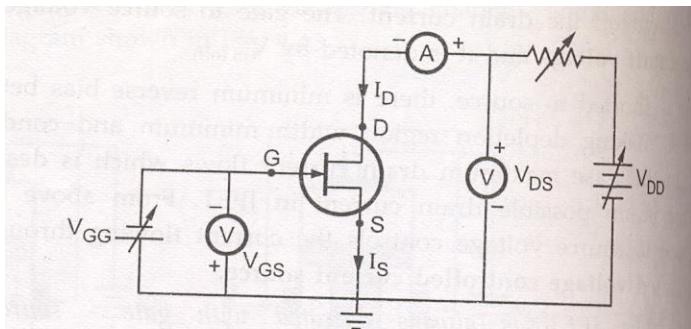
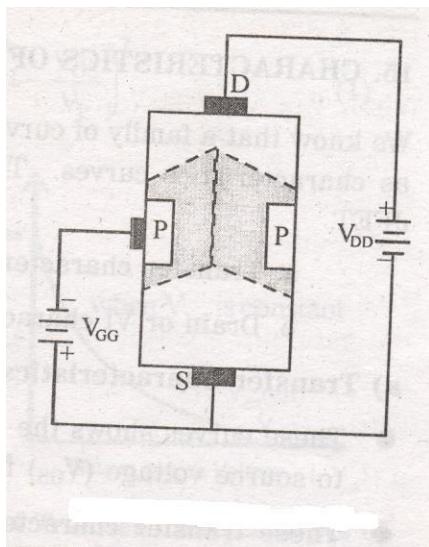


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current I_d to Zero for, if such indeed, could be the case the gate voltage V_{GS} is applied in the direction to provide additional reverse bias

- 1) When voltage is applied between the drain and source with a battery V_{DD} , the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current I_d , its conventional direction is from drain to source.
- 2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by I_{DSS} .



- 3) When V_{GS} is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
- 4) When V_{GS} is further increased a stage is reached at which two depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

6.4 CHARACTERISTICS OF N-CHANNEL JFET :-

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

- 1) Drain or VI Characteristics
- 2) Transfer characteristics

1. Drain Characteristics:-

Drain characteristics shows the relation between the drain to source voltage V_{DS} and drain current I_D . In order to explain typical drain characteristics let us consider the curve with $V_{GS} = 0V$.

- 1) When V_{DS} is applied and it is increasing the drain current I_D also increases linearly up to knee point.
- 2) This shows that FET behaves like an ordinary resistor. This region is called as ohmic region.
- 3) I_D increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

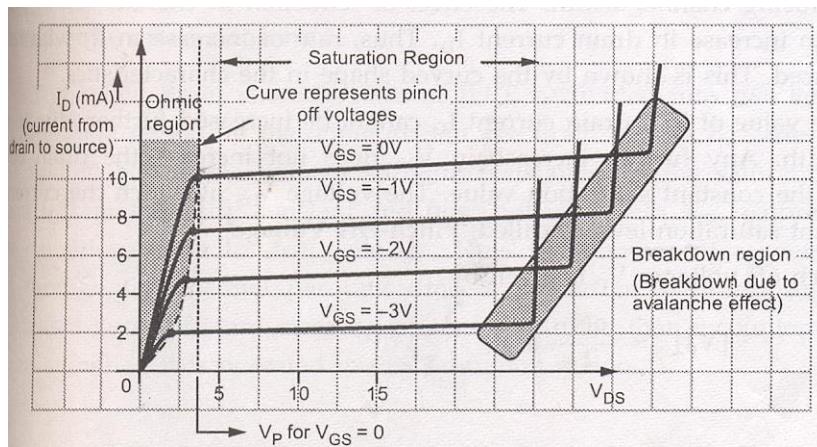


Fig. 4.44 Drain V-I characteristics of n-channel JFET

- 4) It is because of the fact that there is an increase in V_{DS} . This in turn increases the reverse bias voltage across the gate source junction. As a result of this depletion region grows in size thereby reducing the effective width of the channel.
- 5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.
- 6) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(V_p).

PINCH OFF Region:-

- 1) This is the region shown by the curve as saturation region.
- 2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region, the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
- 3) In this drain current remains constant at its maximum value I_{DSS} .
- 4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{DSS} [1 - V_{GS}/V_p]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

- 1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
- 2) It is because of the gate to source junction due to avalanche effect.
- 3) The avalanche break down occurs at progressively lower value of V_{DS} because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction
This causes
 1. The maximum saturation drain current is smaller
 2. The ohmic region portion decreased.
- 4) It is important to note that the maximum voltage V_{DS} which can be applied to FET is the lowest voltage which causes available break down.

2. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current I_D and gate to source voltage V_{GS} for different values of V_{DS} .

- 1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
- 2) Plot the graph between gate to source voltage along the horizontal axis and current I_D on the vertical axis. We shall obtain a curve like this.

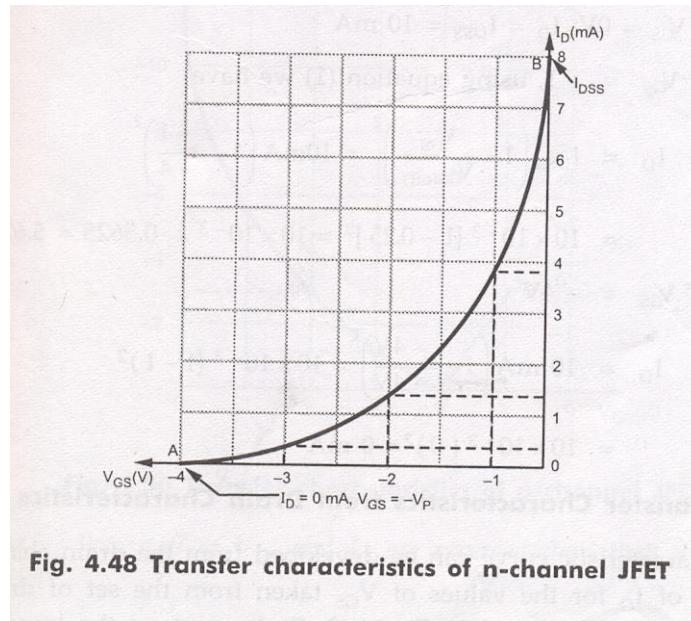


Fig. 4.48 Transfer characteristics of n-channel JFET

- 3) As we know that if V_{GS} is more negative curves drain current to reduce . where V_{GS} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{GS} at the cutoff point is designed as V_{GSOFF}
- 4) The upper end of the curve as shown by the drain current value is equal to I_{DSS} that is when $V_{GS} = 0$ the drain current is maximum.
- 5) While the lower end is indicated by a voltage equal to V_{GSOFF}
- 6) If V_{GS} continuously increasing , the channel width is reduced , then $I_d=0$
- 7) It may be noted that curve is part of the parabola; it may be expressed as

$$I_d = I_{DSS} [1 - V_{GS}/V_{GSOFF}]^2$$

DIFFERENCE BETWEEN V_p AND V_{GSOFF} –

V_p is the value of V_{gs} that causes the JFET to become constant current component, It is measured at $V_{gs} = 0V$ and has a constant drain current of $I_d = I_{dss}$. Where V_{gsoff} is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET 's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

6.5 JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region. It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage V_{gs} .

Mathematically it is expressed as $r_d = \Delta V_{ds} / \Delta I_d$ where V_{gs} is held constant.

TRANSE CONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m = \Delta I_d / \Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu = \Delta V_{ds}/\Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m) and ac drain resistance (r_d)

$$\mu = \Delta V_{ds}/\Delta V_{gs} = g_m r_d$$

6.6 THE FET SMALL SIGNAL MODEL:-

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current i_d as a function f of the gate voltage and drain voltage V_{ds} .

$$I_d = f(V_{gs}, V_{ds}) \text{-----(1)}$$

The transconductance g_m and drain resistance r_d :-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylor's series considering only the first two terms in the expansion

$$\Delta i_d = \frac{\partial i_d}{\partial V_{gs}} |_{V_{ds}=\text{constant}} \Delta V_{gs} + \frac{\partial i_d}{\partial V_{ds}} |_{V_{gs}=\text{constant}} \Delta V_{ds}$$

we can write $\Delta i_d = i_d$

$$\Delta V_{gs} = V_{gs}$$

$$\Delta V_{ds} = V_{ds}$$

$$I_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \rightarrow (1)$$

$$\text{Where } g_m = \frac{\partial i_d}{\partial V_{gs}} |_{V_{ds}} \cong \frac{\Delta i_d}{\Delta V_{gs}} |_{V_{ds}}$$

$$g_m = \frac{i_d}{V_{gs}} |_{V_{ds}}$$

Is the mutual conductance or transconductance .It is also called as gfs or yfs common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d = \frac{\partial V_{ds}}{\partial i_d} \Big|_{V_{gs}} \cong \frac{\Delta V_{ds}}{\Delta i_d} \Big|_{V_{gs}} = \frac{V_{ds}}{i_d} \Big|_{V_{gs}}$$

$$r_d = \frac{V_{ds}}{i_d} \Big|_{V_{gs}}$$

The reciprocal of the r_d is the drain conductance g_d . It is also designated by Yos and Gos and called the common source output conductance. So the small signal equivalent circuit for FET can be drawn in two different ways.

- 1.small signal current –source model
- 2.small signal voltage-source model.

A small signal current –source model for FET in common source configuration can be drawn satisfying Eq \rightarrow (1) as shown in the figure(a)

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to –source voltage. The proportionality factor is the transconductance ' g_m '. The output resistance is ' r_d '. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

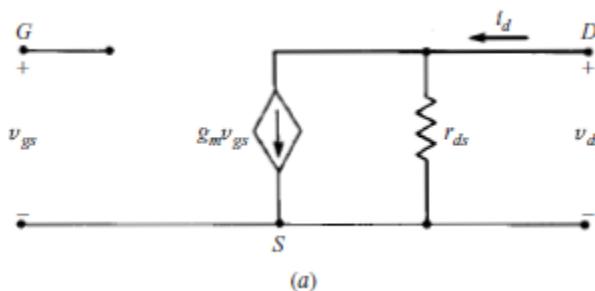
The small signal voltage-source model is shown in the figure(b).

This can be derived by finding the Thevenin's equivalent for the output part of fig(a) .

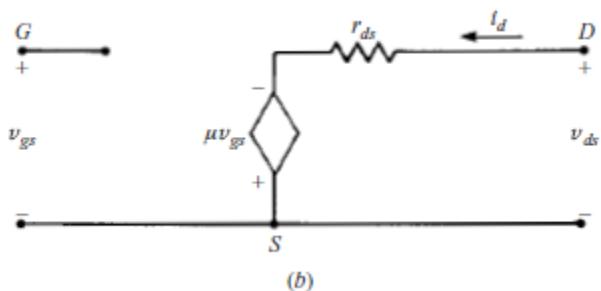
These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

- 1.common source (CS) 2.common drain (CD) or source follower
3. common gate(CG).

(a)Small Signal Current source model for FET



(b)Small Signal voltage source model for FET

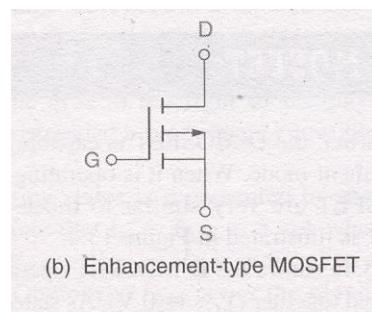
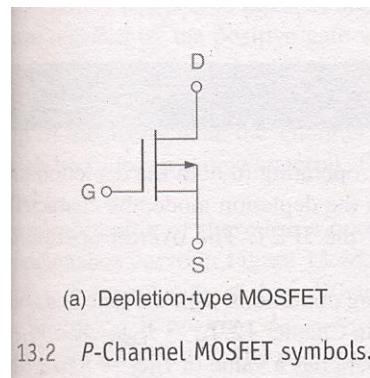


Here the input circuit is kept open because of having high input impedance and the output circuit satisfies the equation for I_D

6.7 MOSFET:-

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.



(a) Depletion type MOSFET

(b) Enhancement type MOSFET

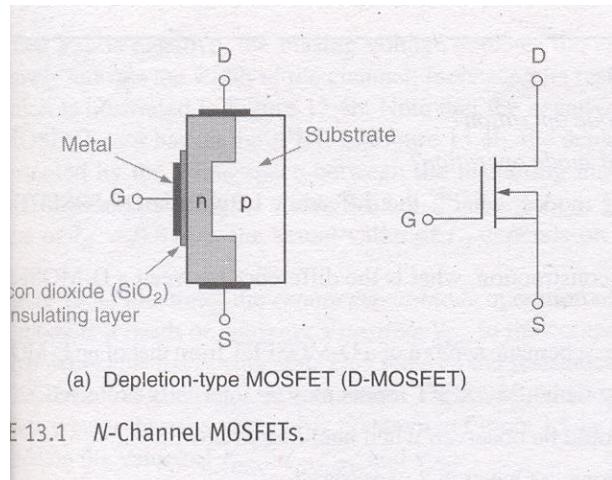
Both of them are P- channel

Here are two basic types of MOSFETS

- (1) Depletion type (2) Enhancement type MOSFET.

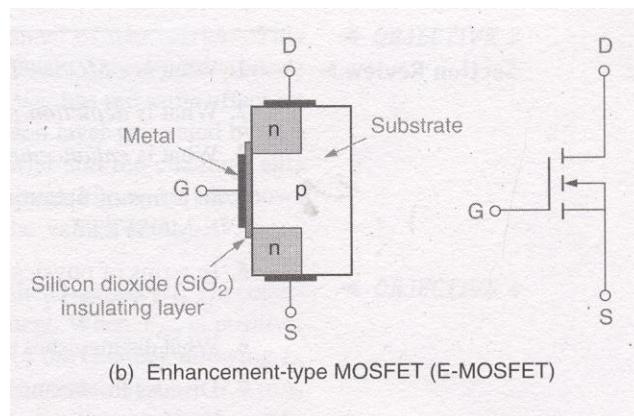
D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

The construction difference between the two is shown in the fig given below.



E 13.1 N-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SiO_2 a glass like insulating material. The gate material is made up of metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:-

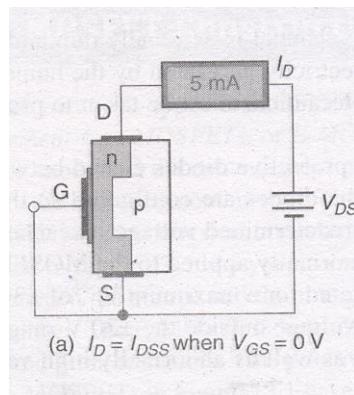
The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain.

A thin layer of insulation silicon dioxide (SiO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of SiO_2

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10¹⁰ to 10¹⁵ ohms) for MOSFET.

6.7.1 DEPLETION MOSFET

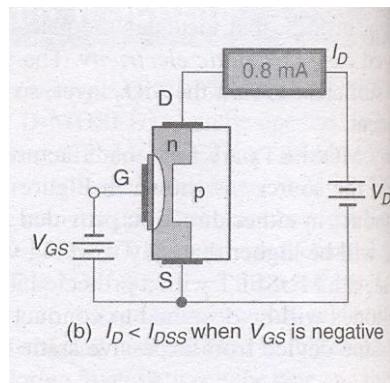
The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current I_{DSS} flows for zero gate to source voltage, $V_{GS}=0$.



Depletion mode operation:-

- 1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together($V_{GS}=0V$)
- 2) At this stage $I_D=I_{DSS}$ where $V_{GS}=0V$, with this voltage V_{DS} , an appreciable drain current I_{DSS} flows.

- 3) If the gate to source voltage is made negative i.e. V_{GS} is negative .Positive charges are induced in the channel through the SiO_2 of the gate capacitor.
- 4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as V_{GS} is made more negative.
- 5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.
- 6) That means biasing voltage V_{GS} depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.
- 7) Note that negative V_{GS} has the same effect on the MOSFET as it has on the JFET.



- 8) As shown in the fig above, the depletion layer generated by V_{GS} (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result , $I_D < I_{DSS}$.The actual value of I_D depends on the value of I_{DSS} , $V_{GS}(\text{off})$ and V_{GS} .

Enhancement mode operation of the D-MOSFET:-

- 1) This operating mode is a result of applying a positive gate to source voltage V_{GS} to the device.
- 2) When V_{GS} is positive the channel is effectively widened. This reduces the resistance of the channel allowing I_D to exceed the value of I_{DSS}
- 3) When V_{GS} is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.
- 4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
- 5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
- 6) The extended n type channel now allows more current, $I_D > I_{DSS}$

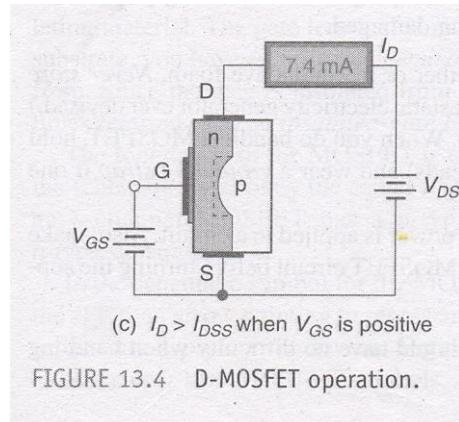
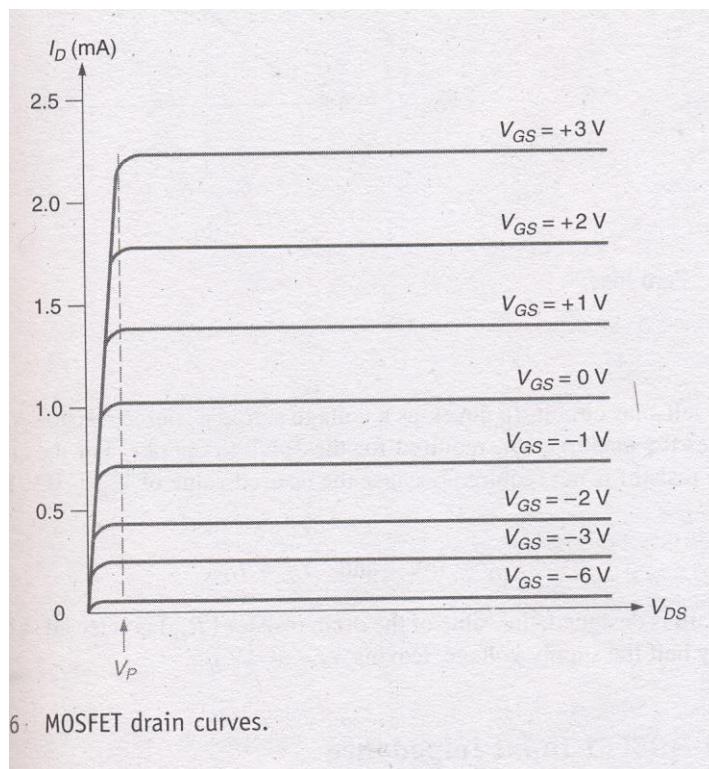


FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

The fig. shows the drain characteristics for the N channel depletion type MOSFET

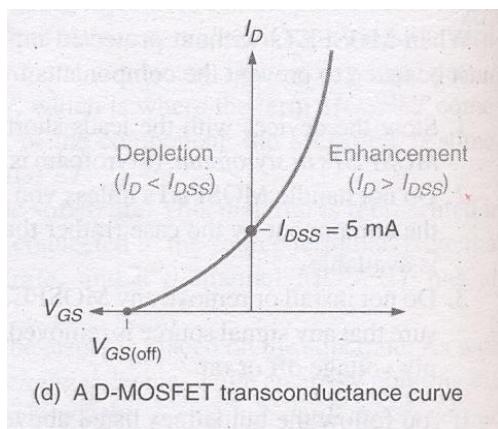
- 1) The curves are plotted for both V_{GS} positive and V_{GS} negative voltages
- 2) When $V_{GS}=0$ and negative the MOSFET operates in depletion mode when V_{GS} is positive ,the MOSFET operates in the enhancement mode.
- 3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of V_{GS} .
- 4) When $V_{DS}=0$, there is no conduction takes place between source to drain, if $V_{GS}<0$ and $V_{DS}>0$ then I_D increases linearly.
- 5) But as $V_{GS},0$ induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. I_D is constant.
- 6) If $V_{GS}>0$ the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6. MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. $V_{GS}=0\text{V}$, $V_{GS}<0\text{V}$, $V_{GS}>0\text{V}$ is represented by the D MOSFET transconductance curve shown in Fig.

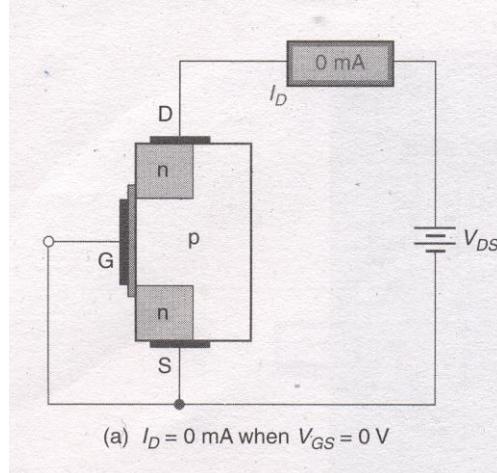


- 1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.
- 2) This curve extends for the positive values of V_{GS}

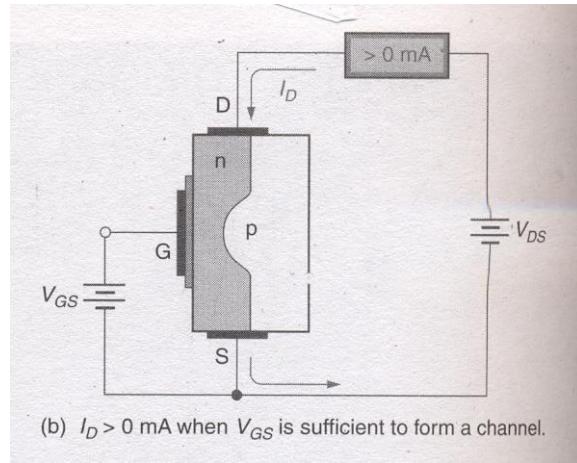
- 3) Note that $I_d = I_{dss}$ for $V_{gs} = 0V$ when V_{gs} is negative, $I_d < I_{dss}$ when $V_{gs} = V_{gs(off)}$, I_d is reduced to approximately $0mA$. Where V_{gs} is positive $I_d > I_{dss}$. So obviously I_{dss} is not the maximum possible value of I_d for a MOSFET.
- 4) The curves are similar to JFET so that the D MOSFET have the same transconductance equation.

6.7.2 E-MOSFETS

The E MOSFET is capable of operating only in the enhancement mode. The gate potential must be positive w.r.t to source.



- 1) when the value of $V_{gs}=0V$, there is no channel connecting the source and drain materials.
- 2) As a result, there can be no significant amount of drain current.
- 3) When $V_{gs}=0$, the V_{dd} supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at $V_{gs}=0$,
- 4) If V_{gs} is positive, it induces a negative charge in the p type substrate just adjacent to the SiO_2 layer.
- 5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for drain current.
- 6) This +ve gate voltage forms a channel between the source and drain.
- 7) This produces a thin layer of N type channel in the P type substrate. This layer of free electrons is called N type inversion layer.



- 8) The minimum V_{GS} which produces this inversion layer is called threshold voltage and is designated by $V_{GS(th)}$. This is the point at which the device turns on is called the threshold voltage $V_{GS(th)}$
- 9) When the voltage V_{GS} is $< V_{GS(th)}$ no current flows from drain to source.
- 10) However when the voltage $V_{GS} > V_{GS(th)}$ the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E MOSFET:-

1. DRAIN CHARACTERISTICS

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the

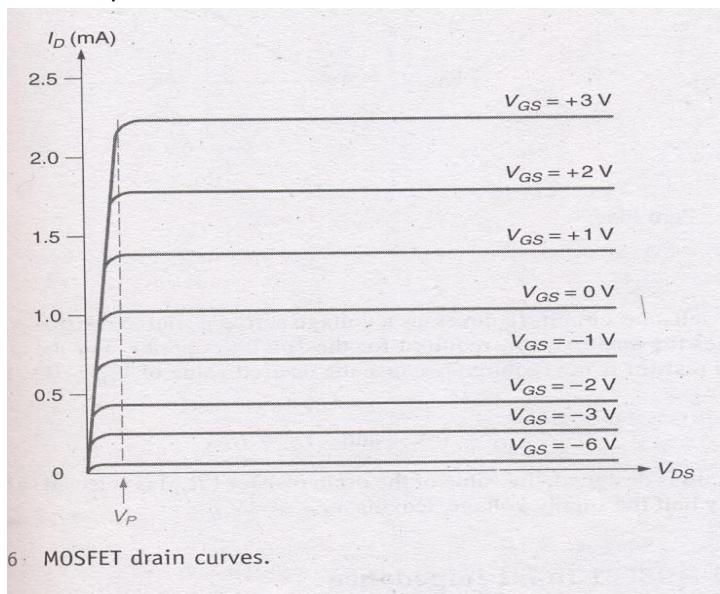


fig.

2. TRANSFER CHARACTERISTICS:-

- 1) The current I_{DSS} at $V_{GS} \leq 0$ is very small being of the order of a few nano amps.
- 2) As V_{GS} is made +ve , the current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS} .
- 3) The standard transconductance formula will not work for the E MOSFET.
- 4) To determine the value of I_D at a given value of V_{GS} we must use the following relation

$$I_D = K [V_{GS} - V_{GS(Th)}]^2$$

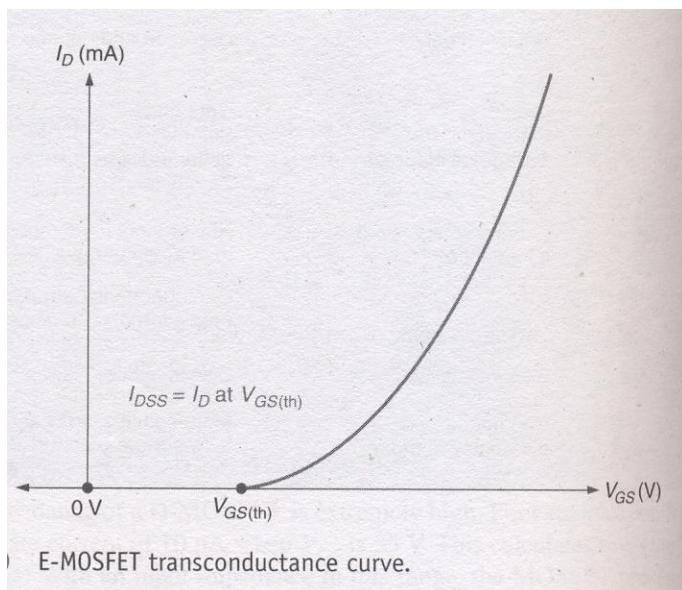
Where K is constant for the MOSFET . found as

$$K = \frac{I_D(\text{on})}{[V_{GS(\text{on})} - V_{GS(\text{Th})}]^2}$$

From the data specification sheets, the 2N7000 has the following ratings.

$I_D(\text{on}) = 75\text{mA}(\text{minimum})$.

And $V_{GS(\text{th})}=0.8\text{(minimum)}$



6.8 APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

6.9 BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage V_{GS} and drain current I_D which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

- 1) Self bias
- 2) Voltage divider bias.

6.9.1 SELF BIAS

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate. A self bias circuit is shown in the fig. Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative V_{GS} for an N channel JFET and a positive V_{GS} for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig. The gate resistor R_G doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V . R_G is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor R_S makes gate source junction reverse biased.

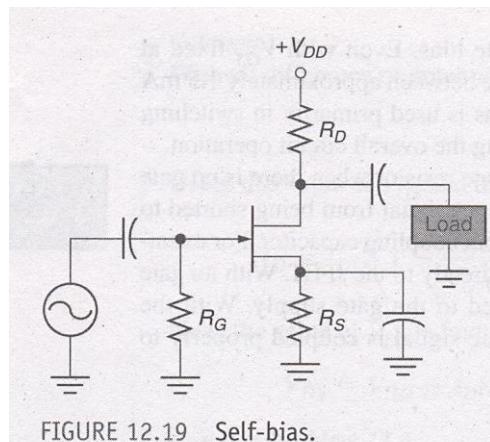


FIGURE 12.19 Self-bias.

For the dc analysis coupling capacitors are open circuits.

For the N channel FET in Fig (a)

I_s produces a voltage drop across R_s and makes the source positive w.r.t ground. In any JFET circuit all the source current passes through the device to the drain circuit. This is due to the fact that there is no significant gate current.

We can define source current as $I_s = I_D$

($V_G = 0$ because there is no gate current flowing in R_G So V_G across R_G is zero)

$$V_G = 0 \text{ then } V_s = I_s R_s = I_D R_s$$

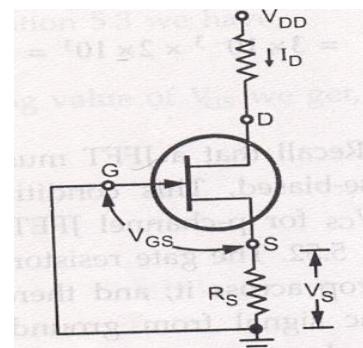
$$V_{GS} = V_G - V_s = 0 - I_D R_s = -I_D R_s$$

DC analysis of self Bias:-

In the following DC analysis, the N channel J FET shown in the fig. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent. $\therefore I_G = 0$. The relation between I_D and V_{GS} is given by

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$



V_{GS} for N channel JFET is $= -I_D R_s$

Substituting this value in the above equation

$$I_D = I_{DSS} \left[1 - \frac{(-I_D R_s)}{V_P} \right]^2$$

$$I_D = I_{DSS} \left[1 + \frac{(I_D R_s)}{V_P} \right]^2$$

For the N-channel FET in the above figure

I_s produces a voltage drop across R_s and makes the source positive w.r.t ground in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current. Therefore we can define source current as $I_s = I_d$ and $V_g = 0$ then

$$V_s = I_s R_s = I_d R_s$$

$$V_{gs} = V_g - V_s = 0 - I_d R_s = -I_d R_s$$

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

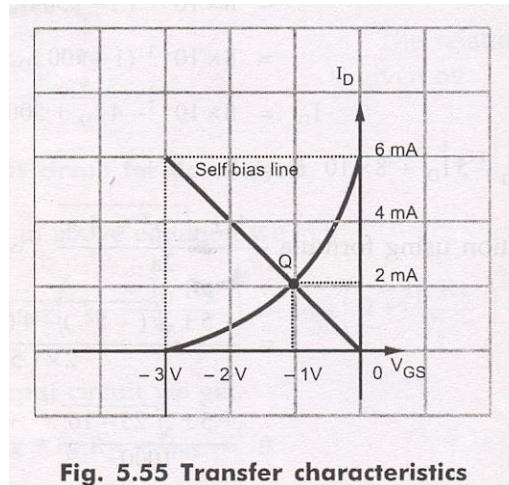


Fig. 5.55 Transfer characteristics

Now using the equation $V_{GS} = -I_d R_s$ and assuming R_s of any suitable value we can draw the self bias line.

Let us assume $R_s = 500\Omega$

With this R_s , we can plot two points corresponding to $I_d = 0$ and $I_d = I_{DSS}$

for $I_d = 0$

$$V_{GS} = -I_d R_s$$

$$V_{GS} = 0 \times (500\Omega) = 0V$$

So the first point is $(0, 0)$

$$(I_d, V_{GS})$$

For $I_D = I_{DSS} = 6\text{mA}$

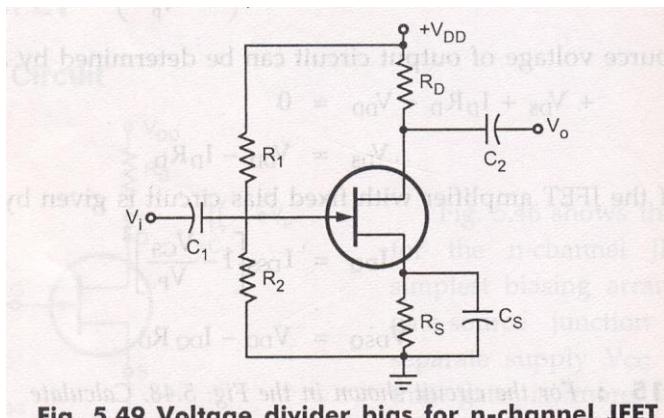
$$V_{GS} = (-6\text{mA}) (500 \Omega) = -3\text{V}$$

So the 2nd Point will be (6mA, -3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point, the I_D is slightly $>$ than 2mA and V_{GS} is slightly $>$ -1V. The Q point for the self bias JFET depends on the value of R_S . If R_S is large, Q point far down on the transconductance curve, I_D is small, when R_S is small Q point is far up on the curve, I_D is large.

6.9.2 VOLTAGE DIVIDER BIAS:-



The fig. shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula.

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

For dc analysis

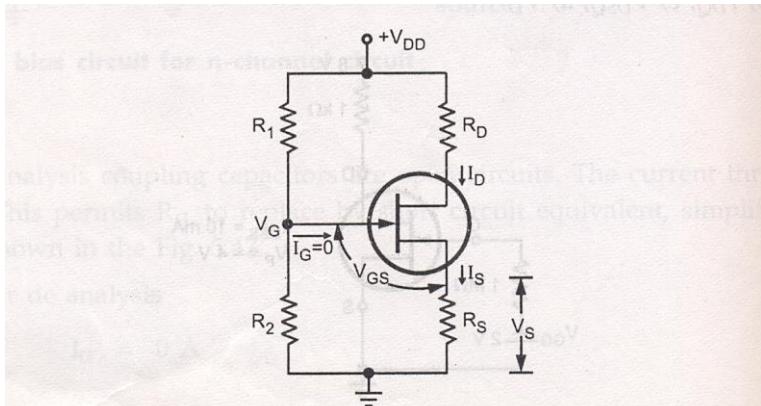


Fig. 5.50 Simplified voltage divider circuit for dc analysis

Applying KVL to the input circuit

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$V_{GS} = V_G - I_D R_S \quad \therefore I_S = I_D$$

Applying KVL to the input circuit we get

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

The Q point of a JFET amplifier, using the voltage divider bias is

$$I_{DQ} = I_{DSS} [1 - V_{GS}/V_P]^{1/2}$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

COMPARISON OF MOSFET WITH JFET

- a. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel.
- b. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.

- c. The gate leakage current in a MOSFET is of the order of 10^{-12}A . Hence the input resistance of a MOSFET is very high in the order of 10^{10} to $10^{15}\Omega$. The gate leakage current of a JFET is of the order of 10^{-9}A , and its input resistance is of the order of $10^8\Omega$.
- d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to $1\text{M}\Omega$) is much higher than that of a MOSFET (1 to $50\text{k}\Omega$).
- e. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.
- f. Comparing to JFET, MOSFETs are easier to fabricate.
- g. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makes them suitable for portable systems.