**Electronics Lab Manual**

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**Analog**

1. CRO Familiarization with voltage, time and frequency measurements.
2. To study the V-I characteristics of a PN junction diode and Zener diode.
3. To study the operation of diode rectifier circuits & draws its input/output wave shape.

4.To study the operation of clipper and clamper circuits using PN junction diode and draw wave shape of given circuits.

5.Plot the output characteristics of a BJT in Common Emitter Configuration.

**Digital**

1. Familiarization with following:

a. Digital Kit.

b. Identifying Basic Logic Gate ICs and their pin configurations.

c. Verifying truth tables of basic logic gates (AND, OR, NOT, NAND, NOR, X-OR).

1. Implementation of Boolean function using basic logic gates. Truth table of given Boolean function is to be generated and then verified by reducing the Boolean function using rules of Boolean Algebra.

8. Implementation of Half Adder using

a. Using AOI logic (AND, OR & NOT)

b. Using any gate (XOR & AND)

c. Using minimum number of NAND gates.

9. Implementation of a Full Adder using Multiplexer and Decoder IC’s and verify

their truth tables.

10. Construct and study behaviour of following Latches/Flip-Flops:

1. SR Latch using NAND & NOR gates.

2. Convert NAND & NOR based SR Latch to Gated Latches.

3. Convert Gated SR Latch to D Flip-Flop.

**Experiment – 1**

**Aim:** CRO Familiarization with voltage, time and frequency measurements.

**Apparatus:** CRO, Function generator, BNC cable (CRO probe).

**Theory:**

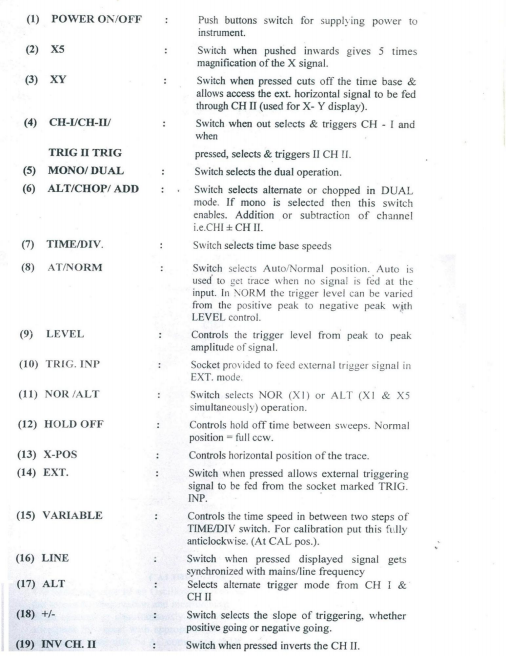
**CRO**

C.R.O. (Cathode Ray Oscilloscope) is the instrument which is used to observe signal  waveforms. Signals are displayed in time domain i.e. variation in amplitude of the signal with  respect to time is plotted on the CRO screen. X-axis represents time and Y-axis represents  amplitude. It is used to measure amplitude, frequency and phase of the waveforms. It is also  used to observe the shape of the waveform. C.R.O. is useful for troubleshooting purpose.  It helps us to find out the gain of amplifier, test oscillator circuits. We can measure amplitude  and frequency of the waveforms at the different test points in our circuit. Thus, it helps us  with fault finding procedures. In dual channel C.R.O. X-Y mode is available which is used to  create Lissajous patterns.

**DSO**

Latest digital storage oscilloscope (DSO) display voltage and frequency directly on the  LCD and does not require any calculations. It can also store waveform for further analysis. In  this practical, we will measure amplitude and frequency of the different waveforms like sine  wave, square wave, and triangular wave.

**Pin description of CRO**

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**Observations:**

**For Voltage measurement:**

Vp-p = (No. vertical Div.) X (Volt/Div.) Time = (No. Horizontal Div.) X (Time/Div.)

i) Frequency Set: 1.027 Hz/time= No. of horizontal div\* Time/Div

Amplitude set= 5V

= Measuring time=2.1(horizontal division)

scale=0.5 us

f=1/T=1/(2.1)(0.5)\*10^6=0.95 Hz

Therefore, error=1.027-0.95=0.077 Hz

=Measuring voltage=4.6V(vertical div)

scale=1

A(obs)=4.6\*1

Therefore, error=5-4.6=0.4

ii) Frequency Set= 100kHz

Amplitude set=7V

=measurement time=2.1(horizontal div)

scale=5us

t=2.1\*5us

f=1/T=95.2kHz

error=4.8

=measured voltage=3.4V(vertical div)

scale =2

A=3.4\*2=6.8

error=0.2

**Experiment – 2**

**Aim**: To study the V-I characteristics of a PN junction diode.

**Apparatus required**:

Items Quantity

PN junction Diode (IN4001) 1

DC variable power supply 1

Multimeter 2

Breadboard 1

Jumper wires As per requirement

**Theory:**

**P-N junction diode :**

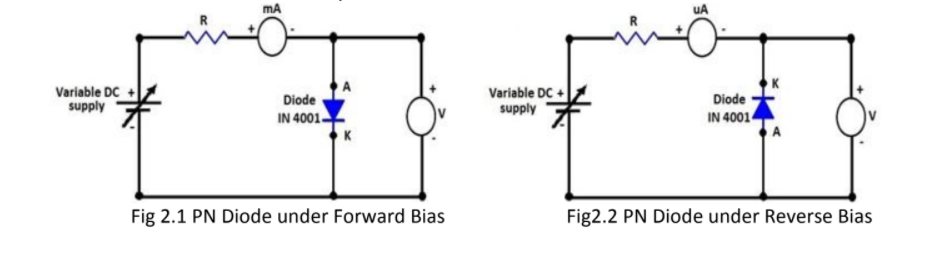
A PN Junction Diode is one of the simplest semiconductor devices around, and which has the characteristic of passing current in only one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential voltage-current (V-I) relationship and therefore we cannot described its operation by simply using an equation such as Ohm’s law.

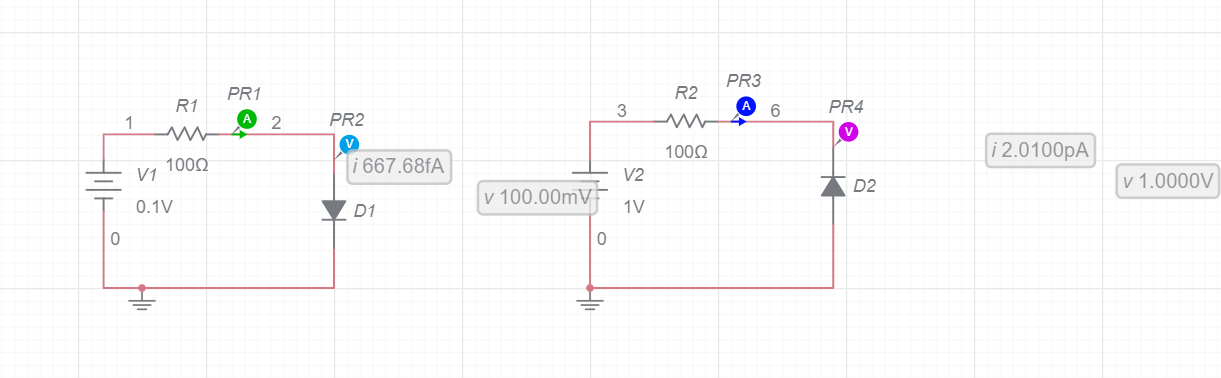
**Forward bias**

Under forward biased condition of a real PN junction diode, the P-side is connected to the positive and N side is connected to the negative terminal of the power supply. This reduces the potential barrier. As a result, current flows from P to N-type in forward direction. When the applied voltage is more than the barrier potential, the resistance is small (ideally 0) and the current increases rapidly. This point is called the Knee-point or turn-on voltage or threshold voltage (Figure 2.3). This voltage is about 0.3 volts for Ge diodes and 0.7 volts for Si diodes.

**Reverse bias**

Under reverse bias condition, the P side of the junction diode is connected to the negative and N-side is connected to the positive terminal of the power supply. This increases the potential barrier due to which no current should flow ideally. But in practice, the minority carriers can travel down the potential barrier to give very small current. This is called as the reverse saturation current. This current is about 2-20 uA for Ge diodes and 2-20 nA for Si diodes (the values might differ for diodes of different makes). When the applied reverse voltage is increased beyond the certain limit, it results in breakdown. During breakdown, the diode current increases tremendously

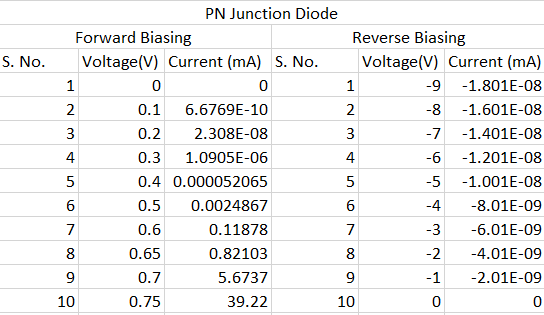


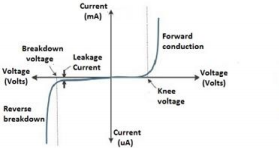


**Observations:**

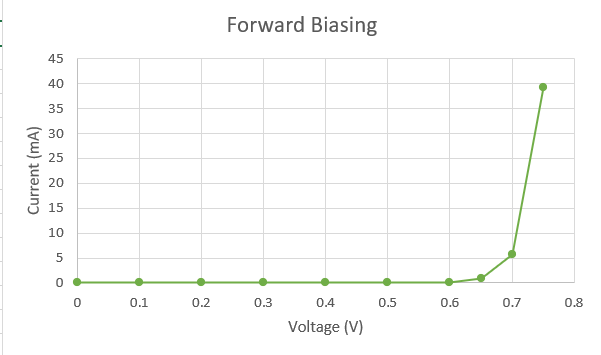
Diode used in circuit is PN junction diode.

**Forward biasing and Reverse Biasing:**

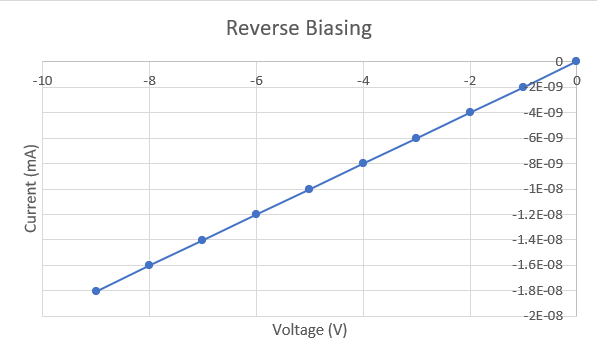
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**Graph for forward bias**



**Graph for reverse bias:**

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**Result:**

The V-I curve shows that only a very small current flows through the diode during initial

stage till the potential barrier is wiped-off. Once the potential barrier is wiped off (i.e.at the

knee voltage), the current rises quickly.

**Precautions:**

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage

of the diode.

2. Always connect the voltmeter in parallel and Ammeter in series as shown in figure2.2.

3. Switch “ON’’ the power supply after completing the circuit.

**Experiment - 2**

**AIM:** To study the V-I characteristics of a Zener diode.

**Apparatus:**

Items Quantity

Zener diode 1

DC variable power supply 1

Multimeter 2

Breadboard 1

Jumper wires as per requirement

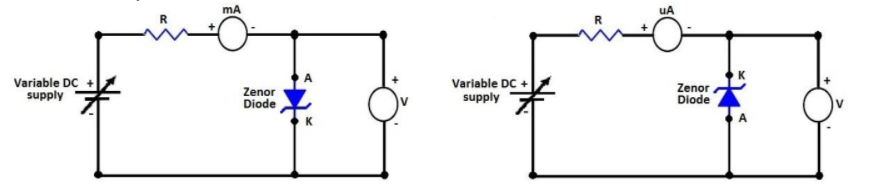
**THEORY:** Zener Diode A Zener Diode is a special kind of diode which permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or ‘zener’ voltage. Zener diodes are designed so that their breakdown voltage is much lower, for example just 2.4 Volts.

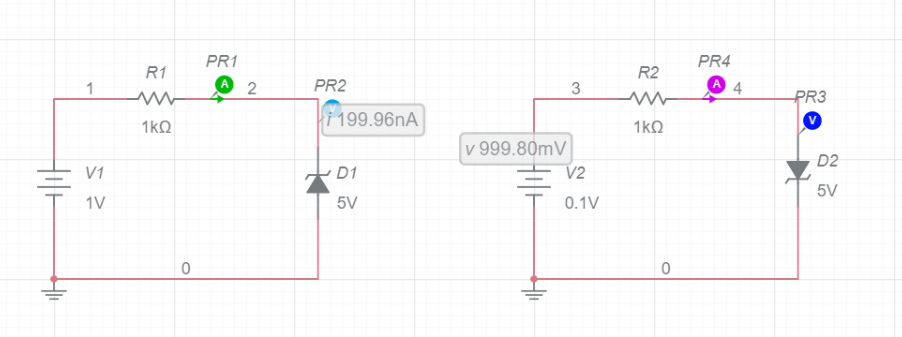
Zener Effect Normally, PN junction of Zener Diode is heavily doped. Due to heavy doping the depletion layer will be narrow. When the reverse bias is increased the potential across the depletion layer is more. This exerts a force on the electrons in the outermost shell. Because of this force the electrons are pulled away from the parent nuclei and become free electrons. This ionization, which occurs due to electrostatic force of attraction, is known as Zener effect. It results in large number of free carriers, which in turn increases the reverse saturation current.

Forward bias with a zener diode connected in the forward direction, it behaves exactly the same as a standard diode - i.e. a small voltage drop of 0.3 to 0.7V with current flowing through pretty much freely.

Reverse bias

When a reverse current above the Zener voltage passes through a Zener diode, there is a controlled breakdown which does not damage the diode. The voltage drop across the Zener diode is equal to the Zener voltage of that diode no matter how high the reverse bias voltage is above the Zener voltage. In the reverse direction however there is a very small leakage current between 0v and the Zener voltage. When the voltage reaches the breakdown voltage (Vz), suddenly current can flow through it.

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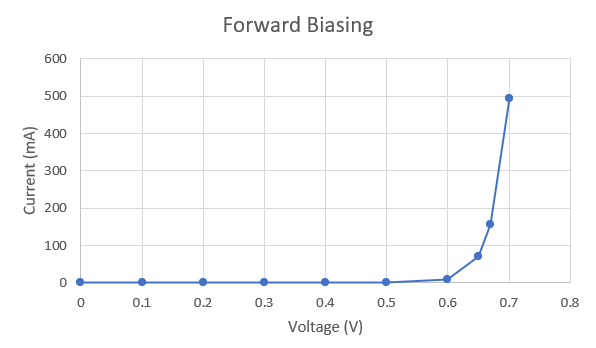
**Observations:** Diode used in circuit is zener diode.

**Forward biasing and Reverse biasing:**

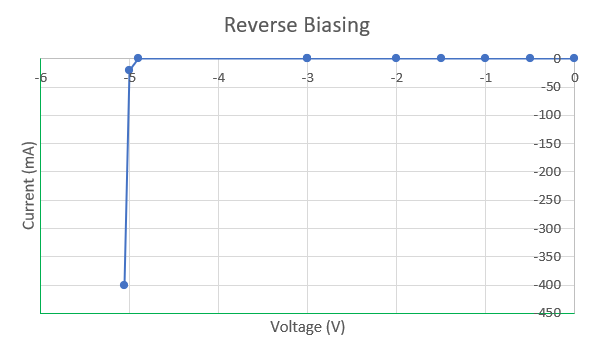
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**Graph for forward bias :**

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**Graph for reverse bias:**

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**Result:**

The V-I curve shows that before breakdown voltage, the increase in the current with the increase in voltage is very small, current flows in the circuit in uA. But once the breakdown voltage reaches, the current rises abruptly.

**Experiment – 3**

**Aim :** To study the operation of diode rectifier circuits & draws its input/output wave shape.

**Apparatus required**:

Items Quantity

PN junction Diode (IN4007) 4

Step down transformer (Centre tap) 1

Breadboard 1

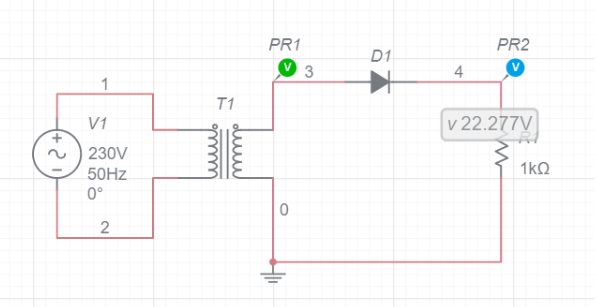
DSO/CRO 1

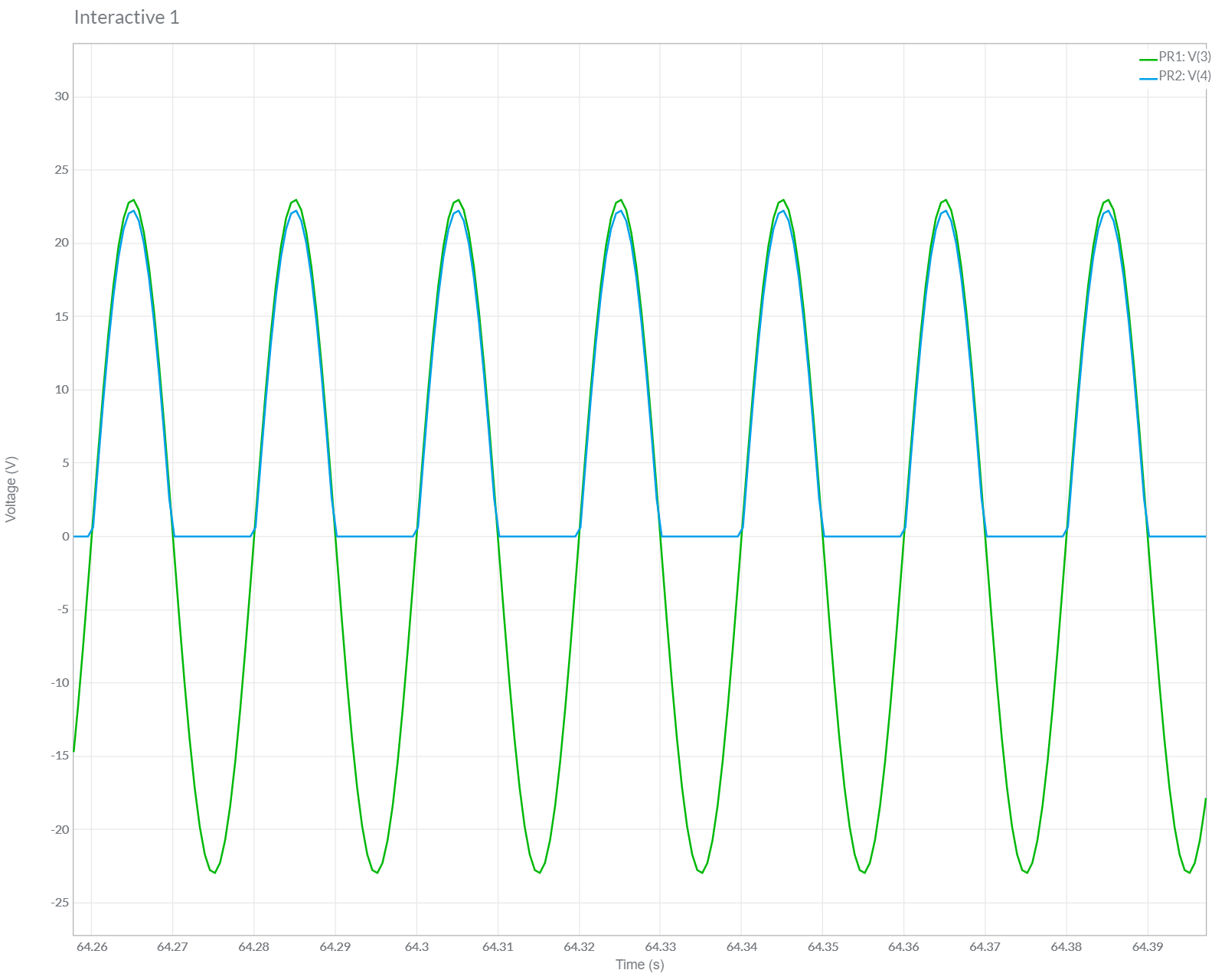
AC voltage source 1

Resistors/ Capacitor as per circuit diagram

Jumper wires as per requirement

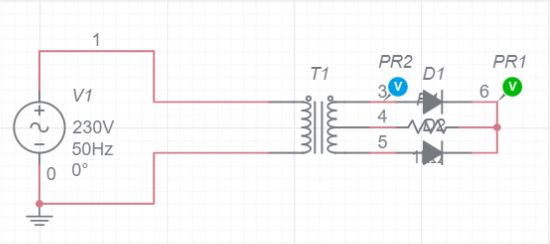
**Half Wave Rectifier:**

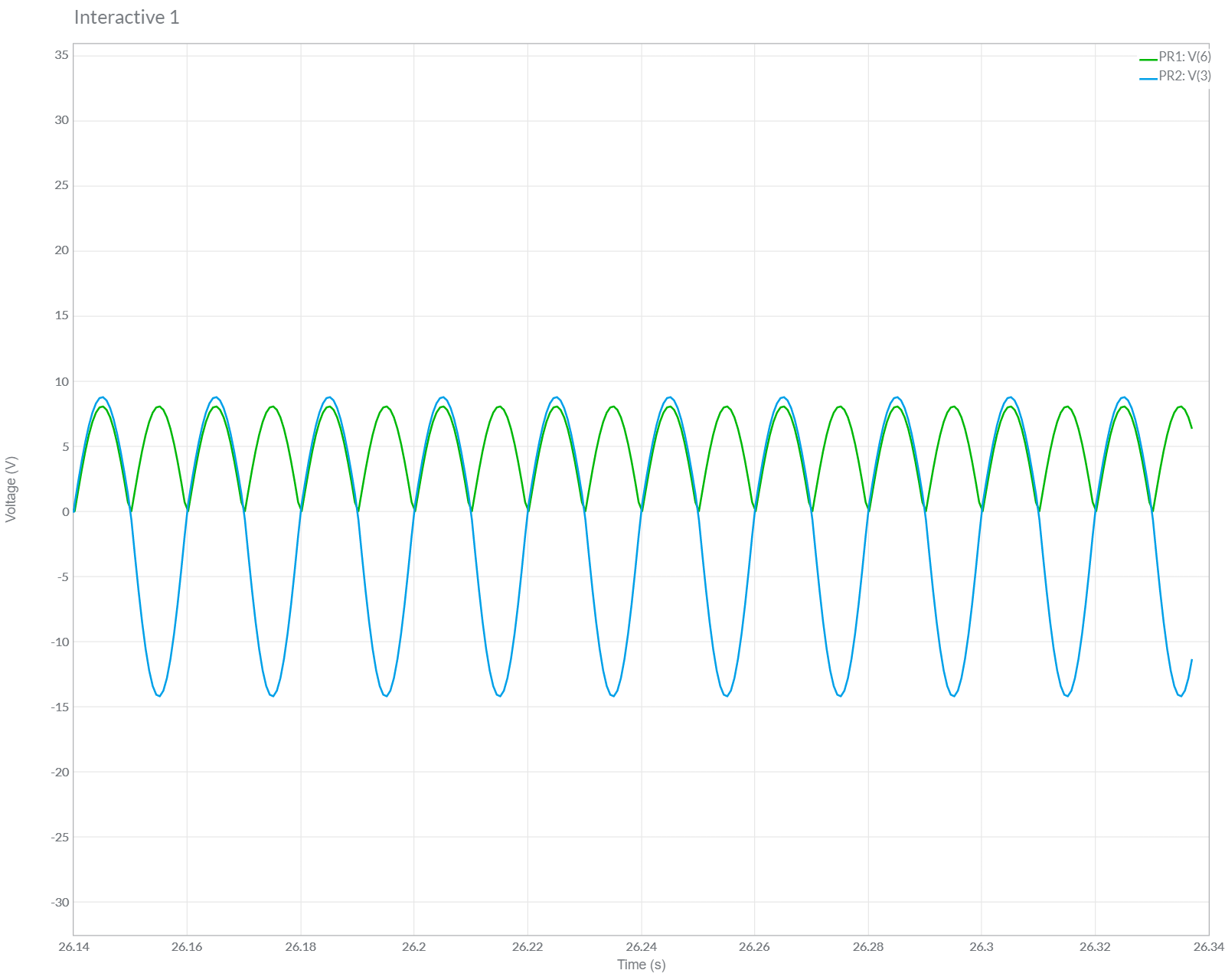
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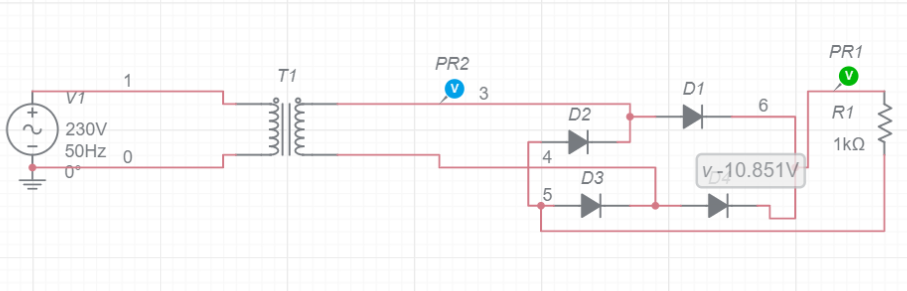
**Full Wave Rectifier:**

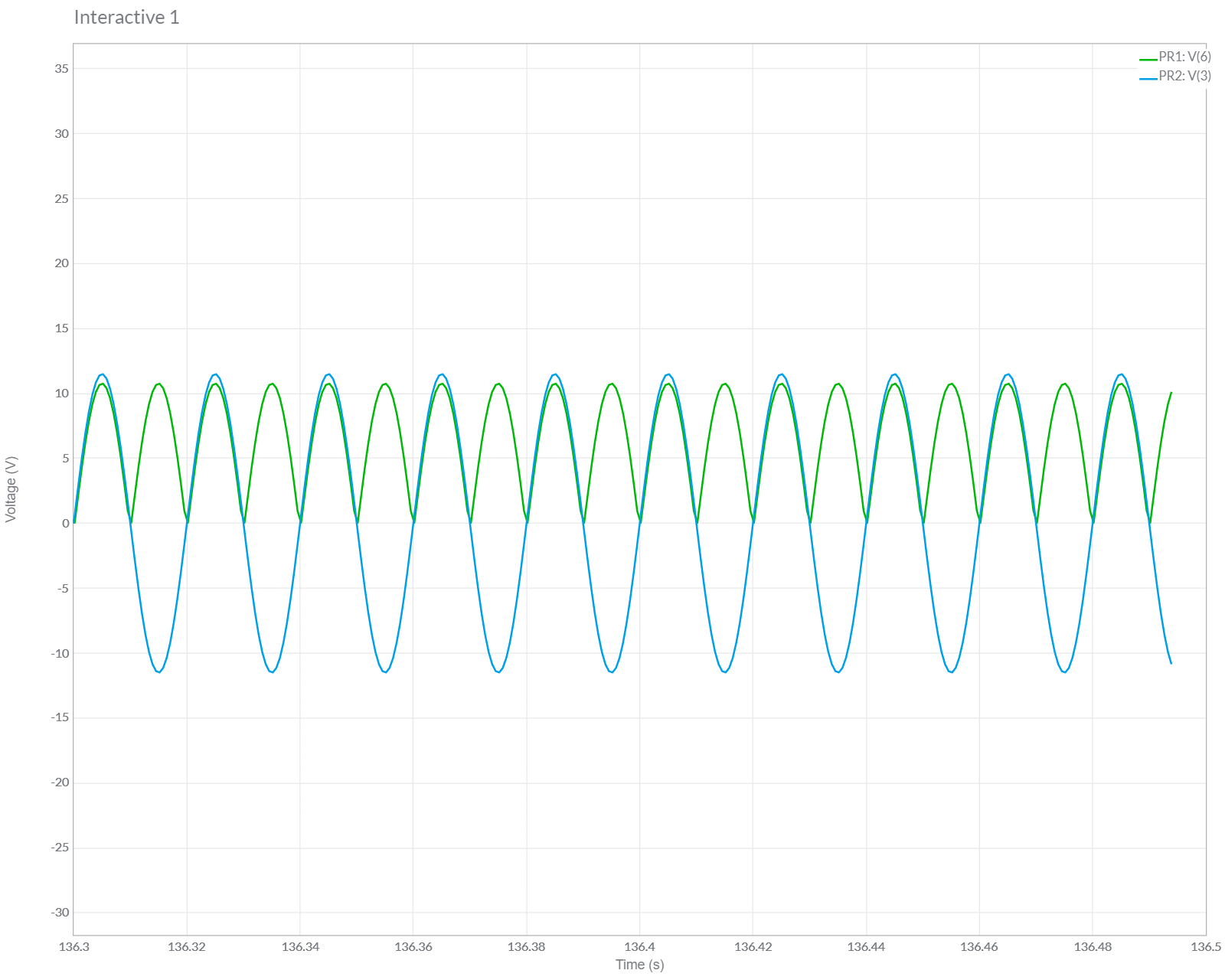
1. **Centre tapped:**

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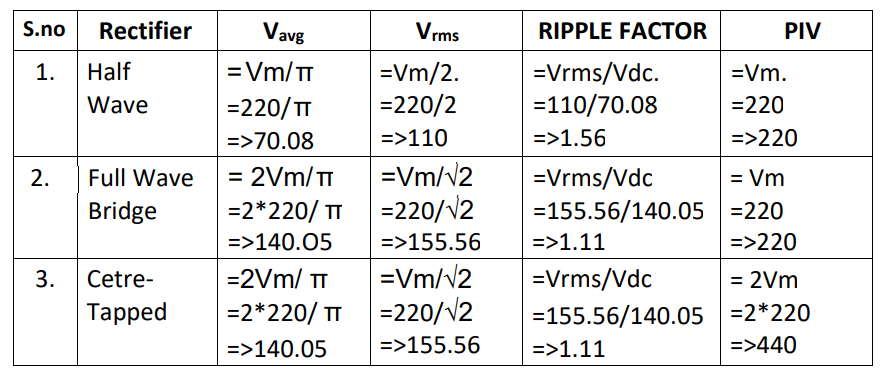


1. **Bridge:**

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**OBSERVATIONS:**



**PIV**: - Peak Inverse Voltage

**CONCLUSIONS:**

1.Half wave rectification produces a pulsating waveform.

2.Full wave rectified DC is not sharply discontinuous as in half wave rectifier.

3. The circuits have been assembled and simulated successfully on multisim and they have been studied carefully. The required waveforms have been compared as well.

**Experiment - 4**

**Aim:** To study the operation of clipper and clamper circuits using PN junction diode and draw wave shape of given circuits.

**Apparatus required:**

Items Quantity

PN junction Diode (IN4001) 2

Function Generator 1

DSO/CRO 1

Resistor (10KΩ) 1

Capacitor (1uF) 1

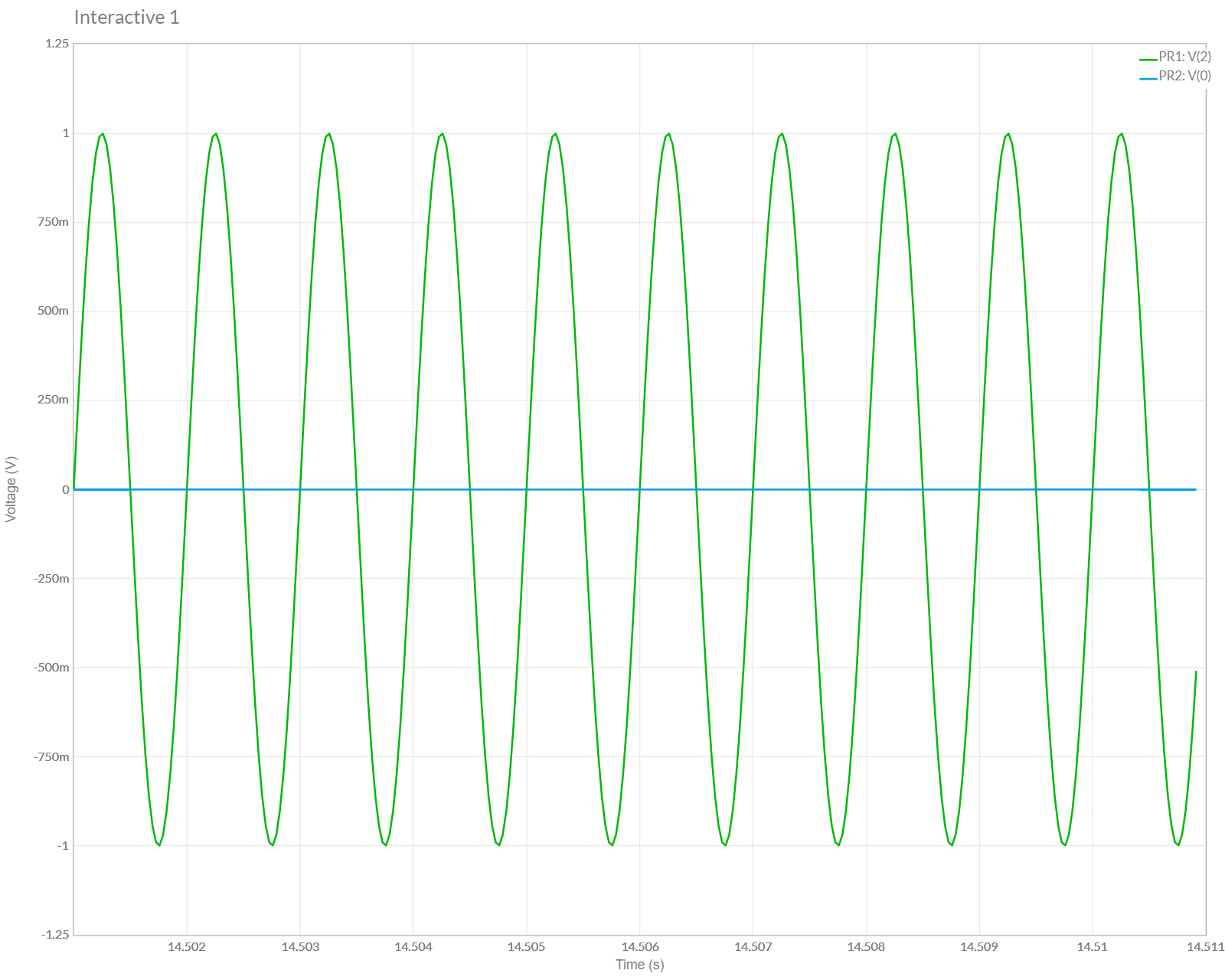
Breadboard 1

Jumper wires as per requirement

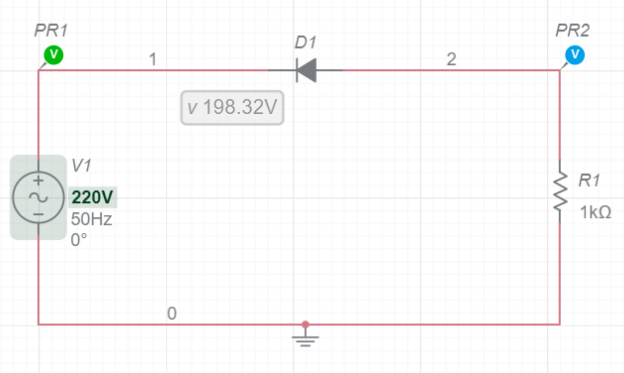
**Series Clippers:**

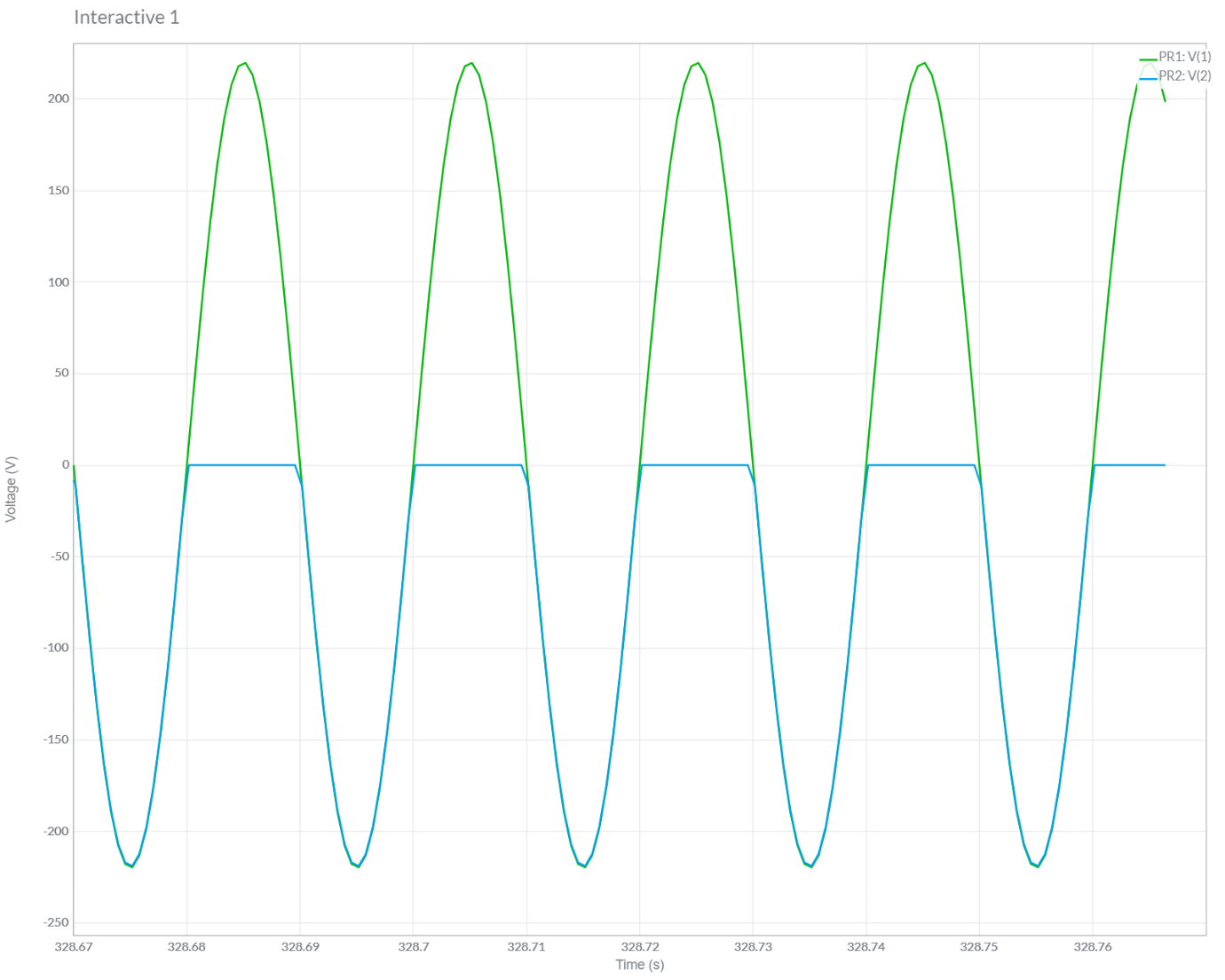
1. **Series Negative Clipper:**

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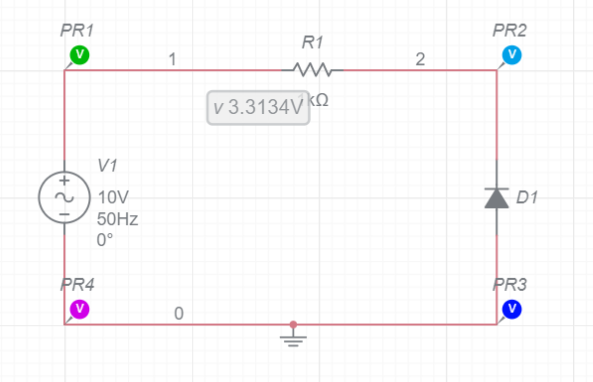
1. **Series Positive Clipper:**

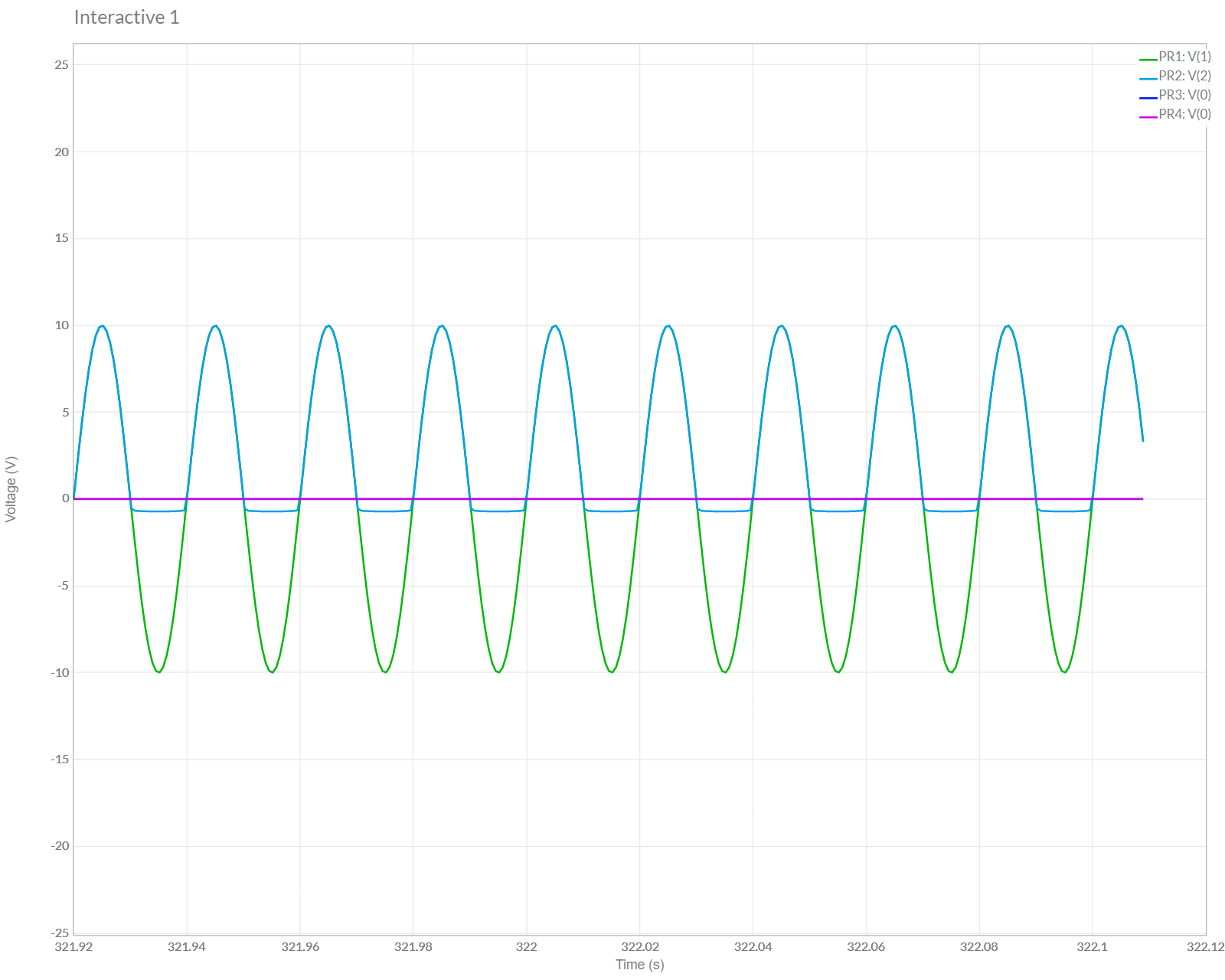
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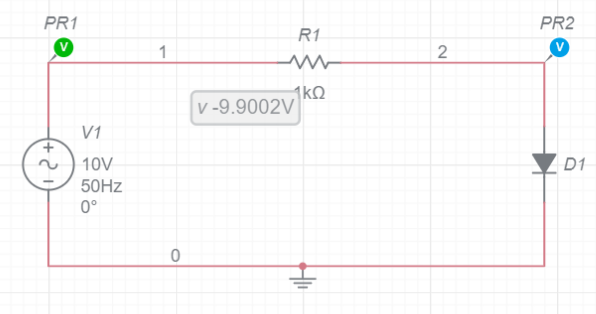
**Parallel Clippers:**

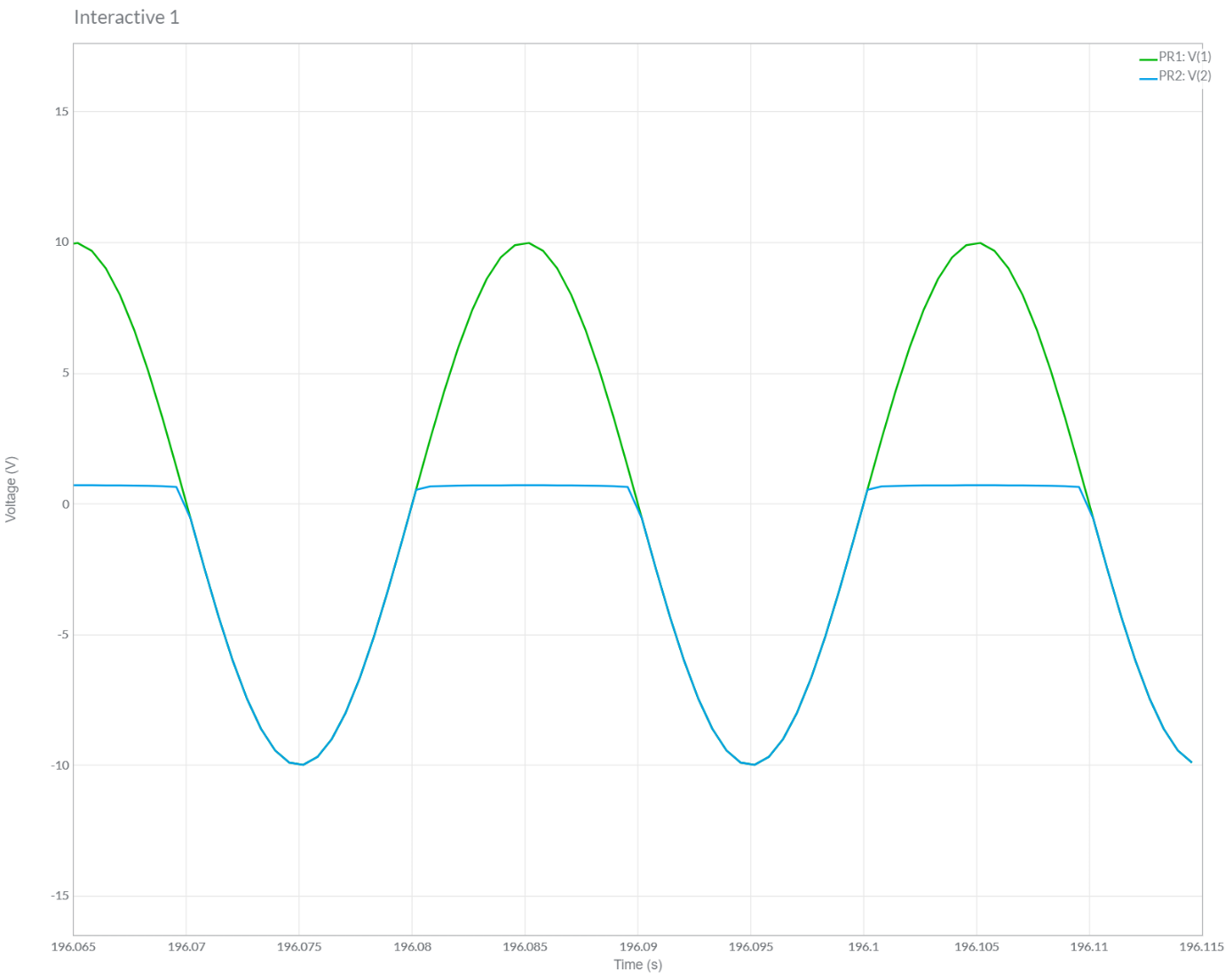
1. **Parallel Negative Clipper:**

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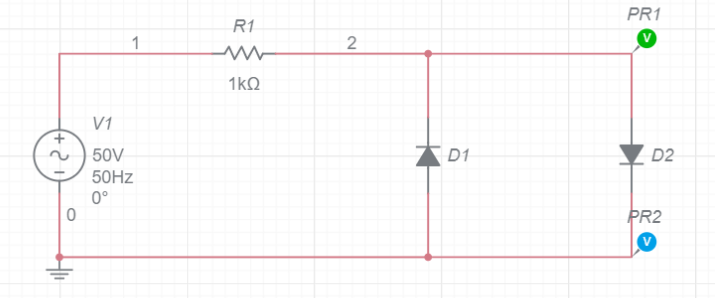


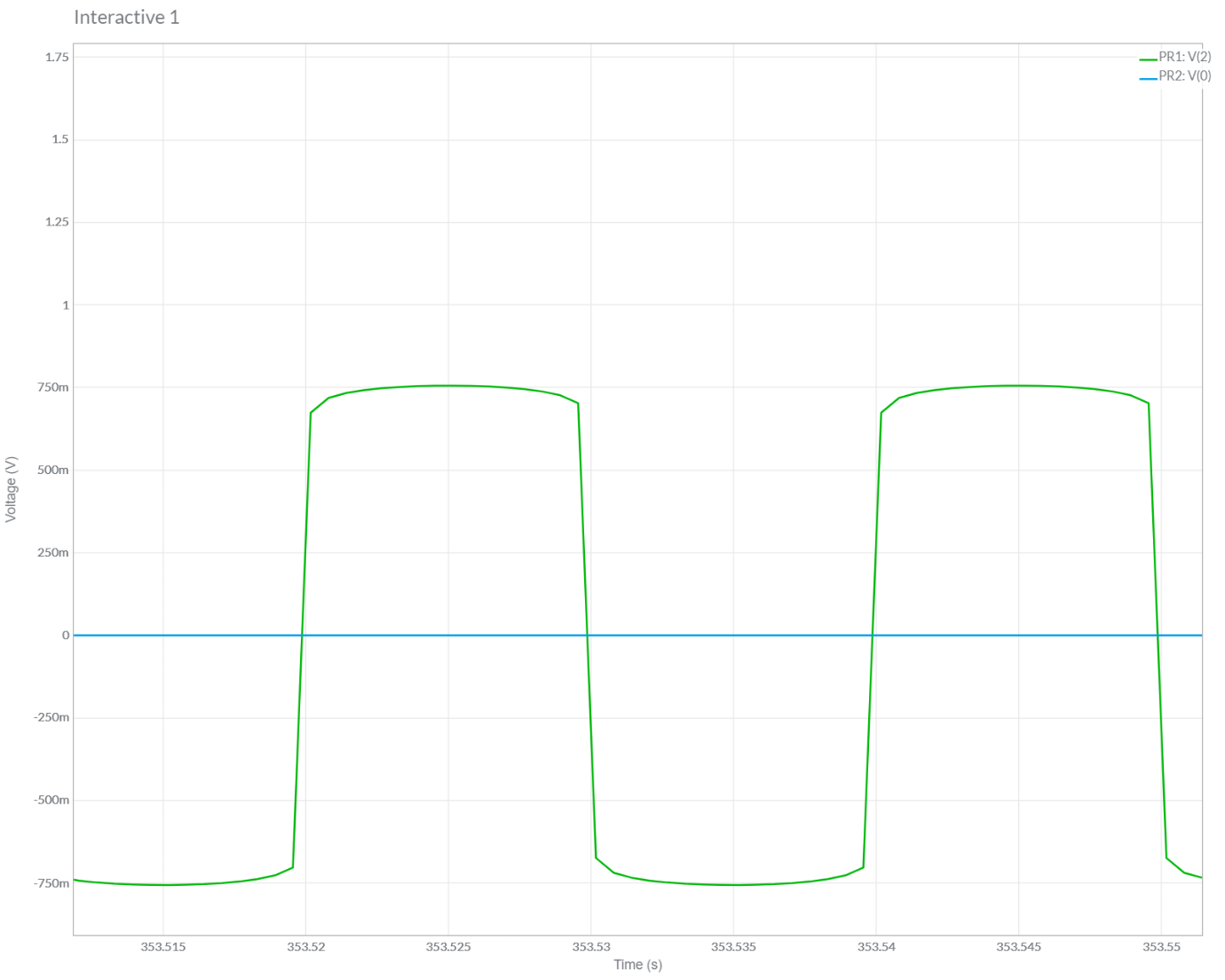
1. **Parallel Positive Clipper:**

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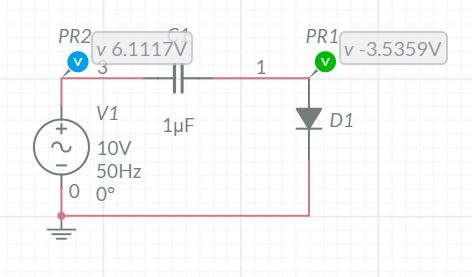
**Combination Clipper:**

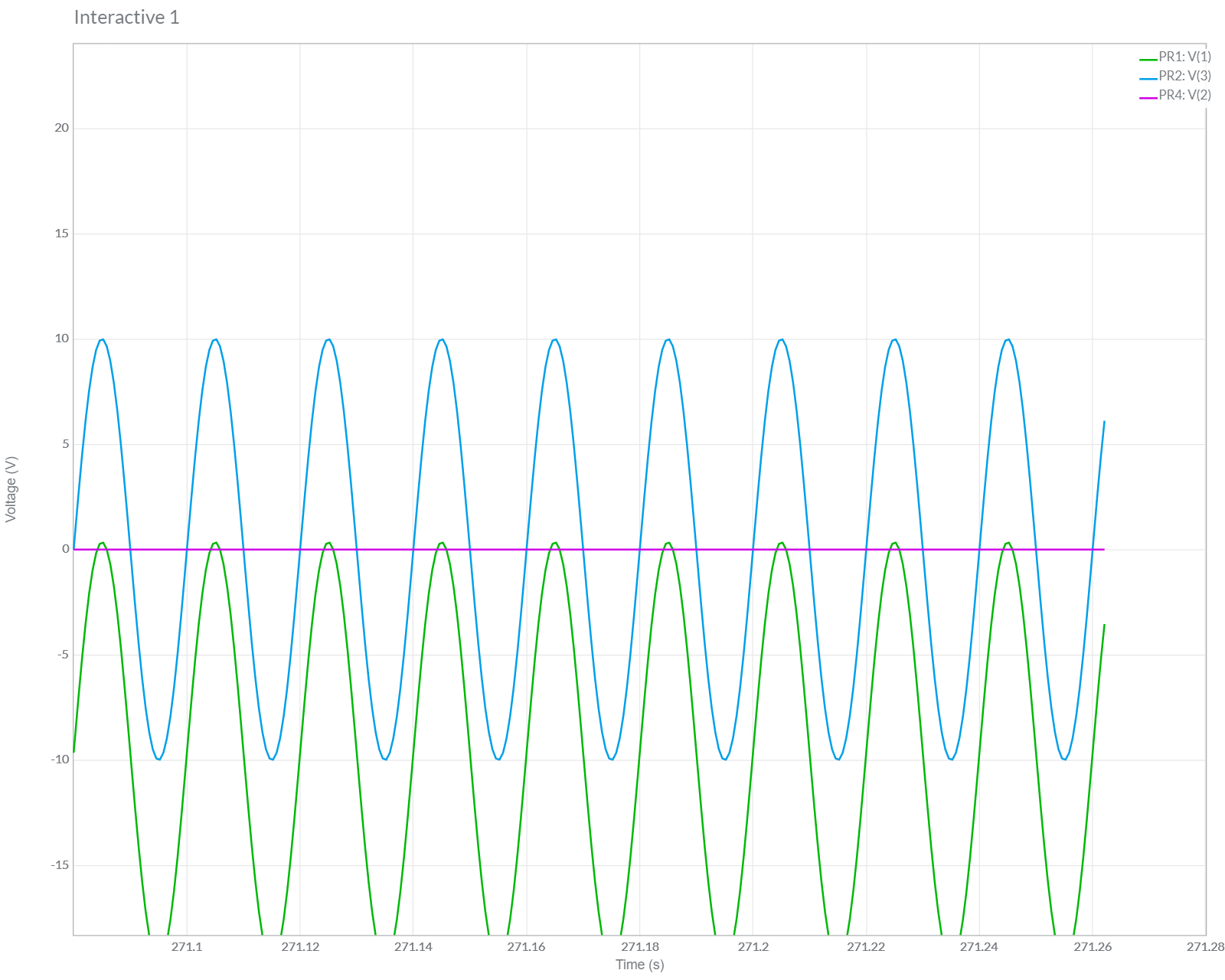
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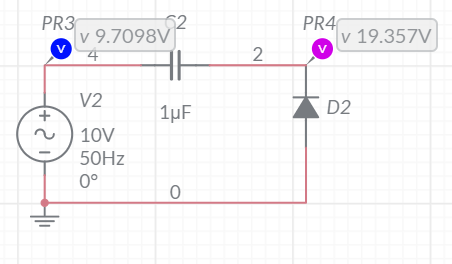
**Clamper Circuit:**

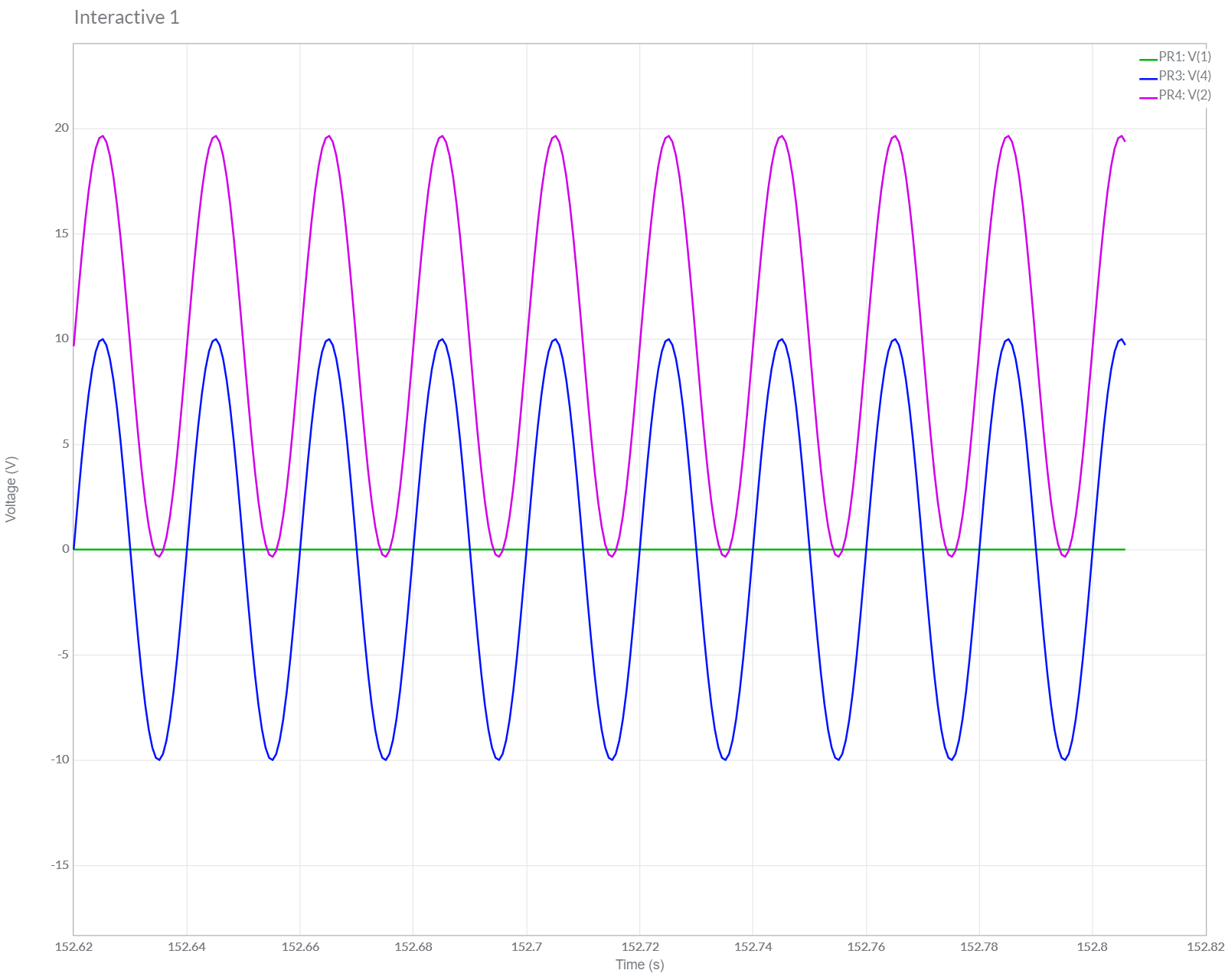
1. **Negative Clamper:**

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1. **Positive Clamper:**





**Result:**

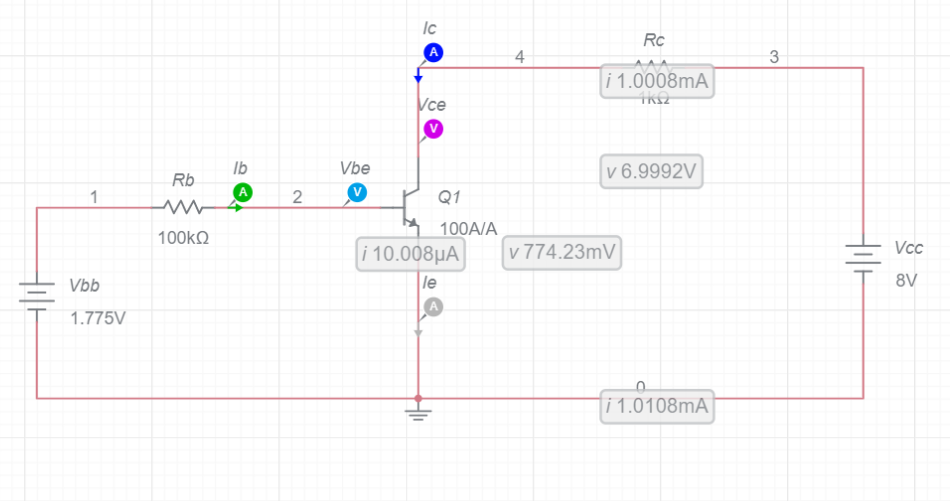
The Clamper circuit design output waveforms have been studied and the required  parameters have been compared.

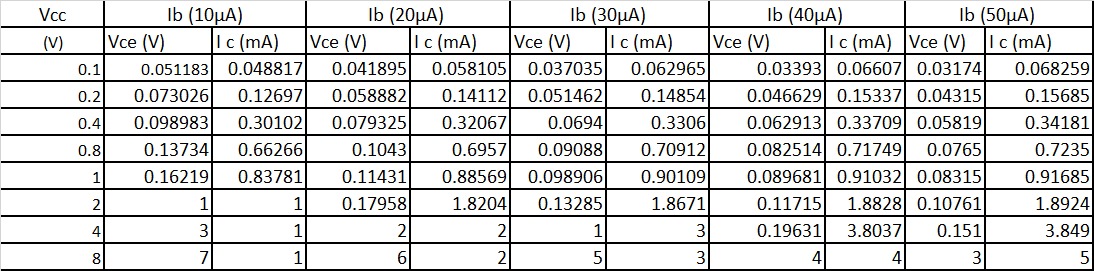
**Experiment – 5**

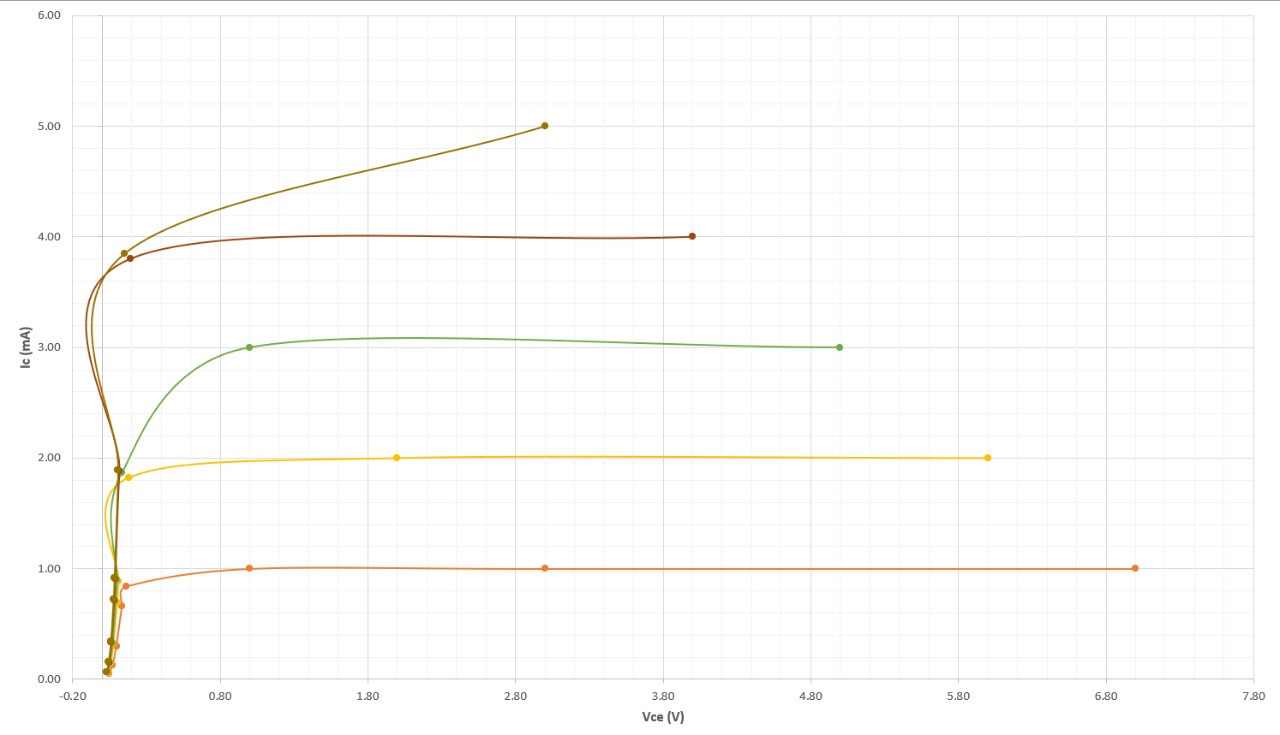
**AIM :** Plot the output characteristics of a BJT in Common Emitter Configuration.

**Apparatus**: BJT, RB=100 KΩ, RC = 1 KΩ, VBB and VCC dc Voltage sources.

**Software**: Multisim







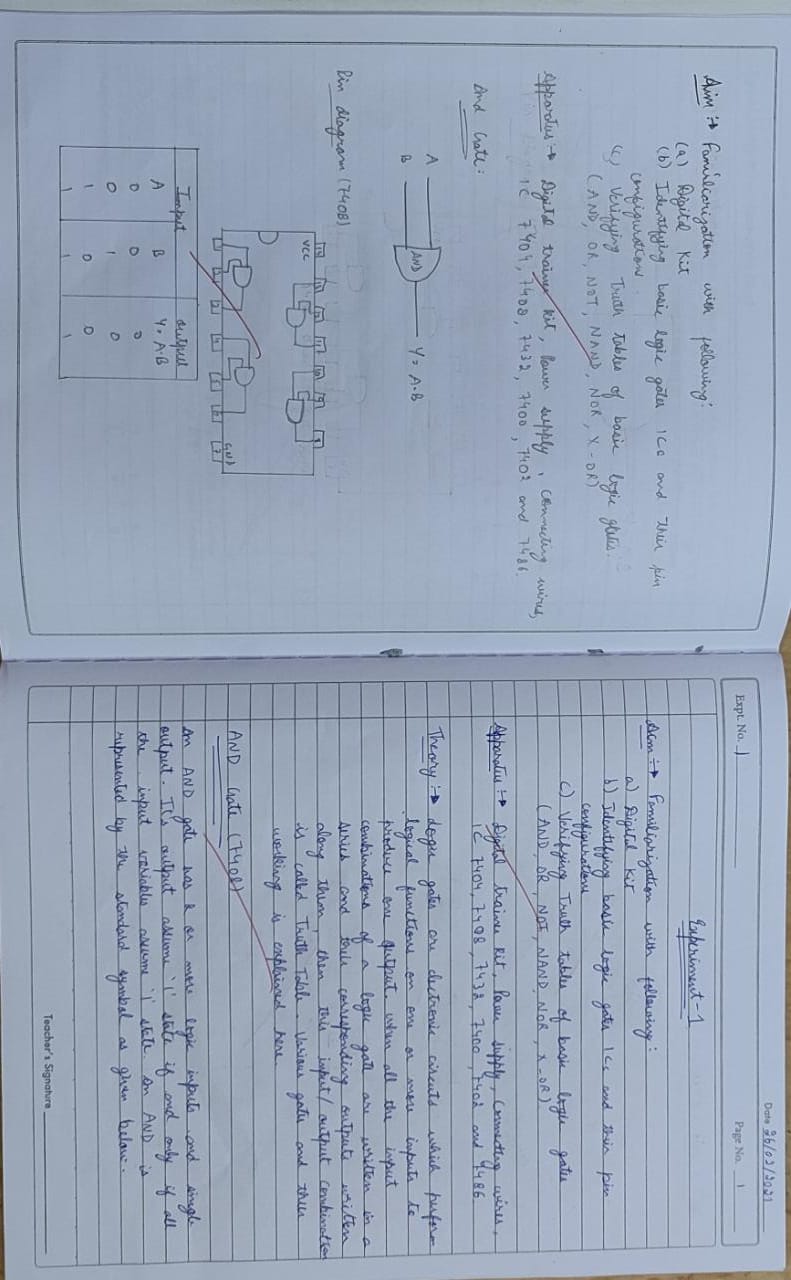
**Experiment – 6**

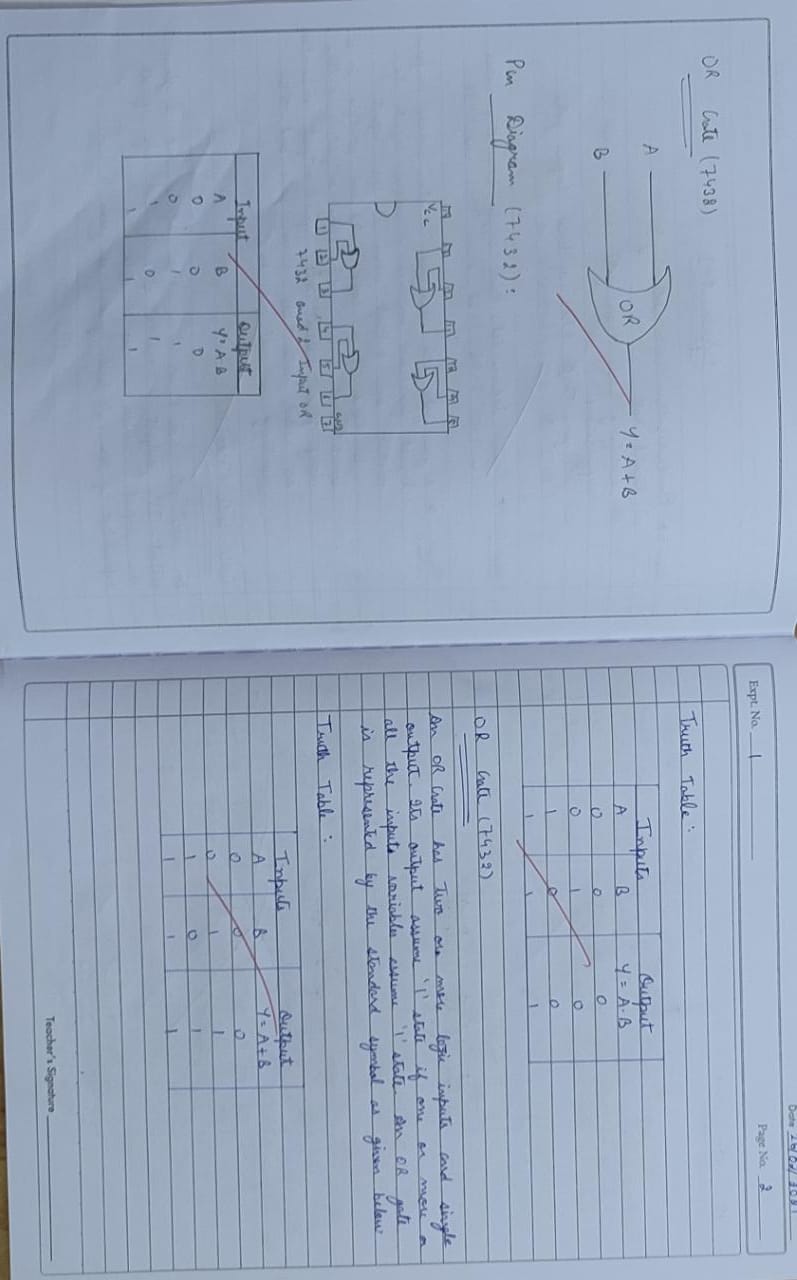
**AIM:** Familiarization with following:

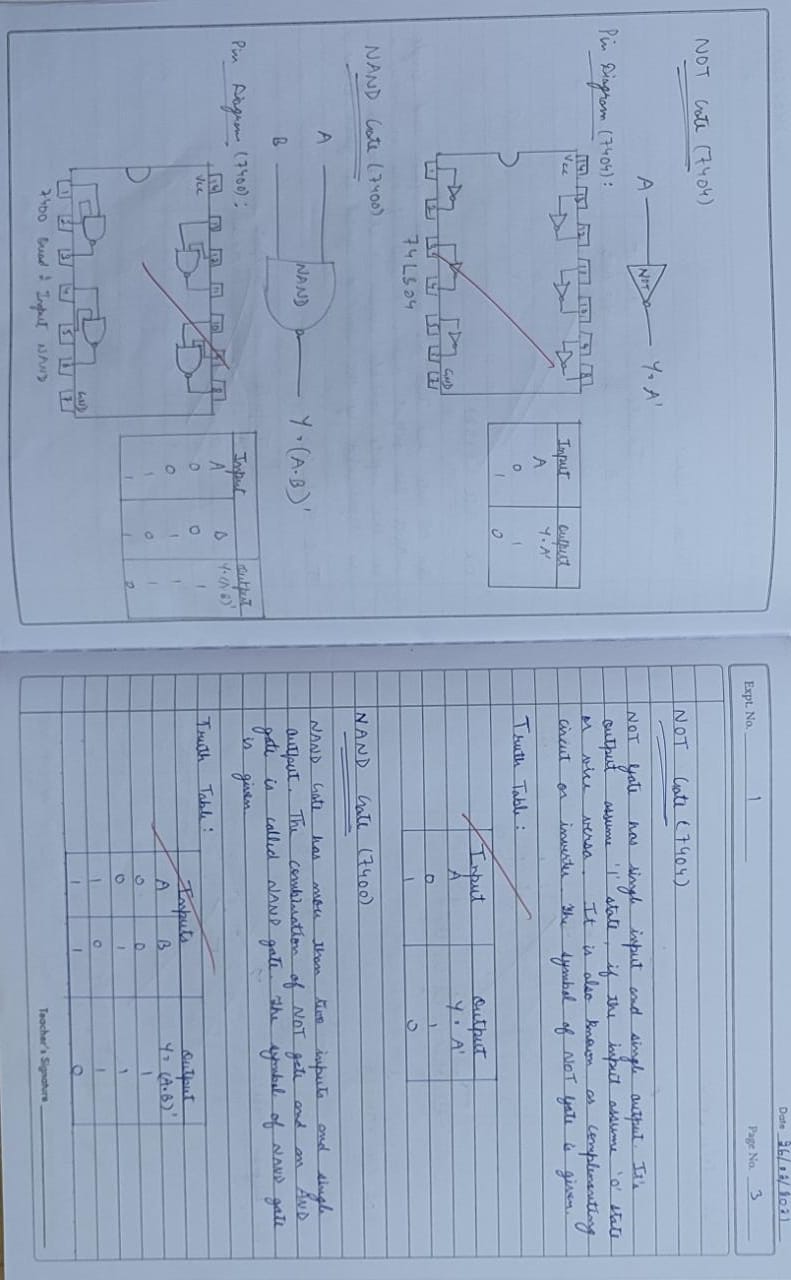
a. Digital Kit.

b. Identifying Basic Logic Gate ICs and their pin configurations.

c. Verifying truth tables of basic logic gates (AND, OR, NOT, NAND, NOR, X-OR).



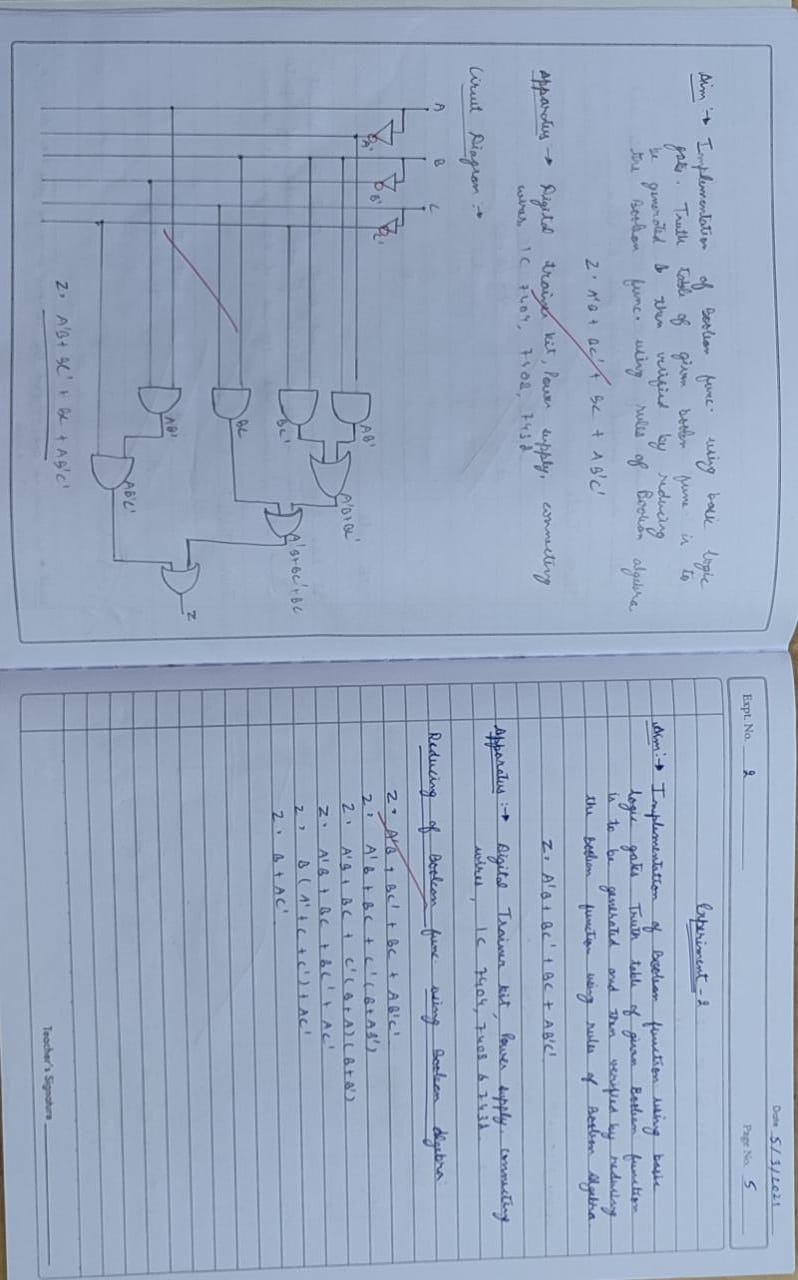


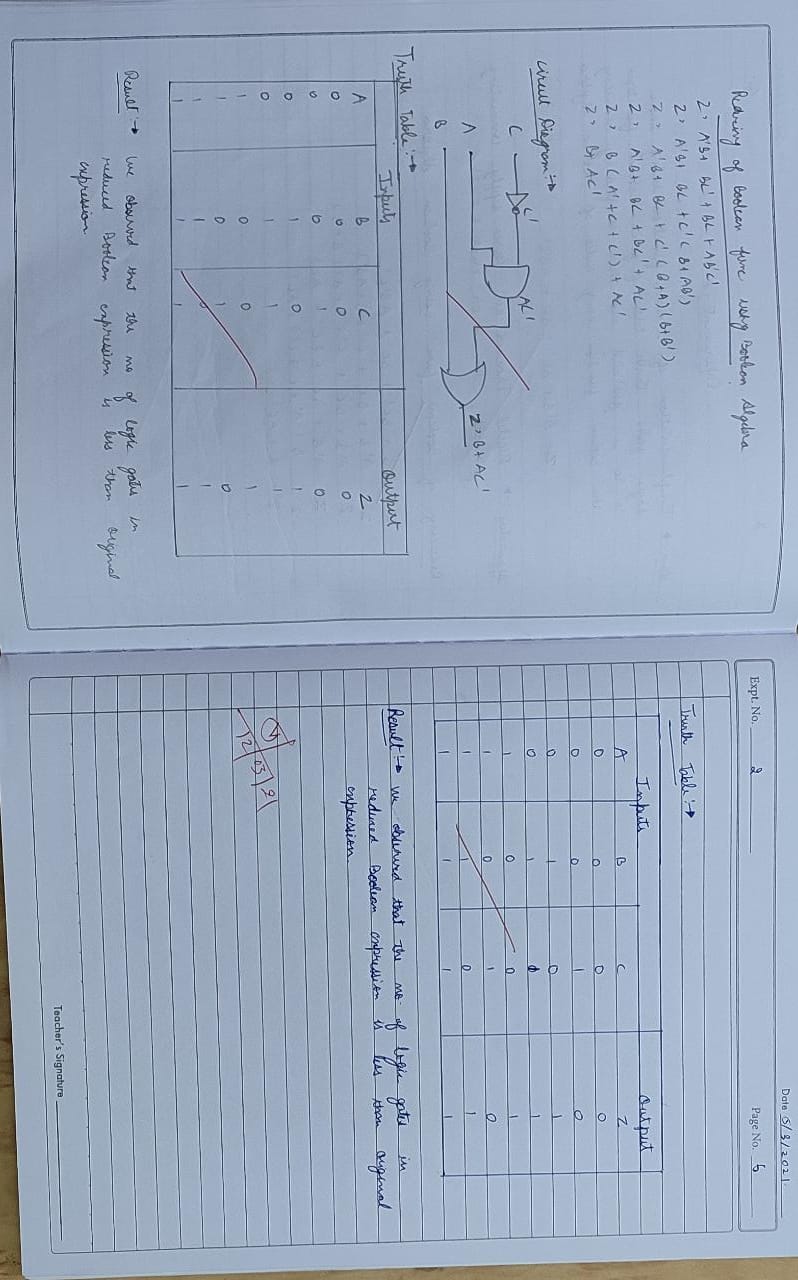




**Experiment – 7**

**AIM:** Implementation of Boolean function using basic logic gates. Truth table of given Boolean function is to be generated and then verified by reducing the Boolean function using rules of Boolean Algebra.





**Experiment – 8**

**AIM:** Implementation of Half Adder using

a. Using AOI logic (AND, OR & NOT)

b. Using any gate (XOR & AND)

c. Using minimum number of NAND gates.

**Equations of SUM and CARRY:**

       SUM = A’B + AB’

         CARRY = AB

**Apparatus**: Digital trainer kit, Power supply, Connecting wires, IC 7404, 7408, 7432, 7400& 7486

**Circuit diagram**:

1.    Using AOI logic (AND, OR & NOT):

2.  Using any gate (XOR & AND):

3.  Using minimum number of NAND Gates:

**Simplification for minimum NAND gates**:

Y = ((A’B + AB’)’)’

= ((AB’ + 0)’ (A’B + 0)’)’

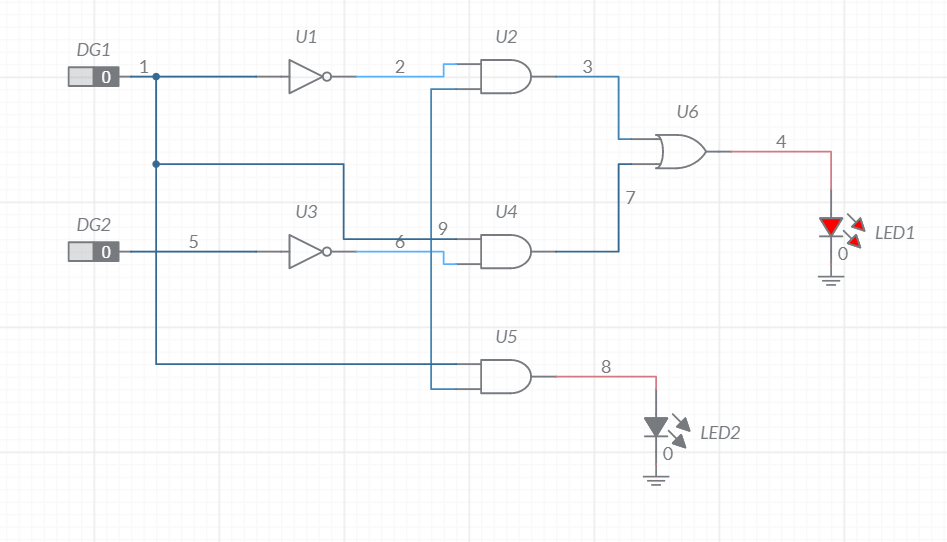
= ((AB’ + AA’)’ (A’B + BB’))’

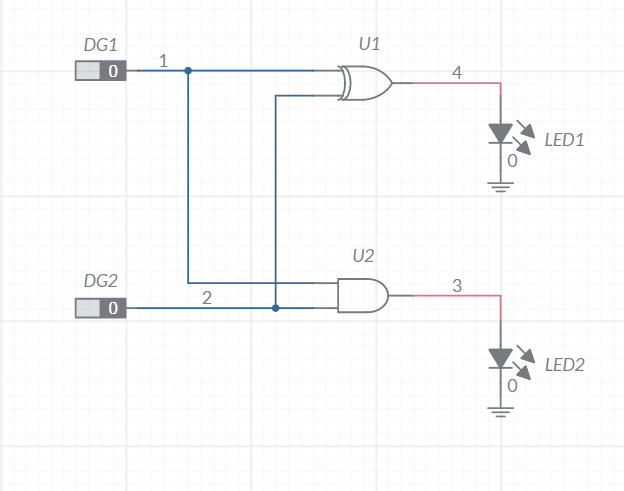
= ((A (B’ + A’))’ (B (A’ + B’))’

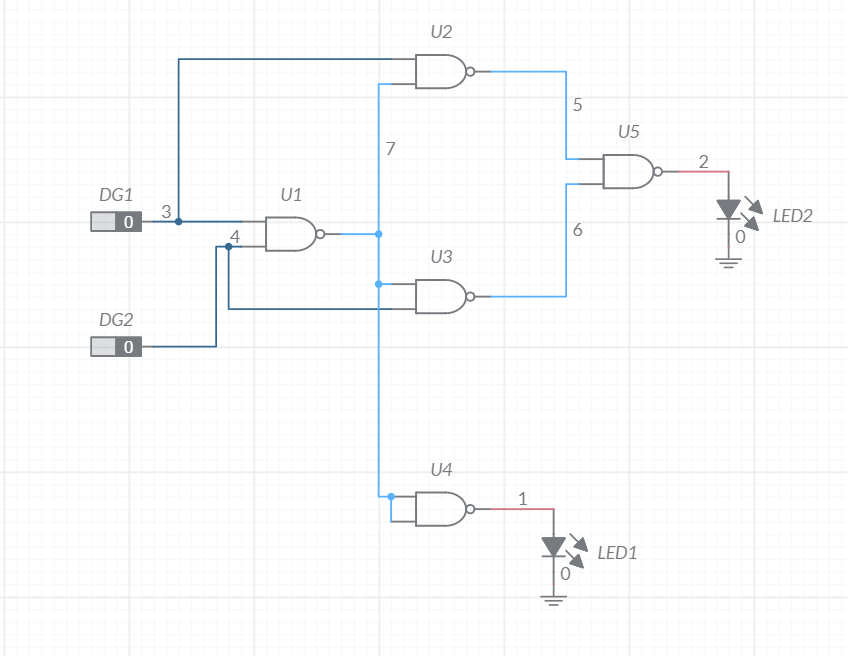
= (((A (AB)’)’ (B (AB)’)’)’

**Truth table:**

|  |  |  |  |
| --- | --- | --- | --- |
| INPUTS | | OUTPUTS | |
| A | B | CARRY | SUM |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |







**Result**: We have studied and implemented the Half Adder using the given logic gates. Schematic diagrams of the same have also been drawn.

**Conclusion:** When we add two binary numbers, we start with the least significant column. This means that we have to add two bits with the possibility of carry. The circuit used for this is called a Half Adder.

**Experiment – 9**

**AIM:**  Implementation of a Full Adder using Multiplexer and Decoder ICs and verify their truth tables.

**Apparatus:** Digital trainer kit, Power Supply, Connecting wires, IC 74153, 7404 & 7420

**Equations:** Multiplexer equation: A’B’I0 + A’BI1 + AB’I2 + ABI3

Sum**:** A + B +  = AB’C’ + A’B’C + ABC + A’BC’

Carry: AB + B  + A = AB’C + A’BC + AB

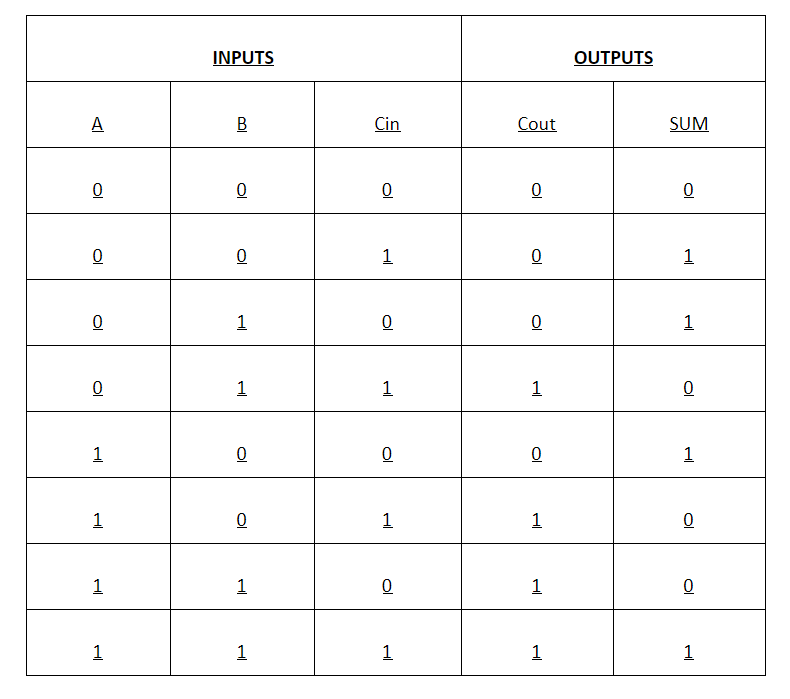
**Circuit Diagrams:**

**1)    SUM**

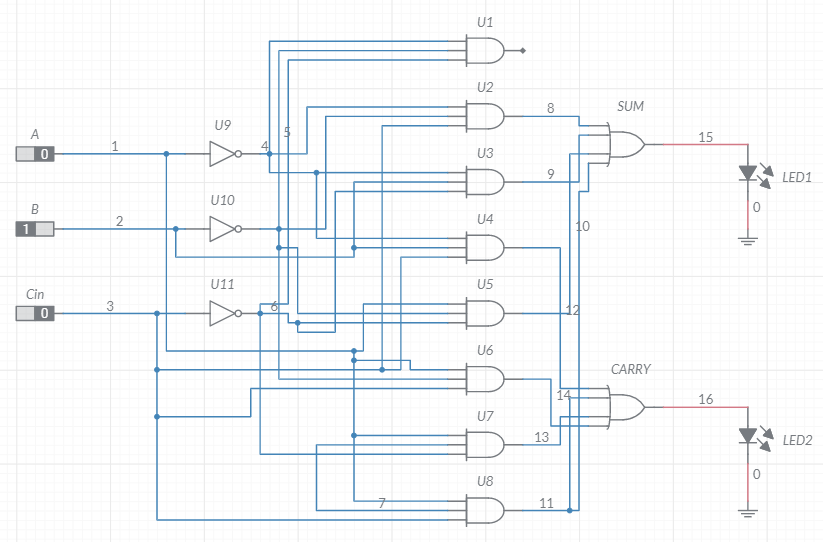
**2)    CARRY**

**3)    DECODER FULL ADDER**

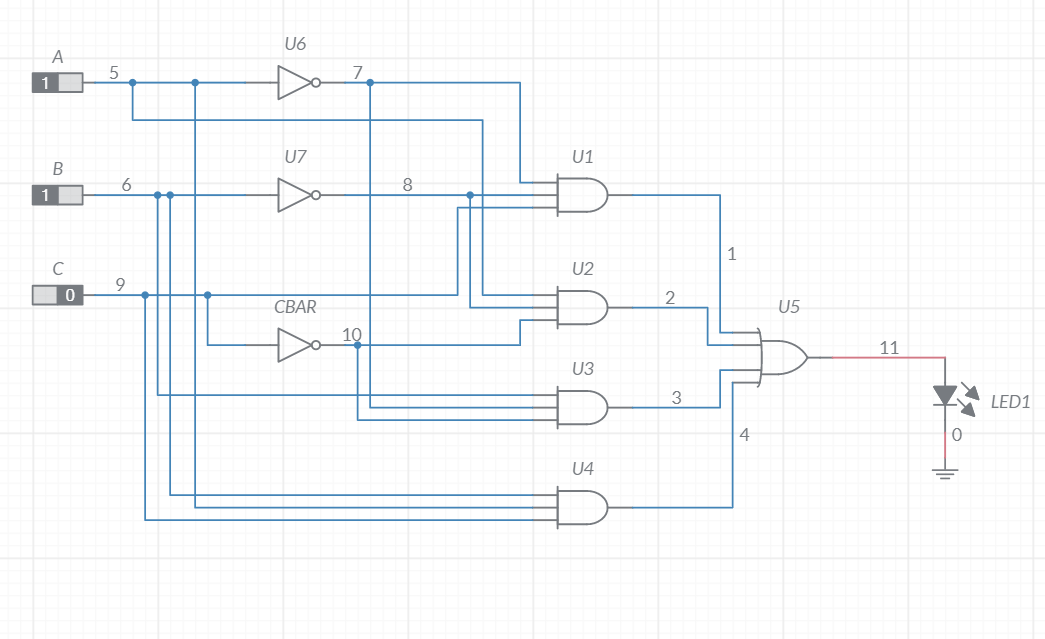
**Truth Table:**



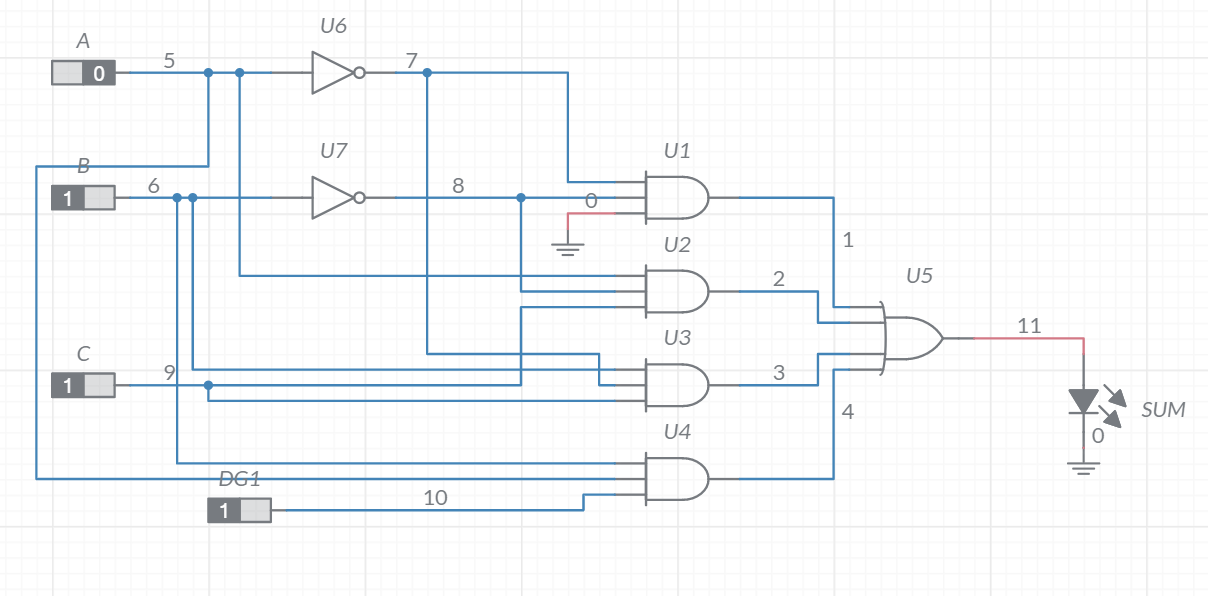
**Decoder:**



**MULTIPLEXER: SUM**



**CARRY:**



**Experiment – 10**

**AIM:**  Construct and study behaviour of following Latches/Flip-Flops:

1. SR Latch using NAND & NOR gates.

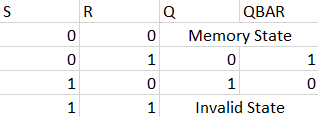
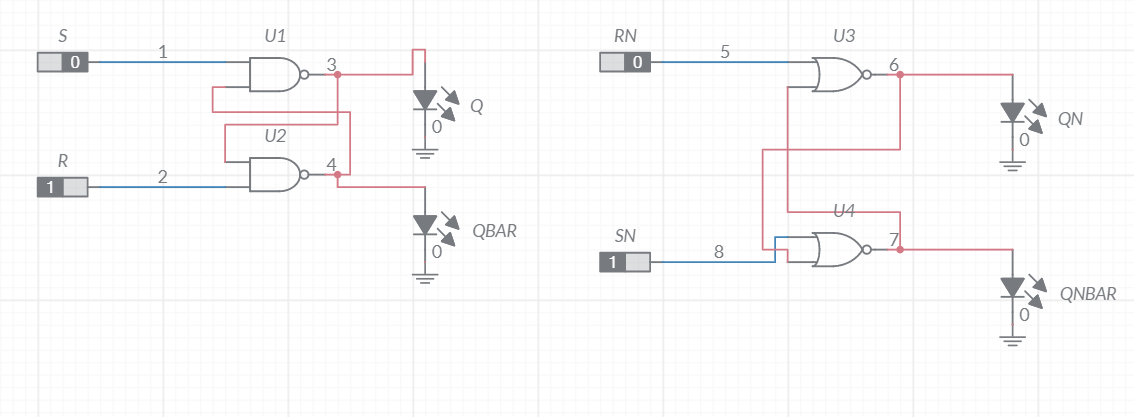
2. Convert NAND & NOR based SR Latch to Gated Latches.

3. Convert Gated SR Latch to D Flip-Flop.

**Apparatus**: Digital trainer kit, Power supply, Connecting wires, IC 7400,7402, 7404, 7408 & 7473.

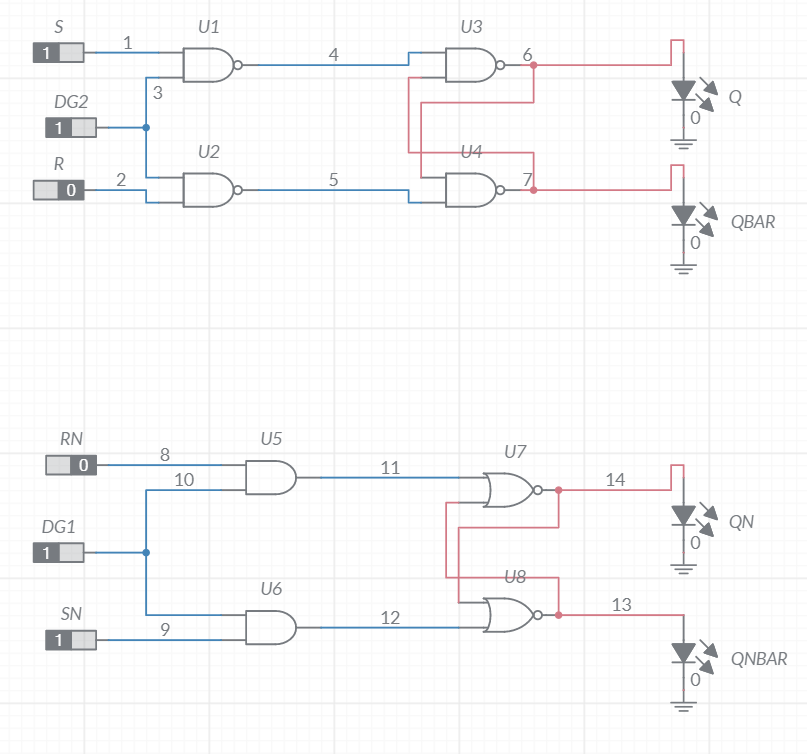
**CIRCUIT DIAGRAMS and TRUTH TABLE:**

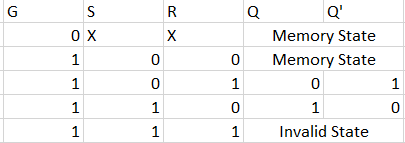
1. **SR Latch (NOR) and SR Latch (NAND):**

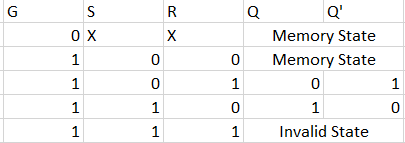
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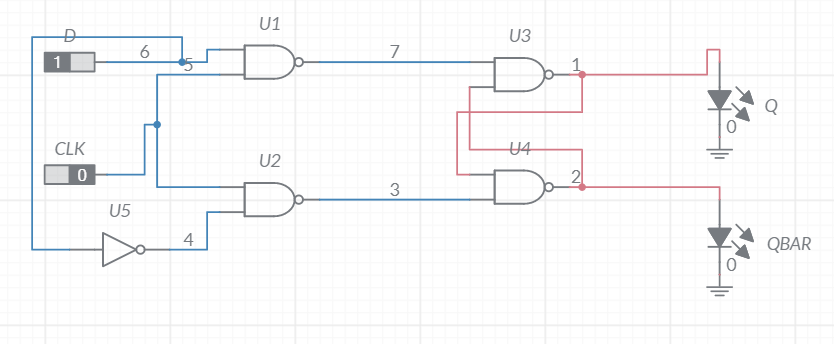
1. **Gated SR Latch (NOR)**  **and** **Gated SR Latch (NAND):**

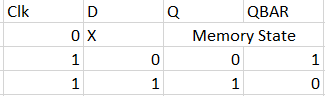
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1. **D FLIP-FLOP:**

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**CONCLUSION**: Hence the result received is calculated and analysed by performing the experiment on multisim and it is true for the given data and verified.