RITISH BEHERA

Aspiring Physical Design Engineer

Portfolio
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SUMMARY

Aspiring Physical Design Engineer with expertise in EDA tools, VLSI design, and semiconductor technology. Proven ability to perform complex simulations and design optimizations. Committed to continuous learning and innovation in the VLSI domain. Explore my skills and projects at **Portfolio**

SKILLS

EDA Tools: Cadence Virtuoso, Sentaurus TCAD, Xilinx Vivado

OpenSource: openLANE flow (Yosys, RePLace, openSTA, openROAD, TritonCTS, TritonRoute), Magic VLSI

Languages: Verilog HDL, C++, Assembly, MATLAB, TCL

Hardware: 8086 Microprocessor, Artix-7 Power FPGA Board

EDUCATION

2022-2025 **Masters in Electronics** — **National Institute of Technology Warangal, India**
Relevant Courses: VLSI Design, Embedded Systems, Microprocessor Interfacing, Digital System Design, Linear Integrated Circits, C++, Computer Architecture, Semiconductor Devices

2018-2021 **Bachelors in Science With Physics Honours** — **Gangadhar Meher University, Sambalpur, India**
Relevant Courses: Solid State Physics, Device Physics, Analog and Digital Electronics

EXPERIENCE

May-July 2023 **Summer Research Intern, VRITIKA Internship** — **IIT Gandhinagar, India**

- Topic: Analysis of BEOL Integration of 2DM Based Pass Transistor in 6T SRAM [**Find Report**]
- Conducted extensive literature review on 3D SRAM technology and 2D materials.
- Carried out circuit simulations and analyzed performance metrics of the novel 6T SRAM circuit, achieving a 70mV improvement in read noise margins for 28nm technology.
- Developed a physical layout model for the SRAM design with approx 30% improved area efficiency.
- Evaluated the feasibility and performance implications of heterogeneous BEOL integration techniques for advanced SRAM designs, addressing interconnect delays and parasitic effects.

`Cadence Virtuoso / Cadence Spectre / UMC28nm`

PROJECTS (MAJOR)

Physical Design **Physical Design Optimization and Timing Analysis of RISC-V Processor Using OpenLane** **[github repo]**

- Characterized and integrated custom cells into a RISC-V design using OpenLane, and executed place and route operations to achieve a complete design layout without timing violations.
- Conducted Static Timing Analysis (STA) to identify and rectify slack violations, optimizing timing through fanout limitation and drive strength adjustment achieving a final setup slack of 4.132ps and hold slack of 2.320ps with some area trade-offs.
- Performed parasitic extraction for accurate timing, power analysis, and signal integrity verification, generating the spef file post-routing.

`SkyWater 130nm openPDK / openLANE PnR flow / NGSpice`

Hybrid SRAM Characterization **Characterization of Si-Mos2 3D Integrated SRAM Cell Architectures** **[github repo]**

- Analyzed DC and transient behaviour to characterize the noise response and delay analysis of heterogeneously integrated Si-MoS2 SRAM architectures at voltage levels of 0.7V, 1.2V and 1.8V .
- Optimized the W/L ratios to meet the on-current specifications whilst improving noise margins by 10-20%.
- Working on 3D layout models for extra interconnects to accurately calculate area efficiency and extract parasitic effects.
- Architectures: Single Bitline 7T SRAM, Read-assist 7T SRAM, NTV 7T SRAM, 9T SRAM, 10T SRAM.

`Cadence Virtuoso / GPDK22nm (FinFET) / GPDK180nm / Custom MoS2 Library`

Minor Projects **Device Simulation of P-N Junction and MOSFET through Sentaurus TCAD and DIBL Coefficient Calculation for NSFET** **[github repo]**

`Sentaurus TCAD / SDE / SDEVICE / SVISUAL`

Traditional and Thin Cell SRAM Layout Design With DRC and LVS Verification **[Link]**

`Cadence Virtuoso / Layout XL / Assura`

12 Hour Digital Clock Through Verilog, Implemented and Tested on FPGA Board Seven Segment Display **[Link]**

`Xilinx Vivado / Artix-7 Power FPGA Board`

KEY INTERESTS

- Physical Design & Algorithms • Emerging Memory Devices • Interconnect Modelling • Computer Architecture • AI/ML in VLSI

CERTIFICATIONS

- **VSD SoC Physical Design**
- **VLSI Flow: RTL to GDS**
- **VLSI Physical Design with STA**
- **Digital IC Design**
- **ISWDP Sentaurus TCAD**
- **ML and Reinforcement Learning Through MATLAB**

ROLES & RESPONSIBILITIES

2022-2023 **Joint Secretary, Physics Association** **National Institute of Technology Warangal**

- Directed a team of four in the digital content creation for various association events, ensuring their success.

`Team Work / Leadership`

2022-2023 **Executive Member, National Service Scheme** **National Institute of Technology Warangal**

- Collaborated with a group of 50-60 people to help leverage the community services which helped me to grow as a person.

`Team Work / Community Services`

ACHIEVEMENTS

2023 **Recipient of VRITIKA Internship funded by DST, SERB, Gov. of India**

2022 **Qualified IIT JAM (Joint Admission test for Masters) 2022**

2015-2018 **Recipient of National Means Cum-Merit Scholarship (NMMS), GoI**

2016 **Awarded with NCC (National Cadet Corps) A-Certificate**

2016 **District Board Topper in 10th Boards, recognized by SAMAJ newspaper**