Ritish Behera

Phone: +917790060202 **Email:** rb22phc1r45@student.nitw.ac.in **LinkedIn:** ritishbehera
Website: ritish-behera.github.io

EXPERIENCE

Summer Research Intern IIT Gandhinagar,Gujarat
May-july 2023

Topic- "Circuit Simulation of Heterogeneous 6T SRAM Cell Featuring MoS2-FET based Pass Transistor"
The research work involved designing of a heterogeneous 6T SRAM cell consisting of Si cross-coupled inverter on the FEOL level and MoS2-FET based pass transistor to be implemented on the BEOL level. Using cadence virtuoso tool, I carried out circuit simulations for noise margin (read, write and hold) calculation of the hybrid cell and further explored some potential solutions for interconnect and parasitic modelling to describe the integration.

PROJECTS

Noise Margin Analysis of Different Si & MoS2 FET based SRAM Architectures (On-going)
Design of various SRAM cells architectures (6T, NTV 7T, Single Bitline 7T, Read-Assited 7T, 9T & 10T) using both Si and MoS2 based mosfet devices and hence calculating their noise margin response. Tool Used- Cadence Virtuoso. Process node- GPDK 180nm.

Traditional and Thin Cell Layout Design of 6T SRAM Cell
Replicated the layout design of traditional and thin cell SRAM cells using Virtuoso Layout XL environment with successful DRC and LVS checks. Process node-180nm.

Design and Analysis of SRAM Cell in Latest UMC 28nm Technology
Done simulations for transient, DC and noise margin analysis of 6T SRAM cell followed by static and dynamic power consumption using the latest UMC28nm technology. Tool used- Virtuoso ADE L

Triboelectric Nanogenerator(TENG) Circuit Modelling Using SIMULINK
Modeled the appropriate circuit for the TENG device with variable capacitance subsytem using SIMULINK, which was further used for simulations of device characteristics.

SKILLS

EDA Tools: Cadence Virtuoso, Sentaurus TCAD, OpenRoad, Xilinx Vivado, DEEDs
Languages: Verilog, Assembly, Perl, C++, MATLAB
Environment: Windows, Linux (Ubuntu).
Hands-on: 8086 Microprocessor, Artix-7 Power FPGA board

INTERESTS

Physical Design (PR, PSV, CTS, Layout), Memory Devices, Interconnect & Parasitic Modelling, Computer Architecture, R&D

CERTIFICATION COURSES

VLSI Physical Design with STA NPTEL,Apr 2024
Digital IC Design NPTEL,Apr 2024
VLSI Design Flow: RTL to GDS NPTEL,Dec 2023
Semiconducter Device Modelling and Simulations NPTEL,Apr 2023

EDUCATION

MSc(Tech) Engineering Physics (Electronics Specialization) GPA: 7.25
NIT Warangal, Telangana **2022-25**
Relevant Courses: VLSI Technology, Microprocessor & Interfacing, Computer Organization, Digital Electronics (STLD & SDSD), Linear Integrated Circuits, Electronic Devices and Circuits, Material Science, Solid State Physics

BSc Physics Honors GPA: 8.2
Gangadhar Meher University, Odisha **2018-21**
Relevant Courses: Digital Circuits, Analog Circuits, Device Physics, Solid State Physics

ACHIEVEMENT

IIT JAM 2022 Qualified 2022
NMMS Scholarship 2015-18
NCC A-Certificate 2016

EXTRA-CURRICULAR

Joint Secretary, Physics Association, NIT Warangal 2022-23
Executive Member, NSS, NIT Warangal 2022-23
Intern, SAMBHAJ NGO 2022