

Analysis of Vertical BEOL Integration of 2DM Based Pass Transistor in 6T SRAM

A report submitted in fulfillment
of the requirements for

VRITIKA Internship

by

Ritish Behera

Under the guidance of

Dr. Tarun Kumar Agrawal



Electrical Department
Indian Institute of Technology Gandhinagar
2023

D E C L A R A T I O N

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/- source in my submission. I understand that any violation of the above can cause disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Ritish Behera

Date : July 14, 2023

C E R T I F I C A T E

It is certified that the work contained in the report titled "**Analysis of Vertical BEOL Integration of 2DM Based Pass Transistor in 6T SRAM**" by **Ritish Behera**, has been carried out under my supervision and that this work has not been submitted elsewhere.

Dr. Tarun Kumar Agrawal

Assistant Professor

Indian Institute of Technology Gandhinagar

A C K N O W L E D G M E N T S

I would like to express my deepest gratitude and sincere appreciation to Prof. Tarun Kumar Agrawal from IIT Gandhinagar for his invaluable guidance and unwavering support throughout the duration of my internship. His expertise and encouragement have been instrumental in shaping my ideas and successfully implementing them. Without his guidance, this research would not have been possible. I would also like to extend my thanks to the MDCL lab facility for providing me with the necessary equipment to carry out this project during my internship. Their support has been vital to the success of my work. I would like to give a special mention to Aayush Bhaiya and Saurabh Bhaiya for their invaluable support and assistance throughout the learning process of this internship. I am forever indebted for their guidance and encouragement. I would also like to express my heartfelt thanks to my co-interns, Naresh Choudhary, Snehal Mondal, and Simran Rawat, for their constant presence and support throughout this period. The engaging discussions and collaboration with them have truly enriched my internship experience. Lastly, I am immensely grateful to Tarun Sir and IIT Gandhinagar for providing me with this incredible opportunity to learn and grow in my professional career. Their support and mentorship have had a profound impact on my personal and academic growth.

TABLE OF CONTENTS

Declaration	i
Certificate	ii
Acknowledgments	iii
List of Figures	vi
List of Tables	vii
List of Abbreviations	viii
Abstract	ix
Chapter	
1 INTRODUCTION	1
1.1 Objectives of this Report	2
2 Literature Review	4
2.1 SRAM	4
2.1.1 Introduction	4
2.1.2 6T SRAM CELL	5
2.1.3 Read Operation	5
2.1.4 Write Operation	7
2.2 Semiconductor Process	8
2.2.1 BEOL Integration	8
2.3 Introduction to 2D Materials	10
2.4 Conclusion	10
3 BEOL Integration of MoS₂ Transistor and SRAM Layout Model	11
3.1 Introduction	11
3.2 BEOL Integration of MoS ₂ Transistor in SRAM	12
3.3 SRAM Layout Model	12
3.4 Additional Parasitics	15
3.4.1 Parasitic Extraction	15
3.5 Conclusion	17
4 Circuit Simulation and Performance Analysis	18
4.1 Introduction	18

4.2 Simulation Methodology	19
4.2.1 MoS ₂ Device Modelling	19
4.2.2 Schematic Design	20
4.2.3 Simulation Setup	21
4.2.4 Transient Analysis	21
4.2.5 Noise Margins	22
4.3 Result Comparison and Analysis	23
4.4 Extraction and Modelling of Parasitics	26
4.5 Conclusion	26
5 Conclusion and Further Work	27
5.1 Conclusion	27
5.2 Further Work	27
References	29

LIST OF FIGURES

2.1	6T SRAM Schematic	5
2.2	Butterfly curve to calculate RSNM of 6T SRAM.	6
2.3	Write margin calculation for 6T SRAM.	8
2.4	Flow Chart of BEOL Integration of Graphene[8]	9
3.1	2D Layout of the BEOL Integrated SRAM Device	13
3.2	3D Layout Model of SRAM with MoS ₂ -FET Integrated at BEOL(1)	14
3.3	3D Layout Model of SRAM with MoS ₂ -FET Integrated at BEOL(2)	14
3.4	Side View of 3D Layout Model of SRAM with MoS ₂ -FET Integrated at BEOL(1)	14
3.5	Side View of 3D Layout Model of SRAM with MoS ₂ -FET Integrated at BEOL(2)	14
3.6	. Illustration of (a) BEOL interconnects and (b) MEOL interconnects and cell-level parasitic RC[14]	15
3.7	Showing Capacitances Produced due to the Arrangement of Interconnects[17]	16
3.8	An Example of 3D Interconnect Model Developed in Raphael	17
4.1	Schematic of MoS ₂ nFET Imported to Cadence	19
4.2	Schematic Diagram of a 6T SRAM Containing MoS ₂ nFET at the Pass Transistor Position	20
4.3	Transient Analysis Result for 6T SRAM (without parasitics)	22
4.4	Read Margin for 6T SRAM having MoS ₂ nFET Pass Transistor with width of 282nm	23
4.5	Read Margin for Si based SRAM	24
4.6	Write Margin for Si based SRAM	24
4.7	Read Margin for MoS ₂ based SRAM	24
4.8	Write Margin for MoS ₂ based SRAM	24
4.9	Variability of RSNM with Different Widths of MoS ₂ Pass Transistor in SRAM	25

LIST OF TABLES

4.1 Comparison of RSNM and WSNM in Different SRAMs	25
4.2 Variation of RSNM with Gate Width of MoS ₂ Pass Transistor .	25

LIST OF ABBREVIATIONS

TMD: Transition-metal dichalcogenide

6T: Six-Transistor

SoC: System on Chip

RSNM: Read Static Noise Margin

WSNM: Write Static Noise Margin

SRAM: Static Random Access Memory

WL: Word Line

BLs: Bit Lines

BLB: Bit Line Bar

ABSTRACT

As the computing landscape continues to evolve, the scaling limitations of silicon have inspired researchers to seek out new materials that can surpass these barriers and unlock enhanced performance and efficiency. In this pursuit, the spotlight has fallen on a remarkable class of materials known as 2D materials, with Transition Metal Dichalcogenides (TMDs) at the forefront. These atomically thin materials have garnered substantial attention due to their unique properties and potential for revolutionizing various technological applications. This internship report presents an analysis of the vertical back-end-of-line (BEOL) integration of a two-dimensional material (2DM) based pass transistor in a 6T static random-access memory (SRAM) circuit with an emphasis on circuit simulation, extra interconnect delay, performance evaluation, and physical 3D layout model considerations. The objective of this internship was to assess the feasibility and performance implications of the new BEOL integration technique for SRAM designs.

The internship encompassed various tasks, including an extensive literature review, circuit simulation utilizing advanced tools and models, assessment of the extra interconnect delay introduced by the BEOL integration, comprehensive performance evaluation of the integrated SRAM circuit, and meticulous development of a physical 3D layout model. The findings of this internship report provide valuable insights into multiple aspects of the new BEOL integrated SRAM. Firstly, through thorough circuit simulation, the electrical behavior and performance characteristics

of the SRAM circuit were meticulously analyzed, encompassing parameters such as read and write access times, power consumption, stability, and susceptibility to parasitic effects. Moreover, the investigation of the extra interconnect delay resulting from the new BEOL integration enabled a comprehensive evaluation of potential performance bottlenecks and trade-offs, taking into account the influence of parasitic effects. The report also delves into the development of a physical 3D layout for the integrated SRAM design, with meticulous attention given to minimizing parasitic effects through proper component placement, routing strategies, and signal integrity considerations.

In conclusion, this internship report presents a detailed analysis of a novel BEOL integrated SRAM circuit, considering circuit simulation, extra interconnect delay, performance evaluation and physical 3D layout considerations, . The insights gained from this analysis contribute to a comprehensive understanding of the performance implications, design challenges, and parasitic limitations associated with the new BEOL integration technique. This information is pivotal for future research and development endeavors in the field of SRAM circuit design and optimization, specifically addressing the impact of parasitic effects.

CHAPTER 1

INTRODUCTION

In today's rapidly evolving technological landscape, the demand for high-performance integrated circuits continues to grow exponentially. This demand is driven by advancements in areas such as artificial intelligence, cloud computing, and Internet of Things (IoT), where efficient data processing and storage are crucial. Static random-access memory (SRAM) serves as a fundamental component in these systems, providing fast, on-chip memory for temporary data storage.

The continuous improvement of SRAM performance, in terms of access times, power consumption, and density, has been a critical objective in the field of semiconductor technology. This drive for improvement is closely tied to Moore's Law [1], which states that the number of transistors on a chip doubles approximately every two years, leading to increased computational power and storage capabilities.

However, as Moore's Law approaches physical limitations, traditional transistor scaling has become increasingly challenging. Shrinking the feature size of transistors, as dictated by Moore's Law, faces obstacles such as increased leakage currents, thermal issues, and quantum effects [2]. These challenges have prompted researchers and engineers to explore alternative strategies for enhancing circuit performance. In parallel, the scaling of memory devices, including SRAM, has become a significant concern. As technology nodes shrink, memory cells must also scale to maintain reasonable area requirements while meeting performance targets. The scaling of SRAM faces challenges such as increased leakage current, reduced noise margins, and degraded stability. Overcoming these challenges is essential for the continued advancement of memory technologies and the realization of high-performance computing systems. One area of focus is the back-end-of-line (BEOL) integration, which deals with the interconnects and metal layers that link transistors within the chip. BEOL integration plays a crucial role in the overall per-

formance and density of integrated circuits, and innovative techniques in this domain have the potential to overcome some of the limitations of transistor scaling.

The motivation behind this internship project is to explore the feasibility and performance implications of vertically integrating (3D Integration [3]) a 2D material-based pass transistor, specifically MoS₂, within the BEOL process of an SRAM circuit [4] [5]. By incorporating novel materials and exploring alternative integration techniques, the aim is to overcome the limitations posed by traditional transistor scaling and enhance the performance of SRAM.

By investigating the integration of 2D materials in SRAM design, this project aims to contribute to the understanding of how BEOL integration and innovative material choices can advance SRAM scaling and overall circuit performance. The findings from this research can provide valuable insights for future advancements in memory technologies and contribute to the ongoing efforts to meet the demands of Moore's Law and the ever-evolving computational landscape.

1.1 Objectives of this Report

- Investigate the feasibility of integrating a two-dimensional material (2DM) based pass transistor within the vertical back-end-of-line (BEOL) process of a 6T static random-access memory (SRAM) circuit.
- Develop a physical 3D layout model for the integrated SRAM design, considering the constraints and requirements of the 2DM pass transistor and optimizing the placement and routing of components to minimize parasitic effects and enhance performance.
- Investigate and quantify the extra interconnect delay introduced by the BEOL integration process and its implications for the performance of the SRAM circuit.
- Perform circuit simulations using appropriate tools and models to validate the electrical behavior and performance metrics of the 6T SRAM circuit, accounting for the impact of the 2DM pass transistor integration and extra parasitic effects.
- Assess the impact of the 2DM pass transistor integration on the overall circuit performance, specifically focusing on read and write

Chapter 1. Introduction

access times, power consumption, and stability of the integrated 6T SRAM circuit.

- Compare the performance of the 2DM-based integrated SRAM circuit with conventional SRAM designs, highlighting the advantages and potential trade-offs associated with the novel integration technique.
- Contribute to the advancement of SRAM design by providing valuable information and recommendations for future research and development in the field of 2DM-based transistor integration and optimization.

CHAPTER 2

Literature Review

2.1 SRAM

2.1.1 Introduction

Currently, SRAM plays a dominant role in System-on-Chip (SoC) architectures, occupying more than 50 percent of the die area and around 70 percent of the transistor count in modern microprocessors. As technology advances, the demand for memory in SoC applications continues to rise. Traditionally, transistor sizing, also known as cell sizing, has been employed in SRAM to optimize various factors such as cell area, noise immunity, write ability, speed, and power.

Moore's Law has driven the semiconductor industry for over three decades, with transistor size reduction enabling cost reduction and technological advancements. However, the physical limitations associated with further size reduction have made it increasingly challenging to maintain the same pace. Variations in circuit fabrication, both global and local, have significant impacts on performance and manufacturing yield. As a result, relying solely on transistor size reduction is no longer sufficient, and new approaches are needed to achieve further scale reduction. Performance dispersion is a major challenge in SRAM design, and the escalating process costs suggest a slowdown in Moore's Law as previously insignificant physical limitations become more apparent.

In light of these considerations, exploring innovative techniques such as vertical Back-End-of-Line (BEOL) integration of pass transistors for SRAM scaling becomes crucial. This approach aims to address the challenges associated with variability and transistor scaling, offering new opportunities for reducing SRAM area and improving overall performance and yield. By integrating pass transistors in a vertical configuration within the BEOL process, novel solutions can be devised to enhance

SRAM scalability while mitigating the limitations imposed by traditional scaling techniques.

2.1.2 6T SRAM CELL

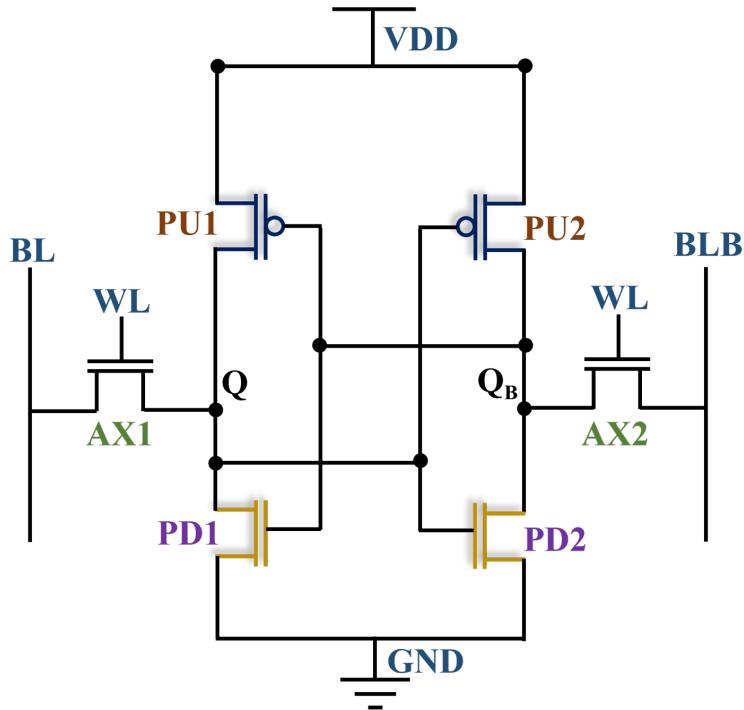


Figure 2.1: 6T SRAM Schematic

The traditional configuration of SRAM bit-cell, known as 6T-SRAM, consists of six transistors. This includes two CMOS inverters formed by pull-up (PU) and pull-down (PD) transistors, as well as two access transistors represented by AX (access transistors). The main functions of the bit-cell encompass writing data into the cell, retaining the stored data, and reading the bit data. These operations are governed by word lines that activate or deactivate the access transistors (AX), thereby establishing or interrupting the connection to the bit-lines (BL and BLB). The bit-lines are responsible for transmitting the bit value to or from the bit cell. In terms of the influence of process variation, the read and write operations hold significant importance within the context of 6T SRAM.

2.1.3 Read Operation

The process of reading data from an SRAM involves two main steps. Firstly, the bit lines are initially charged to the supply voltage, V_{DD} .

Chapter 2. Literature Review

Then, the word line is activated, turning on the access transistors and establishing a connection between the bit lines and the memory cells. Depending on the stored value in the memory cell, the voltage on the bit lines will vary. For instance, if the memory cell contains a 1, the voltage on the corresponding bit line will be high. To detect and interpret the voltage difference between the bit lines, a voltage-sense amplifier is employed.

Among the various operations in an SRAM, the read operation is known to have the highest potential for compromising data integrity. This is primarily due to the activation of access transistors during the read process, which can inadvertently create a current path capable of flipping the stored data at the storage node. As a result, there is a risk of losing the intended value stored in the memory cell. Therefore, it becomes crucial to carefully and accurately size the access transistors to mitigate this issue and ensure reliable data retention in the memory cell.

2.1.3.1 Read Static Noise Margin

RSNM (Read Static Noise Margin) assesses the stability of an SRAM bit-cell during the read operation. It is calculated by finding the largest square within the memory's static transfer function, known as the butterfly curve. This curve represents the behavior of the cell during reading. RSNM indicates the reliability and robustness of the bit-cell. During

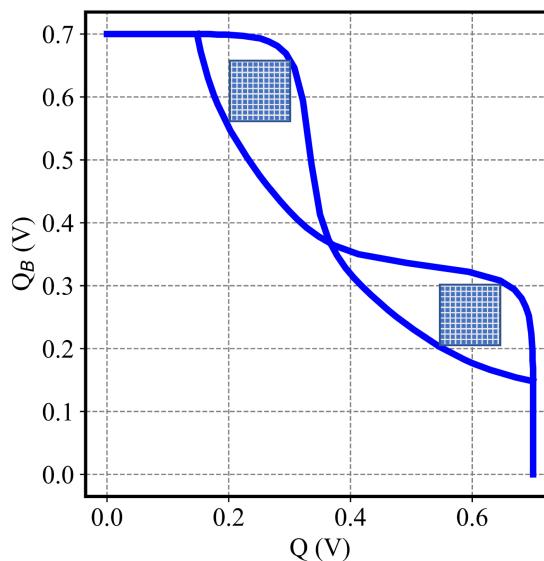


Figure 2.2: Butterfly curve to calculate RSNM of 6T SRAM.

reading, the bit lines (BL and BLB) are precharged to a "1" state (V_{DD}).

The word line (WL) is then activated. If the stored data in the cell (Q) is "0," the BL line discharges through the AX1 pass-gate and PD1 pull-down transistors. The sense amplifier measures the voltage difference between BL and BLB. Minimizing the nonzero read disturb voltage in the data storage node Q is important to prevent data flipping.

RSNM is calculated by fitting the maximum square within the butterfly curve, obtained by sweeping the Q node voltage from "0" to V_{DD} . It evaluates the SRAM's ability to read data reliably.

2.1.4 Write Operation

The write operation is a crucial step in storing data within a 6T SRAM cell. This cell comprises six transistors arranged in a cross-coupled configuration, which plays a vital role in the process. To initiate the write operation, the wordline (WL) associated with the specific memory cell is activated. This activation enables access to the cell, allowing data to be written into it. By activating the wordline, the access transistor establishes a connection between the bit-lines (BL and BLB) and the cell.

For example, if we want to write a logical zero (0) to the cell, the BL (bit-line) is set to a lower voltage level, while the BLB is maintained at a higher voltage level. This arrangement ensures that the cross-coupled inverters within the cell settle into a stable state. In this state, the output of the inverter connected to the bit-line becomes high, while the output of the inverter connected to the BLB becomes low. As a result, the 6T SRAM cell stores the logical zero (0), replacing the previous logical one (1) that may have been stored.

2.1.4.1 Write Static Noise Margin

The write margin (WM) is a measure of the ease with which data can be written to a memory. In other words, the write noise margin is defined as the minimum bitline voltage needed to flip the state of cell. Various definitions of WM have been proposed in the literature for static random access memory (SRAM) cells [6] [7]. The commonly used definition is based on the "butterfly curve." To calculate the write margin, the Q and QB nodes are initialized, and the word line voltage is swept while keeping BL at 0 V and BLB at V_{DD} . The write margin is defined as the difference between V_{DD} and the voltage at which Q and QB switch together.

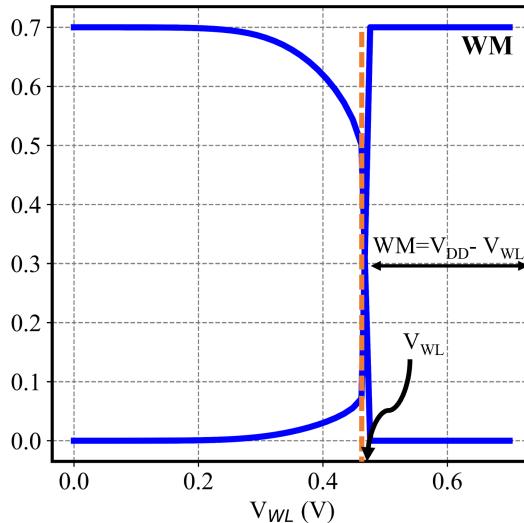


Figure 2.3: Write margin calculation for 6T SRAM.

2.2 Semiconductor Process

The semiconductor manufacturing process involves two essential stages: front-end-of-line (FEOL) and back-end-of-line (BEOL) integration. While the FEOL process focuses on the fabrication of transistors and active components, the BEOL process stage is responsible for interconnecting these components and creating functional electronic circuits.

During the FEOL stage, silicon-based technology, such as metal oxide semiconductor field-effect transistors (MOSFETs) and complementary metal oxide semiconductor (CMOS) technology, is employed to fabricate transistors and other active devices. This stage involves processes like photolithography, etching, and implantation to define the transistor features and create the desired electrical characteristics.

Following the FEOL stage, the BEOL integration stage comes into play. It encompasses the integration of various components, including transistors, resistors, capacitors, and interconnects, to establish electrical connectivity and create functional circuits. This process involves multiple metal layers, dielectric materials, and insulating layers to form interconnections and provide isolation between different circuit elements.

2.2.1 BEOL Integration

The primary objectives of BEOL integration are to establish low-resistance electrical connections, minimize signal delay and loss, manage power

Chapter 2. Literature Review

distribution, and ensure robust functionality of the integrated circuit. Achieving these goals requires careful consideration of factors such as signal integrity, power dissipation, thermal management, and reliability. As technology advances and device dimensions shrink, BEOL integra-

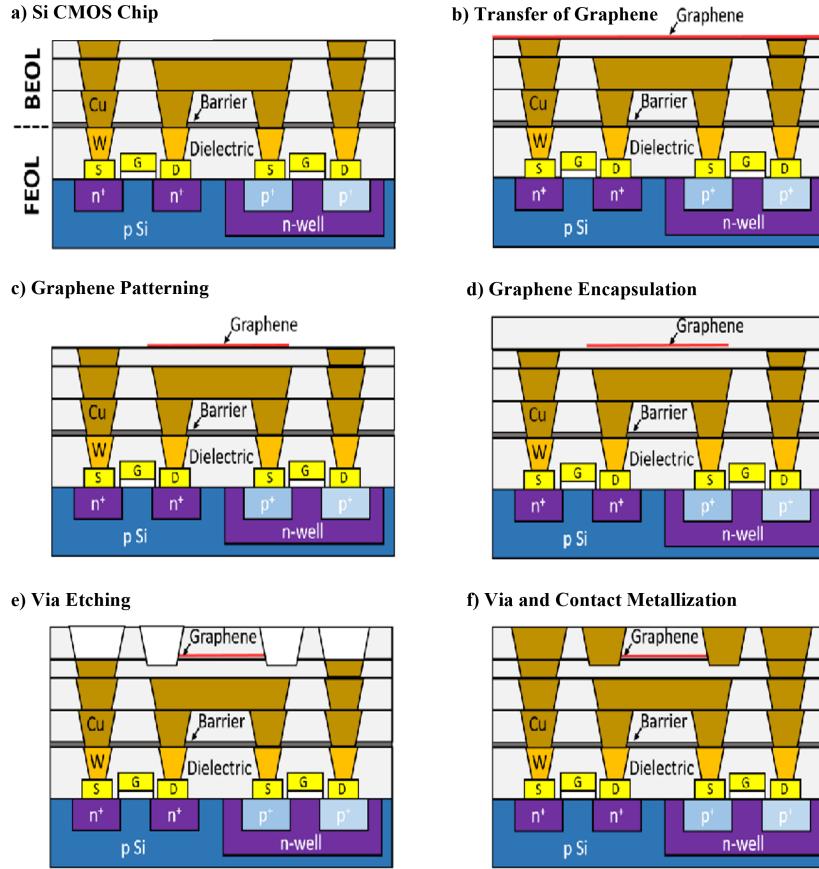


Figure 2.4: Flow Chart of BEOL Integration of Graphene[8]

tion becomes increasingly complex. The fig 2.4 shows the flow of integration of graphene in BEOL of a CMOS [8]. The continued scaling of transistors and the increasing integration density demand innovative techniques to overcome challenges associated with interconnect resistance, parasitic capacitance, crosstalk, and reliability issues. These challenges necessitate the development of advanced materials, processes, and design methodologies to ensure optimal circuit performance. In this internship, the focus lies on the BEOL integration of a 2D material (2DM)-based pass transistor in the context of static random-access memory (SRAM). The incorporation of 2DM materials, such as graphene or transition metal dichalcogenides (TMDs) like MoS₂, has gained significant attention due to their unique electrical properties, scalability, and po-

tential applications in nanoscale electronic devices [9].

The objective of this internship is to investigate the feasibility and performance implications of integrating a 2DM-based pass transistor within the BEOL process of an SRAM circuit. This integration involves integrating the pass transistor along with other circuit components, interconnects, and metal layers to establish the necessary electrical connections and achieve functional integration.

2.3 Introduction to 2D Materials

2D materials are a class of materials that exhibit unique properties due to their ultra-thin structure, typically consisting of a single layer or a few layers of atoms. These materials, such as graphene and transition metal dichalcogenides (TMDs) like MoS₂, possess exceptional electrical, mechanical, and optical characteristics [10]. The 2D nature of these materials allows for efficient electron transport and provides opportunities for novel device architectures and integration in electronic systems. MoS₂, a well-studied TMD, has gained significant attention as a promising material for transistor applications. MoS₂-based 2D transistors [11] exhibit remarkable electrical properties, including high carrier mobility, low leakage current, and excellent electrostatic control. These properties make MoS₂ transistors attractive for high-performance and low-power electronic devices. By integrating MoS₂-based 2D transistors in SRAM, researchers aim to explore and harness the potential benefits of this innovative material system to enhance the performance, power efficiency, scalability, and reliability of SRAM devices.

2.4 Conclusion

In this chapter, we presented the 6T SRAM and its operation and stability metrics. We have also gone through the process of BEOL integration of electronic devices during manufacturing process and also had a look on suitable 2D material that could be beneficial in the integration and performance of the overall device.

CHAPTER 3

BEOL Integration of MoS₂ Transistor and SRAM Layout Model

The focus of the previous chapter was to present a detailed idea of the 6T SRAM and the basics of BEOL integration of devices. In this chapter, we further delve into the design of 6T SRAM using 2D material-based FET technology in BEOL and explore the impact on its overall stability and also modelled the layout for the same.

3.1 Introduction

Advancements in technology scaling have driven researchers and industries to seek alternatives to conventional silicon channel FETs. A promising avenue that has gained traction is the utilization of atomically thin two-dimensional (2D) materials in FETs, especially for gate lengths below 10 nm. Among the various 2D materials, monolayer MoS₂ has attracted considerable interest following the successful demonstration of a functional n-channel monolayer MoS₂ FET. In the realm of advanced technology nodes and extremely scaled channel lengths, 2D materials like molybdenum disulfide (MoS₂) offer improved electrostatic control compared to Silicon FinFETs, thereby providing greater immunity to short-channel effects [12]. This results in reduced leakage current and a higher ratio of ON current to OFF current.

The Six Transistor (6T) SRAM is a highly utilized memory technology due to its efficient power consumption and fast access time. It holds significant importance in modern computer systems, particularly in cache memory, contributing to their enhanced speed. In this chapter we have discussed about the vertical back end of the line (BEOL) integration of MoS₂ pass transistor in 6T SRAM cell and evaluated its impact on the overall cell.

3.2 BEOL Integration of MoS₂ Transistor in SRAM

We embarked on an exciting project focused on advancing the integration of MoS₂ transistors within the Back-End-of-Line (BEOL) structure of SRAM. Our objective was to explore the immense potential and benefits that MoS₂, a two-dimensional material, could offer to enhance the performance and capabilities of SRAM. To achieve this, we strategically integrated the MoS₂ transistor at the BEOL process. In this design, an SRAM-like silicon front-end-of-line (FEOL) circuit was combined with two additional BEOL MoS₂ transistors fabricated on top of the silicon FEOL circuit. [4]

The SRAM circuit comprised two silicon nMOSFETs and two silicon pMOSFETs in the FEOL portion, which formed the core functionality of the memory cell. These silicon-based transistors were responsible for the read and write operations in the SRAM.

To further enhance the performance and functionality as well as the area scaling of the SRAM, two additional MoS₂ transistors were integrated within the BEOL layers. These MoS₂ transistors were fabricated on top of the silicon FEOL circuit, adding an extra layer of functionality to the design.

By incorporating MoS₂ transistors in the BEOL structure, the SRAM design aimed to leverage the unique properties of the material, such as its atomically thin nature and excellent electrical characteristics. The integration of MoS₂ transistors within the BEOL layers provided an opportunity to explore new approaches to optimize the SRAM performance, such as reducing power consumption, enhancing stability, and improving area efficiency as compared to traditional SRAM cell.

3.3 SRAM Layout Model

In this project, we tried to create a three-dimensional (3D) layout model and aerial view of the Back-End-of-Line (BEOL) integrated 2D-material-based pass transistor within a 6T SRAM. The integration of the pass transistor in the BEOL layers brought a new dimension to the SRAM design, enabling enhanced performance and scalability.

Initially, we tried to make a probable 2D layout model of the SRAM to get an overview of the BEOL integrated device. We looked into the

possible arrangement of the various nodes like BL,BLB,WL,VDD etc. for a more realistic model.

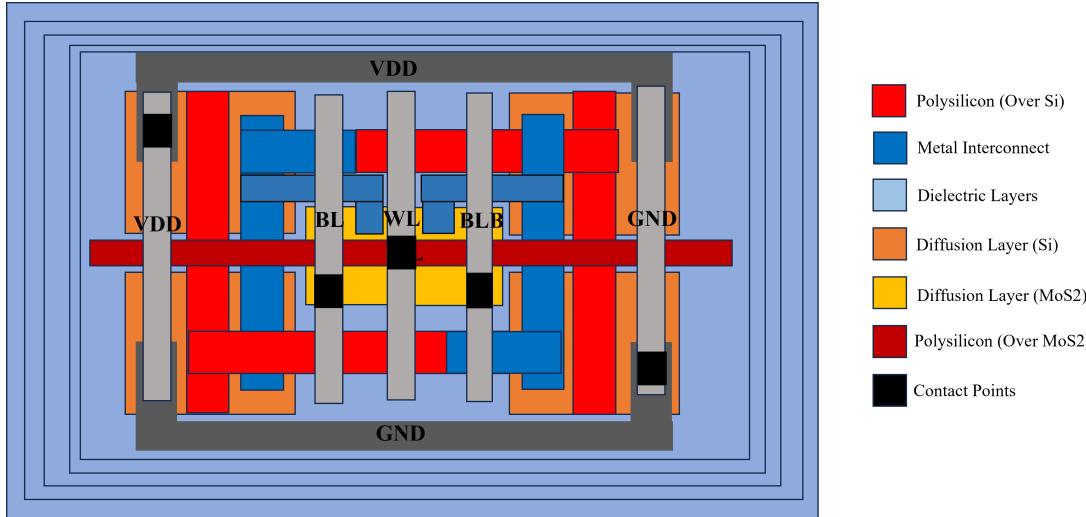


Figure 3.1: 2D Layout of the BEOL Integrated SRAM Device

Moving forward ,we delved into the probable 3D model for more accurate understanding of the interconnect level.The 3D layout provided a comprehensive representation of the physical arrangement of the pass transistor within the SRAM structure. It showcased the intricate interconnections, layer stacking, and spatial organization of the pass transistor and other components, giving insights into the chip's architecture. This layout visualized the precise positioning of the pass transistor in relation to the other elements, allowing for meticulous optimization and refinement of the design.

In addition to showcasing the physical arrangement and integration of the pass transistor within the 6T SRAM, the 3D layout and aerial view also highlighted the interconnect design. These visual representations provided insights into the pathways and connections between various components, enabling a comprehensive understanding of the interconnectivity within the SRAM design. Furthermore, the layout and aerial view revealed that the BEOL-integrated 2D-material-based pass transistor offered advantages in terms of a reduced footprint compared to traditional 6T SRAM designs. The integration of the pass transistor within the BEOL layers allowed for a more compact and efficient layout, optimizing the use of available space on the chip. This reduction in area was a significant achievement as it contributed to higher integration levels and improved overall chip performance.

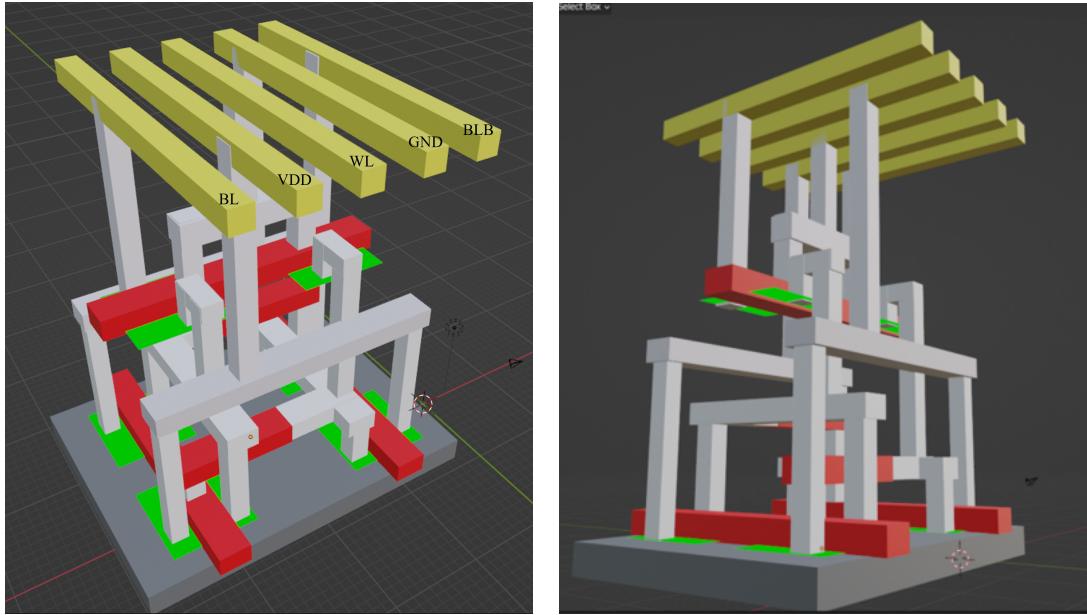


Figure 3.2: 3D Layout Model of SRAM with MoS₂-FET Integrated at BEOL(1)

Figure 3.3: 3D Layout Model of SRAM with MoS₂-FET Integrated at BEOL(2)

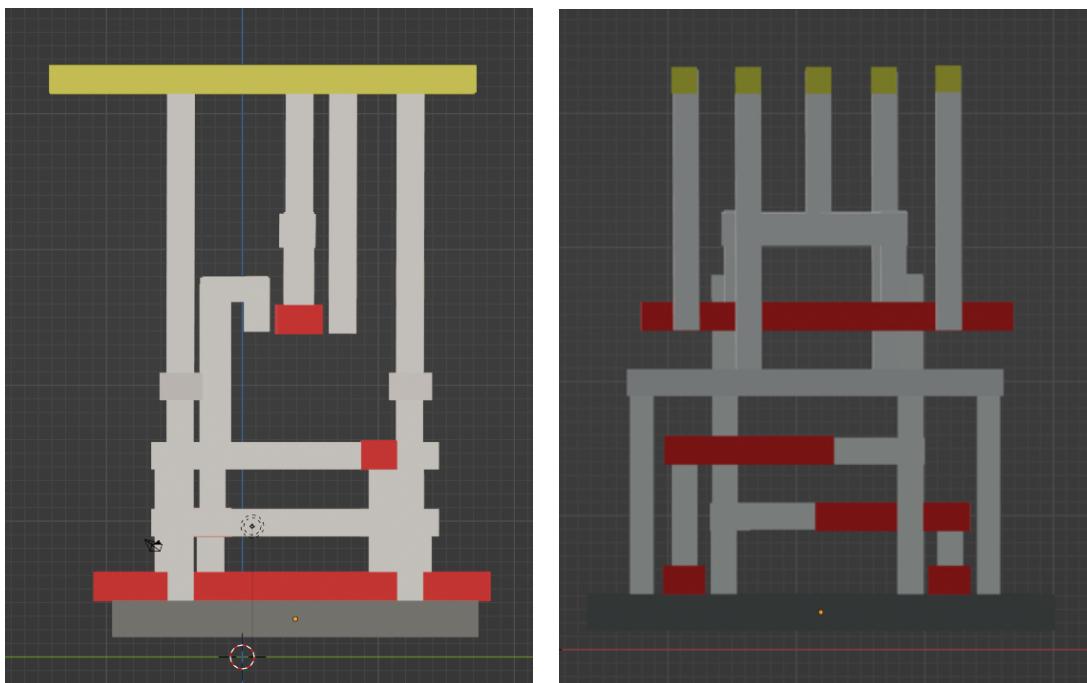


Figure 3.4: Side View of 3D Layout Model of SRAM with MoS₂-FET Integrated at BEOL(1)

Figure 3.5: Side View of 3D Layout Model of SRAM with MoS₂-FET Integrated at BEOL(2)

3.4 Additional Parasitics

The integration of the BEOL 2D transistor within the 6T SRAM design introduces additional interconnects to establish connections with the transistor. While this integration brings numerous benefits, such as improved performance and scalability, it also introduces extra parasitic resistance and capacitance that need to be considered.

Addressing the extra parasitic resistance and capacitance introduced by the additional interconnects is crucial for maintaining the desired performance and functionality of the 6T SRAM. These extra parasitics can lead to delay in access time and other performance degradation [13]. Advanced design techniques, such as employing low-resistance materials, optimizing interconnect layout, and implementing effective shielding and isolation techniques, can help mitigate these parasitic effects. Additionally, accurate modeling and simulation techniques can be employed to predict and analyze the impact of these parasitic elements on the overall performance of the SRAM.

3.4.1 Parasitic Extraction

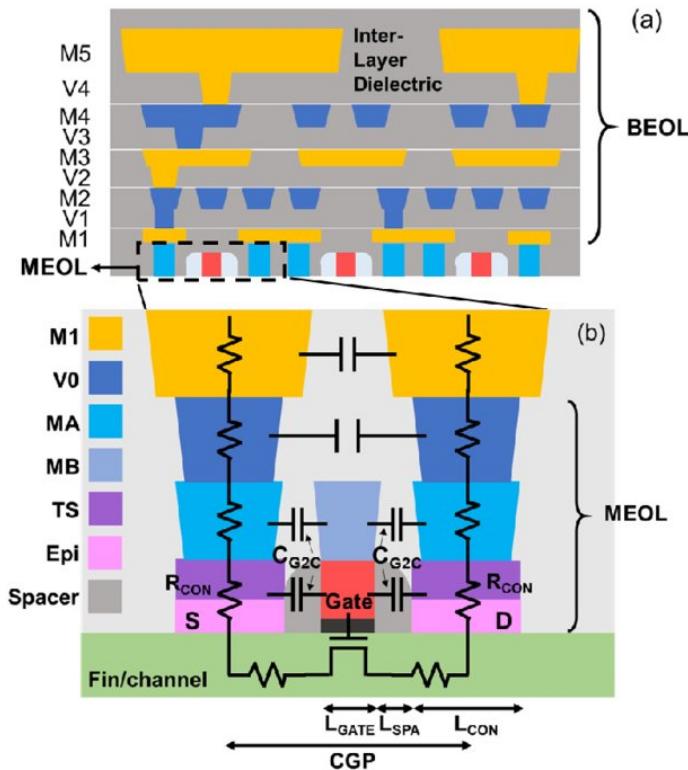


Figure 3.6: . Illustration of (a) BEOL interconnects and (b) MEOL interconnects and cell-level parasitic RC[14]

In order to realistically analyze the stability and reliability of the device, accurate modelling and high efficiency parasitic parameter extraction are needed for the chip interconnect. The typical model of the parasitic resistance and capacitance produced due to the metal contacts and interconnects can be seen from the figure 3.6 [14]. As per the figure, it has divided the interconnects, conceptually, into two parts as local middle-end-of-line (MEOL) and intermediate/global back-end-of-line (BEOL) interconnects. In our work, we mainly tried to deal with the BEOL interconnects as there is some extra interconnects are produced due to the vertical integration.

3.4.1.1 Analytical Method of Parasitic Extraction

Parasitic extraction through analytical methods is a technique used to estimate the parasitic resistance and capacitance in interconnect structures. Analytical methods aim to provide approximate calculations based on mathematical equations and physical principles like finite element method, finite difference method etc.

In this approach, the geometric parameters of the interconnect structure, such as length, width, and thickness, are used as inputs to determine the parasitic parameters. Various analytical models and equations, such as the Wheeler's model or the Haney and Scharfetter model, are employed to calculate the resistance and capacitance values of the cell. While calculating the capacitance due to interconnects in CMOS technology, there are two kinds of parasitic capacitances: parallel plate capacitances which can be evaluated by classical equation and perpendicular plates capacitances (Fringe Capacitances) that can be evaluated with conformal mapping which is properly illustrated in [15] [16]. The general idea of the interconnect capacitances can be understood from

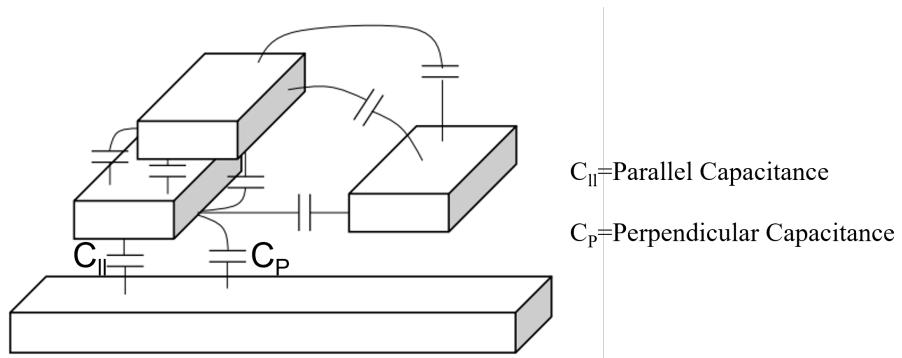


Figure 3.7: Showing Capacitances Produced due to the Arrangement of Interconnects[17]

the figure 3.7 [17].With the help of the respective equations of the both type of capacitances ,we can calculate the parasitic at different level.

3.4.1.2 Extraction Through EDA Tools

However, it's important to note that the accuracy of analytical methods may vary depending on the complexity of the interconnect structure and the accuracy of the assumptions made. For more precise parasitic extraction, advanced simulation tools like field solvers or commercial software tools such as Synopsis Raphael or Star RCX are often employed. These tool basically employ the 3D model of the interconnect on the basis of scaled layout,netlist templates and an ITF (Interconnect Technology Format) file,which includes the dimensions, resistivities, and dielectric constants of each layer, and hence performs the cell level parasitic extraction to generate extracted SC netlists with all the parasitic RCs [14]. Further these netlists can be implemented in Cadence environment or in Spectre netlist simulation of the device to get the performance analysis.

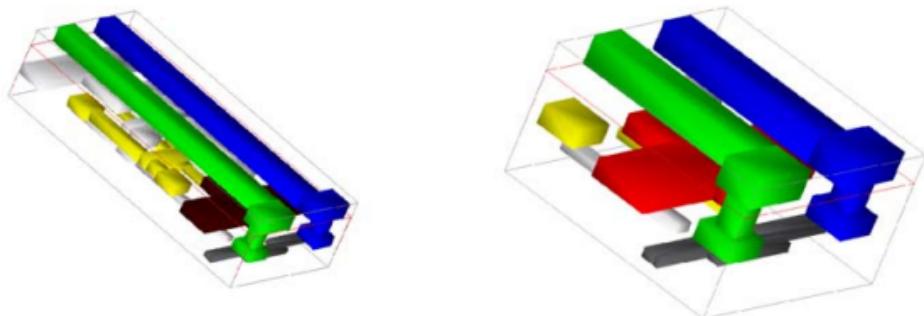


Figure 3.8: An Example of 3D Interconnect Model Developed in Raphael

3.5 Conclusion

In this chapter we thoroughly discussed about the integration of the MoS₂ transistor in SRAM and also looked on the layout for the same.Again we discussed thoroughly the methods for the extraction of parasitics and its implementation in the simulation model.Furthermore we will discuss the analysis of the the performance of the SRAM cell.

CHAPTER 4

Circuit Simulation and Performance Analysis

In the preceding section, the Back-End-of-Line (BEOL) integration of a pass transistor was examined, including its layout and the discussion of its parasitic effects. In this chapter, comprehensive circuit simulations were conducted utilizing Cadence and Spectre netlist tools [18]. These simulations aimed to analyze diverse facets of Static Random-Access Memory (SRAM) operation, encompassing read and write access times, power consumption, stability, as well as noise behavior.

4.1 Introduction

Circuit simulation plays a crucial role in the analysis and optimization of Static Random-Access Memory (SRAM) designs. SRAM is a key component of many electronic systems, used for storing data in digital circuits. By employing circuit simulation techniques, engineers can assess various aspects of SRAM operation, including read and write access times, power consumption, stability, and noise behavior.

Through the use of specialized simulation tools like Cadence and Spectre netlist, we can create accurate models of SRAM circuits and analyze their behavior under different conditions. Simulations enable the evaluation of critical performance parameters such as the speed at which data can be read from or written into the SRAM cells. This information helps in optimizing the SRAM design to achieve faster access times and improved overall system performance.

In this project, our aim was to perform a comprehensive analysis and comparison of the performance characteristics of the MoS₂-Si integrated SRAM with different types of conventional SRAM. Specifically, we investigated the performance of the pure Silicon (Si) based SRAM, the purely

Molybdenum Disulfide (MoS_2) based SRAM, with the SRAM configuration that integrated MoS_2 pass transistors with Si transistors through Back-End-of-Line (BEOL) integration. Our analysis focused on evaluating key performance metrics such as read and write stability, delay, and power consumption. Importantly, all of these Si transistor designs were based on the Si umc28 nm technology, allowing for a fair and direct comparison of their performance characteristics.

4.2 Simulation Methodology

In this study, we utilized Cadence-Virtuoso, a widely adopted circuit simulation tool, to thoroughly examine the feasibility and performance of the integrated SRAM model as previously described. To accomplish the comprehensive circuit simulation of the device, we followed a systematic methodology consisting of the following steps:

4.2.1 MoS_2 Device Modelling

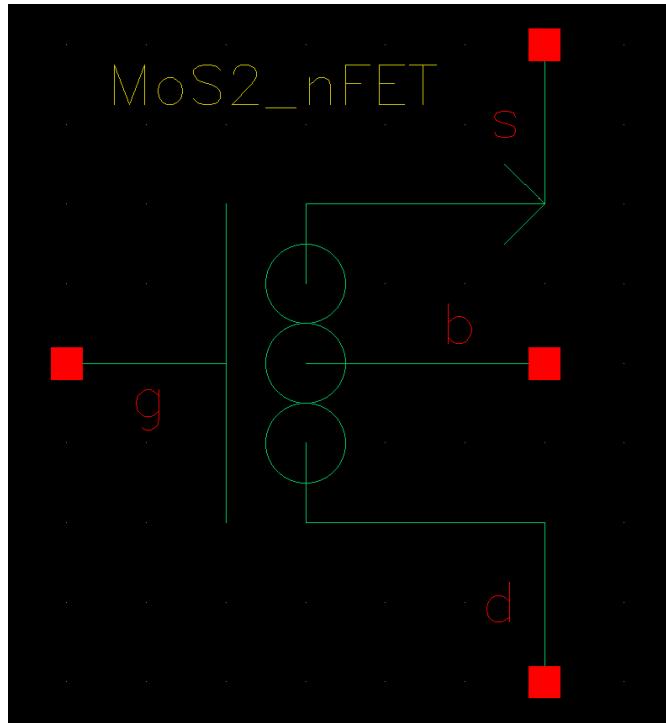


Figure 4.1: Schematic of MoS_2 nFET Imported to Cadence

The first step in our simulation methodology involved the development of precise device models for the MoS_2 -based pass transistor. To

achieve this, we gathered a verilog-A file that implemented a 2D FET using MoS₂, incorporating experimental parameters such as a gate length of 12nm, a width of 282nm, and an oxide thickness of 2.8nm. The transistor was designed to operate within a supply voltage range of 700mV. Subsequently, we imported the verilog-A file into the Cadence library and thoroughly assessed its suitability for integration into the schematic diagram, ensuring its feasibility for subsequent usage.

4.2.2 Schematic Design

As previously mentioned, as part of the integration process, we have replaced the Si-based nMOS pass transistor of the SRAM with a suitable MoS₂-based 2D nMOS transistor. Consequently, in the schematic design of the 6T SRAM, we have incorporated two cross-coupled CMOS inverters, which consist of conventional Si-based nMOS and pMOS transistors fabricated using the FEOL process. These inverters have been strategically connected with the MoS₂-based nMOS transistor at the pass transistor position, as depicted in the schematic diagram (refer to the figure).

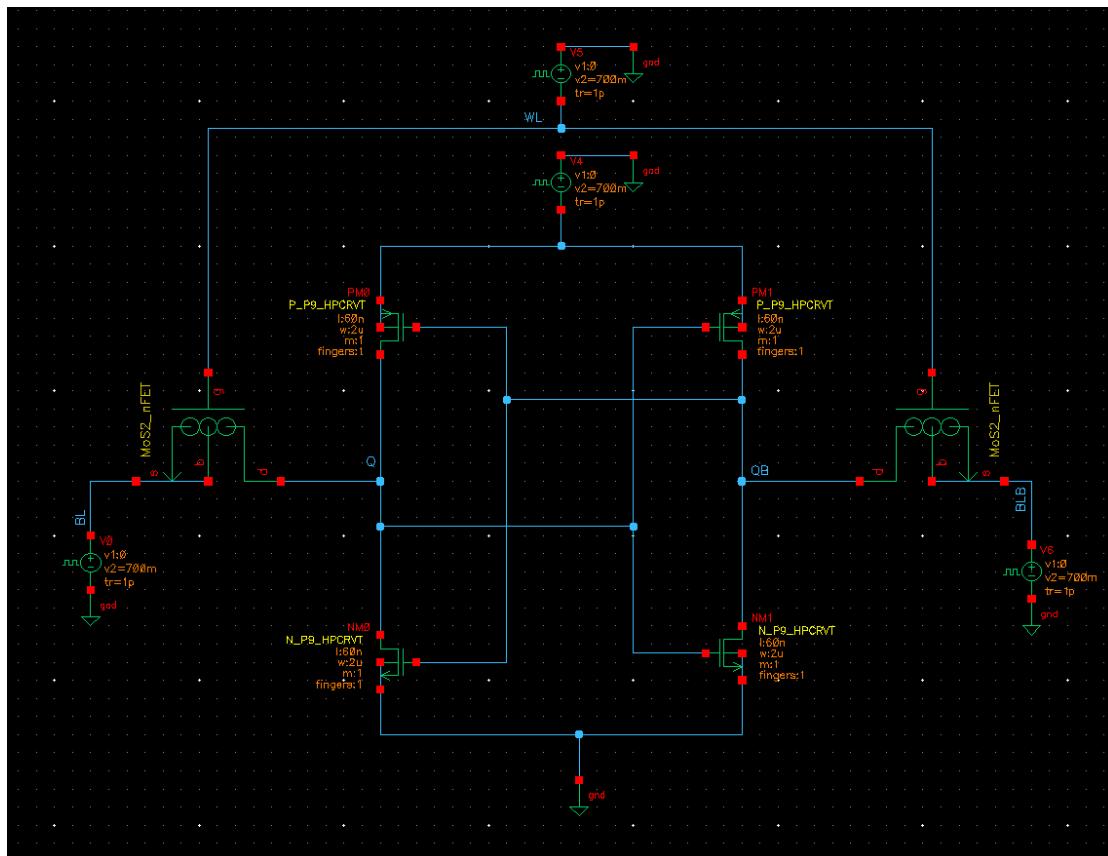


Figure 4.2: Schematic Diagram of a 6T SRAM Containing MoS₂ nFET at the Pass Transistor Position

To ensure compatibility and optimal performance, we selected the UMC28nm technology for the Si CMOS transistors, which have a gate length of 60nm and a width of 2um. This choice was made due to the comparable supply voltage of 900mV, which closely aligns with the operating characteristics of the MoS₂-FET, facilitating the proper functioning of the overall SRAM device. Subsequently, we established the necessary connections for the supply voltage to the respective nodes of BL (Bit Line), BLB (Bit Line Bar), WL (Word Line), and VDD, meticulously verifying the proper wiring for the seamless operation of the 6T SRAM.

To ensure the accuracy and integrity of the schematic design, the aforementioned steps were implemented within the Cadence tool, leveraging its capabilities for creating and validating the circuit diagram.

4.2.3 Simulation Setup

The simulation environment is configured to conduct circuit-level simulations. The necessary parameters, including supply voltage, temperature, and input stimulus, are defined. Within the Cadence simulation setup, relevant configurations were implemented to accurately capture the behavior and characteristics of the SRAM design. The chosen parameters, such as supply voltage, were set to match the intended operating conditions, ensuring realistic simulation results. To analyze read and write noise, specific test scenarios were created, simulating data read and write operations while monitoring the noise levels present in the SRAM circuit. Additionally, transient analysis was performed to evaluate the dynamic response of the SRAM circuit under varying input stimuli.

4.2.4 Transient Analysis

Transient analysis is a critical simulation technique that captures the circuit's response over time, providing valuable insights into voltage waveforms, current waveforms, and timing characteristics. In our study, we conducted transient analysis to assess the behavior and feasibility of the integrated SRAM design.

To accurately represent the operating conditions of both Si and MoS₂ transistors, we applied a dc pulse voltage ranging from 0 to 900mV during the transient analysis. This voltage range ensured proper functioning of the SRAM and allowed us to evaluate its performance under

realistic conditions. The transient analysis results were graphically represented, showcasing voltage waveforms of BL, BLB, Q and QB. The provided figure visually depicts the transient analysis of the SRAM, offering a comprehensive representation of its dynamic behavior.

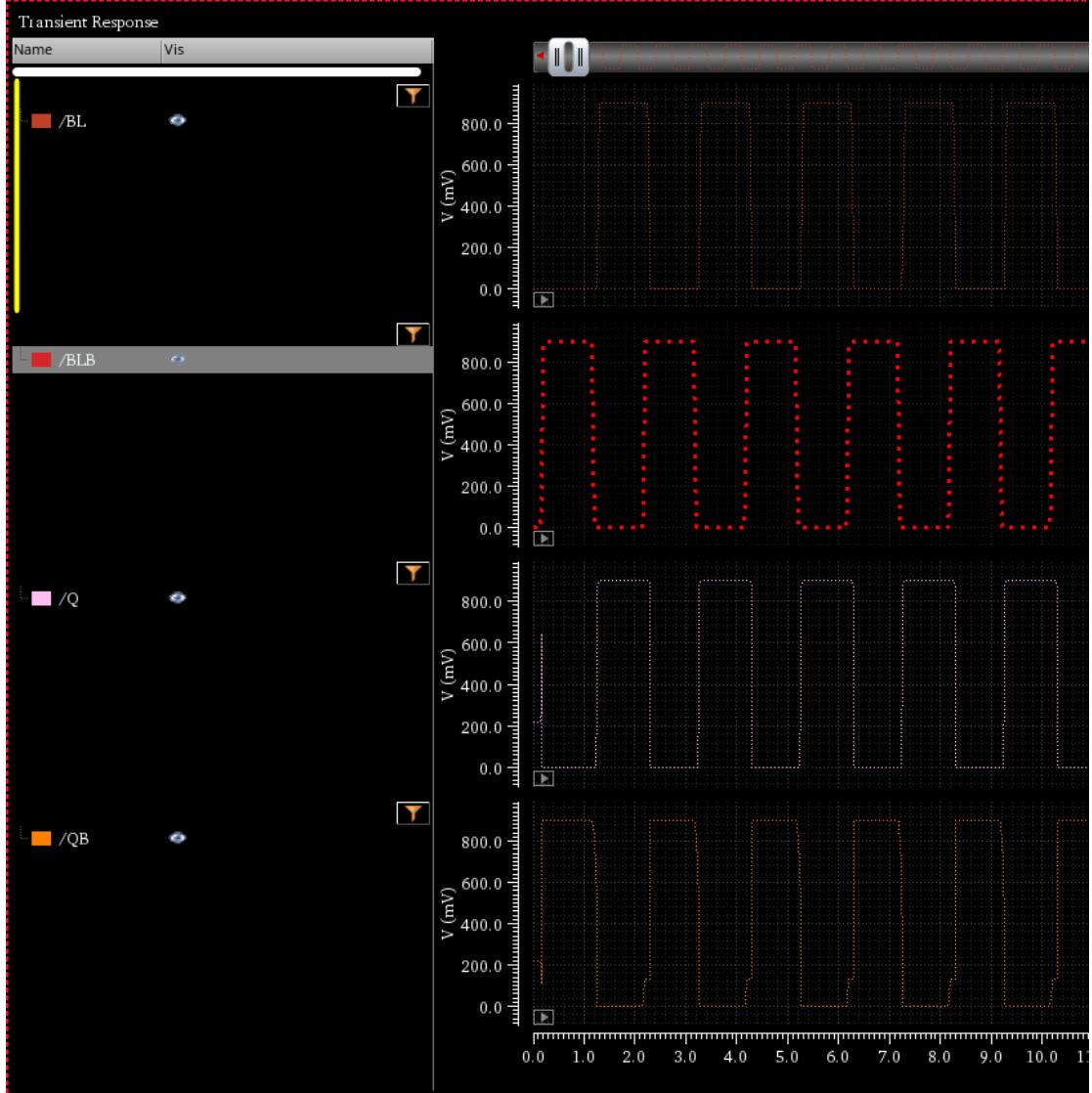


Figure 4.3: Transient Analysis Result for 6T SRAM (without parasitics)

4.2.5 Noise Margins

Analyzing the read and write margin is crucial as it directly correlates with the robustness of the device. Therefore, we conducted thorough simulations to evaluate these parameters within the integrated SRAM design.

For read operation the bit and bit bar were held high i.e were given the supply voltage of 700mV and the point Q was swept from 0 to 700mV

for the analysis. The read curve for SRAM was plotted and the respective read margin was calculated by fitting the largest square inside the butterfly curve(Graphical Method of Noise Margin Calculation). For a gate length of 12nm and width of 282nm of the MoS₂ nMOS transistor, the RSNM was calculated to be around 192mV. Additionally, we can calculate the write margin by setting one of the bits to a low voltage level while sweeping both Q and QB. This analysis provided insights into the device's ability to reliably flip the data. The calculation of noise margin

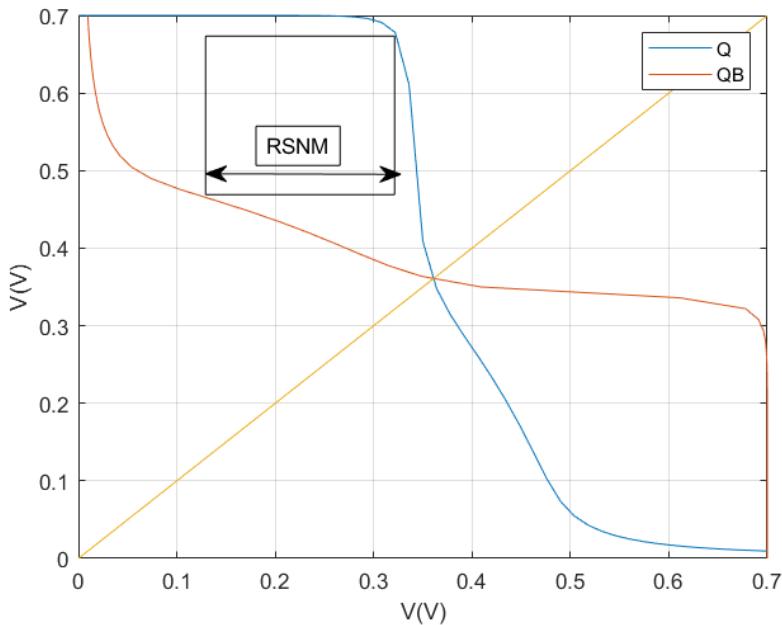


Figure 4.4: Read Margin for 6T SRAM having MoS₂ nFET Pass Transistor with width of 282nm

offers an approximate understanding of the device's robustness in terms of data stability. To gain a comprehensive understanding, we will later compare these results with those obtained from a conventional SRAM, allowing for a more informed assessment of the performance and advantages of the integrated SRAM design.

4.3 Result Comparison and Analysis

In order to compare the various results obtained from the simulation of MoS₂ pass transistor based SRAM, we took into account two more type of SRAM i.e one is purely made on Si nMOS and pMOS transistor (having the same length and width as of the cross coupled inverter used in BEOL integrated SRAM) and the other is purely made on MoS₂ based nMOS

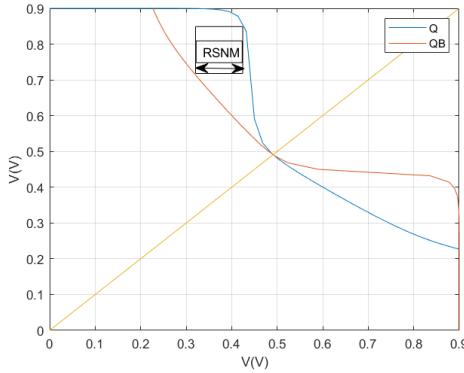


Figure 4.5: Read Margin for Si based SRAM

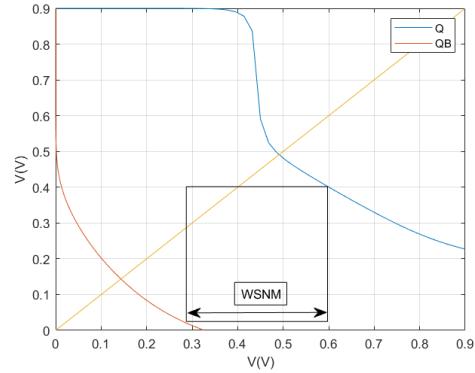


Figure 4.6: Write Margin for Si based SRAM

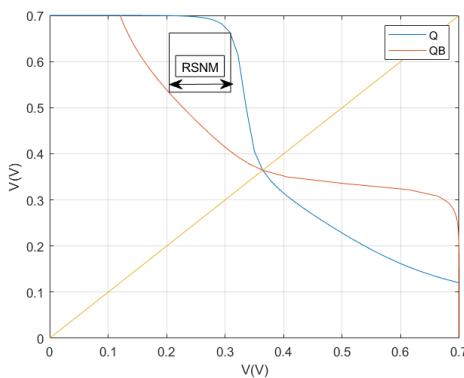


Figure 4.7: Read Margin for MoS₂ based SRAM

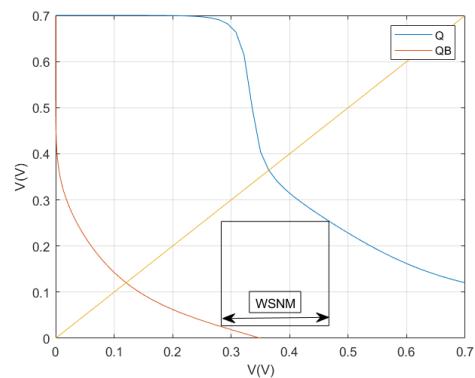


Figure 4.8: Write Margin for MoS₂ based SRAM

and pMOS transistors(having the same length and width as of the MoS₂ pass transistor used in BEOL integrated SRAM).Then we performed the respective simulation to obtain the read and write curves of both the SRAMs and hence calculated their read static noise margin(RSNM) and write static noise margin(WSNM).The result are shown in the fig 4.5-4.8 and table 4.1.

As per the result,in case of the BEOL integrated SRAM it has a slight increased read noise margin as compared to pure Si or MoS₂ based SRAM which implies that it is less prone to data flipping which can be taken as an

advantage.Furthermore the write margin can also be compared and can be taken into account.

Again to check the variability of the read margin on the basis of different width of the pass transistor we simulated the SRAM taking the width as 282nm,350nm and 500nm and got the following results as shown in fig 4.9 and table 4.2.It shows that with increasing gate length

Chapter 4. Circuit Simulation and Performance Analysis

Table 4.1: Comparison of RSNM and WSNM in Different SRAMs

Noise Type	Pure Si SRAM	Pure MoS ₂ SRAM	MoS ₂ -Si Integrated SRAM
RSNM	116mV	104mV	192mV
WSNM	303mV	187mV	-

Table 4.2: Variation of RSNM with Gate Width of MoS₂ Pass Transistor

Width of MoS ₂ nFET	RSNM
282nm	192mV
350nm	187mV
500nm	180mV

of the MoS₂ based pass transistor the read margin is decreasing that means it is more prone to data flip. So we have to take into consideration the width of the MoS₂ pass transistor whenever we are looking for this BEOL integrated SRAM. However, while looking for the width of the pass transistor ,we also have to make sure that the on-state current is also comparable to that of total current of Si transistor making the SRAM cell functional.

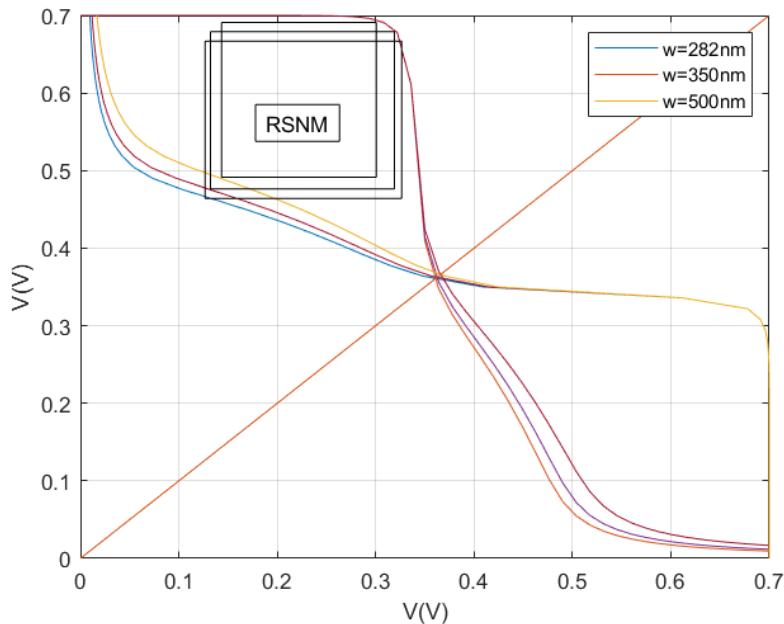


Figure 4.9: Variability of RSNM with Different Widths of MoS₂ Pass Transistor in SRAM

4.4 Extraction and Modelling of Parasitics

As discussed in the previous chapter, we can calculate the extra parasitics produced due to vertical interconnect and later we can integrate it with the netlist simulation to get the exact realistic performance as well as the delay and power consumption of the SRAM. However, in this study, the consideration of parasitic effects was left as an area for future work. While this initial analysis focused on the core functionality of the SRAM design, accounting for parasitic effects would be a valuable addition to further enhance the accuracy and reliability of the simulations.

4.5 Conclusion

In this chapter, we have discussed all the methodology for the circuit level simulation of the heterogeneously integrated SRAM and hence analyzed and compared the results with pure SRAMs to get the insights of performance and viability of it.

CHAPTER 5

Conclusion and Further Work

5.1 Conclusion

In conclusion, this report focused on addressing the current trend in the semiconductor industry, which is scaling down the size of IC cells while maintaining comparable or improved performance. The integration of a BEOL pass transistor in the SRAM design was explored as a means of reducing the cell area compared to traditional SRAM cells.

The initial phase of the study involved modeling the potential 3D layout of the SRAM, taking into account the integration of MoS₂ transistors at the BEOL stage. Subsequently, circuit-level simulations were performed by importing the MoS₂ transistor model into the Cadence environment and integrating it with Si-based transistors. This allowed for the comprehensive evaluation of the integrated SRAM design. The simulations were designed to analyze transient behavior, followed by the calculation of read and write margins, which were then compared with those of pure SRAM designs. The results obtained provided valuable insights for further research and indicated that heterogeneous integration could be a viable approach in the evolving semiconductor industry.

Overall, this study contributes to the understanding of scaling down IC cell size while improving power efficiency and performance. The integration of MoS₂ transistors at the BEOL stage demonstrates the potential for reducing the footprint of SRAM cells, opening up avenues for future advancements in the semiconductor industry.

5.2 Further Work

In this report we have studied the performance of the MoS₂ based pass transistor SRAM without including the extra parasitic produced due to the extra interconnect by integration of the transistor at BEOL

Chapter 5. Conclusion and Further Work

process of the cell. For more realistic result this work can be moved further by calculating the extra parasitic resistance and capacitance produced due to the interconnect at various level. The parasitic can be calculated either analytically [15] [16] [19] or, for more accuracy, tools like Synopsis Raphael, Star RCX etc can be used to develop interconnect model. By calculating the parasitics we can approximate the delay and power consumption of the cell and can compare it to conventional SRAM. This future work can really be helpful for the heterogeneous integration of devices and hence the area scaling could be more feasible in the semiconductor industry.

REFERENCES

- [1] G. E. Moore, "Lithography and the future of moore's law," *IEEE Solid-State Circuits Society Newsletter*, vol. 11, no. 3, pp. 37–42, 2006.
- [2] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of si mosfets and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, 2001.
- [3] S. Kim, J. Seo, J. Choi, and H. Yoo, "Vertically integrated electronics: New opportunities from emerging materials and devices," *Nano-Micro Letters*, vol. 14, 10 2022.
- [4] J. Zhu, J.-H. Park, S. A. Vitale, W. Ge, G. S. Jung, J. Wang, M. Mohamed, T. Zhang, M. Ashok, M. Xue, X. Zheng, Z. Wang, J. Hansryd, A. P. Chandrakasan, J. Kong, and T. Palacios, "Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform," *Nature Nanotechnology*, vol. 18, no. 5, pp. 456–463, May 2023. [Online]. Available: <https://doi.org/10.1038/s41565-023-01375-6>
- [5] V. P.-H. Hu, C.-W. Su, Y.-W. Lee, T.-Y. Ho, C.-C. Cheng, T.-C. Chen, T. Y.-T. Hung, J.-F. Li, Y.-G. Chen, and L.-J. Li, "Energy-efficient monolithic 3-d sram cell with beol mos2 fets for soc scaling," *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 4216–4221, 2020.
- [6] K. Takeda, H. Ikeda, Y. Hagihara, M. Nomura, and H. Kobatake, "Redefinition of write margin for next-generation sram and write-margin monitoring circuit," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, 2006, pp. 2602–2611.
- [7] N. Gierczynski, B. Borot, N. Planes, and H. Brut, "A new combined methodology for write-margin extraction of advanced sram," in *2007 IEEE International Conference on Microelectronic Test Structures*, 2007, pp. 97–100.
- [8] D. Neumaier, S. Pindl, and M. Lemme, "Integrating graphene into semiconductor fabrication lines," 12 2019.

Chapter 5. Conclusion and Further Work

- [9] D. Geng and H. Y. Yang, "Recent advances in growth of novel 2d materials: Beyond graphene and transition metal dichalcogenides," *Advanced Materials*, vol. 30, no. 45, p. 1800865, 2018. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201800865>
- [10] W. Choi, N. Choudhary, G. H. Han, J. Park, D. Akinwande, and Y. H. Lee, "Recent development of two-dimensional transition metal dichalcogenides and their applications," *Materials Today*, vol. 20, no. 3, pp. 116–130, 2017. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S1369702116302917>
- [11] A.-J. Cho, K. Park, and J.-Y. Kwon, "A high-performance complementary inverter based on transition metal dichalcogenide field-effect transistors," *Nanoscale Research Letters*, vol. 10, 12 2015.
- [12] J. Huang, "Research progresses on suppressing the short-channel effects of field-effect transistor," *Highlights in Science, Engineering and Technology*, vol. 27, p. 361–367, Dec. 2022. [Online]. Available: <https://drpress.org/ojs/index.php/HSET/article/view/3779>
- [13] Y. Luo, G. Yan, L. Cao, J. Huo, X. Zhang, Y. Wei, G. Tian, Q. Zhang, Z. Wu, and H. Yin, "Influence of parasitic capacitance and resistance on performance of 6t-sram for advanced cmos circuits design," in *2022 China Semiconductor Technology International Conference (CSTIC)*, 2022, pp. 1–3.
- [14] C.-S. Lee, B. Cline, S. Sinha, G. Yeric, and H. S. P. Wong, "Device-to-system performance evaluation: from transistor/interconnect modeling to vlsi physical design and neural-network predictor," 2021.
- [15] J. Lacord, G. Ghibaudo, and F. Boeuf, "Comprehensive and accurate parasitic capacitance models for two- and three-dimensional cmos device structures," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1332–1344, 2012.
- [16] J. Lacord, S. Martinie, O. Rozeau, M.-A. Jaud, S. Barraud, and J. C. Barbé, "Parasitic capacitance analytical model for sub-7-nm multigate devices," *IEEE Transactions on Electron Devices*, vol. 63, no. 2, pp. 781–786, 2016.
- [17] M. S. Abouelyazid, S. Hammouda, and Y. Ismail, "A fast and accurate middle end of line parasitic capacitance extraction for mosfet and finfet technologies using machine learning," in *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2022, pp. 371–376.
- [18] D. Mittal, "Performance analysis of 6t and 11t sram cell topologies at 45nm era," in *2022 International Conference for Advancement in Technology (ICONAT)*, 2022, pp. 1–4.

Chapter 5. Conclusion and Further Work

- [19] H. Q. Jin, Y. M. Wu, W. J. Wang, and H. J. Zhou, “Study on extraction of capacitance parameters of three dimensional interconnect structures based on finite element method,” in *2021 International Applied Computational Electromagnetics Society (ACES-China) Symposium, 2021*, pp. 1–2.