Ritish Behera

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EXPERIENCE

Summer Research Intern IIT Gandhinagar,Gujarat
May-july 2023

Topic- "Circuit Simulation of Heterogeneous 6T SRAM Cell Featuring MoS2 based Pass Transistor at BEOL Level"
The research work involved designing of a heterogeneous 6T SRAM cell consisting of Si cross-coupled inverter on the FEOL level and MoS2 based pass transistor to be implemented on the BEOL level. Using cadence virtuoso tool, I carried out circuit simulations for noise margin (read, write and hold) calculation of the hybrid cell and further explored some potential solutions for interconnect and parasitic modelling to describe the integration.
Supervisor-**Prof. Tarun Agrawal**, IIT GN
The project report can be found **here**.

PUBLICATION

Noise Margin Analysis of Heterogeneously Integrated Si & MoS2 FET based SRAM Architectures (In-preparation)
Design of various SRAM cells architectures (6T, NTV 7T, Single Bitline 7T, Read-Assited 7T, 9T & 10T) using both Si and MoS2 based FETs and hence calculating their noise margin responses. Tool Used- Cadence Virtuoso. Process node- GPDK 180nm.
Guide-**Prof. Vadthiya Narendar**, NIT W

PROJECTS

Traditional and Thin Cell Layout Design of 6T SRAM Cell
Replicated the layout design of traditional and thin cell SRAM cells using Virtuoso Layout XL environment with successful DRC and LVS checks.

Design and Analysis of SRAM Cell in Latest UMC 28nm Technology
Done simulations for transient, DC and noise margin analysis of 6T SRAM cell followed by static and dynamic power consumption using the latest UMC28nm technology. Tool used- Virtuoso ADE L

16x8 Memory Verification Design and Verification in Verilog
Designed a 16x8 memory array module and generated test cases for verifying its read and write functionality in Verilog.The codes can be viewed **here**.
For more verilog related projects of mine you can checkout my **EDA playground**.

Modeling and Simulation of 2D PN Junction Device using Sentaurus TCAD
Modeled a 2 dimensional PN junction device structure, incorporating careful meshing techniques to generate and analyze its I-V characteristics using the Sentaurus TCAD tool. This was a part of my certification course on ISWDP Sentaurus TCAD level-1.

Triboelectric Nanogenerator(TENG) Circuit Modelling Using SIMULINK
Modeled the appropriate circuit for the TENG device with variable capacitance subsytem using SIMULINK, which was further used for simulations of device characteristics.

SKILLS

EDA Tools: Cadence Virtuoso, Sentaurus TCAD, OpenRoad, Xilinx Vivado, DEEDs
Languages: Verilog, Assembly, Perl, C++, MATLAB
Environment: Windows, Linux (Ubuntu).
Hands-on: 8086 Microprocessor, Artix-7 Power FPGA board

INTERESTS

Physical Design (PR, PSV, CTS, Layout), Emerging Memory Devices, Interconnect & Parasitic Modelling, Computer Architecture, R&D

CERTIFICATION COURSES

VLSI Physical Design with STA	NPTEL,Apr 2024
Digital IC Design	NPTEL,Apr 2024
VLSI Design Flow: RTL to GDS	NPTEL,Dec 2023
Semiconducter Device Modelling and Simulations	NPTEL,Apr 2023

EDUCATION

MSc(Tech) Engineering Physics (Electronics Specialization) GPA: 7.25
NIT Warangal, Telangana **2022-25**
Relevant Courses: VLSI Technology, Microprocessor & Interfacing, Computer Organization, Digital Electronics (STLD & SDSD), Linear Integrated Circuits, Electronic Devices and Circuits, Material Science, Solid State Physics

BSc Physics Honors GPA: 8.2
Gangadhar Meher University, Odisha **2018-21**
Relevant Courses: Digital Circuits, Analog Circuits, Device Physics, Solid State Physics

ACHIEVEMENT

IIT JAM 2022 Qualified	2022
NMMS Scholarship	2015-18
NCC A-Certificate	2016

EXTRA-CURRICULAR

Joint Secretary, Physics Association, NIT Warangal	2022-23
Executive Member, NSS, NIT Warangal	2022-23
Social Work Intern, SAMBHAJ NGO	2022

SUMMARY

In the end, I am a passionate and work-driven personnel with a strong ambition to contribute to and grow within the semiconductor industry.With a keen eye for detail and a commitment to continuous learning, I aim to be a valuable asset to the organizations in the VLSI domain.
For a more detailed exploration of my skills and experiences, please visit my **portfolio**.