RITISH BEHERA

Semiconductor & VLSI Design

Portfolio
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SUMMARY

Aspiring VLSI Engineer with expertise in VLSI design, EDA tools, and semiconductor technology.Proven ability to perform complex simulations and design optimizations. Committed to continuous learning and innovation in the VLSI domain.
Explore my skills and projects at my Portfolio

SKILLS

EDA Tools: Cadence Virtuoso, Sentaurus TCAD, Xilinx Vivado

OpenSource: openLANE flow (Yosys, RePLace, openSTA, openROAD, TritonRoute), Magic VLSI, Ngspice

Languages: Verilog HDL, C++, Assembly, MATLAB, TCL

Hardware: 8086 Microprocessor, Artix-7 Power FPGA Board

EDUCATION

2022-2025 **Masters in Electronics** — **National Institute of Technology Warangal, India**
Relevant Courses: VLSI Design, Embedded Systems, Microprocessor Interfacing, Digital System Design, Linear Integrated Circuits, C++, Computer Architecture, Semiconductor Devices

2018-2021 **Bachelors in Science With Physics Honours** — **Gangadhar Meher University, Sambalpur, India**
Relevant Courses: Solid State Physics, Device Physics, Analog and Digital Electronics

EXPERIENCE

May-July 2023 **Summer Research Intern, VRITIKA Internship** — **IIT Gandhinagar, India**

- Topic: Analysis of BEOL Integration of 2DM Based Pass Transistor in 6T SRAM [Find Report]
- Conducted extensive literature review on 3D SRAM technology and 2D materials.
- Validated the feasibility and performance implications of heterogeneous BEOL integration techniques for advanced SRAM designs
- Carried out circuit simulations and compared performance metrics of the novel 6T SRAM cell, achieving improvement in read noise margins for 28nm technology.
- Developed a physical layout model for the SRAM design with approx 30% improved area efficiency, addressing interconnect delays and parasitic effects.

`Cadence Virtuoso / Cadence Spectre / UMC28nm`

PROJECTS (MAJOR)

Hybrid SRAM Characterization

Electrical Characterization of Si-Mos2 based 3D Integrated SRAM Cell Architectures

- Analyzed DC and transient behaviour to characterize the noise response and delay analysis of heterogeneously integrated Si-MoS2 SRAM architectures at different voltage range.
- Optimized the W/L ratios to meet the on-current specifications whilst improving noise margins by 10-20%.
- Currently working on 3D layout models for extra interconnects to accurately calculate area efficiency and extract parasitic effects.
- Architectures: Single Bitline 7T SRAM, Read-assist 7T SRAM, NTV 7T SRAM, 9T SRAM, 10T SRAM.

`Cadence Virtuoso / GPDK22nm (FinFET) / Custom MoS2 Model Library`

Physical Design

Physical Design Optimization and Timing Analysis of a RISC-V Processor Using OpenLane [Find Here]

- Characterized a custom cell through SPICE simulations and integrated it into a RISC-V design using OpenLane flow in Linux enviroment
- Executed place and route (through TCL commands) operations to achieve a complete design layout without timing violations.
- Conducted timing analysis (STA) post-CTS to identify and rectify slack violations, optimizing timing through fanout limitation and drive strength adjustment achieving a final setup slack of 4.132ps and hold slack of 2.320ps with an area trade-off.
- Performed parasitic extraction for accurate timing, power analysis, and signal integrity verification, generating the spef file post-routing.

`SkyWater 130nm openPDK / openLANE PnR flow / NGSpice / TCL`

Minor Projects

Device Simulations of P-N Junction and MOSFET through Sentaurus TCAD
`Sentaurus TCAD /`

6T SRAM Analysis and Layout Design (Traditional and Thin Cell) With DRC and LVS Verification using 22nm FinFET Technology [Find Here]
`Cadence Virtuoso / Layout XL / Assura`

12 Hour Digital Clock Through Verilog, Implemented and Tested on FPGA Board Seven Segment Display and GDS Layout Generation through open-source "Tiny Tapeouts" [Find Here]
`Xilinx Vivado / Artix-7 Power FPGA Board / Tiny Tapeouts`

KEY INTERESTS

- Advance CMOS Technology • State-of-the-art Memory Devices • Interconnect Modelling • Physical Design • Computer Architecture • AI/ML in VLSI

CERTIFICATIONS

- VSD Digital VLSI SoC Design and Planning [Link] — VSD, May 2024
- ML and Reinforcement Learning Through MATLAB [Link] — Mathworks, May 2024
- ISWDP Sentaurus TCAD [Link] — IISc Banglore, Mar 2024
- Digital IC Design [Link] — NPTEL, Feb 2024
- VLSI Physical Design with STA [Link] — NPTEL, Feb 2024
- VLSI Flow: RTL to GDS [Link] — NPTEL, July 2023

ROLES & RESPONSIBILITIES

2022-2023 **Joint Secretary, Physics Association** — **National Institute of Technology Warangal**

- Directed a team of four in the digital content creation for various association events, ensuring their success.
  `Team Work / Leadership`

2022-2023 **Executive Member, National Service Scheme** — **National Institute of Technology Warangal**

- Collaborated with a group of 50-60 people to help leverage the community services which helped me to grow as a person.
  `Team Work / Community Services`

ACHIEVEMENTS

- Recipient of VRITIKA Internship funded by DST, SERB, Gov. of India
- Qualified IIT JAM (Joint Admission test for Masters) 2022
- Recipient of National Means Cum-Merit Scholarship (NMMS), Gov. of India
- Awarded with NCC (National Cadet Corps) A-Certificate
- District Board Topper in 10th Boards, recognized and felicitated by THE SAMAJ