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BEC101 / BEC201 : Fundamentals of Electronics Engineering

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UNIT

Semiconductor Diode

CONTENTS

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Semiconductor Diode

PART-1

Semiconductor Diode : Depletion Layer, V-I Characteristics,
Ideal and Practical Diodes, Diode Equivalent Circuits.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

- Que 1.1.** Explain semiconductor diode and also draw its equivalent circuit.

Answer

1. A diode is an electrical device allowing current to flow only in one direction (forward bias) with far greater ease than in the other direction (reverse bias).
2. The most common type of diode in modern circuit design is the semiconductor diode (*p-n* junction).
3. A diode is a two-layer semiconductor consisting of *p*-type semiconductor material and *n*-type semiconductor material the equivalent circuit of diode is shown in Fig. 1.1.1.

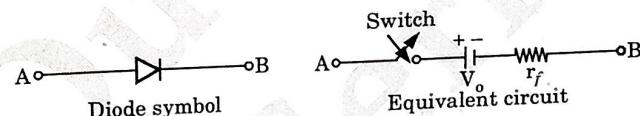


Fig. 1.1.1.

4. In an equilibrium, *p-n* junction, the free electrons from the *n*-type region will diffuse across the junction to the *p*-type side where they will recombine with some of the holes in the *p*-type material. Similarly, holes will diffuse across the junction in the opposite direction and recombine.
5. The recombination of free electrons and holes in the vicinity of the junction leaves a narrow region on either side of the junction that contains no mobile charge. This narrow region which has been depleted of mobile charge is called the depletion layer.
6. Diffusion of electrons into the *p*-region will leave positively charged ions (donors) in the *n*-region.
7. Similarly, diffusion of holes near the *p-n* interface in the *n*-type region leaves fixed ions (acceptors) with negative charge.

8. The regions nearby the *p-n* interfaces lose their neutrality and become charged, forming the space charge region or depletion layer.

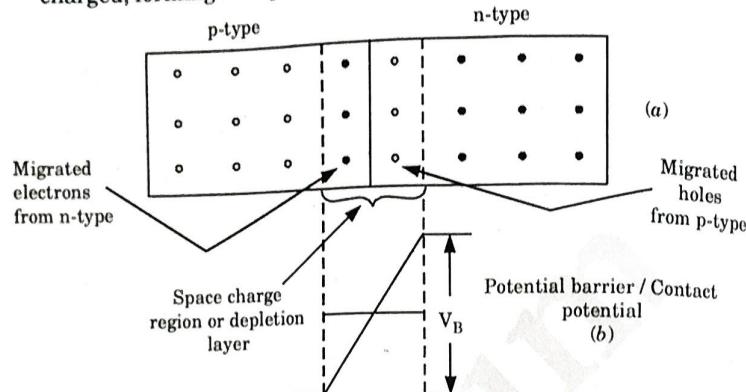


Fig. 1.1.2. *p-n* junction semiconductor.

9. This separation of charges causes an electric field to extend across the depletion layer. A potential difference must therefore exist across the depletion layer.

Que 1.2. Explain the V-I characteristic of *p-n* junction diode.

Draw well labelled characteristic.

AKTU 2016-17, (Sem-I) Marks 05

Answer

i. **Forward bias :**

- For the forward bias of a *p-n* junction, *p-type* is connected to the positive terminal while the *n-type* to negative terminal of battery.
- The potential can be varied with potential divider. At some forward voltage (0.3 V for Ge and 0.7 V for Si) the potential barrier is eliminated and current starts flowing. This voltage is known as threshold or knee voltage (V_K).
- As the forward voltage applied increases beyond threshold voltage, the forward current rises exponentially as shown in Fig. 1.2.1.
- Beyond a certain safe value, it produces an extremely large current which may destroy the junction due to overheating.

ii. **Reverse bias :**

- The *p-type* is connected to the negative terminal while *n-type* is connected to the positive terminal of a battery.
- In this case, the junction resistance becomes very high and practically no current flows through the circuit.

3. In practical, a small current of the order of μA flows in the circuit due to minority carriers. This is known as reverse current. The reverse current is shown in Fig. 1.2.1.

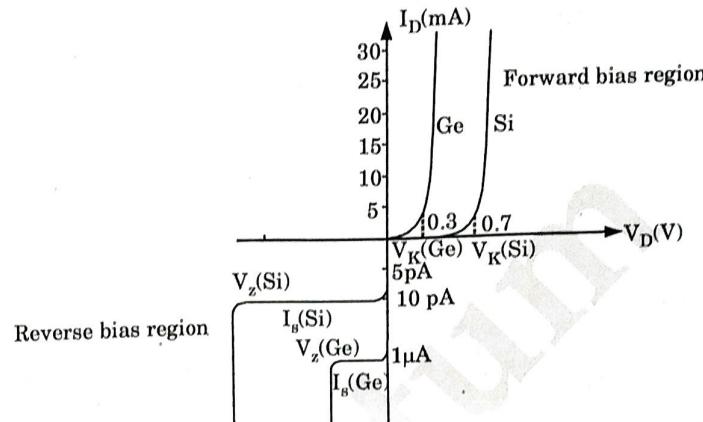


Fig. 1.2.1. Volt-ampere characteristics of *p-n* junction.

- As the reverse bias is increased from zero, the reverse current quickly rises to its maximum or saturation value. The slight increase is due to impurities on the surface, which behaves as a resistor and hence obeys ohm's law. This gives rise to a current called surface leakage current.
- If the reverse voltage is further increased, the kinetic energy of electrons becomes so high that they knock out from the semiconductor atoms. At this stage, breakdown of junction occurs and there is a sudden rise of reverse current. Now the junction is destroyed completely.
- Thus, *p-n* junction diode is one-way device which offers a low resistance when forward biased and behaves like an insulator when reverse biased. Thus, it can be used as a rectifier *i.e.*, for converting alternating current into direct current.

Que 1.3. Sketch and explain ideal and practical V-I characteristics of a *p-n* junction diode.

Answer

A. **Ideal V-I characteristic :**

- An ideal diode is perfect conductor in forward bias and a perfect resistor in reverse bias.
- The current-voltage characteristic of the ideal diode is shown in Fig. 1.3.1.

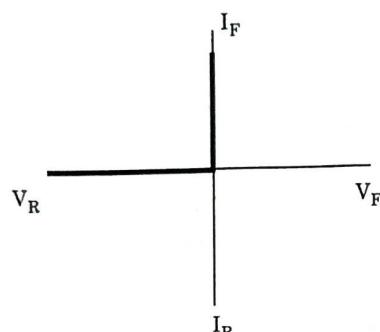


Fig. 1.3.1. V-I characteristics of an ideal diode.

3. A diode acts as a short circuit when it is forward biased. When it is reverse biased, it acts as an open circuit.
4. Therefore, an ideal diode acts as unilateral switch. No power is dissipated in an ideal diode biased in either direction. Since in forward direction, the voltage across the diode is zero and in the reverse direction, the current through the diode is zero as shown in Fig. 1.3.1.

B. Practical :

1. In practical, the battery introduced a small offset voltage (V_o) in forward biased. The value of the offset voltage is determined by the type of semiconductor used in a $p-n$ junction but cannot be measured directly.

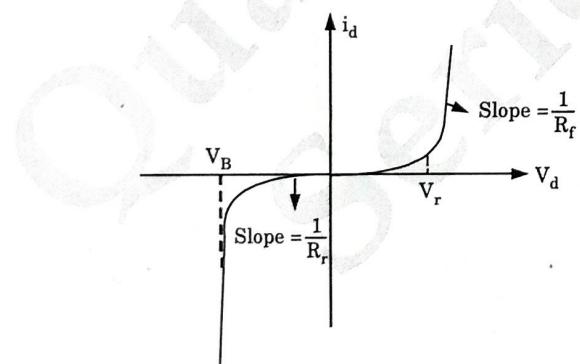


Fig. 1.3.2.

2. The resistor approximates the semiconductor resistance when diode is ON / OFF or forward bias / reverse bias.
3. A reverse biased diode conducts a very small amount of current called leakage current.

4. The ability of diode to withstand reverse-bias voltage is limited. If the applied reverse-bias voltage becomes too large diode will experience a heavy conduction known as breakdown, which is usually destructive.
5. The current versus voltage curve for a real diode looks like as shown in Fig. 1.3.2.

PART-2*Zener Diodes Breakdown Mechanism (Zener and Avalanche).***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

- Que 1.4.** Explain the V-I characteristic of $p-n$ junction diode. How it is differ from zener diode ? AKTU 2016-17, (Sem-II) Marks 07

OR

Explain input and output characteristics of zener diode.

AKTU 2015-16, (Sem-II) Marks 05**Answer**

- A. **V-I characteristic of $p-n$ junction diode :** Refer Q. 1.2, Page 1-3J, Unit-1.
- B. **Zener diode :**
1. Zener diode is a reverse-biased heavily doped $p-n$ -junction diode which is operated in the breakdown region. Fig. 1.4.1 shows the symbol of zener diode.



Fig. 1.4.1. Zener diode.

2. When a zener diode is forward biased, its characteristics are just same as the ordinary diode and it is shown in Fig. 1.4.2.
3. When zener diode is reverse biased then it gives constant current up to a certain voltage. When the reverse bias voltage is increased beyond that voltage, the current increased rapidly as shown in Fig. 1.4.2.

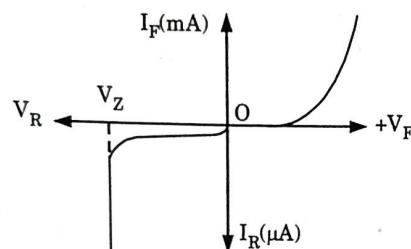


Fig. 1.4.2. V-I characteristic of zener diode.

4. The cut-off value of voltage beyond which zener diode reverse current increases rapidly is called zener voltage V_Z or breakdown voltage.
5. The breakdown or zener voltage depends upon the amount of doping.
6. A zener diode can be used as a voltage regulator to provide a constant voltage to a load.

C. Difference :

S. No	p-n junction diode	Zener diode
1.	The electricity flows in one direction.	The electricity flows in both the direction.
2.	The reverse bias permanently damages the depletion region.	The reverse bias makes the electricity flow in both the direction.
3.	The width of depletion region is large because the p and n region is lightly doped.	The width of depletion region is narrow because the p and n region is heavily doped.
4.	This is used for rectification.	This is used for voltage regulation.

Que 1.5. Explain reverse breakdown of a diode.

Answer

Reverse breakdown can occur by two mechanisms that are zener breakdown and avalanche breakdown.

i. Zener breakdown :

1. It takes place in very thin junction (*i.e.*, depletion layer is narrow due to heavily doped junctions on both sides).
2. When a small reverse bias voltage is applied, a very strong electric field (approximately 10^7 V/m) is set up across the thin depletion layer.
3. This field is enough to break the covalent bonds. This breaking of covalent bonds produces large number of electrons and holes which constitute the reverse saturation current (*i.e.*, zener current).

4. Zener current is independent of the applied voltage. It depends only on the external resistance.
5. This breakdown is called as zener breakdown as shown in Fig. 1.5.1. This breakdown occurs at low voltage.

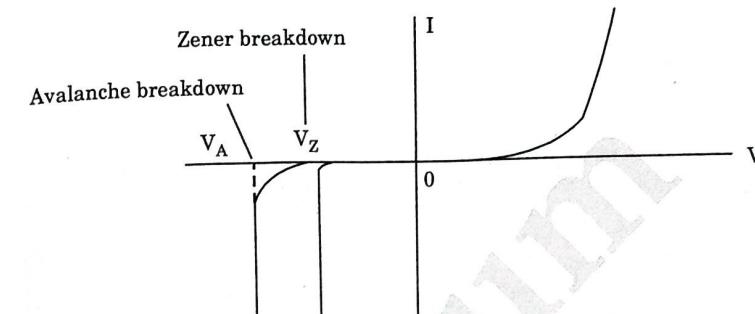


Fig. 1.5.1. The I-V characteristics comparison between zener and avalanche breakdown.

ii. Avalanche breakdown :

1. Avalanche breakdown takes place in slightly thick junction than the zener breakdown case. It means both sides of junction are lightly doped.
2. In this case, the electric field across the depletion region (layer) is not so strong to produce zener breakdown for the same applied voltage of zener breakdown case.
3. Here, the minority carriers accelerated by the field collide with the semiconductor atoms in the depletion region.
4. During collision the kinetic energy of electrons is transferred to other covalent bonds, thus the energy transferred to covalent bonds increases the band energy, hence covalent bonds are broken and electron-hole pairs are generated.
5. The newly generated carriers transfer their energy to other covalent bonds and break more bonds and thus extremely large numbers of carriers are generated due to cumulative process of avalanche multiplication.
6. This breakdown is called avalanche breakdown as shown in Fig. 1.5.1. This breakdown occurs at higher voltages.

PART-3

Diode Application : Diode Configuration, Half and Full Wave Rectification.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.6. Explain the series diode configuration.

Answer

1. The series circuit of diode is shown in Fig. 1.6.1.
2. The state of the diode is first determined by replacing the diode with a resistive element as shown in Fig. 1.6.2(a). The resulting direction of I is a match with the arrow in the diode symbol and since $E > V_K$, the diode is in the "ON" state.
3. The network is then redrawn as shown in Fig. 1.6.2(b) with the appropriate equivalent model for the forward biased silicon diode.

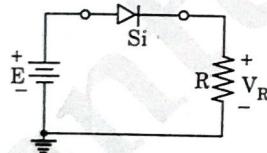


Fig. 1.6.1. Series diode configuration.

4. The resulting voltage and current level are the following:

$$\begin{aligned}V_D &= V_K \\V_R &= E - V_K \\I_D = I_R &= \frac{V_R}{R}\end{aligned}$$

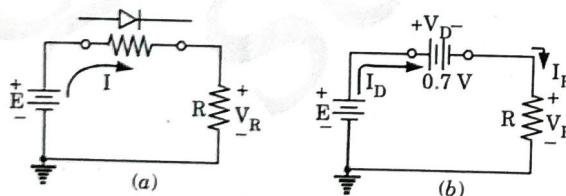


Fig. 1.6.2.

5. In Fig. 1.6.3 the diode is reversed. Replacing the diode with a resistor element as shown in Fig. 1.6.4 (a) will reveal that the resulting current direction does not match the arrow in the diode symbol.
6. The diode is in the "OFF" state, resulting in the equivalent circuit of Fig. 1.6.4(b).

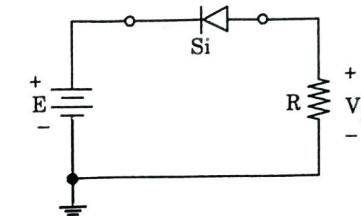


Fig. 1.6.3. Reversing the diode.

7. Due to open circuit, the diode current is 0 A and the voltage across the resistor R is the following :

$$V_R = I_R R = I_D R = (0 \text{ A}) R = 0 \text{ V}$$

$$V_D = E$$

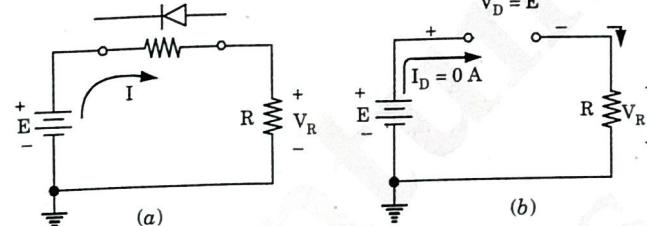


Fig. 1.6.4.

Que 1.7. Sketch V_O for given circuit configuration (Fig. 1.7.1).

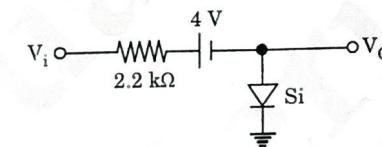


Fig. 1.7.1.

AKTU 2017-18 (Sem-II), Marks 3.5

Answer

1. Assume input waveform,

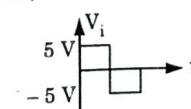


Fig. 1.7.2.

2. For positive half cycle, Diode is in ON state.

$$V_O = 0.7 \text{ V}$$

3. For negative half cycle, Diode is in OFF state.

$$V_O = -4 + V_i = -4 - 5 = -9 \text{ V}$$

4. Output waveform as shown in Fig. 1.7.3.

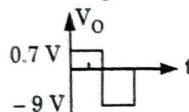


Fig. 1.7.3.

Que 1.8. For the circuit shown in Fig. 1.8.1, determine I_1, I_2, I_3, I_4, V_O

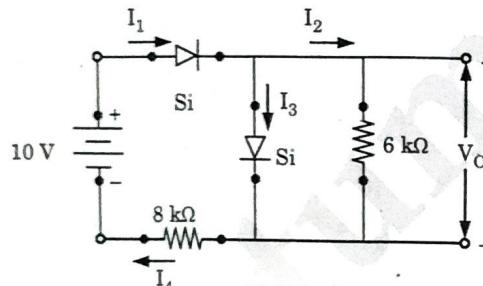


Fig. 1.8.1.

AKTU 2016-17(Sem-I), Marks 05

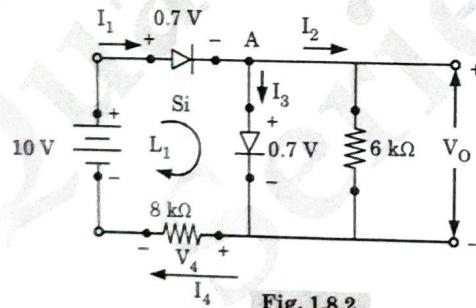
Answer

Fig. 1.8.2.

$$I_2 = \frac{0.7 \text{ V}}{6 \text{ k}\Omega} = 0.1167 \text{ mA}$$

$$V_O = 0.7 \text{ V}$$

Voltage across $8 \text{ k}\Omega$, applying KVL in loop L_1 ,
 $-V_4 + 10 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} = 0$

$$V_4 = 8.6 \text{ V}$$

We have,

$$I_4 = \frac{V_4}{R} = \frac{8.6 \text{ V}}{8 \text{ k}\Omega} = 1.075 \text{ mA}$$

$$I_4 = I_1 = 1.075 \text{ mA}$$

Apply KCL at node A, $I_3 = I_1 - I_2 = 1.075 \text{ mA} - 0.1167 \text{ mA}$
 $I_3 = 0.96 \text{ mA}$

Que 1.9. Explain the working of half wave and full wave bridge rectifier.

OR

Explain the bridge rectifier with clear diagram.

AKTU 2017-18(Sem-I), Marks 3.5

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveform.

AKTU 2016-17(Sem-I), Marks 05

OR

With help of neat circuit diagrams, explain the working of a full wave bridge rectifier.

AKTU 2020-21 (Sem-I), Marks 05

Answer

A. **Half wave rectifier:** It is shown in Fig. 1.9.1. As the name signifies only half portion of input is rectified (either positive half or negative half). Only single diode and a step down transformer are required for this circuit.

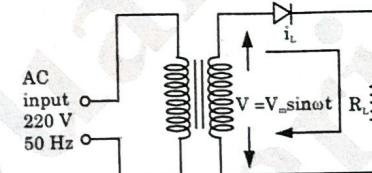


Fig. 1.9.1. Half wave rectifier circuit.

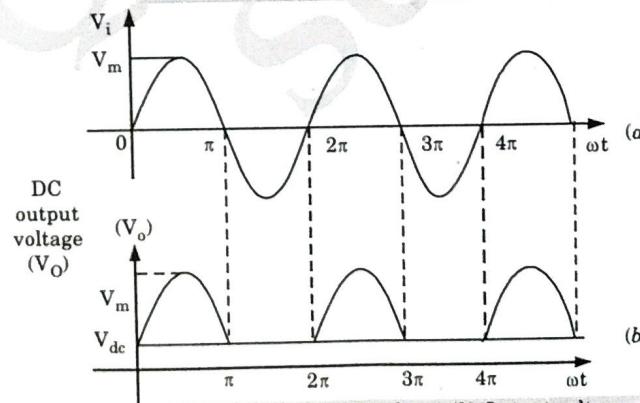


Fig. 1.9.2. (a) Input voltage (b) Output voltage.

B. Full wave rectifier: This circuit gives the output for full cycle (i.e., for both positive and negative half cycles). There are two types of circuits used for it :

i. **Center-tap rectifier :**

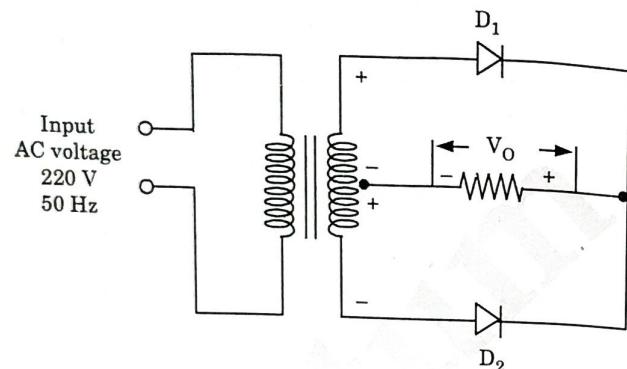


Fig. 1.9.3. Full wave rectifier.

1. In center-tap full wave rectifier circuit, diode D_1 will be ON for positive half cycle (i.e., 0 to π) and the diode D_2 will be OFF during this cycle.
2. The diode D_2 will be ON for negative half cycle (i.e., π to 2π) while the diode D_1 will be OFF during this cycle.
3. The input and output waveforms are shown in Fig. 1.9.4.

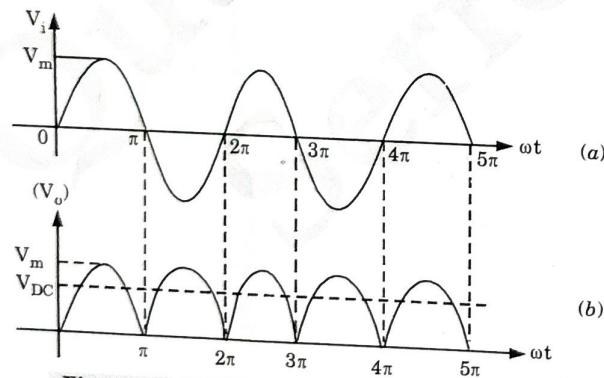


Fig. 1.9.4. (a) Input waveform (b) Output waveform.

- ii. **Bridge rectifier :** As shown in Fig. 1.9.5(b) only diodes D_2 and D_4 are active during positive half cycle while diodes D_1 and D_3 are active for negative half cycle as shown in Fig. 1.9.5(c) and Fig. 1.9.5(d) shows the total output with the active diodes for a particular cycle.

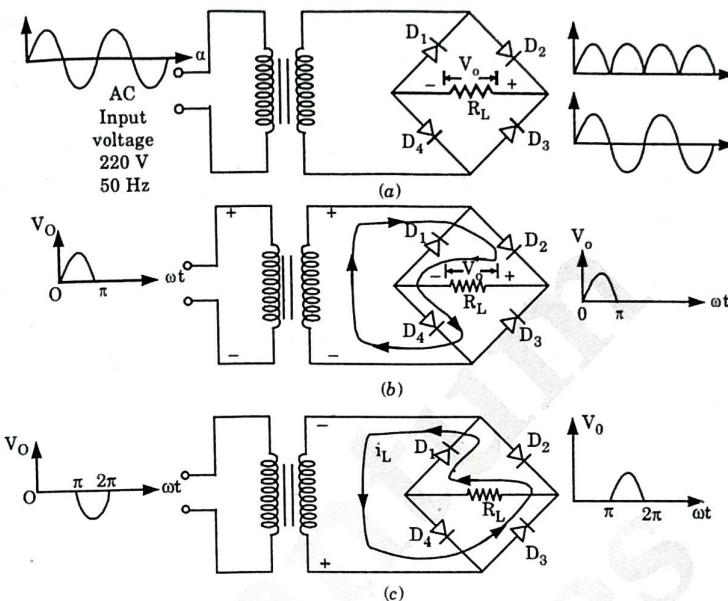


Fig. 1.9.5. (a) Basic bridge rectifier circuit
(b) Output of bridge rectifier for positive half cycle.
(c) Output of bridge rectifier for negative half cycle.
(d) Output for full cycle.

- Que 1.10.** Explain the following terms in context with half wave rectifier and full wave rectifier :
 i. DC voltage and DC current
 ii. RMS value of current

OR

For a half wave rectifier, derive an expression for ripple factor.

AKTU 2015-16(Sem-II), Marks 7.5

OR

Explain the operation of full wave bridge rectifier with the help of a circuit diagram. Also sketch the input and output waveforms. Define its PIV. Also derive its ripple factor and rectification efficiency.

AKTU 2017-18(Sem-II), Marks 07

OR

Draw the circuit and discuss the working of full wave bridge rectifier with suitable input-output waveforms. What is PIV of bridge rectifier?

AKTU 2016-17(Sem-II), Marks 07

OR

Define the term ripple factor. What is the value of the ripple factor for a half wave rectifier and a full wave rectifier?

AKTU 2020-21 (Sem-I), Marks 05

Answer

A. Half wave rectifier :

i. Operation : Refer Q. 1.9, Page 1-12J, Unit-1.

ii. PIV :

- As we know during negative half cycle, diode will be reverse biased and there will be no output voltage.
- In the negative half cycle the voltage across diode will be maximum when input reaches to its maximum value V_m . This maximum voltage during negative half cycle is called as the peak inverse voltage (PIV).
- PIV for half wave rectifier is given by

$$\text{PIV} = V_m$$

iii. DC voltage and DC current :

Suppose current in load

$$i_L = I_m \sin \omega t \quad 0 \leq \omega t \leq \pi \\ = 0 \quad \pi \leq \omega t \leq 2\pi \quad \dots(1.10.1)$$

Here,

I_m = Peak value of current i_L

$$I_m = \frac{V_m}{R_L}$$

DC voltage for half wave rectifier, $V_{DC} = I_{DC} \times R_L$

$$V_{DC} = \frac{I_m}{\pi} \times R_L$$

$$V_{DC} = \frac{V_m}{\pi} \quad \dots(1.10.2)$$

$$I_{DC} = \frac{I_m}{\pi} \quad \dots(1.10.3)$$

iv. RMS value of current :

- The rms value of the current flowing through the load is given as

$$I_{Rm} = \frac{I_m}{\sqrt{2}} - \text{peak current}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_L^2 d(\omega t)}$$

$$V_{avg} = \frac{2V_0}{\pi}$$

- Replacing the value of i_L from eq. (1.10.1)

$$I_{rms} = \sqrt{\frac{1}{2\pi} \left[\int_0^\pi I_m^2 \sin^2 \omega t d(\omega t) + \int_\pi^{2\pi} 0 d(\omega t) \right]} \\ = \sqrt{\frac{I_m^2}{2\pi} \int_0^\pi (1 - \cos 2\omega t) d(\omega t)} \\ = \sqrt{\frac{I_m^2}{2\pi \times 2} \left| \omega t - \frac{\sin 2\omega t}{2} \right|_0^\pi}$$

$$I_{rms} = \frac{I_m}{2} \quad \text{half}$$

... (1.10.4)

- Eq. (1.10.4) gives total current (AC and DC).

- Thus instantaneous value of AC in output is,

$$i_{AC} = i_L - I_{DC}$$

$$(I_{AC})_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (i_L - I_{DC})^2 d(\omega t)} \\ = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (i_L^2 + I_{DC}^2 - 2i_L I_{DC}) d(\omega t)} \\ = \sqrt{I_{rms}^2 + I_{DC}^2 - 2I_{DC}^2}$$

$$(I_{AC})_{rms} = \sqrt{I_{rms}^2 - I_{DC}^2} \quad \dots(1.10.5)$$

- Ripple factor : It is define as the ratio of r.m.s value of AC component to the DC component in the rectifier output.

The ripple factor is given as

$$r = \frac{(I_{AC})_{rms}}{I_{DC}} = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

Since, $I_{rms} = I_m/2$ and $I_{DC} = I_m/\pi$. So, $r = 1.21$

- Rectification efficiency : The efficiency is given as

$$\eta = \frac{\text{Output DC power}}{\text{Input AC power}} = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{I_{rms}^2 (R_L + r_d)}$$

where, $R_L \rightarrow$ load resistance, $r_d \rightarrow$ diode resistance

$$= \frac{(I_m/\pi)^2 \cdot R_L}{(I_m/2)^2 (r_d + R_L)}$$

$$\eta = 0.406$$

($\because r_d \ll R_L$)

$$\eta = 40.6\%$$

B. Full wave rectifiers :

- i. Operation and waveforms of full wave bridge rectifier :
Refer Q. 1.9, Page 1-12J, Unit-1.
ii. RMS value of current :

$$I_{\text{rms}} = \sqrt{\frac{1}{\pi} \int_0^{\pi} I_L^2 d(\omega t)} = \sqrt{\frac{1}{\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \frac{(1 - \cos 2\omega t)}{2} d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi} \left| \omega t - \frac{\sin 2\omega t}{2} \right|_0^{\pi}}$$

$$I_{\text{rms}} = \frac{I_m}{\sqrt{2}} \quad \text{full}$$

- iii. PIV (Peak Inverse Voltage) : It is same as the half wave rectifier, but the value of PIV is different for center-tap type full wave rectifier.

In centre-tap full wave rectifiers, $\boxed{\text{PIV} = 2V_m}$

In bridge type full wave rectifiers, $\boxed{\text{PIV} = V_m}$

- iv. DC voltage and DC current :

$$I_{DC} = \frac{1}{\pi} \int_0^{\pi} i_L d(\omega t) = \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t d(\omega t)$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$V_{DC} = I_{DC} \times R_L$$

$$\boxed{V_{DC} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi}}$$

- v. Ripple factor :

$$r = \frac{(I_{AC})_{\text{rms}}}{I_{DC}} = \sqrt{\left(\frac{I_{\text{rms}}}{I_{DC}} \right)^2 - 1} = \sqrt{\left(\frac{I_m / \sqrt{2}}{2I_m / \pi} \right)^2 - 1}$$

$$r = 0.482$$

- vi. Rectification efficiency :

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{(2I_m / \pi)^2 R_L}{(I_m / \sqrt{2})^2 (r_d + R_L)} \times 100 \% \\ = 81.2 \% \quad (\because r_d \ll R_L)$$

Que 1.11. In the bridge rectifier circuit, the secondary voltage

$V_s = 100 \sin 50t$ and load resistance is $1\text{k}\Omega$. Calculate :

- DC current
- RMS value of current
- Efficiency
- Ripple factor.

AKTU 2021-22 (Sem-II), Marks 10

Answer

Given :

$$V_s = 100 \sin 50t$$

$$R_L = 1\text{k}\Omega$$

V_m = Peak secondary voltage

$$V_m = 100$$

$$V_{DC} = \frac{2V_m}{\pi} = 63.66$$

$$V_{RMS} = \frac{V_m}{\sqrt{2}} = 70.71$$

- i. DC current, $I_{DC} = \frac{V_{DC}}{R_L} = \frac{63.66}{1\text{k}\Omega} = 0.0636 \text{ A}$

- ii. RMS value of current,

$$I_{RMS} = \frac{V_{RMS}}{R_L} = 0.0707 \text{ A}$$

- iii. Efficiency, $\eta = \frac{V_{DC} \times I_{DC}}{V_{RMS} \times I_{RMS}} = \frac{63.66 \times 0.063}{70.71 \times 0.0707} = 0.8022 \text{ or } 80 \%$

- iv. Ripple factor $= \sqrt{\left(\frac{V_{RMS}}{V_{DC}} \right)^2 - 1} = \sqrt{\left(\frac{70.71}{63.66} \right)^2 - 1} = 0.4834$

Que 1.12. Differentiate between half wave and full wave rectifiers.

AKTU 2015-16(Sem-I), Marks 05

Answer

S. No.	Full wave rectifier	Half wave rectifier
1.	Full wave rectifier is an electronic circuit which converts entire cycle of AC into pulsating DC.	A Half wave rectifier is an electronic circuit which converts only one-half of the AC cycle into pulsating DC.
2.	Full wave rectifier, is bi-directional, it conducts for positive half as well as negative half of the cycle.	The Half wave rectifier is unidirectional; it means it will allow the conduction in one direction only.
3.	Peak inverse voltage (PIV) is twice of the maximum value of supplied input.	Peak inverse voltage (PIV) is the maximum value of supplied input.
4.	Ripple factor is low.	Ripple factor is high.

Que 1.13. Determine the output waveform for the given network as shown in Fig. 1.13.1. Determine the output DC level and compute PIV for each diode.

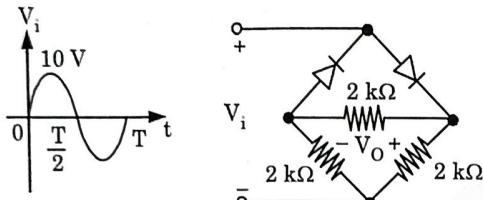


Fig. 1.13.1.

AKTU 2017-18(Sem-II), Marks 07

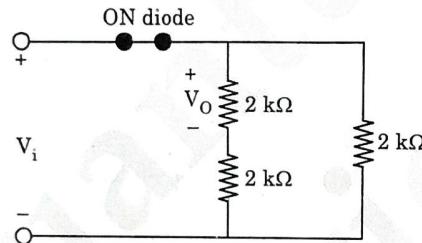
AnswerFor positive half-cycle of V_i :

Fig. 1.13.2.

Using voltage divider rule,

$$V_{o\max} = \frac{2 \text{ k}\Omega (V_{i\max})}{2 \text{ k}\Omega + 2 \text{ k}\Omega} = \frac{1}{2} (10 \text{ V}) = 5 \text{ V}$$

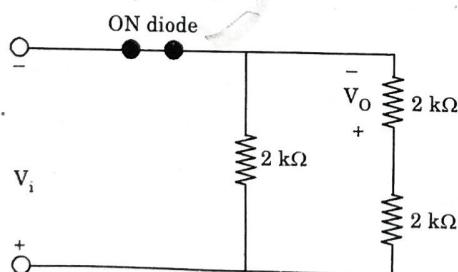
For negative half-cycle of V_i :

Fig. 1.13.3.

Using voltage divider rule,

$$V_{o\max} = \frac{2 \text{ k}\Omega (V_{i\max})}{2 \text{ k}\Omega + 2 \text{ k}\Omega} = \frac{1}{2} V_{i\max} = \frac{1}{2} (10) = 5 \text{ V}$$

$$V_{DC} = 0.636 V_{o\max} = 0.636 (5 \text{ V}) = 3.18 \text{ V}$$

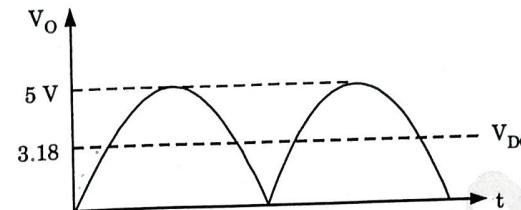


Fig. 1.13.4.

Peak inverse voltage of each diode = $V_m = 10 \text{ V}$ **PART-4**

Clippers, Clampers.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.14. Draw a simple clipping circuit with suitable waveform and explain types of clippers.

Answer**A. Clipping circuit :**

A wave shaping circuit which controls the shape of output waveform by removing (clipping) a portion of the applied wave is known as clipping circuit. For a clipping circuit at least one resistance and one diode are required.

B. Types of clippers : There are mainly two types of clippers i.e., positive and negative clippers. They are further divided into two categories :**1. Series clippers (for ideal diode) :****a. Simple series clippers :**

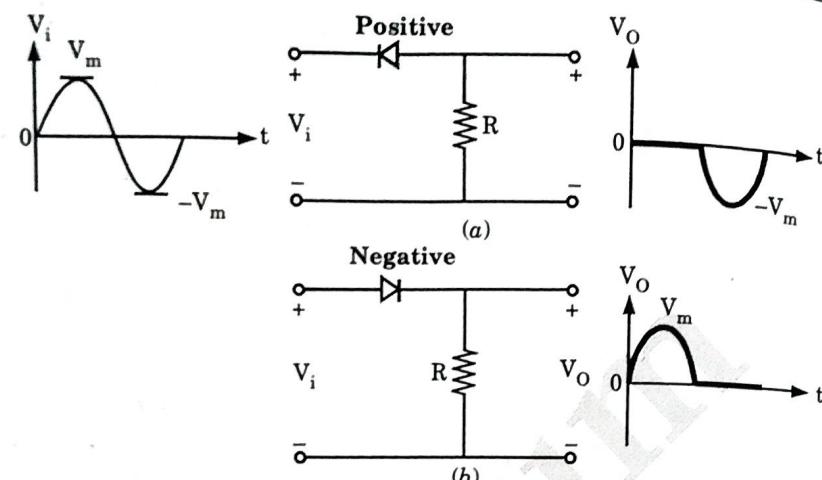


Fig. 1.14.1.

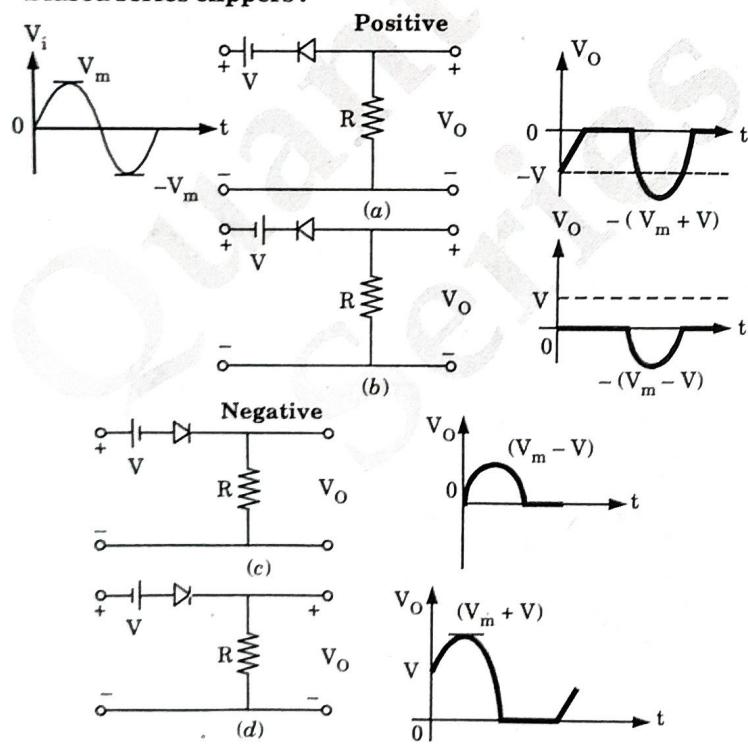
b. Biased series clippers:

Fig. 1.14.2.

- 2. Parallel clippers (for ideal diodes):**
a. Simple parallel clippers:

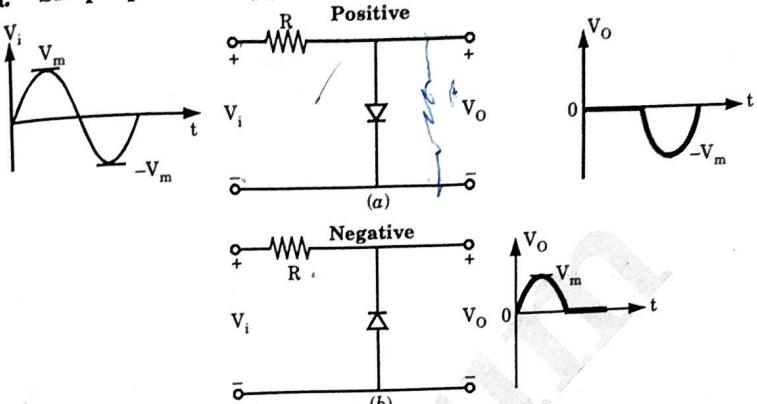


Fig. 1.14.3.

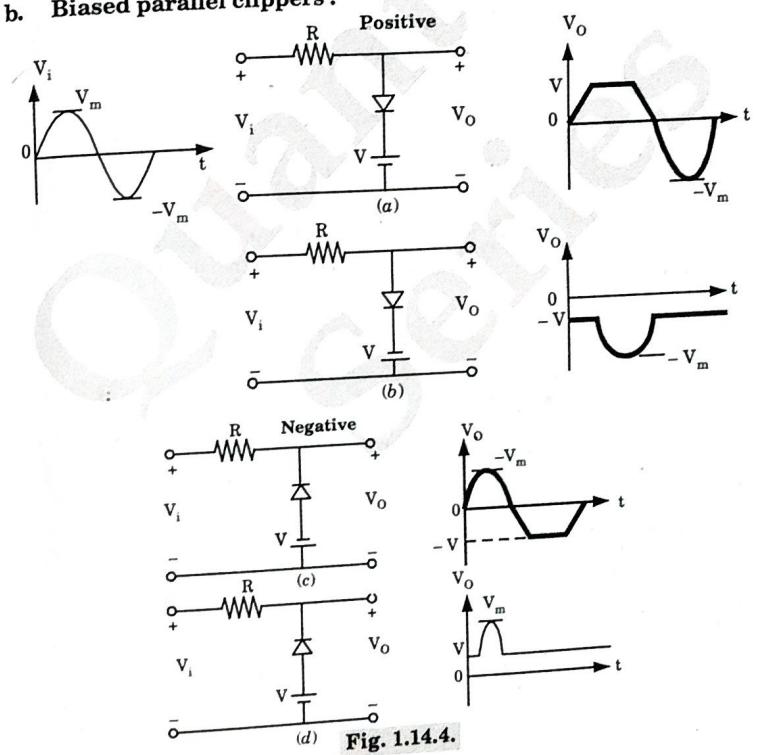
b. Biased parallel clippers:

Fig. 1.14.4.

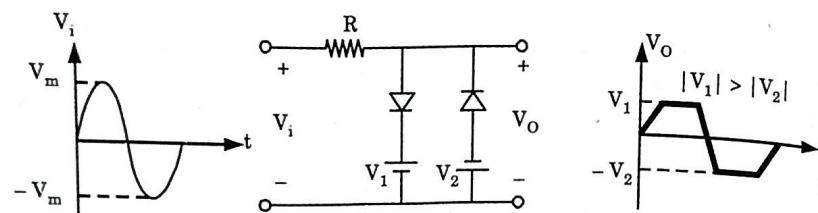
c. Combination clipper (Positive and Negative) :

Fig. 1.14.5.

Que 1.15. What do you mean by clamper circuit? What are the different types of clamper circuits?

OR

Explain Positive and Negative Clamper using suitable circuit diagram and input/output waveform.

AKTU 2021-22 (Sem-I), Marks 05

Answer**A. Clamp circuit :**

A clamping circuit is a device that 'clamps' a signal to a different DC level. A clamping circuit must have a diode, a resistance and a capacitor, an independent DC supply is also required to introduce an additional shift.

B. Types of clamp circuit : There are two types of clamp circuits.

1. **Positive Clamp :** It shifts the original signal in vertical upward direction.

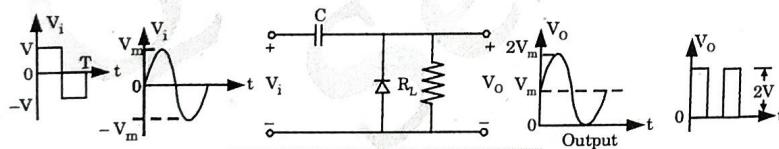
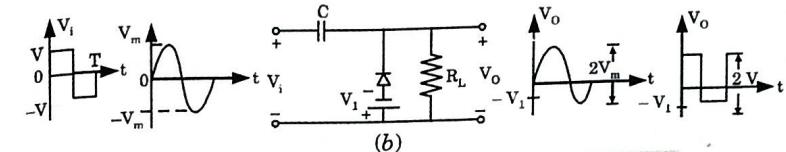
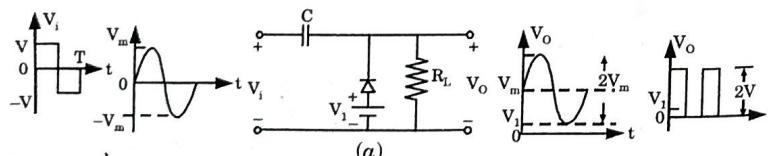


Fig. 1.15.1. Positive clamp.

$$\text{Output voltage } V_o = V_m + V_c = V_m + V_m = 2V_m$$

Positive clamp with bias :Fig. 1.15.2. (a) Positive clamp with positive biased,
(b) Positive clamp with negative biased.

2. **Negative clamp :** It shifts the original signal in vertical downward direction.

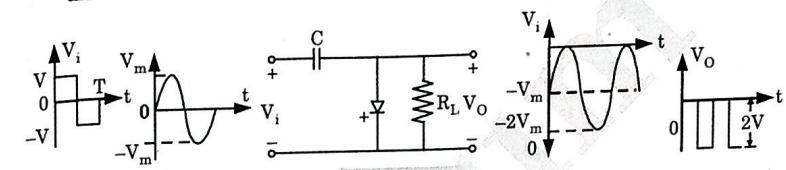
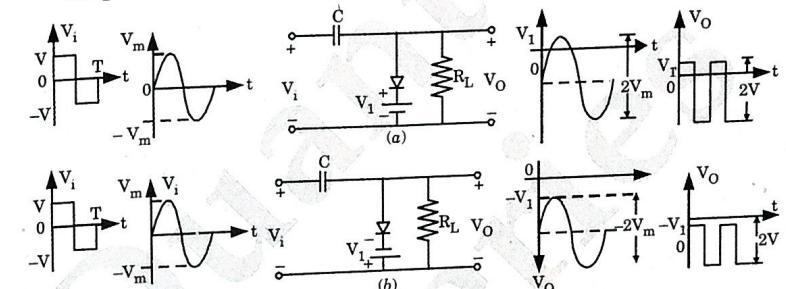
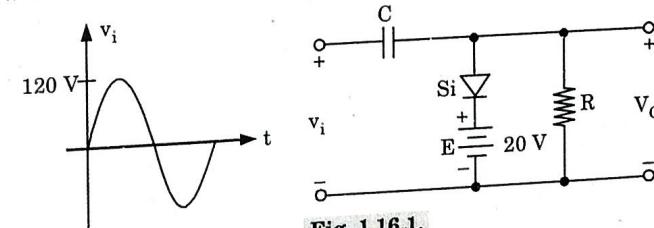


Fig. 1.15.3.

Negative clamp with bias :Fig. 1.15.4. (a) Negative clamp with positive bias,
(b) Negative clamp with negative bias.

- Que 1.16.** Sketch V_o for each network of Fig. 1.16.1, for the input shown.



AKTU 2015-16(Sem-I), Marks 05

OR

Sketch the output for given clamper circuit with shown input is
Fig. 1.16.1.

AKTU 2017-18(Sem-II), Marks 3.5

Answer

- For positive half cycle capacitor charges to peak value of $120 \text{ V} - 20 \text{ V} - 0.7 \text{ V} = 99.3 \text{ V}$ with polarity (+ + - -). The output $V_O = 20 \text{ V} + 0.7 \text{ V} = 20.7 \text{ V}$.
- For next negative half cycle $V_O = V_i - 99.3 \text{ V}$ with negative peak value of $V_O = -120 \text{ V} - 99.3 \text{ V} = -219.3 \text{ V}$.

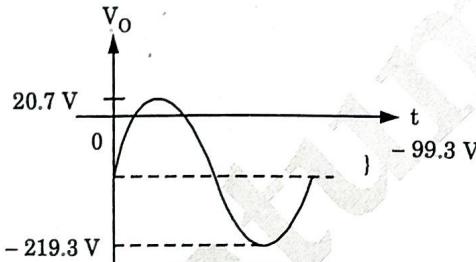
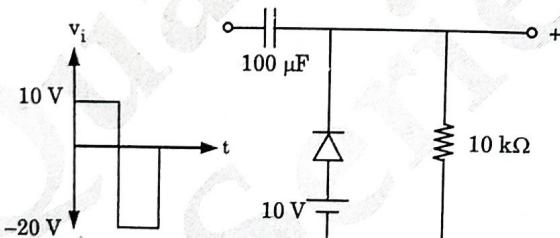


Fig. 1.16.2.

Que 1.17. Define clamper. Determine output voltage for the given network.



AKTU 2021-22 (Sem-II), Marks 10

Answer

- A. Clamper : Refer Q. 1.15, Page 1-23J, Unit-1.
 B. Numerical :
 Output voltage for the given network : Let diode be ideal.
 Forward bias :

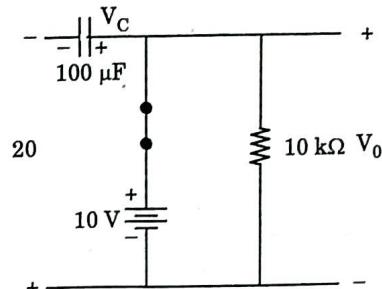


Fig. 1.17.2.

Diode is short circuited therefore voltage across resistor will be same as across the battery $V_0 = 10 \text{ V}$

The voltage that charge up the capacitor

$$-20 \text{ V} + V_C - 10 \text{ V} = 0 \\ V_C = 30 \text{ V}$$

Reverse bias :

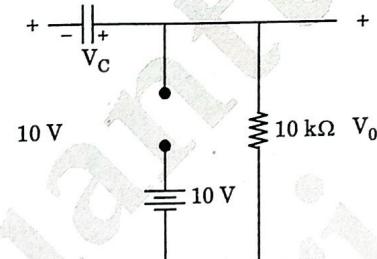


Fig. 1.17.3.

Diode is open circuit therefore current start to flow in resistor.

Apply KVL

$$10 \text{ V} + V_C - V_0 = 0 \\ V_0 = 40 \text{ V}$$

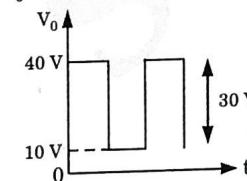
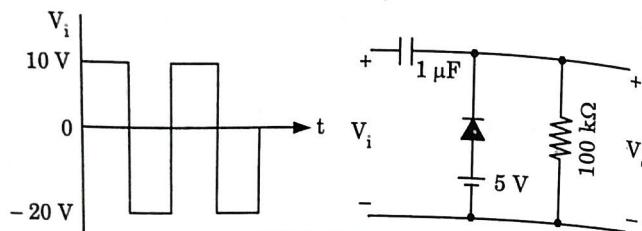


Fig. 1.17.4.

Que 1.18. Determine the output waveform of the following circuit, by presenting all the necessary calculations which have been done to determine this output.



AKTU 2020-21 (Sem-I), Marks 05

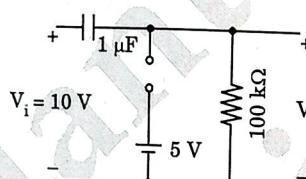
Answer

- i. 1. For positive pulse of
- V_i
- ,

Diode OFF and it acts as an open circuit.

∴

$$V_o = 5 \text{ V}$$



2. For negative pulse of
- V_i
- ,

Diode ON and it act as a short circuit.

$$V_o = 0.7 + 5 = 5.7 \text{ V}$$

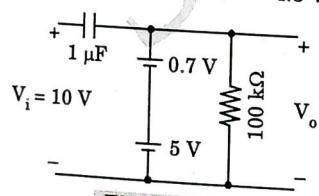
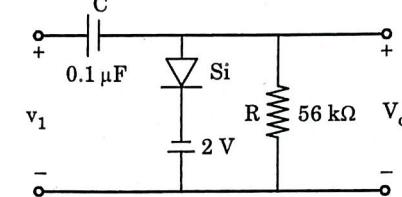
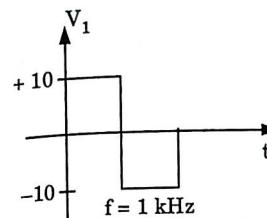
Capacitor charge to $-10 \text{ V} + 0.7 \text{ V} + 5 \text{ V} = -4.3 \text{ V}$ Que 1.19. Determine V_o for the circuit shown in Fig. 1.19.1.

Fig. 1.19.1.

AKTU 2017-18 (Sem-I), Marks 3.5

Answer

i.

$$\tau = RC = (56 \text{ k}\Omega)(0.1 \mu\text{F}) = 5.6 \text{ ms}$$

$$5\tau = 28 \text{ ms}$$

ii.

$$5\tau = 28 \text{ ms} \gg \frac{T}{2} = \frac{1 \text{ ms}}{2} = 0.5 \text{ ms},$$

$$\frac{5\tau}{T/2} = \frac{28}{0.5} = \frac{56}{1} = 56 : 1$$

iii.

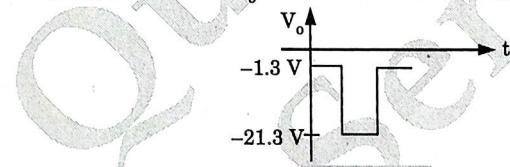
Positive pulse of V_i Diode 'ON' and $V_o = -2 \text{ V} + 0.7 \text{ V} = -1.3 \text{ V}$ Capacitor charge to $10 \text{ V} + 2 \text{ V} - 0.7 \text{ V} = 11.3 \text{ V}$ Negative pulse of V_i Diode 'OFF' and $V_o = -10 \text{ V} - 11.3 \text{ V} = -21.3 \text{ V}$ 

Fig. 1.19.2.

Que 1.20. Determine the output waveform of the following circuit.

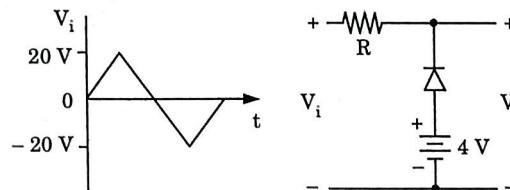


Fig. 1.20.1.

AKTU 2020-21 (Sem-I), Marks 05

Answer**i. For positive half cycle of V_i :**

Diode will be reverse biased and output will follow input voltage.

$$V_o = V_i$$

ii. For negative half cycle of V_i :

- When $-3.3 V < V_i < 0$, diode will be reverse biased.

So output will follow input voltage i.e. $V_o = V_i$

- When $V_i < -3.3 V$, then diode will be forward biased.

So $V_o = (0.7 - 4) = -3.3 V$

- The output waveform is shown in Fig. 1.20.2.

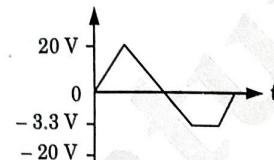


Fig. 1.20.2.

Que 1.21. Define clipper circuit. Sketch the output waveform for the circuit shown below given input.

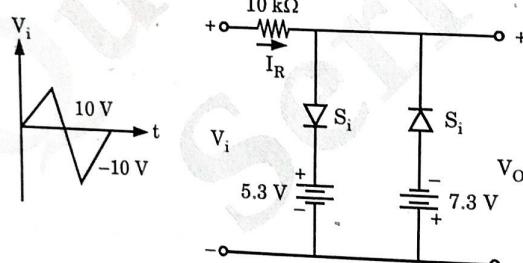


Fig. 1.21.1.
AKTU 2017-18(Sem-II), Marks 07

Answer

- A. Clipper : Refer Q. 1.14, Page 1-20J, Unit-1.
B. Numerical :

i. During positive half cycle of V_i :

- When $0 < V_i < 6 V$, then both diode D_1 and D_2 will be reverse biased and output will follow input voltage.

i.e.,

- When

$V_o = V_i$
 $V_i > 6 V$, then D_1 will be forward biased and D_2 will be reverse biased.

So,

- The current i_R will flow only when either of the two diodes will be forward biased.

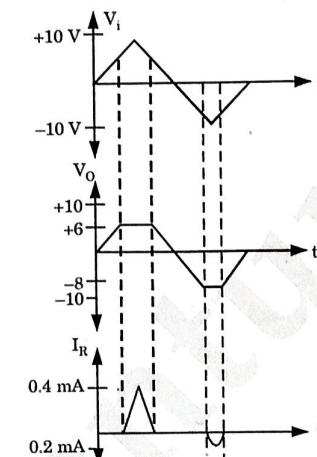


Fig. 1.21.2.

- For $V_{in} = 10 V$

$$I_R = \frac{V_{in} - 0.7 - 5.3}{10 \text{ k}\Omega} = \frac{10 - 6}{10 \text{ k}\Omega} = 0.4 \text{ mA (Peak).}$$

ii. During negative half cycle of V_i :

- When $-7 V < V_i < 0$, both diodes will be reverse biased so output will follow input voltage i.e., $V_o = V_i$

- When $V_i < -8 V$, then D_1 will be reverse biased and D_2 will be forward biased

So,

$$V_o = -(0.7 + 6.3) = -8 V \text{ (constant)}$$

For

$$V_{in} = -10 V$$

$$I_R = \frac{V_{in} + 0.7 + 7.3}{10 \text{ k}\Omega} = \frac{-10 + 8}{10 \text{ k}\Omega} = -0.2 \text{ mA.}$$

- The waveforms for V_o and I_R are shown in Fig. 1.21.2.

Que 1.22. What do mean by clipper ? Draw the output waveform of the given circuit.

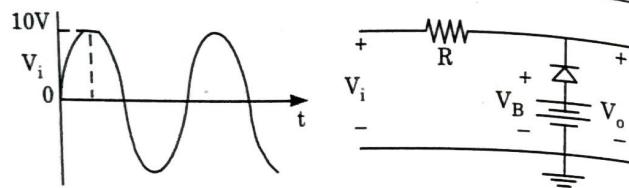


Fig. 1.22.1.

AKTU 2021-22 (Sem-I), Marks 10

Answer

A. Clipper : Refer Q. 1.14, Page 1-20J, Unit-1.

B. Numerical :

For positive half cycle of V_i : Diode will be reverse biased and output will follow input voltage,

$$V_o = V_i$$

For negative half cycle of V_i :

1. When $-V_B + 0.7 < V_i < 0$, diode will be reverse biased. So output will follow input voltage i.e., $V_o = V_i$.

2. When $V_i < -V_B + 0.7 < 0$, then diode will be forward biased.

So $V_o = (0.7 - V_B)$

3. The output waveform is shown in Fig. 1.22.2.

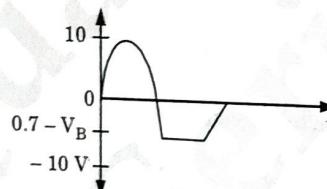


Fig. 1.22.2.

Que 1.23. Determine and draw output voltage for given network.

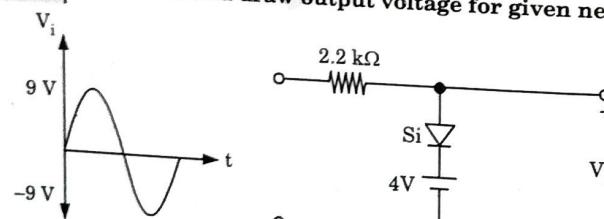


Fig. 1.23.1.

AKTU 2021-22 (Sem-II), Marks 10

Answer

Diode “on” for $V_i = 4.7 \text{ V}$
for $V_i > 4.7 \text{ V}$, $V_o = 4 \text{ V} + 0.7 \text{ V} = 4.7 \text{ V}$
for $V_i < 4.7 \text{ V}$, diode “off” and therefore

$$V_o = V_i$$

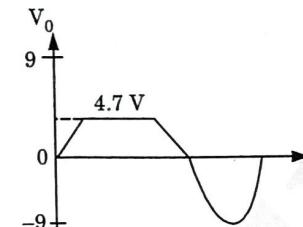


Fig. 1.23.2.

PART-5

Zener Diode as Shunt Regulator, Voltage-Multiplier Circuits.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 1.24. How zener diode is used as shunt regulator ? Explain it.

Answer

1. The circuit diagram for zener voltage/shunt regulator circuit is shown in Fig. 1.24.1.
2. The zener diode is selected with V_z equal to the voltage desired across the load.
3. Under reverse biased condition, voltage across zener diode practically remains constant, even if the current through it changes by a large extent.
4. Under normal conditions, the input current $I_i = I_L + I_z$ flows through resistor R . The input voltage V_i can be written as

$$V_i = I_i R + V_z = (I_L + I_z) R + V_z$$

5. When the input voltage V_i increases, as the voltage across zener diode remains constant, the drop across R will increase with a corresponding increase in $I_L + I_z$.

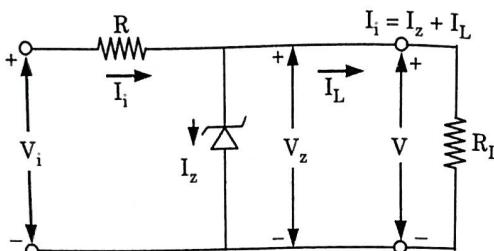


Fig. 1.24.1. Zener voltage regulator.

6. As V_z is a constant, the voltage across the load will also remain constant and hence, I_L will be a constant.
7. Therefore, an increase in $I_L + I_z$ will result in an increase in I_z which will not alter the voltage across load. Thus, zener diode is used as a voltage regulator.
8. To operate zener diode as voltage regulator, the reverse voltage applied to zener diode never exceeds PIV of the diode and at the same time, the applied input voltage must be greater than the breakdown voltage of the zener diode.

Que 1.25. For the circuit shown below, determine the value of maximum and minimum zener diode current.

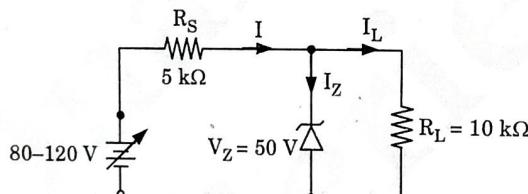


Fig. 1.25.1.

AKTU 2020-21 (Sem-I), Marks 10

Answer

Given : $R_S = 5 \text{ k}\Omega$, $V_z = 50 \text{ V}$, $R_L = 10 \text{ k}\Omega$, $V_{i\min} = 80 \text{ V}$, $V_{i\max} = 120 \text{ V}$
To Find : Maximum and minimum zener diode current.

1. Apply KCL at node A,
$$I = I_z + I_L \quad \dots(1.25.1)$$
2. We have,
$$I_L = \frac{V_z}{R_L} = \frac{50 \text{ V}}{10 \text{ k}\Omega} = 5 \text{ mA}$$

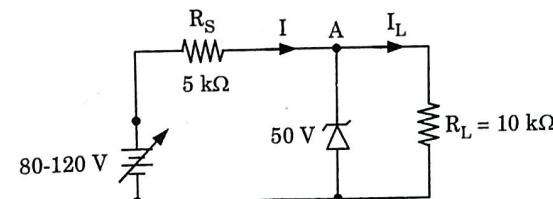


Fig. 1.25.2.

3. From the circuit,

$$I_{\min} R_S = V_{i\min} - V_z \\ I_{\min} = \frac{V_{i\min} - V_z}{R_S} = \frac{80 - 50}{5} = \frac{30}{5} = 6 \text{ mA}$$

$$\text{Similarly, } I_{\max} = \frac{V_{i\max} - V_z}{R_S} = \frac{120 - 50}{5} = \frac{70}{5} = 14 \text{ mA}$$

4. From eq. (1.25.1),

$$I_{\min} = I_{z(\min)} + I_L \\ I_{z(\min)} = I_{\min} - I_L = 6 - 5 = 1 \text{ mA}$$

$$\text{Similarly, } I_{z(\max)} = I_{\max} - I_L = 14 - 5 = 9 \text{ mA}$$

Que 1.26.

- i. Find the range of R_L and I_L that will maintain a constant output of 10 V (Fig. 1.26.1).
- ii. Also determine the maximum wattage rating of the zener diode for given circuit.

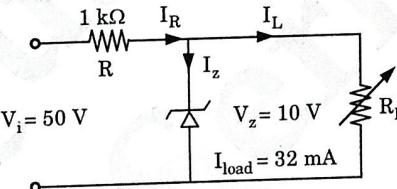


Fig. 1.26.1.

AKTU 2017-18(Sem-II), Marks 07

Answer

Given : $I_{z,\max} = 32 \text{ mA}$, $V_z = 10 \text{ V}$
To Find : Range of I_L and R_L , maximum wattage.

1. From the circuit, $I = I_z + I_L$
where, $I = \frac{V_i - V_z}{R} = \frac{50 - 10}{1 \text{ k}\Omega} = 40 \text{ mA}$
2. When I_L is minimum, I_z is maximum and vice versa.
Therefore, $I = I_{z,\max} + I_{L,\min} = I_{z,\min} + I_{L,\max}$

$$40 \times 10^{-3} = 32 \times 10^{-3} + I_{L,\min}$$

$$I_{L,\min} = 8 \text{ mA}$$

3. Hence, $R_{L,\max} = \frac{V_o}{I_{L,\min}} = \frac{10}{8 \times 10^{-3}} = 1.25 \text{ k}\Omega$

and

4. Let $I = I_{z,\min} + I_{L,\max}$
Therefore, $I_{L,\max} = 40 \text{ mA} - 5 \text{ mA} = 35 \text{ mA}$

$$R_{L,\min} = \frac{V_o}{I_{L,\max}} = \frac{10}{35 \text{ mA}} = 285.72 \Omega$$

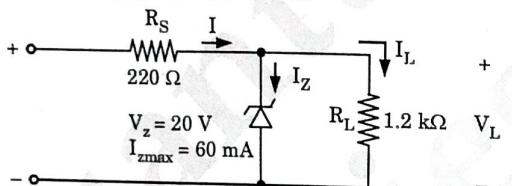
5. Hence, the range of I_L is between 8 mA and 35 mA while range of R_L is between 285.72 Ω and 1.25 k Ω .

6. Maximum wattage of zener diode is,

$$P_{z\max} = I_{z\max} V_z$$

$$= 32 \text{ mA} \times 10 = 320 \times 10^{-3} = 0.32 \text{ W}$$

Que 1.27. Determine the range of V_i for the Fig. 1.27.1, that will maintain the zener diode in "ON" state.



AKTU 2017-18 (Sem-I), Marks 3.5

Answer

Given : $R_S = 220 \Omega$, $V_z = 20 \text{ V}$, $I_{z\max} = 60 \text{ mA}$, $R_L = 1.2 \text{ k}\Omega$, $V_L = V_z = 20 \text{ V}$
To Find : Range of V_i .

1. We have $I_L = \frac{V_L}{R_L} = \frac{20}{1.2 \times 10^3} = 16.67 \text{ mA}$

2. So, $V_{i\min} = \frac{(R_S + R_L) \cdot V_z}{R_L} = \left(\frac{220 + 1200}{1200} \right) \times 20$
 $V_{i\min} = 23.67 \text{ V}$

3. Now, current through R_S

4. So, $I = I_{z\max} + I_L = 60 + 16.67 = 76.67 \text{ mA}$
 $V_{i\max} = I \cdot R_S + V_z = 76.67 \times 10^{-3} \times 220 + 20$
 $V_{i\max} = 36.87 \text{ V}$

Hence, the range of V_i lies between 23.67 V and 36.87 V

Que 1.28. Draw the V-I characteristics of zener diode. Determine the network of figure given below, determine the range of V_{in} that will maintain V_L at 8 V and not exceed the maximum power rating of the zener diode.

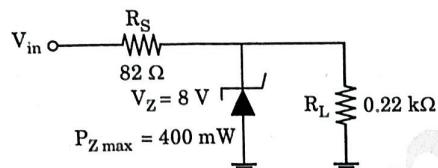


Fig. 1.28.1.

AKTU 2021-22 (Sem-I), Marks 10

Answer

A. V-I characteristics of zener diode : Refer Q. 1.4, Page 1-6J, Unit-1.

B. Numerical :

Given : $R_S = 82 \Omega$, $V_z = 8 \text{ V}$, $P_{z\max} = 400 \text{ mW}$, $R_L = 0.22 \text{ k}\Omega$, $V_L = 8 \text{ V}$.

To Find : Range of V_i .

1. We have

$$I_L = \frac{V_L}{R_L} = \frac{8 \text{ V}}{0.22 \text{ k}\Omega} = 36.36 \text{ mA}$$

2. So, $V_{i\min} = \frac{(R_S + R_L) \cdot V_z}{R_L} = \frac{(82 + 0.22) \cdot 8 \text{ V}}{0.22 \text{ k}\Omega}$
 $= \frac{302 \times 8}{220} = 10.98 \text{ V}$

3. We know, $P_{z\max} = I_{z\max} \cdot V_z$
 $400 \text{ mW} = I_{z\max} \cdot 8 \text{ V}$

$$\Rightarrow I_{z\max} = \frac{400 \text{ mW}}{8 \text{ V}} = 50 \text{ mA}$$

4. Now, current through R_S

$$I = I_{z\max} + I_L$$

$$= 50 \text{ mA} + 36.36 \text{ mA} = 86.36 \text{ mA}$$

5. So, $V_{i\max} = I \cdot R_S + V_z = 86.36 \text{ mA} \times 82 + 8 \text{ V}$
 $= 7.08 \text{ V} + 8 \text{ V} = 15.08 \text{ V}$

Que 1.29. | Describe with the help of circuit diagram working of voltage tripler.

AKTU 2015-16(Sem-I), Marks 05

OR

Explain with suitable circuit that how diode acts as a voltage multiplier ?

OR

Draw and discuss voltage tripler circuit.

AKTU 2016-17(Sem-I), Marks 05

OR

Define Voltage Multiplier. Draw the circuit and explain the working of Voltage Tripler and Quadrupler circuit.

AKTU 2021-22 (Sem-I), Marks 10

Answer

- Fig. 1.29.1 shows a circuit of general multiplier i.e., this circuit can be used as a doubler, tripler and quadrupler.
- Circuit-1 is a Doubler ($2V_m$).
- Circuit-2 is a Tripler ($3V_m$).
- Circuit-3 is a Quadrupler ($4V_m$).
- During positive half cycle, the diode D_1 is ON and it charges capacitor C_1 to V_m .
- In the first negative half cycle, the diode D_2 is ON and it charges C_2 to $2V_m$ ($V_{C2} = V_m + V_{C1} = 2V_m$). In this cycle the charge on capacitor C_1 starts discharging.

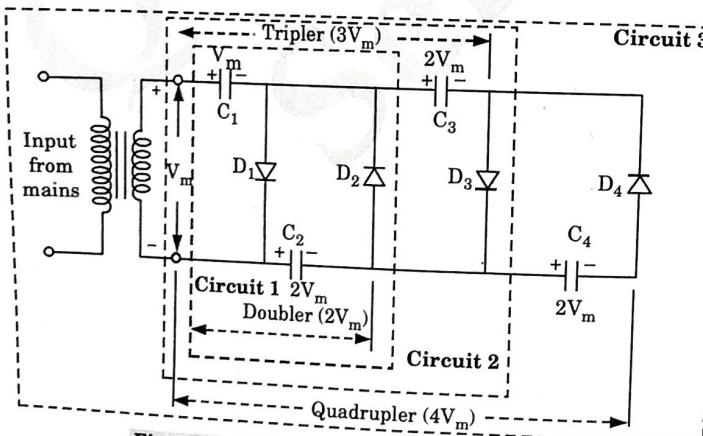


Fig. 1.29.1. General circuit diagram of multiplier.

- In the second positive half cycle the diode D_1 and D_3 are ON, the capacitor C_1 will be charged to V_m and the capacitor C_3 will be charged to

$$V_{C3} = V_i + (-V_{C1}) + V_{C2} = V_m - V_m + 2V_m \\ V_{C3} = 2V_m \text{ (Voltage across } C_3\text{)}$$

- During second negative half-cycle, the diode D_2 and diode D_4 are ON. The voltage across capacitor is given as :

$$V_{C4} = V_i + (V_{C2} + V_{C3} + V_{C1}) = V_m - 2V_m + 2V_m + V_m \\ V_{C4} = 2V_m$$

- Now

$$\text{Voltage across } C_1 \rightarrow V_{C1} = V_m$$

$$\text{Voltage across } C_2 \rightarrow V_{C2} = 2V_m$$

$$\text{Voltage across } C_3 \rightarrow V_{C3} = 2V_m$$

$$\text{Voltage across } C_4 \rightarrow V_{C4} = 2V_m$$

- Voltage doubler :** Taking output across C_2 .

$$V_O = V_{C2} = 2V_m$$

- Voltage tripler :** Taking output across C_3 and C_1 .

$$V_1 = V_{C1} + V_{C3} = V_m + 2V_m = 3V_m$$

- Voltage quadrupler :** Taking output across C_2 and C_4

$$V_O = V_{C2} + V_{C4} = 2V_m + 2V_m = 4V_m$$

Que 1.30. | What is voltage multiplier using p-n junction diode ?

Explain the operation of voltage doublers.

OR

Explain full wave voltage doubler with clear diagram.

AKTU 2017-18(Sem-I), Marks 3.5

OR

With help of a neat diagram, explain the working of a voltage doubler circuit.

AKTU 2020-21 (Sem-I), Marks 05

Answer

- The circuit which produces a greater DC output voltage than AC input voltage using a rectifier circuit is called as voltage multiplier.
- The output of voltage doubler is twice the peak input voltage.
- There are two types of voltage doubler circuits :
- Half wave voltage doubler :**
 - The circuit diagram is shown in Fig. 1.30.1.
 - During positive half-cycle of the input voltage, diode D_1 is forward biased (ON) and diode D_2 is reverse biased (OFF). Capacitor C_1 charges to the peak value of secondary voltage V_m with polarity.

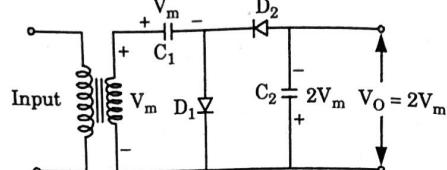


Fig. 1.30.1. Half wave voltage doubler.

3. During negative half-cycle, diode D_2 is ON while diode D_1 is OFF. Capacitor C_2 is charged up to a voltage i.e., the sum of peak-supply voltage and the voltage across C_1 .
4. During positive half-cycle : $V_{C1} = V_m$

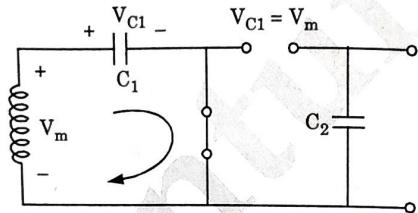


Fig. 1.30.2.

5. During negative half cycle :

$$\begin{aligned}-V_m - V_{C1} + V_{C2} &= 0 \\ -V_m - V_m + V_{C2} &= 0 \\ V_{C2} &= 2V_m\end{aligned}$$

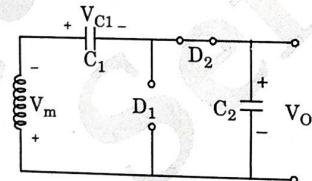


Fig. 1.30.3.

ii. Full wave voltage doubler :

1. The circuit diagram is shown in Fig. 1.30.4.
2. During positive half cycle, D_1 is ON and D_2 is OFF. Capacitor C_1 will be charged to a peak value V_m .
3. During negative half cycle, D_1 is OFF and D_2 is ON. Capacitor C_2 is charged to peak value V_m . Thus output voltage with no load connected : $V_O = V_{C1} + V_{C2}$

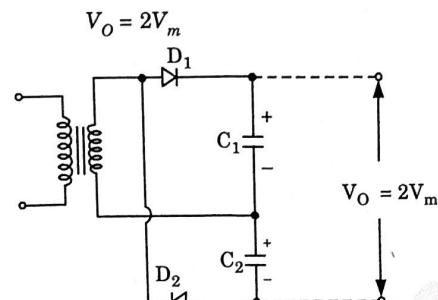


Fig. 1.30.4. Full wave voltage doubler.

PART-6

Special Purpose Two Terminal Devices : Light Emitting Diodes, Photodiodes.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 1.31. What is LED ? Give its principle of working, construction and applications.

Answer

A. **LED :** LED is a special type of semiconductor *p-n* junction that under forward bias emits external radiations in ultraviolet, visible and infrared regions of electromagnetic spectrum.

B. Construction of LED :

1. LED is just not an ordinary *p-n* junction diode where silicon is used. Here we use compound having elements like gallium, arsenic and phosphorus which are semitransparent unlike silicon which is opaque.
2. In all semiconductor *p-n* junctions, some of its energy will be given off as heat and some in the form of photons.
3. In the materials, such as gallium arsenide phosphide (GaAsP) or gallium phosphide (GaP), the number of photons of light energy emitted is sufficient to create a visible light source.

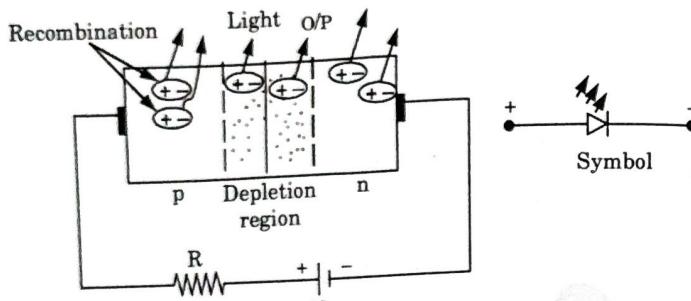


Fig. 1.31.1

C. Principle of LED :

1. The process involves :
 - i. Generation of electron-hole pair (EHP) by excitation of semiconductor.
 - ii. Recombination of EHP.
 - iii. Extraction of photons from the semiconductor.
2. The characteristic for LED is given in Fig. 1.31.2.

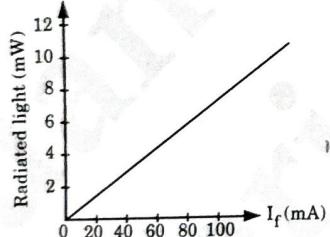


Fig. 1.31.2. Characteristics.

D. Working :

1. When LED is in forward bias condition, the electrons from n-type material cross the p-n junction and recombines with holes in the p-type material.
2. When recombination takes place, the recombining electrons release energy in the form of heat and light.
3. The emission depends upon the type of material, i.e.,
 - GaAs \rightarrow infrared radiation (invisible)
 - GaP \rightarrow red or green light (visible)
 - GaAsP \rightarrow red or yellow light (visible).

E. Applications :

1. Display LEDs like calculator, digital clocks etc.
2. Light source in optical fibre communication.
3. Light source in a source detector package like smoke detectors, tachometers, proximity detectors etc.

Que 1.32. What is photodiode ? What are its different types ? Describe the construction of a photodiode with its operation.

Answer**A. Photodiodes :**

1. Two terminal devices designed to respond to photon absorption are called photodiodes.
2. Photodiode is a semiconductor p-n junction device whose operation is limited to reverse bias region.
3. The types of photodiode are :
 - i. p-n diode
 - ii. p-i-n diode
 - iii. Avalanche diode
4. The output current of a reverse bias p-n junction changes when device is exposed to illumination.
5. The variation in the output current is linear with respect to luminous flux. The construction and symbol is shown in Fig. 1.32.1.

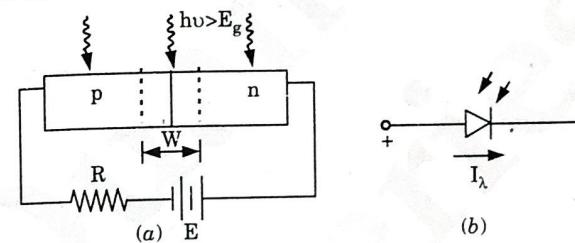


Fig. 1.32.1.

6. This diode is designed in such a manner that the rays are allowed to fall only on one surface across the junction. The remaining sides are restricted for the light to penetrate.
7. As the temperature due to illumination increases, more and more electron-hole pairs are generated and results in increasing the reverse saturation current.
8. When light rays fall on depletion width 'W', it creates electron-hole pair and electrons are swept into n-region and holes into p-region very rapidly. This gives rise to a photo current. This is the basic principle of operation of photodiode.

B. Photodiode characteristics :

1. The Fig. 1.32.2 shows the V-I characteristics of p-n junction photodiode with different illumination level.

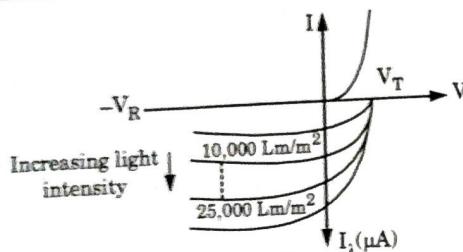


Fig. 1.32.2.

2. When no light ray is incident, the diode has a small reverse current I_λ known as dark current.
3. The dark current is that current which exists only with no applied illumination.
4. The increase in reverse voltage does not increase the reverse current significantly because all available charge carriers have already been swept across the junction.
5. The photodiode can also be used as a variable resistor controlled by light intensity.
6. Photodiode operates in quadrants, i.e., in third quadrant, both I and V are negative and power is being delivered to the device from external circuit.
7. In fourth quadrant, V is positive and I is negative and power is delivered from the junction to the external circuit. In applications, usually third quadrant operation is preferred.

PART-7*Varactor Diodes, Tunnel Diodes.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

Que 1.33. Explain input and output characteristics of varactor diode. AKTU 2015-16(Sem-II), Marks 05

OR

Write a short note on varactor diode.

AKTU 2020-21 (Sem-I), Marks 05**Answer**

1. This is also called as varicap, VVC (voltage variable capacitance), or tuning diode.
2. This is constructed from semiconductor materials. It is simply a voltage dependent variable capacitor.

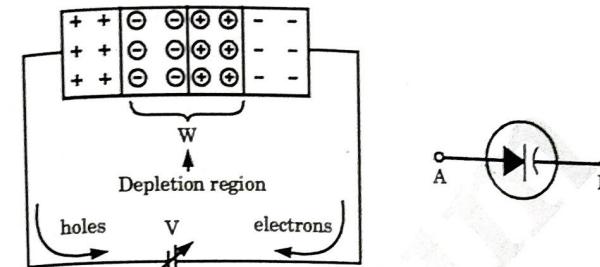


Fig. 1.33.1.

3. Fig. 1.33.1 shows the varactor diode in reverse-bias condition and symbol of varactor diodes.
If $V \rightarrow$ larger, then $W \rightarrow$ wider
 $V \rightarrow$ smaller, then $W \rightarrow$ narrower
4. The depletion region W in this case acts like an insulator preventing the conduction between the n and p region of the diode, just like a dielectric which separates the two plates of a capacitor.
5. Let area of plates = A
If distance between two capacitor plates = W
then capacitance, $C = \epsilon \cdot \frac{A}{W}$
where ϵ = Permittivity of the semiconductor materials.

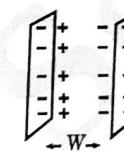


Fig. 1.33.2.

Varicap characteristics :

1. Fig. 1.33.3 shows the characteristics of a typical commercially available varicap diode.
2. We see that there is the initial sharp decline in C_T with increase in reverse bias.
3. The normal range of V_R for varactor diodes is limited to about 20 V.
4. In terms of the applied reverse bias, the transition capacitance is given approximately by

$$C_T = \frac{k}{(V_T + V_R)^n}$$

where k = Constant determined by the semiconductor material and construction technique

V_T = Knee potential

V_R = Magnitude of the applied reverse bias potential

$n = 1/2$ for alloy junction = $1/3$ for diffused junction

C_T (pF)

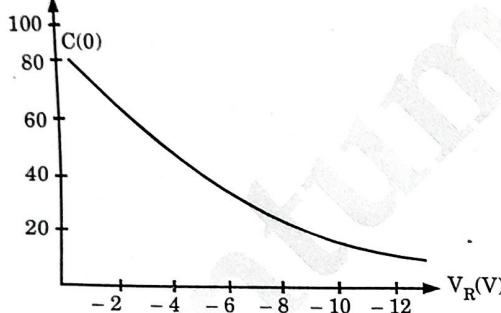


Fig. 1.33.3.

5. In terms of the capacitance at the zero-bias condition $C(0)$, the capacitance as a function of V_R is given by :

$$C_T(V_R) = \frac{C(0)}{(1 + |V_R/V_T|)^n}$$

Que 1.34. Explain working and characteristics of Tunnel diode with the help of neat diagram. AKTU 2015-16(Sem-I), Marks 05

OR

Discuss the construction and working of tunnel diode. Also sketch its I-V characteristics and explain.

AKTU 2017-18(Sem-II), Marks 07

OR

Explain principle of operation and construction of tunnel diode. Draw its V-I characteristic. AKTU 2016-17(Sem-II), Marks 5.25

OR

Explain the V-I characteristic of tunnel diode.

AKTU 2016-17(Sem-I), Marks 05

OR

Explain tunnel diode.

AKTU 2017-18(Sem-I), Marks 3.5

Answer

- A. Principle of Operation of tunnel Diode :

- i. In forward bias condition :
1. A small forward bias is applied across the junction.
2. Since, the potential of the p-side under this condition is higher than the potential of n-side, E_{Fn} will move below E_{Fn} , as shown in Fig. 1.34.1 (a) states in the valence band on the p-side, at same energy level.

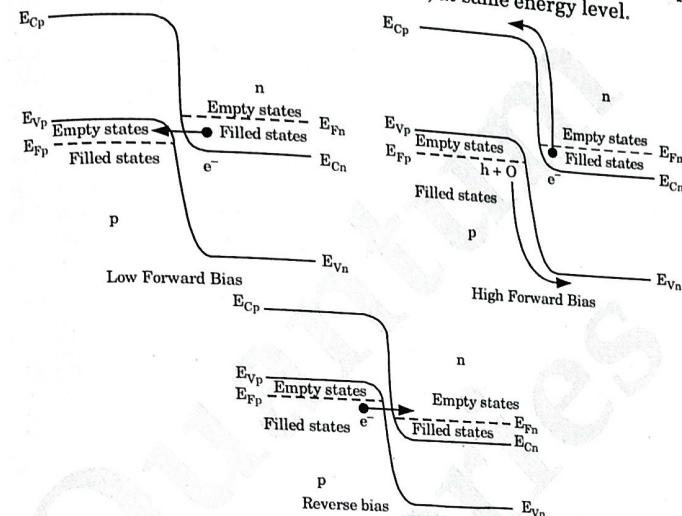


Fig. 1.34.1.

3. The thin barrier across the junction would permit tunneling of electrons from n-side to p-side, with the consequent current flowing from the p-side to n-side. Thus, I_D is positive for this case. As the forward bias is increased, more such filled states on the n-side would come opposite to the empty states.
4. With further increase in the forward bias, a specific condition would be reached when the maximum number of filled states in the conduction band on the n-side would face the maximum number of empty states in the valence band on the p-side. The tunneling current would reach a peak.
5. If the forward bias is increased further, then the conduction band of n-side would move away from the valence band of the p-side, and there would be no empty states on the p-side corresponding to the filled states on n-side.
6. Hence, tunneling current would go to zero and the normal diffusion component of current would dominate. This results in normal p-n junction diode characteristics.

ii. In reverse bias condition :

- When negative voltage is applied to the *p*-side with respect to *n*-side, this would push E_{Fp} above E_{Fn} with their separation being equal to the applied voltage.
 - The filled states of the *p*-side are directly opposite to the empty states on the *n*-side across a very narrow barrier.
 - Thus, the electrons from *p*-side would easily tunnel through this thin barrier by the process of quantum mechanical tunneling and appear on the *n*-side.
 - Since, electrons travel from *p*-side to *n*-side, the actual direction of current is from *n* to *p*-side and is negative.
 - As the amount of reverse bias is increased, more number of filled states in the valence band of the *p*-side would appear opposite to the number of empty states in the conduction band of the *n*-side and the reverse current would keep on increasing with reverse voltage.
- B. Characteristics :** Due to heavy doping, the current in negative resistance region is suddenly increased with a small applied voltage. Due to this reduced depletion region the sudden increase in current (at small applied voltage) is called "carrier punching through" effect.

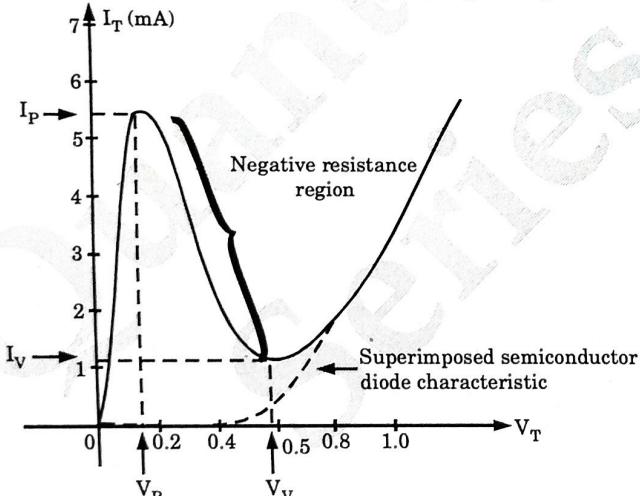


Fig. 1.34.2.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Semiconductor Diode

- Q. 1.** Explain the V-I characteristic of *p-n* junction diode. Draw well labelled characteristic.

Ans. Refer Q. 1.2.

- Q. 2.** Explain the working of half wave and full wave bridge rectifier.

Ans. Refer Q. 1.9.

- Q. 3.** Explain the following terms in context with half wave rectifier and full wave rectifier;

- DC voltage and DC current
- RMS value of current

Ans. Refer Q. 1.10.

- Q. 4.** Sketch V_o for each network of Fig. 1, for the input shown.

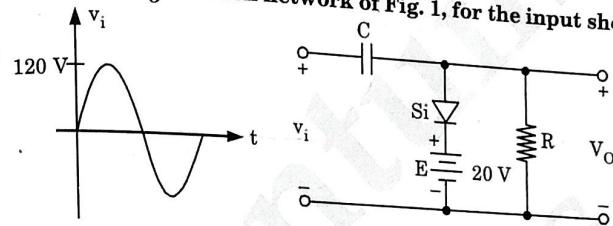


Fig. 1.

Ans. Refer Q. 1.16.

- Q. 5.** What do mean by clipper ? Draw the output waveform of the given circuit.

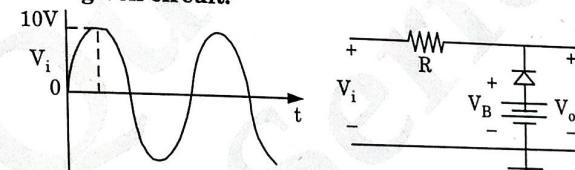


Fig. 2.

Ans. Refer Q. 1.22.

- Q. 6.** Describe with the help of circuit diagram working of voltage tripler.

Ans. Refer Q. 1.29.

- Q. 7.** What is voltage multiplier using *p-n* junction diode ? Explain the operation of voltage doublers.

Ans. Refer Q. 1.30.

- Q. 8.** Explain working and characteristics of Tunnel diode with the help of neat diagram.

Ans. Refer Q. 1.34.



2

UNIT

BJT and FET

CONTENTS

- Part-1 :** Bipolar Junction Transistor : **2-2J to 2-7J**
Transistor Construction,
Operation, Amplification Action
- Part-2 :** Common Base, Common **2-7J to 2-17J**
Emitter, Common
Collector Configuration
- Part-3 :** Field Effect Transistor : **2-18J to 2-26J**
Constructions and Characteristics
of JFETs, Transfer Characteristics
- Part-4 :** MOSFET (MOS) (Depletion and **2-26J to 2-39J**
Enhancement) Type,
Transfer Characteristic

PART-1

Bipolar Junction Transistor : Transistor Construction, Operation, Amplification Action.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 2.1. Explain BJT.

Answer

1. A junction transistor is a three-layer semiconductor device, sandwich of one type of semiconductor material between two layers of the other type.
2. There are two types of transistors :
 - a. *npn* transistor and
 - b. *pnp* transistor.
3. When a layer of *p*-type material is sandwiched between two layers of *n*-type material, the transistor is known as *npn* as shown in Fig. 2.1.1(a).
4. Similarly, when a layer of *n*-type material is sandwiched between two layers of *p*-type material, the transistor is known as *pnp* transistor as shown in Fig. 2.1.1(b).
5. The transistors are made either from silicon or germanium crystal.
6. The symbols for *npn* and *pnp* transistors are also shown in Fig. 2.1.1.

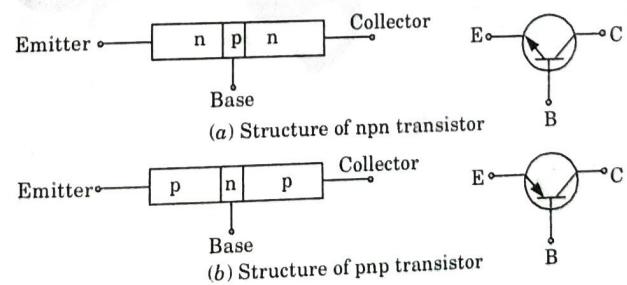


Fig. 2.1.1.

7. A transistor has three doped region :

a. Emitter :

- This is the left hand section of the transistor.
- The main function of this region is to supply majority charge carriers (either holes or electrons) to the base and hence it is more heavily doped in comparison to other regions.

b. Base :

- The middle section of the transistor is known as base.
- This is very lightly doped and is very thin (10^{-6} m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

c. Collector :

- The right hand section of transistor is known as collector.
- The main function of the collector is to collect majority charge carriers through the base. This is moderately doped.
- The arrow head direction indicates the conventional direction of current flow i.e., in case of *npn* it is from base to emitter while in case of *pnp* it is from emitter to base.
- In most of the cases the collector region is made large due to the fact that collector has to dissipate much greater power.
- The junction between emitter and base may be called as emitter-base junction and junction between base and collector may be called as collector-base junction.
- The emitter-base junction is always forward biased while the collector-base junction is reversed biased.
- The resistance of emitter-base junction is very small as compared to collector-base junction.
- So, forward bias applied to emitter-base junction is generally very small and reverse bias on collector-base junction is much higher.

Que 2.2. | Describe the operation of *pnp* transistor.

Answer

- pnp* transistor with emitter base junction as forward bias and collector base junction as reversed biased is shown in Fig. 2.2.1.
- The holes of *p*-region are repelled by positive terminal of battery V_{EE} towards the base.
- The potential barrier at emitter base junction is reduced as it is forward bias and holes cross this junction and penetrate into *n*-region, constitute the emitter current I_E .
- The width of base is very thin and only 5 % of holes recombine with the free electrons of *n*-region which constitutes the current I_B .

- The remaining holes are able to drift across the base and enter into the collector region.
- They are swept up by negative collector voltage V_{CC} . This constitutes the collector current I_C .

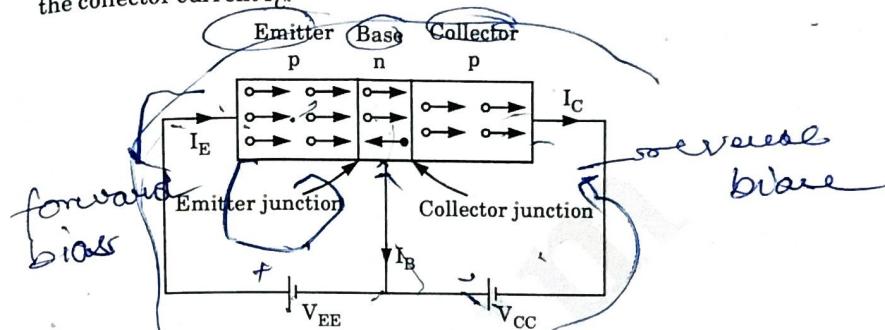


Fig. 2.2.1. Operation of *pnp* transistor.

- As holes reach the collector, electrons are emitted from the negative terminal of battery and neutralize these holes.
- Now a covalent bond near the emitter electrode breaks down. The liberated electron enters the positive terminal of battery V_{EE} . This process is repeated again and again.
- As the width of the base region is very small, the ratio of hole current to electron current is very large so the electron current may be neglected.
- Thus only the hole current plays the important role in the operation of *pnp* transistor.

Que 2.3. | Explain the operation of *npn* transistor.

OR

Explain various current components in *npn* transistor with help of suitable diagram.

AKTU 2016-17(Sem-I), Marks 05

Answer

- The biasing of *npn* transistor is shown in Fig. 2.3.1.
- The emitter base junction is forward biased because electrons are repelled from the negative terminal of battery V_{EE} towards the junction.
- The collector base junction is reversed biased because electrons are flowing away from the collector junction towards the positive collector battery terminal V_{CC} .
- The electrons in emitter region are repelled from the negative terminal of the battery towards the emitter junction.

5. Since the potential barrier at the junction is reduced due to forward bias and base region is very thin and lightly doped, electrons cross the *p*-type base region.
6. A few electrons combine with the holes in *p*-region and are lost as charge carrier.
7. Now electrons in *n*-region swept up by positive collector voltage V_{CC} . In this way electron conduction takes place, continuously so long as the two junctions are properly biased.
8. So the current conduction in *npn* transistor is carried out by the electrons.

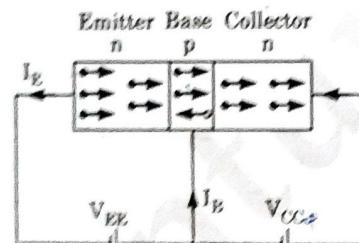


Fig. 2.3.1.

9. Applying Kirchhoff's current law,

$$I_E = I_C + I_B$$

10. The collector current has two components the majority and minority carriers. The minority current component is called leakage current I_{CO} .

So,

$$I_C = I_{C \text{ majority}} + I_{CO \text{ minority}}$$

Que 2.4. Describe the biasing of BJT circuit.

Answer

1. Biasing is necessary to establish the proper region of operation for AC amplification.
2. The emitter layer is heavily doped, base is lightly doped and collector is moderately doped.
3. This low doping level decreases the conductivity and hence increases the resistance of the material by limiting the number of "free" carriers.

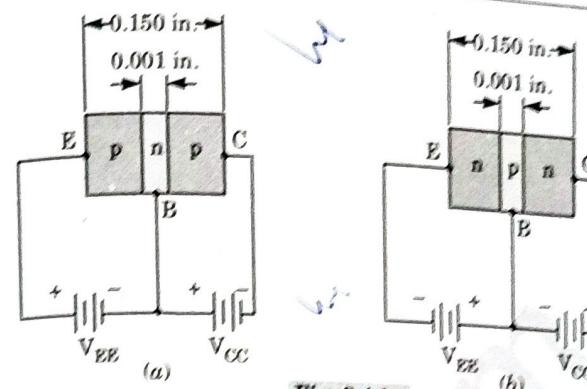


Fig. 2.4.1.

A. For *pnp* transistor :

- i. *pnp* transistor with emitter-base junction as forward bias and collector-base junction as reverse biased.
- ii. The potential barrier at emitter-base junction is reduced as it is forward biased and holes pass through this junction.
- iii. By applying a negative voltage at collector, the holes are easily drifted across the collector-base junction to constitute a current I_C .

B. For *npn* transistor :

- i. The emitter-base junction of *npn* is forward bias and the electron is repelled by a negative forward junction.
- ii. The collector-base function is reverse bias because electrons flow toward positive collector battery terminal V_{CC} to constitute a current I_C .

Que 2.5. Explain transistor as an amplifier in detail.

Answer

1. The transistor has two *p-n* junctions i.e., it is like two diodes. The junction between emitter and base may be called emitter-base diode or simply emitter diode. The junction between base and collector may be called as collector-base diode or collector diode. The basic circuit of a transistor amplifier is shown in Fig. 2.5.1.
2. The weak signal to be amplified is applied between emitter-base circuit and the output is taken across the load resistor R_L connected in the collector-base circuit.
3. Let us assume for instant V_{EE} is disconnected.
4. Now for negative peak of signal, the emitter base junction will be reversed bias, which is not desirable, because to achieve amplification, the input circuit should remain forward bias.

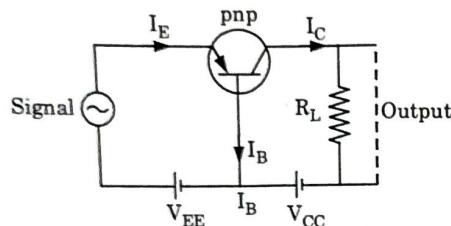


Fig. 2.5.1. Transistor as an amplifier.

5. A small change in signal voltage produces an appreciable change in emitter current because the input circuit has low resistance.
6. Due to transistor action, the change in emitter current causes almost the same change in collector current.
7. When the collector current flows through the load resistance R_L , a large voltage is developed across it.
8. In this way, a weak signal applied in the input circuit appears in the amplified form across the output circuit.
9. Let, small voltage change ΔV_i causes large emitter current change ΔI_E . We define it by the symbol α that fraction of this current change is collected and pass through R_L .

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ i.e., } \Delta I_C = \alpha \Delta I_E$$

10. The change in output voltage across load resistor

$$\begin{aligned}\Delta V_O &= R_L \times \Delta I_C \\ &= R_L \times \alpha \times \Delta I_E\end{aligned}$$

11. The voltage amplification

$$A = \frac{\Delta V_O}{\Delta V_i}$$

will be greater than unity and transistor acts as an amplifier.

PART-2

Common Base, Common Emitter, Common Collector Configuration.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

- Que 2.6.** Draw the basic structure of CB BJT and explain its principle of operation with in neat diagram along with its input and output characteristics. AKTU 2017-18(Sem-II), Marks 07

OR

Explain the working of a common base circuit with its circuit diagram.

AKTU 2015-16(Sem-II), Marks 05

OR

Derive the relationship between current amplification factor for common emitter and common base configuration of a bipolar junction transistor.

AKTU 2020-21(Sem-I), Marks 05

OR

Draw and explain common base N-P-N Transistor with its input and output characteristic graph. Also write an expression for output current.

AKTU 2021-22(Sem-II), Marks 10

Answer

emitter and base.

A. Common-base (CB) configuration :

1. In this configuration, the input signal is applied between emitter and base. The output is collected from collector and base as shown in Fig. 2.6.1.

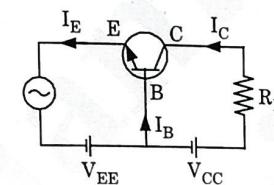


Fig. 2.6.1. Common-base npn transistor amplifier.

Current amplification factor (α) :

1. It is defined as the ratio of the collector current to the emitter current of a transistor when no signal is applied and is called DC alpha (α_{DC}).

$$\alpha_{DC} = \frac{I_C}{I_E}$$

2. Simply α_{DC} is α

$$\text{Then } \alpha = \frac{I_C}{I_E}$$

3. Higher the value of α better is the transistor in the sense that collector current approaches the emitter current.

$$\begin{aligned}I_C &= \alpha I_E \text{ and } I_B = I_E - I_C \\ I_B &= I_E - \alpha I_E = I_E(1 - \alpha)\end{aligned}$$

4. Now, when signal is applied, the ratio of change in collector to emitter current at constant collector base voltage is defined as current amplification factor.

$$\alpha_{AC} = \frac{\Delta I_C}{\Delta I_E} \Big|_{V_{CB} = \text{constant}}$$

Practically $\alpha_{DC} = \alpha_{AC} = \alpha = 0.9$ to 0.99

5. Total collector current $I_C = \underbrace{\alpha I_E}_{\text{Majority}} + \underbrace{I_{CBO}}_{\text{Minority}}$

6. The collector current can also be expressed as

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1 - \alpha} \right) I_B + \left(\frac{1}{1 - \alpha} \right) I_{CBO}$$

7. The relation between α and β is given by

$$\alpha = \frac{\beta}{1 + \beta} \quad \text{or} \quad 1 - \alpha = \frac{1}{1 + \beta}$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

B. Characteristics of CB circuit :

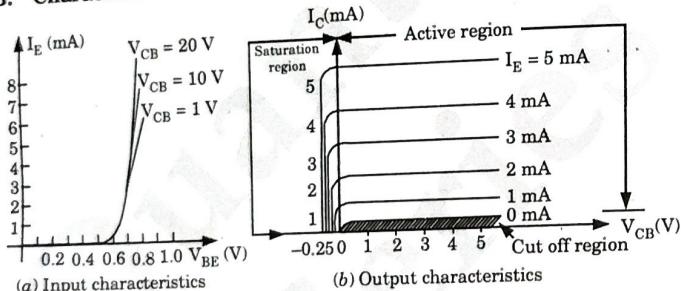


Fig. 2.6.2.

a. Input characteristics :

- i. There exists a cut in, offset or threshold voltage V_{BE} below which the current is very small.
- ii. I_E increases rapidly with small increase in V_{BE} i.e., input resistance is very small.

b. Output characteristics :

- i. In active region, the collector current is independent of collector voltage and depends upon emitter current but if V_{CB} increases beyond a certain value, I_C increases rapidly due to avalanche breakdown.

In this region, the base-emitter function is forward biased whereas collector-base function is reversed biased.

- ii. In cut off region, a small amount of collector current flows even when $I_E = 0$, i.e., leakage current I_{CBO} .

Here emitter base and collector base junctions both are reversed biased.

iii. In saturation region, current I_C flows even if $V_{CB} \approx 0$.

Here collector and emitter junctions both are forward biased.

C. **Expression for output current :** In common base NPN transistor, collector current I_C is output current. Therefore, the expression for output current is,

$$I_C = \left(\frac{\alpha}{1 - \alpha} \right) I_B + \left(\frac{1}{1 - \alpha} \right) I_{CBO}$$

Que 2.7. Draw and explain the input and output characteristics of common emitter configuration.

AKTU 2015-16(Sem-I), Marks 05

OR

Draw the common emitter circuit and sketch the input and output characteristics. Also explain active region, cut-off region and saturation region by indicating them on the characteristics curve.

AKTU 2017-18(Sem-I), Marks 07

OR

Draw the CE configuration circuit of BJT and explain its input and output characteristics.

AKTU 2015-16(Sem-II), Marks 7.5

OR

Draw the circuit diagram of BJT in CE configuration. Draw output characteristic curves and indicate the different regions of operation.

AKTU 2016-17(Sem-I), Marks 05

OR

Why is transistor biasing required ? Describe collector to base biasing in CE n-p-n transistor circuit.

AKTU 2016-17(Sem-I), Marks 05

OR

Describe the construction of an npn bipolar junction transistor. Draw well labeled input and output characteristics of an npn transistor in common emitter configuration. Also mark all the regions of operation.

AKTU 2020-21(Sem-I), Marks 10

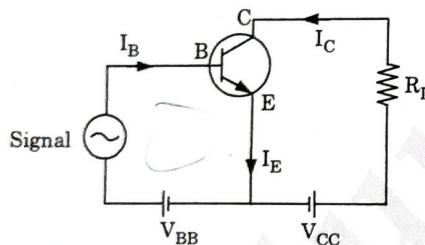
OR

Describe the construction and working of an NPN transistor in CE configuration with respect to size and doping. Also, draw the input and output characteristic graph.

AKTU 2021-22(Sem-I), Marks 10

Answer**A. CE configuration :**

1. In CE configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter.
2. As emitter is common to input and output circuits, hence the name common emitter configuration and is shown in Fig. 2.7.1.

**Fig. 2.7.1. Common-emitter npn transistor amplifier.**

3. The base current amplification factor is the ratio of collector current to the base current and is also called DC beta (β_{DC}) of a transistor, when no signal is applied.

$$\beta_{DC} = \beta = \frac{I_C}{I_B}$$

4. When signal is applied, the ratio of change in collector current to the change in base current is defined as current amplification factor.

$$\beta_{AC} = \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_C = \beta I_B$$

β is generally greater than 20 and ranges from 20 to 500. Hence, this configuration is frequently used when current gain as well as voltage gain is required.

5. Total collector current

$$I_C = \beta I_B + I_{CEO}$$

6. We know that $I_E = I_B + I_C$

$$I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

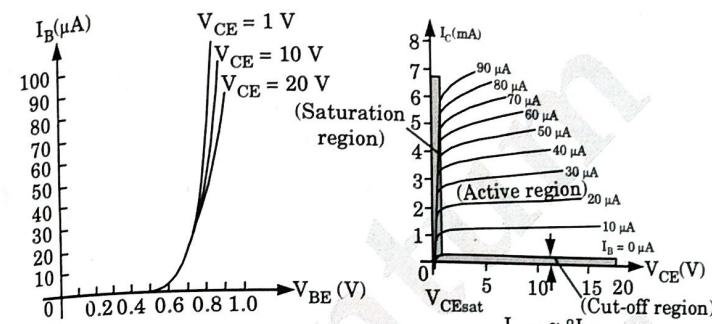
$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

7. On solving we get $\beta = \frac{\alpha}{1 - \alpha}$ and $I_{CEO} = \frac{1}{1 - \alpha} I_{CBO}$

B. Characteristics of common emitter circuit :
Input characteristic :

- i. The forward biased diode curve is expected because the base emitter section of transistor is a diode and it is forward biased.
- ii. In this case, I_B increases less rapidly with V_{BE} as compared to common base configuration i.e., input resistance of common emitter is higher than common base circuit.

**Fig. 2.7.2.****b. Output characteristics :**

- i. In active region, for small values of base current, the effect of collector voltage over collector current is small while for large base current values effect increases. Thus, the current gain of this configuration is greater than unity.
- ii. When V_{CE} has very low value, the transistor is said to be saturated. The change in I_B does not produce a corresponding change in I_C .
- iii. In cut-off region, a small amount of I_C flows even when $I_B = 0$. i.e., $I_{CEO} \approx \beta I_{CBO}$

C. Transistor biasing : Refer Q. 2.4, Page 2-5J, Unit-2.**D. npn transistor :** Refer Q. 2.3, Page 2-4J, Unit-2.

Que 2.8. Explain the operation of common collector configuration with suitable characteristics in detail.

Answer

1. The circuit diagram for determining the static characteristics of an npn transistor in the common collector configuration is shown in Fig. 2.8.1.

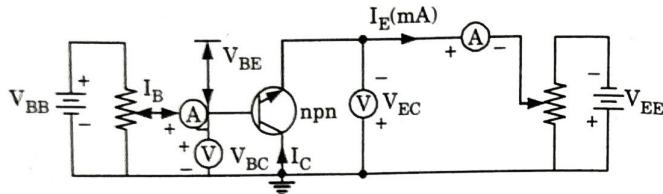


Fig. 2.8.1.

Input characteristics :

1. To determine the input characteristics, V_{EC} is kept at a suitable fixed value.
2. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted.
3. This is repeated for different fixed values of V_{EC} . Plot of V_{BC} versus I_B for different values of V_{EC} is shown in Fig. 2.8.2.

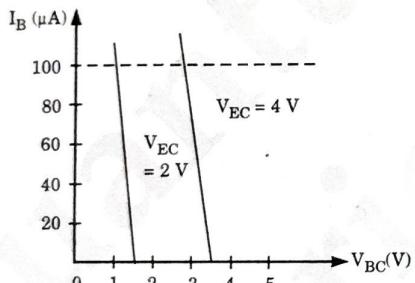


Fig. 2.8.2. Input characteristics.

Output characteristics :

1. The output characteristics shown in Fig. 2.8.3 are the plots of V_{EC} versus I_C for different values of I_B .

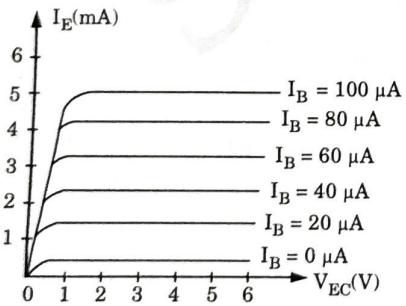


Fig. 2.8.3. Output characteristics.

Que 2.9. Derive the relation between α , β and γ .

Answer

1. We know, $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$
2. $I_E = I_B + I_C$, $I_B = I_E - I_C$
3. Now $\beta = \frac{I_C}{I_E - I_C} = \frac{I_C / I_E}{1 - I_C / I_E} = \frac{\alpha}{1 - \alpha}$
 $\beta(1 - \alpha) = \alpha$ or $\beta - \beta\alpha = \alpha$
 $\beta = \alpha(1 + \beta)$
 $\alpha = \frac{\beta}{1 + \beta}$
 $\therefore \frac{1}{1 - \alpha} = 1 + \beta$
4. $\gamma = \frac{I_E}{I_B}$ and $\alpha = \frac{I_C}{I_E}$
5. Also $I_B = I_E - I_C$
6. $\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - (I_C / I_E)} = \frac{1}{1 - \alpha}$... (2.9.1)
7. We have, $1 - \alpha = \frac{1}{1 + \beta}$... (2.9.2)
8. Put values of eq. (2.9.2) in eq. (2.9.1)
 $\gamma = \frac{1}{1 - \alpha} = 1 + \beta$

Que 2.10. An *npn* transistor with $\beta = 98$ is operated in the CB configuration, if the emitter current is 2 mA and reverse saturation current is 12 μA . What are the base and collector current ?

AKTU 2016-17(Sem-I), Marks 05

Answer

Given : $\beta = 98$, $I_E = 2\text{ mA}$, $I_{sat} = 12\text{ }\mu\text{A}$
To Find : I_B , I_C

$$\alpha = \frac{\beta}{1 + \beta} = \frac{98}{1 + 98} = 0.989$$

$$\alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E = 0.989 \times 2 = 1.978 \text{ mA}$$

$$I_B = I_E - I_C = 2 - 1.978 = 0.022 \text{ mA}$$

Que 2.11. For the network of Fig. 2.11.1

- a. Determine R_B and R_E
- b. Find V_B , V_{CE} , and V_{BC}

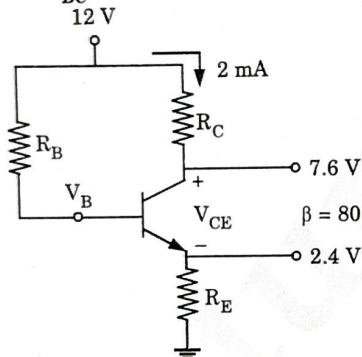


Fig. 2.11.1.

AKTU 2017-18(Sem-I), Marks 07

Answer

Given : $V_{CC} = 12 \text{ V}$, $V_C = 7.6 \text{ V}$, $V_E = 2.4 \text{ V}$, $\beta = 80$

To Find : R_B , R_E , V_B , V_{CE} , V_{BC}

1. We have, $V_{CE} = V_C - V_E = 7.6 \text{ V} - 2.4 \text{ V} = 5.2 \text{ V}$
2. Now $\alpha = \frac{\beta}{\beta + 1} = \frac{80}{80 + 1} = 0.98$
So, $I_E = I_C/\alpha = 2 \text{ mA}$ and $I_B = I_C/80 = 0.025 \text{ mA}$
 $R_E = \frac{V_E}{I_E} = \frac{2.4 \text{ V}}{2 \text{ mA}} = 1.2 \text{ k}\Omega$
3. Now $V_{CC} = V_{CE} + I_C R_C + I_E R_E$
 $12 = 5.2 + 2R_C + 1.2 \times 2$
 $R_C = 2.2 \text{ k}\Omega$
and $V_{CC} = I_B R_B + V_{BE} + I_E R_E$
 $12 = 0.025 \text{ mA} \times R_B + 0.7 \text{ V} + 1.2 \times 2$
 $R_B = 356 \text{ k}\Omega$
 $V_B = V_E + V_{BE} = 2.4 + 0.7 = 3.1 \text{ V}$
 $V_{BC} = V_B - V_C$
 $= 3.1 - 7.6 = -4.5 \text{ V}$

Que 2.12. Define α and β with respect to BJT and derive the relationship between them. A transistor having $\alpha = 0.975$ and reverse saturation current $I_{CBO} = 10 \mu\text{A}$ is operated in CE mode. If the base current is $250 \mu\text{A}$. Calculate I_E and I_C .

AKTU 2021-22(Sem-I), Marks 10

Answer

- A. α : Refer Q. 2.6, Page 2-7J, Unit-2.
- B. β : Refer Q. 2.7, Page 2-10J, Unit-2.
- C. Derivation : Refer Q. 2.9, Page 2-14J, Unit-2.
- D. Numerical :

Given : $\alpha = 0.975$, $I_{CBO} = 10 \mu\text{A}$, $I_B = 250 \mu\text{A}$

To Find : I_E , I_C

$$1. \text{ We know, } \beta = \frac{\alpha}{1 - \alpha} = \frac{0.975}{1 - 0.975} = 39$$

$$2. \quad \beta = \frac{I_C}{I_B}$$

$$I_C = \beta \times I_B = 250 \times 39 = 9750 \mu\text{A} = 9.75 \text{ mA}$$

$$I_E = I_C + I_B = 9750 + 250 = 10000 \mu\text{A} = 10 \text{ mA}$$

Que 2.13. Given that $I_{CQ} = 2 \text{ mA}$ and $V_{CEQ} = 10 \text{ V}$, determine R_1 and R_C for the network of Fig. 2.13.1.

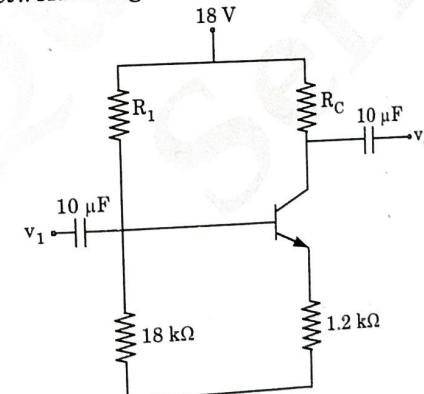


Fig. 2.13.1.

AKTU 2016-17(Sem-II), Marks 07

Answer

Given : $I_{CQ} = 2 \text{ mA}$, $V_{CEQ} = 10 \text{ V}$, $R_E = 1.2 \text{ k}\Omega$, $R_2 = 18 \text{ k}\Omega$

To Find : R_1, R_C

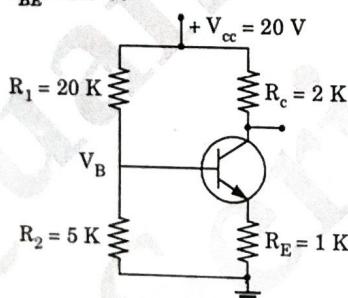
$$1. \quad V_B = \frac{18 \text{ k}\Omega}{R_1 + 18 \text{ k}\Omega} \times 18 \text{ V} = \frac{324 \times 10^3}{R_1 + 18 \times 10^3} \text{ V} \quad \dots(2.13.1)$$

$$2. \quad I_C = I_E = \frac{V_B - V_{BE}}{R_E}$$

$$2 \times 10^{-3} = \frac{\frac{324 \times 10^3}{R_1 + 18 \times 10^3} - 0.7}{1.2 \times 10^3}$$

$$3. \quad R_1 = 86.5 \text{ k}\Omega \\ V_{CE} = V_{CC} - I_C(R_C + R_E) \\ 10 = 18 - 2 \times 10^{-3}(R_C + 1.2 \times 10^3) \\ R_C = 2.8 \text{ k}\Omega$$

Que 2.14. For the circuit shown in Fig. 2.14.1, determine V_B, I_C, V_C . Given that $\beta = 80$, $V_{BE} = 0.7 \text{ V}$.



AKTU 2016-17(Sem-I), Marks 7.5

Answer

$$R_{th} = R_1 \parallel R_2 = \frac{20 \times 5}{20 + 5} = 4 \text{ K}$$

$$V_{th} = V_B = \frac{20 \times 5}{20 + 5} = 4 \text{ V}$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1 + \beta)R_E} = \frac{4 - 0.7}{4 + 81} = 0.0388 \text{ mA}$$

$$I_c = \beta I_B = 80 \times 0.0388 = 3.11 \text{ mA}$$

$$V_c = V_{cc} - I_c R_c = 20 - (3.11 \times 2) = 13.8 \text{ V}$$

PART-3

Field Effect Transistor : Construction and Characteristics of JFETs, Transfer Characteristics.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 2.15. Explain the transconductance curve of a JFET.

AKTU 2015-16(Sem-II), Marks 05

OR

Draw the circuit and explain the drain characteristic for N-channel JFET.

AKTU 2016-17(Sem-I), Marks 05

OR

Draw and explain the n-channel JFET and draw its transfer characteristics.

AKTU 2016-17(Sem-II), Marks 5.25

OR

Explain the formation of depletion region in JFET.

AKTU 2016-17(Sem-I), Marks 7.5

OR

Explain the construction and working of N-channel JFET. Draw the drain characteristics and transfer curve.

AKTU 2017-18(Sem-I), Marks 3.5

Answer

JFET (Junction Field Effect Transistor) :

A. Basic construction :

- The structure of n-channel field effect transistor is shown in Fig. 2.15.1.

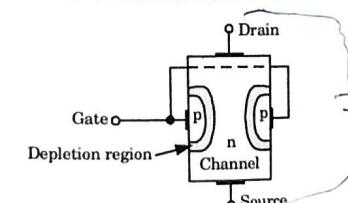


Fig. 2.15.1. Junction field-effect transistor (JFET).

2. For the fabrication of *n*-channel JFET, a narrow bar of *n*-type semiconductor material is taken. Now on opposite sides of its middle part, two heavily doped *p*-type regions are formed by diffusion as shown in Fig. 2.15.1.
3. The junctions form two *p-n* diodes or gates.
4. The area between the gates is called a channel.
5. Actually the two *p*-regions are internally connected and a single lead is taken out, which is called as gate junction.
6. Ohmic contacts are made at the two ends of *n*-type semiconductor bar.
7. One lead is called as source terminal *S* and the other as drain terminal *D*.
8. When a potential difference is established between source and drain, a current flows from one end to the other end in *n*-type material which forms a sort of channel. This current consists of majority carriers which in this case are electrons.

B. Operation of *n*-channel FET :

1. The operation of *n*-channel FET can be understood with the help of Fig. 2.15.2.
2. First suppose that the gate has been reversed biased by gate battery V_{GG} and drain battery is not connected. So that space charge region or depletion region on either side of a reverse biased *p-n* junction are formed.
3. Further consider effect of drain battery V_{DD} while V_{GG} is removed.
4. The voltage V_{DD} is dropped across the *n*-channel resistance (say R_{DS}) giving rise to a drain current.

$$I_D = V_{DD} / R_{DS}$$

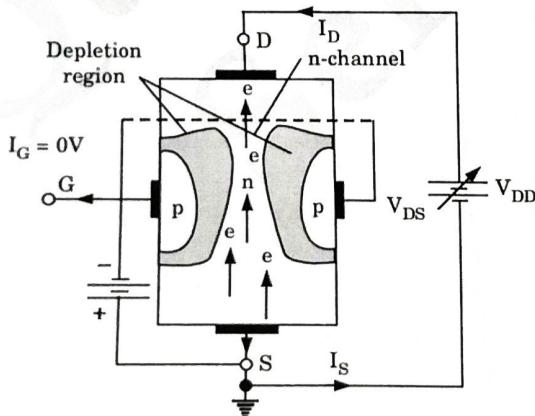


Fig. 2.15.2. Operation of FET.

5. Consider two points *A* and *B* in *n*-channel as shown in Fig. 2.15.3.

6. Let V_A and V_B be potential drop at these points. Certainly $V_A > V_B$, so due to progressive voltage drop, the reverse biasing effect is stronger near drain.

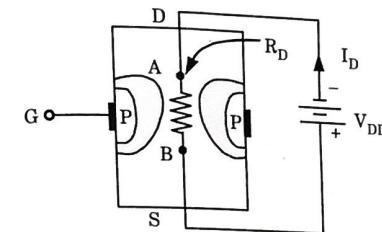


Fig. 2.15.3. Voltage drop across channel.

7. This explains why the depletion regions extend farther into the channel at point *A* than at point *B*.
8. This gate bias increases the depletion regions and thereby decreases the cross-section of *n*-channel due to which I_D decreases. Since negative gate voltage controls the drain current, FET is called a voltage controlled device.
- C. Static Characteristics of FET (*V-I*) :
1. Static means I_D versus V_{DS} for different values of V_{GS} .
2. Let us consider the characteristics for $V_{GS} = 0$, the curve is shown in Fig. 2.15.4.
3. When $V_{DS} = 0$, there is no attracting potential at the drain and hence drain current $I_D = 0$, although the channel between the gates is fully open as $V_{GS} = 0$.
4. As V_{DS} is increased, the electrons flow from source to drain through channel between depletion layers and the drain current I_D increases linearly up to a point *A* (knee point).

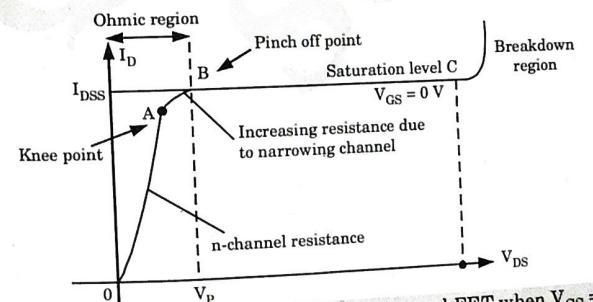


Fig. 2.15.4. Drain characteristics of *n*-channel FET when $V_{GS} = 0$.

5. With the increase of I_D , the ohmic resistance drop in the material of semiconductor bar. So as the voltage V_{DS} is progressively increased,

the drain current I_D , from point A, increases at reverse square law rate up to point B which is called pinch-off point. The corresponding voltage is called pinch-off voltage and is denoted by V_p .

6. As V_{DS} is further increased, the channel resistance also increases in such a way, that I_D remains constant up to point C. The region BC is known as saturation region or amplifier region.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

where I_{DSS} = Drain current when gate is shorted to source, and V_{GS} = Voltage between gate and source.

7. With continued increase of V_{DS} corresponding to point C (called avalanche breakdown voltage V_A), eventually breakdown across the gate junction takes place and current I_D shoots to a high value.

D. Transfer characteristics :

1. The transfer characteristics is a plot of drain current I_D , versus voltage between gate and source V_{GS} for a constant value of voltage between drain and source V_{DS} . This is shown in Fig. 2.15.5.
2. When $V_{GS} = 0$, $I_D = I_{DSS}$
and $I_D = 0$, $V_{GS} = V_p$
3. The transfer characteristic follows the equation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS}(\text{off})} \right)^2$$

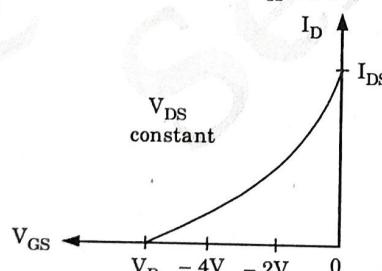


Fig. 2.15.5. Transfer characteristics.

- Que 2.16.** Discuss the various FET parameters with respect to common source configuration.

Answer

- i. **DC drain resistance R_{DS} :** This is the static or ohmic resistance of the channel.
It is given by :

$$R_{DS} = \left[\frac{V_{DS}}{I_D} \right]$$

- ii. **AC drain resistance :**

$$r_d = \left[\frac{\Delta V_{DS}}{\Delta I_D} \right] \quad V_{GS} \text{ held constant}$$

This is evaluated at $V_{GS} = 0$ i.e., when FET is operating in the pinch-off region.

- iii. **Transconductance :** The control that the gate voltage has over drain current is measured by forward transconductance g_{fs} and is similar to mutual conductance g_m . It is simply the slope of transfer characteristics.

$$g_{fs} = \left(\frac{\Delta I_D}{\Delta V_{GS}} \right) \quad V_{DS} \text{ held constant}$$

The unit of g_{fs} is siemens (mho).

- iv. **Amplification factor :** The amplification factor μ is defined as

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}} \right) \quad I_D \text{ held constant}$$

- Que 2.17.** Explain with the help of necessary diagrams, how FET can be used as (Voltage Variable Resistor) VVR.

Answer

1. In most of the linear applications, JFET is operated in constant current portion of its output characteristics i.e., in saturation region.
2. FET can also be used in the region before pinch-off where V_{DD} is small.
3. FET when used in region before pinch-off, it works as variable resistance device i.e., the channel resistance is controlled by the gate bias voltage (V_{GS}).
4. In such applications, the FET is referred as voltage variable resistor (VVR) or voltage dependent resistor (VDR).
5. The VVR can be used to vary the voltage gain of a multistage amplifier. This action is referred as automatic gain control (AGC).
6. If the signal is low then voltage gain of the stages can be increased and when becomes high, the gain can be reduced automatically. In this way, the general level of amplification is maintained fairly constant.

7. The circuit arrangement of AGC amplifier using the FET as voltage variable resistor is shown in Fig. 2.17.1.

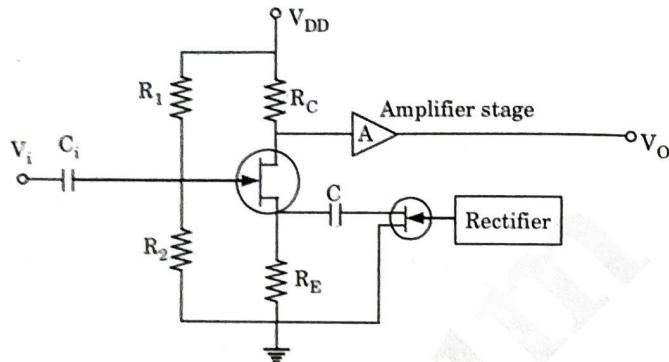


Fig. 2.17.1. FET as VVR.

8. The input signal V_i is amplified by amplifier.
9. It is then rectified and filtered to produce DC voltage proportional to output signal level. This voltage is applied to the gate of the FET so that the AC resistance between drain and source changes.
10. Capacitor 'C' isolates the transistor from FET so that the bias conditions of transistor are not affected.
11. Thus, when output increases, V_{GS} also increases and R_{DS} changes so that the gain of the transistor decreases. Thus automatically the gain is controlled.

Que 2.18. Show that the transconductance g_m of JFET is related to drain current I_{DS} by

$$g_m = \frac{2}{V_p} \sqrt{I_{DSS} I_{DS}}$$

Answer

1. As we know, the saturation drain current, I_{DS} is given by

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad \dots(2.18.1)$$

where V_p is pinch-off voltage and I_{DSS} is the value of I_{DS} when $V_{GS} = 0$.

2. Differentiating eq. (2.18.1) with respect to V_{GS} , we get

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2 \left(1 - \frac{V_{GS}}{V_p}\right) \left(-\frac{1}{V_p}\right)$$

3. We know that, $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, V_{DS} is constant

$$g_m = -\frac{2I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right) \quad \dots(2.18.2)$$

4. From eq. (2.18.1), we have

$$\left(1 - \frac{V_{GS}}{V_p}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

5. Substituting this value in eq. (2.18.2), we get

$$g_m = \frac{-2I_{DSS}}{V_p} \sqrt{\frac{I_{DS}}{I_{DSS}}} \\ g_m = \frac{-2}{V_p} \sqrt{\frac{(I_{DSS})^2 I_{DS}}{I_{DSS}}} = \frac{2}{|V_p|} \sqrt{I_{DSS} I_{DS}}$$

[$\because V_p$ may be positive or negative]

Que 2.19.

- i. Draw the schematic diagram of self-biasing JFFT amplifier.
- ii. Explain the CMOS inverter circuit working operation.

AKTU 2015-16(Sem-II), Marks 10

OR

Draw the CE n-p-n BJT characteristics. Also explain the self bias configuration in DC bias configuration.

AKTU 2016-17(Sem-II), Marks 10.5

Answer

- A. CE characteristics : Refer Q. 2.7, Page 2-10J, Unit-2.

B. Self bias configuration :

1. The self bias configuration eliminates the need of two DC supplies i.e., only drain supply is used and no gate supply is connected.
2. Fig. 2.19.1 shows the arrangement, a resistor R_S is connected in the source leg of the configuration. This is known as bias resistor.
3. The DC component of drain current I_D flowing through R_S makes a voltage drop across resistor R_S .
4. The capacitor C_S bypasses the AC component of drain current.
5. The addition of R_G in circuit does not upset the DC bias, but avoid the short-circuiting of the AC input voltage. Otherwise, the leakage current would build up static charge at the gate which could change the bias.
6. R_S also help to prevent any variation in FET drain current.

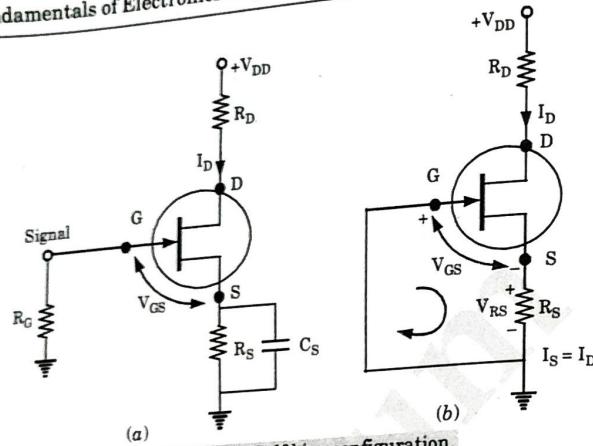


Fig. 2.19.1. Self bias configuration.

7. Let there be an increase in the drain current. This will increase the voltage drop across resistor R_S and this results in decrease of channel width. So, the drain current is reduced.
8. For DC analysis, the capacitors can be replaced by open circuit and the resistor R_G replaced by short-circuit equivalent. Since $I_G = 0$ A. The equivalent circuit is shown in Fig. 2.19.1(b).
9. For the indicated loop, we have

$$-V_{GS} - V_{RS} = 0$$

$$V_{GS} = -V_{RS}$$

$$V_{GS} = -I_D R_S$$

10. The gate is kept at this much negative potential with respect to ground.

but $I_O = I_S$

and $V_{DS} = V_{DD} - I_D(R_S + R_D)$

In addition $V_S = I_D R_S$, $V_G = 0$ V

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

C. CMOS Inverter :

1. An inverter is a logic element that "inverts" the applied signal. That is, if the logic level of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level 5 V, and vice versa.
2. In Fig. 2.19.2, both gates are connected to the applied signal and both drain to the output V_O .
3. The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS} , whereas the source of the n-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output.

4. With 5 V at V_i (with respect to ground), $V_{GS1} = V_i$, and Q_1 is ON, resulting in a relatively low resistance between drain and source as shown in Fig. 2.19.2.
5. Since V_i and V_{SS} are at 5 V, $V_{GS2} = 0$ V, which is less than the required V_T for the device, resulting in an OFF state.
6. The resulting resistance level between drain and source is quite high for Q_2 , as shown in Fig. 2.19.2.
7. A simple application of the voltage-divider rule will reveal that V_O is very close to 0 V, or the 0-state, establishing the desired inversion process.
8. For an applied voltage V_i of 0 V (0-state), $V_{GS1} = 0$ V, and Q_1 will be OFF with $V_{SS2} = -5$ V, turning on the p-channel MOSFET.
9. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_O = V_{SS} = 5$ V (the 1-state).
10. Since the drain current that flows for either case is limited by the OFF transistor to the leakage value, the power dissipated by the device in either state is very low.

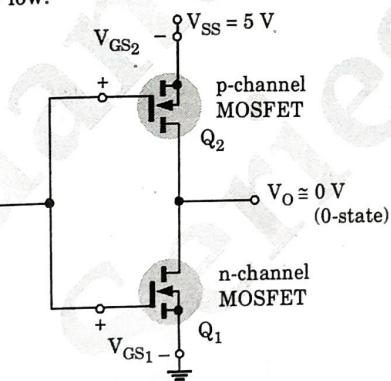


Fig. 2.19.2. CMOS inverter.

PART-4

MOSFET (MOS) (Depletion and Enhancement) Type, Transfer Characteristic.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 2.20. Draw the circuit of *n*-channel depletion type MOSFET and explain its operation. Also draw its drain and transfer characteristics.

AKTU 2017-18(Sem-II), Marks 07

OR

Describe the construction and basic connection of depletion MOSFET.

AKTU 2016-17(Sem-I), Marks 05

OR

Explain construction and working of depletion MOSFET.

AKTU 2017-18(Sem-I), Marks 3.5

OR

Draw the structure of depletion type *N*-MOSFET. Explain its operation with characteristic graph.

AKTU 2021-22(Sem-I), Marks 10

Answer

- For the depletion mode, the gate is maintained at negative potential while the drain is maintained at positive potential.
- When voltage between gate and source is zero ($V_{GS} = 0$), as shown in the Fig. 2.20.1., significant current flows for a given V_{DS} , like a FET.

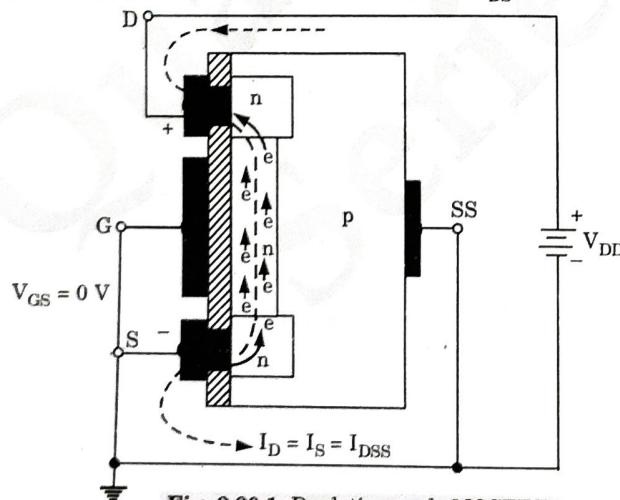


Fig. 2.20.1. Depletion mode MOSFET.

- Let negative potential is applied at the gate. In such case positive charges are induced in *n*-channel through SiO_2 as shown in Fig. 2.20.2.
- This mechanism depletes the channel from majority carriers i.e., electrons, and hence conductivity decreases.

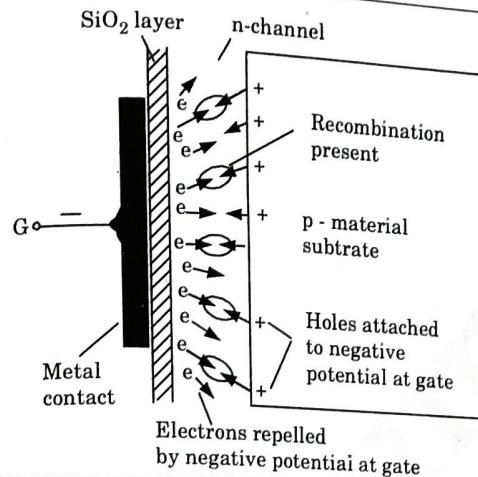


Fig. 2.20.2. Reduction in free carriers in a channel due to a negative potential at the gate terminal.

- Here it should be remembered that because of the voltage drop due to drain current I_D , the channel region near the drain end is more depleted than the region near the source.
- Here too much negative gate voltage can pinch-off the channel. Hence a MOSFET behaves like a FET.

Characteristics curves of MOSFET :

- Fig. 2.20.3 shows the drain characteristics and transfer characteristics for *n*-channel MOSFET respectively.

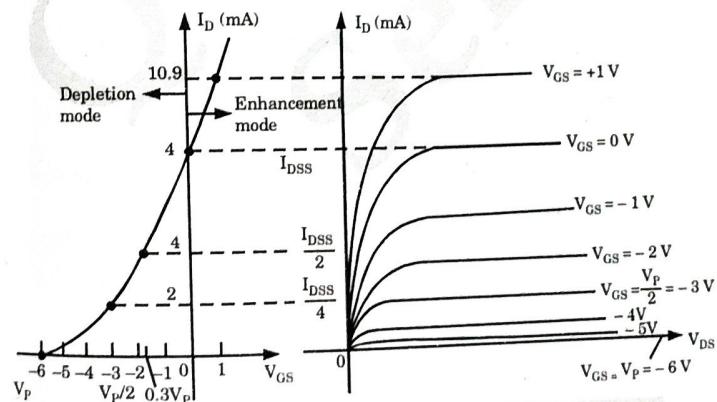


Fig. 2.20.3. Drain and transfer characteristics for an *n*-channel depletion-type MOSFET.

2. The two modes, namely depletion mode and enhancement mode correspond to negative and positive gate voltages respectively.
3. It is obvious, that for $V_{GS} = 0$, the drain current I_D is not zero, but it has appreciable value.
4. The gate voltage at which I_D reduces at a recommended drain voltage V_{DS} is called gate source cut-off voltage. This is denoted by $V_{GS(\text{OFF})}$ and corresponds to pinch-off voltage V_p .

Que 2.21. Draw and explain the construction and working of p-channel depletion type MOSFET. Also draw the characteristics of p-channel depletion type MOSFET.

AKTU 2016-17(Sem-II), Marks 07

OR

Describe the construction and working of p-channel depletion MOSFET, with characteristic graph. Also justify that it is a voltage controlled device.

AKTU 2021-22(Sem-II), Marks 10

Answer

A. Construction and working of p-channel depletion type MOSFET:

1. Fig. 2.21.1 shows a p-channel depletion type MOSFET.
2. When zero voltage is applied to the gate, a p-channel or an inversion layer of holes exist under the oxide.
3. Since the p-channel interconnects the p^+ -type source and p^+ -type drain, a drain-to-source current flows even though the gate voltage is equal to zero.
4. The depletion states that the channel exists even at zero gate voltage.
5. If a positive gate voltage is applied between gate to source of the p-channel depletion type MOSFET, the device will be turned OFF.

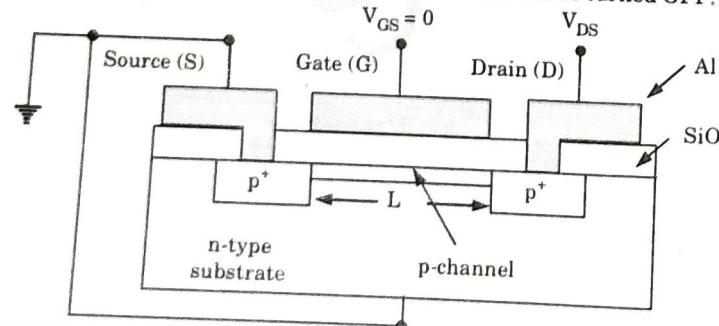


Fig. 2.21.1. Cross-section of a p-channel depletion MOSFET with $V_{GS} = 0$.

6. A p-channel depletion type MOSFET with positive gate voltage is shown in Fig. 2.21.2.

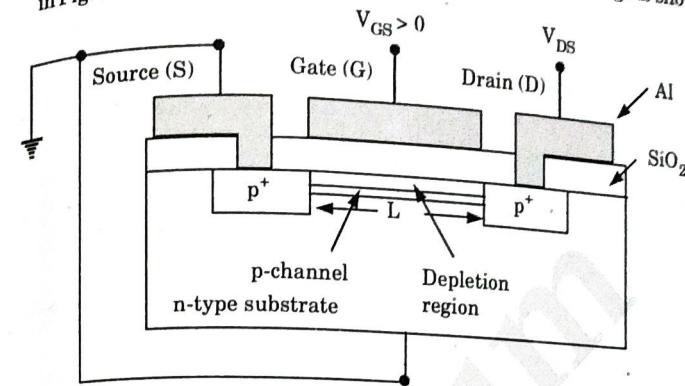


Fig. 2.21.2. Cross-section of a p-channel depletion type MOSFET with $V_{GS} > 0$.

7. Due to positive gate voltage, a space charge region is induced under the oxide. Consequently, the thickness of the p-channel region will be reduced.
8. Since the channel thickness is reduced, the channel conductance is also reduced and in turn drain current reduces.
9. If positive gate voltage is equal to the threshold voltage, the induced space charge region extends completely through the p-channel region and drain current becomes zero.
10. When a negative gate voltage is applied between gate to source, this negative gate voltage creates a hole accumulation layer as shown in Fig. 2.21.3.

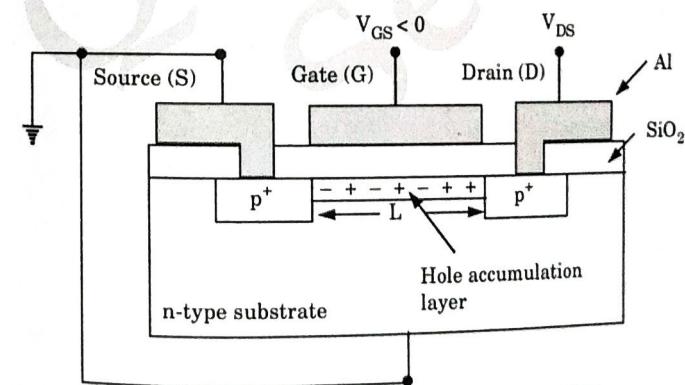


Fig. 2.21.3. Cross-section of a p-channel depletion MOSFET with $V_{GS} < 0$.

11. Due to accumulation of holes in the *p*-type channel, drain current increases.
12. The drain and transfer characteristics are shown in Fig. 2.21.4.

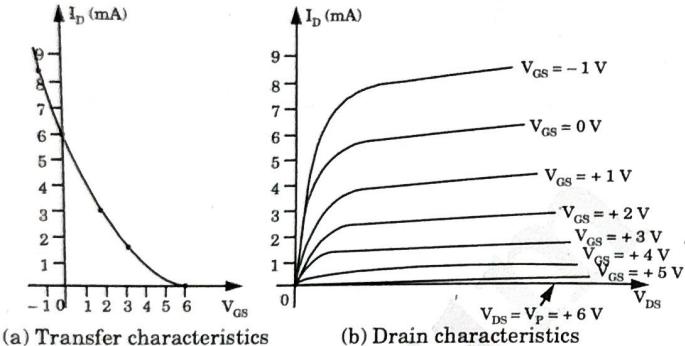


Fig. 2.21.4.

B. Reason :

1. It is called as a voltage controlled device because voltage applied at the gate terminal decides the conductivity of the MOSFET.
2. It is a special type of transistor which works on the principle of field effect.
3. This means field applied at the gate terminal creates voltage which decide the output current flowing between source and drain.
4. By varying the voltage we can control the output current of the MOSFET. That's why MOSFET is called as voltage controlled device.

Que 2.22. Describe the working operation of enhancement mode and depletion mode MOSFET. Also derive an expression for g_m of JFET configuration.

AKTU 2015-16(Sem-II), Marks 7.5

OR

Explain the working of enhancement type MOSFET along with their transfer characteristics.

AKTU 2021-22(Sem-II), Marks 10

Answer

A. Depletion mode MOSFET : Refer Q. 2.20, Page 2-27J, Unit-2.

B. Expression for g_m : Refer Q. 2.18, Page 2-23J, Unit-2.

C. Enhancement MOSFET :

1. Fig. 2.22.1 shows the cross-sectional view of *n*-channel enhancement MOSFET.
2. It consists of a lightly doped *p*-type substrate into which two heavily doped *n*⁺-regions are diffused. These *n*⁺-regions act as source and drain respectively.

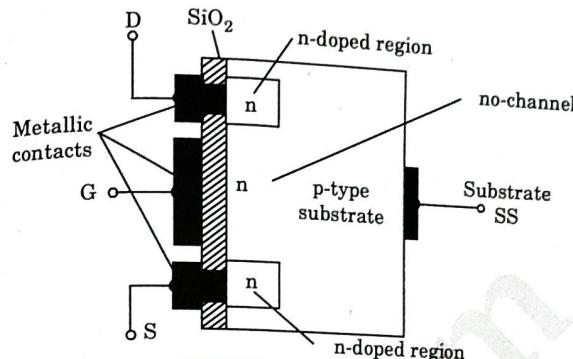


Fig. 2.22.1. Enhancement MOSFET.

3. A thin layer of insulating SiO_2 is grown over the entire surface and holes are cut into the oxide layer through which metal contacts are to be made for source and drain terminals.
4. On SiO_2 layer, a conducting layer of aluminium overlaid, covering entire channel length from source to drain, constitute the gate.

Working of Enhancement MOSFET :

1. The channel, the insulating dielectric SiO_2 and metal layer of gate forms a parallel plate capacitor.
2. When a positive potential is applied at the gate with respect to substrate, negative charges are induced on semiconductor side.
3. These negative charges, induced on *p*-type substrate consist of electrons which forms an inversion layer as shown in Fig. 2.22.2.
4. The inversion layer forms an effective *n*-type channel.
5. When the positive potential at the gate is increased, the magnitude of the induced negative charges in semiconductor increases.
6. Thus, the conductivity of induced *n*-channel increases and results in increased drain current.
7. For a constant drain voltage, the drain current increases as the positive drain voltage increases i.e., the drain current has been enhanced by the application of positive gate voltage. Such MOSFET is termed as an enhancement MOSFET.

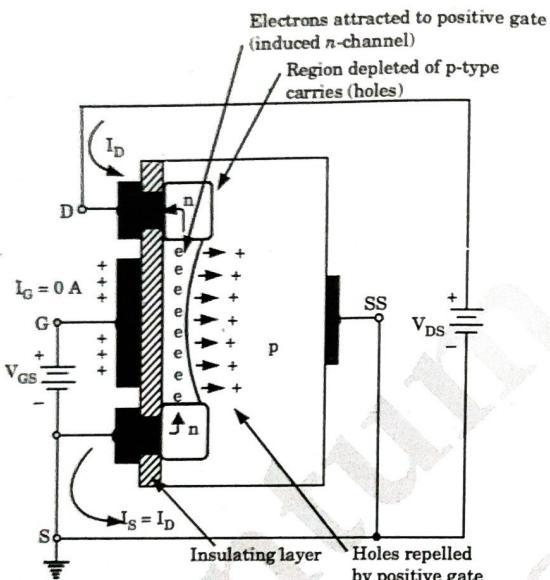


Fig. 2.22.2. Channel formation in the n-channel enhancement type MOSFET.

Characteristics curves of enhancement MOSFET :

- Fig. 2.22.3 shows the static drain and transfer characteristics of n-channel enhancement MOSFET.
- From Fig. 2.22.3, as V_{GS} is made positive, the drain current first increases slowly and then at relatively fast rate with increase of V_{GS} .

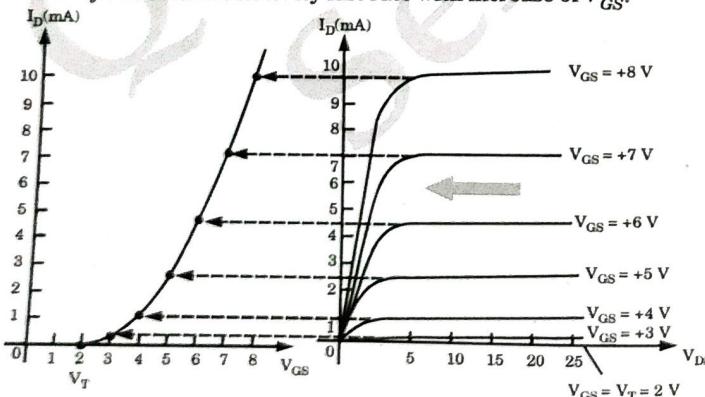


Fig. 2.22.3. Drain and transfer characteristics for an n-channel enhancement-type MOSFET.

- The threshold voltage is defined as the gate voltage at which channel is induced to produce the flow of current I_D of prescribed value and is denoted by V_T . Such type of FET is very useful in switching applications, since no gate voltage is required to hold it off.

Que 2.23. Explain construction, working and characteristics of p-channel enhancement MOSFET.

AKTU 2015-16(Sem-I), Marks 05

Answer

A Construction :

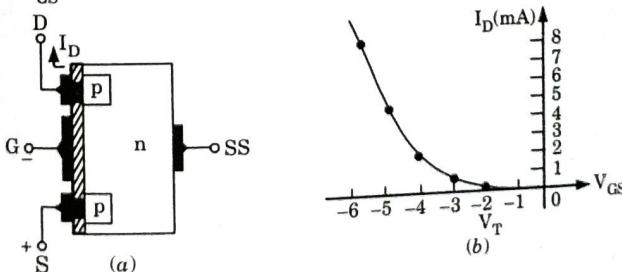
- The construction of a p-channel enhancement type MOSFET is exactly the reverse of that n-channel enhancement type MOSFET. It is shown in Fig. 2.23.1(a).
- There is an n-type substrate and p-doped regions under the drain and source connections.
- The terminal remains as identified, but all the polarities and the current directions are reversed.

B Operation :

- When $V_{SG} < |V_{tp}|$: There is no channel and transistor operates in cut-off mode i.e., $i_D = 0$.
- When $V_{DG} > |V_{tp}|$ or $V_{SD} < |V_{ov}|$: The continuous channel is created and transistor operates in triode region.
- When $V_{DG} \leq |V_{tp}|$ or $V_{SD} \geq |V_{ov}|$: The channel is pinched-off and the transistor operates in saturation region.

C Characteristics :

- The drain characteristics will appear as shown in Fig 2.23.1(b), with increasing levels of current resulting from increasingly negative values of V_{GS} .



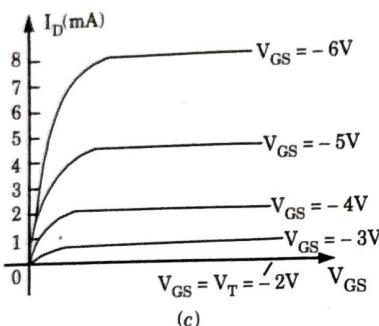


Fig. 2.23.1. p-channel enhancement-type MOSFET.

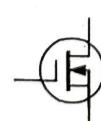
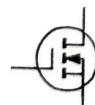
2. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of n-channel enhancement MOSFET.
3. The transfer curve is shown in Fig. 2.23.1(c), with I_D increasing with increasingly negative values of V_{GS} beyond V_T .

Que 2.24. Give the basic difference between an enhancement and depletion type MOSFET. Discuss the construction of a n-channel depletion type MOSFET. Also draw its transfer and drain characteristics.

AKTU 2020-21(Sem-I), Marks 10

Answer**A. Difference between enhancement and depletion type MOSFET:**

S. No.	E-MOSFET	D-MOSFET
1.	Operates only in enhancement mode.	Operates in both depletion mode and enhancement mode.
2.	There is no physical channel from source to drain. We have to enhance it by applying V_{GS} .	The channel is already formed between source and drain.
3.	Commonly used bias circuits : Gate bias, Voltage divider bias, Drain-feedback bias.	Commonly used bias circuits : Gate bias, Self bias, Voltage-divider bias, Zero bias
4.	Schematic symbol of E-MOSFET	Schematic symbol of D-MOSFET



B. n-channel depletion type MOSFET : Refer Q. 2.20, Page 2-27J, Unit-2.

Que 2.25. Determine Z_i , Z_o , V_o for the network of Fig. 2.25.1 if $V_i = 20 \text{ mV}$.

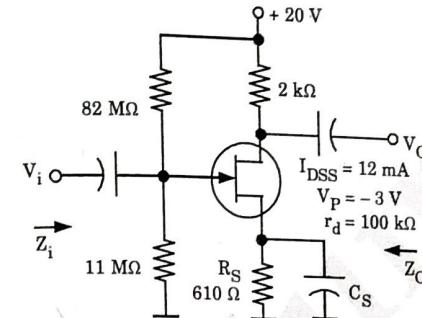


Fig. 2.25.1.

Answer

1. Converting Fig. 2.25.1 to Fig. 2.25.2 as shown below :

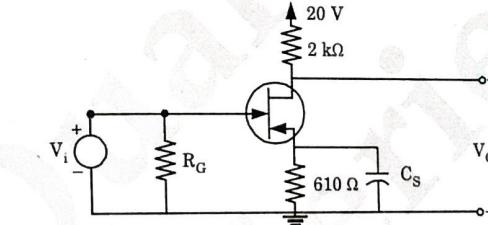


Fig. 2.25.2.

where,

$$R_g = 82 \text{ M}\Omega \parallel 11 \text{ M}\Omega$$

$$2. Z_i = R_g = 82 \text{ M}\Omega \parallel 11 \text{ M}\Omega = \frac{82 \times 11 \times 10^6}{82 + 11} = 9.698 \text{ M}\Omega$$

$$3. Z_o = r_d \parallel R_D \\ = \frac{100 \times 10^3 \times 2 \times 10^3}{(100 + 2) \times 10^3} = 1.96 \text{ k}\Omega$$

$$4. \text{ For } V_{GS}, \quad \frac{20 \times 11}{82 + 11} = I_D \times 610$$

$$I_D = 3.880 \text{ mA}$$

$$5. I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

- $$3.88 \times 10^{-3} = 12 \times 10^{-3} \left[1 - \frac{V_{GS}}{-3} \right]^2$$
- $$\frac{3.88 \times 10^{-3}}{12 \times 10^{-3}} = \left[1 + \frac{V_{GS}}{3} \right]^2$$
- $$V_{GS} = -1.294$$
6. We know that $g_m = \frac{-2 I_{DSS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right]$
- $$g_m = \frac{-2 \times 12 \times 10^{-3}}{-3} \left(1 - \frac{(-1.294)}{(-3)} \right) = 4.55 \text{ mS}$$
7. $V_{GS} = V_i = 20 \text{ V}$
8. We know, $V_O = -g_m V_{GS} (r_d || R_D)$
- $$V_O = -4.55 \times 10^{-3} \left[\frac{100 \times 2 \times 10^3}{100 + 2} \right] = -8.92 \text{ V}$$

Que 2.26. Determine Z_i , Z_o and A_v for the network of Fig. 2.26.1, if $I_{DSS} = 12 \text{ mA}$, $V_p = -6 \text{ V}$, and $Y_{OS} = 40 \text{ micro siemens}$.

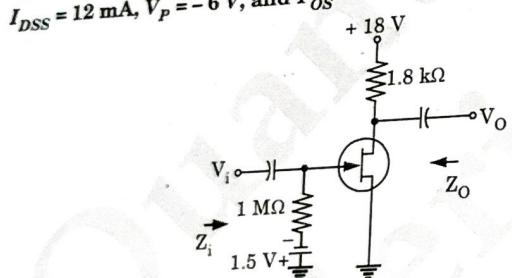


Fig. 2.26.1.
AKTU 2015-16(Sem-I), Marks 05

Answer

Given : $I_{DSS} = 12 \text{ mA}$, $V_p = -6 \text{ V}$, $Y_{OS} = 40 \mu\text{S}$, $R_G = 1 \text{ M}\Omega$, $R_D = 1.8 \text{ k}\Omega$, $Z_i = R_G = 1 \text{ M}\Omega$

To Find : Z_i , Z_o , A_v

- We have, $Z_o = R_D || r_d$
- $r_d = \frac{1}{Y_{OS}} = \frac{1}{40 \mu\text{S}} = 25 \text{ k}\Omega$
- $Z_o = (1.8 \text{ k}\Omega) || (25 \text{ k}\Omega) = 1.68 \text{ k}\Omega$

- $$g_m = g_{mO} \left(1 - \frac{V_{GSQ}}{V_p} \right)$$
4. $g_{mO} = \frac{2 I_{DSS}}{|V_p|} = \frac{2 \times 12 \times 10^{-3}}{6} = 4 \text{ mS}$
5. $g_m = 4 \times 10^{-3} \left(1 - \frac{(-1.5)}{(-6)} \right) = 3 \text{ mS}$
6. $A_V = -g_{mO} (R_D || r_d)$
7. $A_V = -(3 \text{ mS}) (1.8 \text{ k}\Omega || 25 \text{ k}\Omega)$
8. $A_V = -(3 \text{ mS}) \times (1.68 \text{ k}\Omega)$
- $A_V = -5.04$

Que 2.27. For the voltage divider network shown in Fig. 2.27.1. Given $I_{DSS} = 10 \text{ mA}$, $V_p = -3.5 \text{ V}$, determine V_G , I_{DQ} , V_{GSQ} , V_D , V_S and V_{DSQ} .

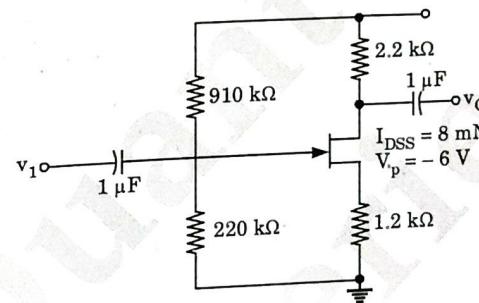


Fig. 2.27.1.

AKTU 2017-18(Sem-II), Marks 07

Answer

Given : $I_{DSS} = 10 \text{ mA}$, $V_p = -3.5 \text{ V}$

To Find : V_G , I_{DQ} , V_{GSQ} , V_D , V_S , V_{DSQ}

- $V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{220 \text{ k}\Omega \times 16 \text{ V}}{910 \text{ k}\Omega + 220 \text{ k}\Omega}$
 $= 3.11 \text{ V}$
 $V_{GS} = V_G - I_D R_S = 3.11 - 1.2 I_D$

3. As, $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$

4. On solving, $I_D = I_{DQ} = 28.2 \text{ mA}$

5. $V_{GSQ} = V_{GS} = 3.11 - 1.2 \times 28.2 \times 10^{-3} \text{ A}$
 $= -3.07 \text{ V}$

6. $V_D = V_{DD} - I_D R_D = 16 - 28.2 \text{ mA} \times 1.2 \text{ k}\Omega$
 $= -17.84 \text{ V}$

7. $V_S = I_D R_S = 28.2 \text{ mA} \times 1.2 \text{ k}\Omega = 33.84 \text{ V}$

8. $V_{DS} = V_D - V_S = -17.84 - 33.84 \text{ V} = -51.68 \text{ V}$
 $V_{DG} = V_D - V_G = -17.84 - 3.11 = -20.95 \text{ V}$

Note : '-' indicates the direction will be opposite.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Explain various current components in *n-p-n* transistor with help of suitable diagram.
Ans: Refer Q. 2.3.

Q. 2. Explain the working of a common base circuit with its circuit diagram.
Ans: Refer Q. 2.6.

Q. 3. Draw and explain the input and output characteristics of common emitter configuration.
Ans: Refer Q. 2.7.

Q. 4. An *n-p-n* transistor with $\beta = 98$ is operated in the CB configuration, if the emitter current is 2 mA and reverse saturation current is $12 \mu\text{A}$. What are the base and collector current?
Ans: Refer Q. 2.10.

Q. 5. Explain the transconductance curve of a JFET.
Ans: Refer Q. 2.15.

Q. 6. Describe the construction and basic connection of depletion MOSFET.
Ans: Refer Q. 2.20.

Q. 7. Explain the working of enhancement type MOSFET along with their transfer characteristics.
Ans: Refer Q. 2.22.



3

UNIT

Operational Amplifiers

CONTENTS

Part-1 : Operational Amplifier : 3-2J to 3-4J
Introduction, Op-Amp Basic

Part-2 : Practical Op-Amp Circuits 3-4J to 3-17J
(Inverting Amplifier,
Non-inverting Amplifier,
Unit Follower, Summing Amplifier,
Integrator, Differentiator)

Part-3 : Differential and 3-17J to 3-24J
Common-Mode
Operation, Comparators

3-2 J (Sem-1 & 2)

Operational Amplifiers

PART-1

Operational Amplifier : Introduction, Op-Amp Basic.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 3.1. Define Op-Amp with the help of block diagram. Also draw its equivalent circuit.

Answer

1. Op-Amp is designed to perform various mathematical operations.
2. The Fig. 3.1.1 represents the block diagram approach of an operational amplifier.

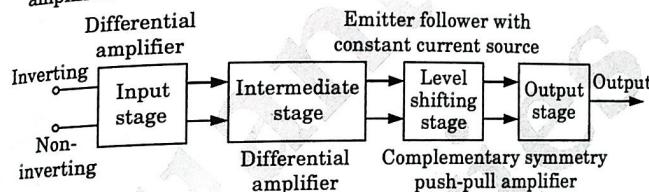


Fig. 3.1.1. Block diagram of Op-Amp.

3. It consists of two differential amplifiers followed by level shifter and an output stage.
4. The input stage is a dual input differential amplifier which provides most of the voltage gain to operational amplifier. It also provides high resistance to operational amplifier.
5. The intermediate stage is also dual input. This is driven by the output of first stage and is used to provide some additional gain. The DC level at the output of intermediate stage is well above the ground level.
6. The level shifter is an emitter follower using constant current source. The function of level shifter is to shift DC level at the output of intermediate stage downwards to zero volt with respect to ground.
7. The output stage is generally push-pull amplifier. Its function is to increase large output voltage swing capability and to provide low output resistance.
8. Fig. 3.1.2 shows the equivalent circuit of operational amplifier.
9. V_{ud} is the difference of two input voltages i.e., $(V_2 - V_1)$. R_i is the input resistance.

3-1 J (Sem-1 & 2)

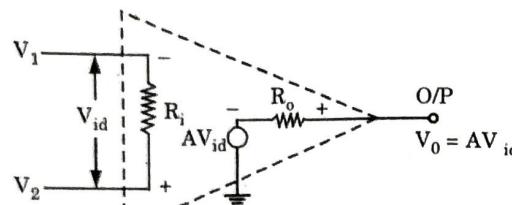


Fig. 3.1.2. Equivalent circuit.

10. R_o is the output resistance which is Thevenin's equivalent.
11. The voltage source AV_{id} is an equivalent Thevenin's voltage source.
12. The output voltage is directly proportional to the difference between the two input voltages.
13. It has open-loop voltage gain of 1,00,000, input impedance of $2 M\Omega$, and output impedance of 75Ω .
14. Fig. 3.1.3 shows popular package style and the pin diagram.

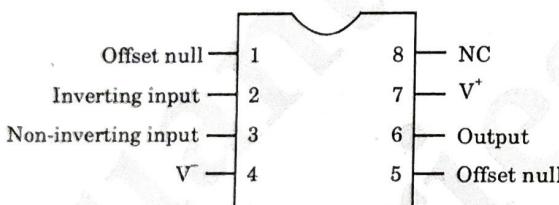


Fig. 3.1.3. Dual in line package.

Que 3.2. Define Op-Amp with the help of block diagram. Also describe the equivalent circuit along with its ideal and practical characteristics.

OR

Define Op-Amp with the help of block diagram. Also draw its equivalent circuit. List the ideal characteristics of Op-Amp.

AKTU 2017-18(Sem-II), Marks 07

OR

Draw the block diagram and equivalent circuit of an Op-Amp. Explain ideal characteristics of an Op-Amp.

AKTU 2015-16(Sem-II), Marks 7.5

OR

What is an operational amplifier? Draw its block diagram. Write the characteristics of an ideal operational amplifier.

AKTU 2020-21(Sem-I), Marks 05

Answer

A. Op-Amp : Refer Q. 3.1, Page 3-2J, Unit-3.

B. Characteristics of Op-Amp in ideal and practical cases :

S. No.	Characteristic	Ideal	Practical
1.	CMRR	∞	10^6 or 120 dB
2.	Slew rate	∞	$80 V/\mu sec$
3.	Input resistance	∞	$10^6 \Omega$
4.	Output resistance	0	100Ω
5.	Voltage gain A_V	∞	10^6
6.	Bandwidth	∞	10^6 Hz
7.	Offset voltage	0	Negligible
8.	Offset current	0	Negligible

PART-2

Practical Op-Amp Circuits (Inverting Amplifier, Non-inverting Amplifier, Unity Gain Amplifier, Summing Amplifier, Integrator, Differentiator).

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 3.3. Draw the circuit of an Op-Amp as voltage follower and find an expression for its voltage gain.

OR

Draw and derive relationship for Op-Amp as closed loop non-inverting amplifier circuit. AKTU 2016-17(Sem-I), Marks 05

OR

Derive an expression for voltage gain of inverting and non-inverting ideal operational amplifier configurations.

AKTU 2017-18(Sem-I), Marks 07

OR

Write down the characteristics of ideal OP-AMP. Derive the expression for gain of OP-AMP as non-inverting amplifier.

AKTU 2021-22(Sem-I), Marks 10

OR

Briefly explain op-amp as non-inverting amplifier.

AKTU 2021-22(Sem-II), Marks 03

Answer

A. Characteristics of ideal op-amp : Refer Q. 3.2, Page 3-3J, Unit-3.

B. Inverting Op-Amp :

- Fig. 3.3.1 shows the basic inverting amplifier with input resistance R_1 and feedback resistance R_f .

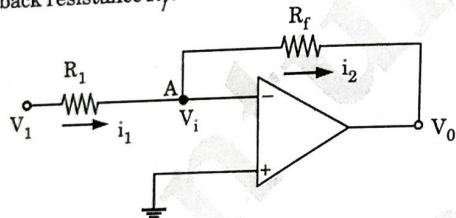


Fig. 3.3.1. Inverting amplifier.

- The current i_1 flowing through R_1 is given by,

$$i_1 = \frac{V_i - V_i}{R_1} = \frac{V_i}{R_1} \quad (\because V_i = 0 \text{ due to virtual ground})$$

and

$$i_2 = \frac{V_i - V_o}{R_f} = \frac{-V_o}{R_f}$$

- At point A,

$$\frac{V_i}{R_1} = -\frac{V_o}{R_f}$$

$$A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

C. Non-inverting amplifier :

- The circuit for non-inverting amplifier is shown in Fig. 3.3.2.

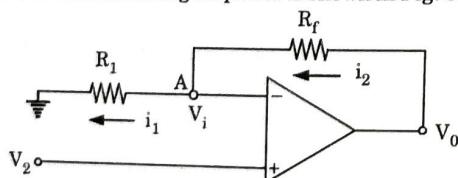


Fig. 3.3.2. Non-inverting amplifier.

- The currents i_1 and i_2 are given as :

$$i_1 = \frac{V_2}{R_1} \text{ and } i_2 = \frac{V_o - V_2}{R_f} \quad (\because V_i = V_2 \text{ due to virtual ground})$$

- Applying KCL at point A,

$$(-i_1) + i_2 = 0 - \frac{V_2}{R_1} + \frac{V_o - V_2}{R_f} = 0$$

$$\frac{V_o}{R_f} = \frac{V_2}{R_1} + \frac{V_2}{R_f} = V_2 \left(\frac{1}{R_1} + \frac{1}{R_f} \right)$$

$$\frac{V_o}{V_2} = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1} \right)$$

$$A_v = \left(1 + \frac{R_f}{R_1} \right)$$

D. Unity gain Op-Amp (Voltage Follower) :

- Fig. 3.3.3 represents unity gain Op-Amp where $R_1 \rightarrow \infty$.

$$A_v = 1$$

$$\frac{V_o}{V_{in}} = 1$$

$$V_o = V_{in}$$

- The voltage gain is unity and the output voltage follows the input voltage.

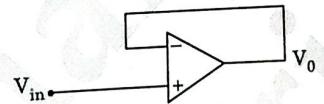


Fig. 3.3.3.

Que 3.4. Explain summing amplifier using Op-Amp.

AKTU 2015-16(Sem-II), Marks 03

OR

Briefly explain inverting summer.

AKTU 2021-22(Sem-II), Marks 03

Answer

- Fig. 3.4.1 shows the three input summer circuit. This circuit provides a means of algebraically summing three input voltages, each multiplied by a constant gain factor.

- At point A (virtual ground), the different currents are given as :

$$i_1 = \frac{V_1}{R_1}, i_2 = \frac{V_2}{R_2}, i_3 = \frac{V_3}{R_3} \text{ and } i = -\frac{V_o}{R_f}$$

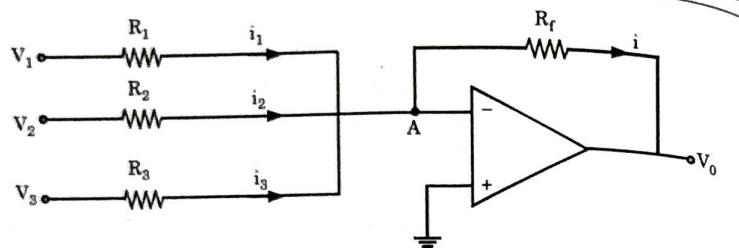


Fig. 3.4.1. Summer circuit.

3. Applying KCL at point A, we get,

$$i_1 + i_2 + i_3 - i = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_0}{R_f} = 0$$

$$V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

4. If $R_1 = R_2 = R_3 = R$, then

$$V_0 = -\frac{R_f}{R} [V_1 + V_2 + V_3]$$

5. Thus the output voltage is proportional to the algebraic sum of three input voltages.

Again, if

$$R_f = R,$$

$$V_0 = -[V_1 + V_2 + V_3]$$

- Que 3.5.** Calculate the output voltage for the circuit of Fig. 3.5.1 with inputs of $V_1 = 40 \text{ mV rms}$ and $V_2 = 20 \text{ mV rms}$.

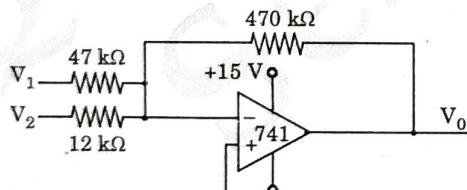


Fig. 3.5.1.

AKTU 2016-17(Sem-II), Marks 07

Answer

Given : $V_1 = 40 \text{ mV rms}$, $V_2 = 20 \text{ mV rms}$, $R_1 = 47 \text{ k}\Omega$, $R_2 = 12 \text{ k}\Omega$, $R_f = 470 \text{ k}\Omega$.

To Find : V_0 .

$$V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right] = -\left[\frac{470}{47} \times 40 + \frac{470}{12} \times 20 \right] \\ = -[400 + 783.3] = -1183.33 \text{ mV rms} \\ = -1.18 \text{ V rms}$$

- Que 3.6.** Determine the output of the following circuit.
Given $V_1 = V_2 = 0.15 \text{ V}$

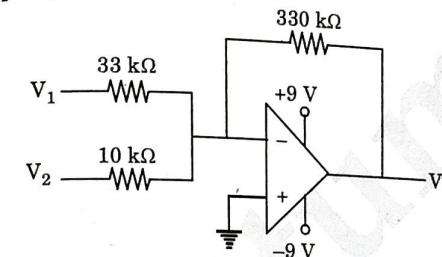


Fig. 3.6.1.

AKTU 2021-22(Sem-I), Marks 05

Answer

Given : $V_1 = 0.15 \text{ V}$, $V_2 = 0.15 \text{ V}$, $R_1 = 33 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_f = 330 \text{ k}\Omega$

To Find : V_0 .

$$V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right] = -\left[\frac{330}{33} + \frac{330}{10} \right] \times 0.15 \\ = -[10 + 33] \times 0.15 = -43 \times 0.15 \\ = -6.45 \text{ V}$$

- Que 3.7.** Determine the output for the circuit :

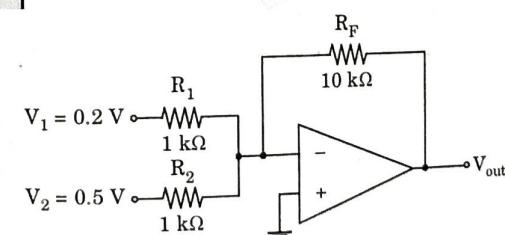


Fig. 3.7.1.

AKTU 2020-21(Sem-I), Marks 05

Answer

The given circuit is a summing amplifier and the output voltage of summing amplifier is,

$$\begin{aligned} V_o &= - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right] \\ &= - \left[\frac{10}{1} \times 0.2 + \frac{10}{1} \times 0.5 \right] \\ &= -(2+5) = -7 \text{ V} \end{aligned}$$

Que 3.8. Determine the output for the circuits :

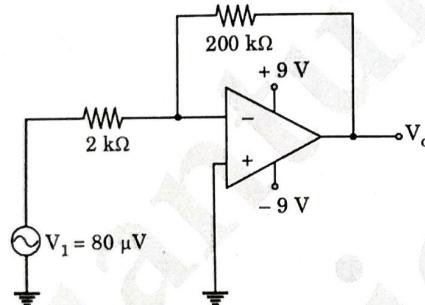


Fig. 3.8.1.

AKTU 2020-21(Sem-I), Marks 05

Answer

The given circuit is inverting amplifier. So the output voltage of the inverting amplifier is,

$$\begin{aligned} V_o &= - \frac{R_f}{R_1} V_{in} \\ &= - \frac{200}{2} \times 80 \times 10^{-6} \text{ V} \\ &= -8 \text{ mV} \end{aligned}$$

Que 3.9. Explain the concept of virtual ground in OP-AMP. Determine output voltage for given network.

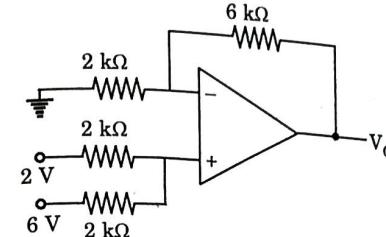


Fig. 3.9.1.

AKTU 2021-22(Sem-II), Marks 10

Answer

- A. **Concept of virtual ground in OP-AMP:** In op-amps the term virtual ground means that the voltage at that particular node is almost equal to ground voltage (0 V). It is not physically connected to ground. This concept will make a lot of calculations very simple.

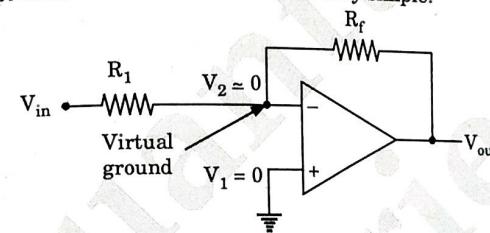


Fig. 3.9.2.

In above inverting amplifier V_1 is connected to ground so $V_1 = 0$. Thus V_2 also will be at ground potential.

$$\text{As gain} = \frac{V_o}{V_{in}}$$

$$\text{As gain is infinite, } V_{in} = 0 \\ V_{in} = V_2 - V_1$$

B. Numerical :

The given circuit is shown in Fig. 3.9.3.

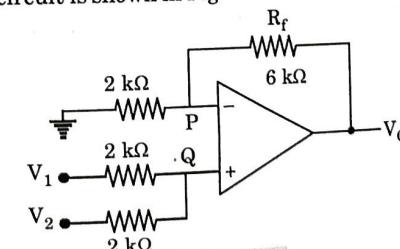


Fig. 3.9.3.

According to virtual ground concept

$$\text{If } V_+ = V_- \\ V_+ = V_Q = V_P \\ \therefore V_Q = V_P$$

At point Q

$$\frac{V_1 - V_Q}{R} + \frac{V_2 - V_Q}{R} = 0$$

$$V_1 - V_Q + V_2 - V_Q = 0$$

$$V_Q = \frac{V_1 + V_2}{2}$$

$$\therefore V_Q = \frac{2+6}{2} = 4 \text{ V}$$

At point P

$$\frac{0 - V_P}{2} + \frac{V_O - V_P}{6} = 0$$

So,

$$V_O = \left[1 + \frac{6}{2} \right] V_P$$

$$V_O = 4 \times 4 = 16 \text{ V}$$

Que 3.10. Explain integrator circuit using Op-Amp.

AKTU 2015-16(Sem-II), Marks 04

OR

Explain how Op-Amp can be used as

- i. Integrator
- ii. Inverting summer and
- iii. Voltage follower.

AKTU 2017-18(Sem-I), Marks 07

OR

Explain the operation of Op-Amp as integrator.

AKTU 2017-18(Sem-II), Marks 3.5

OR

Draw the circuit diagram of an integrator using Op-Amp and explain its working.

AKTU 2016-17(Sem-I), Marks 05

OR

Write a short note on differentiator.

OR

With help of the circuit diagram, explain the working of op-amp as differentiator.

AKTU 2020-21(Sem-I), Marks 05

OR

Draw and explain the working of Integrator and Differentiator using OP-AMP.

AKTU 2021-22(Sem-I), Marks 05

Answer

A. Integrator :

1. The circuit of integrator is shown in Fig. 3.10.1.
2. This circuit produces an output voltage which is proportional to the time integral of the input voltage. Due to this reason it is known as integrator.
3. The integrator is an inverting Op-Amp in which feedback resistor R_f has been replaced by a capacitor C.
4. Feedback through capacitor forces a virtual ground to exist at the inverting input terminal.
5. The capacitive reactance X_c can be expressed as :

$$i_1 = \frac{V_1}{R_1} \text{ and } i_2 = \frac{d q_2}{dt} = C \frac{d(V_A - V_0)}{dt}$$

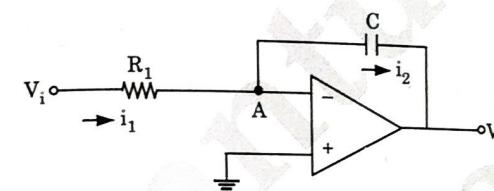


Fig. 3.10.1.

6. At point A :

$$i_1 = i_2$$

$$\frac{V_1}{R_1} = -C \frac{d V_0}{dt}$$

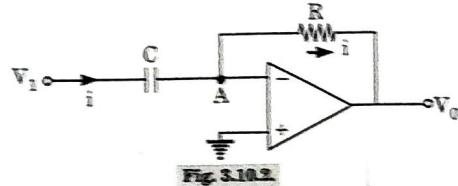
$$d V_0 = \frac{-1}{R_1 C} V_1 dt$$

$$V_0(t) = - \frac{1}{R_1 C} \int V_1(t) dt$$

The above equation shows that the output is the integral of the input with an inversion and scale multiplier of $1/R_1 C$.

B. Differentiator :

1. The function of a differentiator is to give an output voltage which is proportional to the rate of change of input voltage.
2. The circuit of a differentiator is shown in Fig. 3.10.2.
3. When we feed linearly increasing voltage to the differentiator, we get a constant DC output. So it is an inverse mathematical operation to that of an integrator.



4. At point A, $V_1 = \frac{q}{C}$

$$\frac{dV_1}{dt} = \frac{1}{C} \frac{dq}{dt} = \frac{i}{C} \text{ where } i = \frac{dq}{dt} \quad \dots (3.10.1)$$

$$V_0 = -iR \quad \dots (3.10.2)$$

5. Put the value of i from eq. (3.10.1) in eq. (3.10.2)

$$V_0 = -CR \frac{dV_1}{dt} \quad \dots (3.10.3)$$

6. The eq. (3.10.3) shows that the output voltage V_0 is equal to a constant ($-CR$) times the time derivative of the input voltage V_1 .

C. **Unity gain amplifier (voltage follower)** : Refer Q. 3.3, Page 3-4J, Unit-3.

D. **Inverting summer** : Refer Q. 3.4, Page 3-6J, Unit-3.

Que 3.11. Determine the output voltage for the given circuit shown in Fig. 3.11.1.

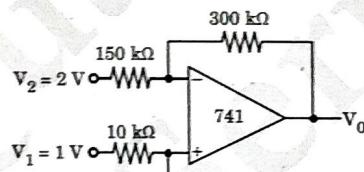


Fig. 3.11.1.

AKTU 2017-18(Sem-II), Marks 3.5

Answer

1. We can get V_0 by superposition method,
2. Let $V_1 = 1$ V and V_2 is at ground, so output due to V_1 , V_{01} , will be due to input at non-inverting terminal,

$$V_{01} = \left(1 + \frac{300}{150}\right) \left(\frac{10}{(10+10)}\right) = \frac{1}{2} \times \frac{450}{150} = \frac{3}{2} = 1.5 \text{ V}$$

3. Let $V_2 = 2$ V and V_1 is at ground, so output due to V_2 , V_{02} will be due to input at inverting terminal,

$$V_{02} = -\frac{300}{150} \times 2 = -4 \text{ V}$$

4. Now total output, $V_0 = V_{01} + V_{02}$
 $V_0 = +1.5 - 4 = -2.5 \text{ V}$

Que 3.12. Find out the voltage V_2 and V_3 of the given network of Fig. 3.12.1.

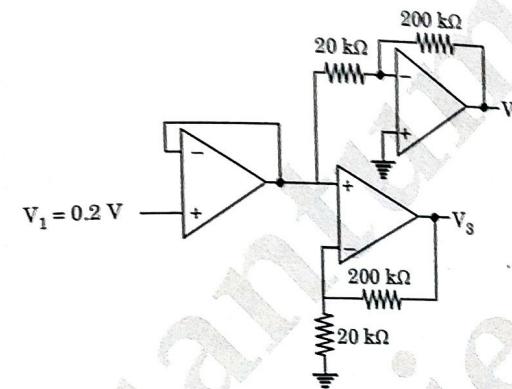


Fig. 3.12.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

1. Let V_A be the output of 1st Op-Amp.
 $V_A = 0.2 \text{ V}$ (\because Unity gain follower)
2. Thus,
 $V_2 = -\left(\frac{200 \text{ k}\Omega}{20 \text{ k}\Omega}\right) V_A = -10 \times 0.2 = -2 \text{ V}$
3.
 $V_3 = \left(1 + \frac{200}{20}\right) V_A = 11 \times 0.2 = 2.2 \text{ V}$

Que 3.13. Design and draw an inverting amplifier using Op-Amp

with a gain of -5 and $R_i = 10 \text{ k}\Omega$. AKTU 2016-17(Sem-I), Marks 05

Answer

Gain,

$$A_v = -5$$

$$R_i = 10 \text{ k}\Omega$$

$$A_v = \frac{-R_f}{R_i} = -5$$

$$R_f = 5 \times R_i = 5 \times 10 = 50 \text{ k}\Omega$$

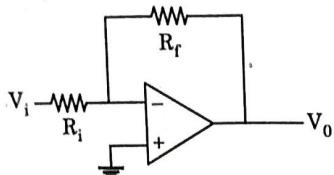


Fig. 3.13.1.

Que 3.14. Enlist the characteristics of ideal OP-Amp. Also determine the output voltage of following circuit.

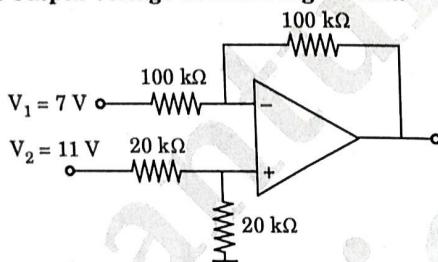


Fig. 3.14.1.

AKTU 2021-22(Sem-II), Marks 10

Answer

- A. Characteristics of ideal op-amp : Refer Q. 3.2, Page 3-3J, Unit-3.
B. Numerical :

The output voltage of the given circuit

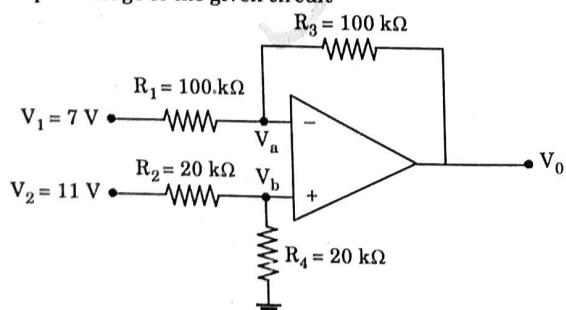


Fig. 3.14.2.

If $V_2 = 0$ then

$$V_{\text{out}(a)} = -V_1 \left(\frac{R_3}{R_1} \right)$$

$$\text{If } V_1 = 0 \text{ then } V_{\text{out}(b)} = V_2 \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

$$V_{\text{out}} = V_{\text{out}(a)} + V_{\text{out}(b)}$$

$$= -V_1 \left(\frac{R_3}{R_1} \right) + V_2 \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

Putting the respective value, we get

$$\begin{aligned} V_{\text{out}} &= -7 \left(\frac{100}{100} \right) + 11 \left(\frac{20}{20+20} \right) \left(\frac{100+100}{100} \right) \\ &= -7 + 11 \left(\frac{20}{40} \times \frac{200}{100} \right) \\ &= 4 \text{ V} \end{aligned}$$

Que 3.15. Calculate the output voltage V_0 of the circuit.

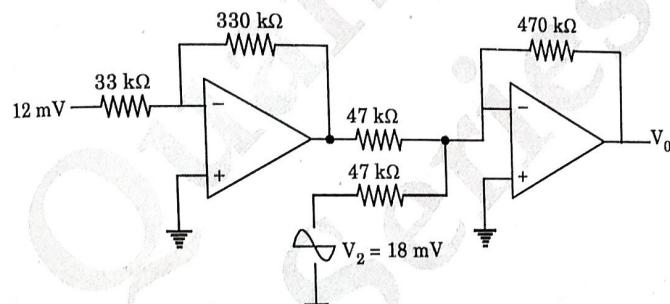


Fig. 3.15.1.

AKTU 2017-18(Sem-I), Marks 3.5

Answer

$$V_3 = -\left(\frac{R_2}{R_1} \right) V_1 = \frac{-330}{33} \times 12 \text{ mV} = -120 \text{ mV}$$

$$\text{Now } V_0 = -\left(\frac{R_6}{R_3} V_3 + \frac{R_6}{R_4} V_2 \right)$$

$$= - \left[\frac{470}{47} \times (-120) + \frac{470}{47} \times 18 \right]$$

$$= -[-1200 + 180] = 1020 \text{ mV}$$

$$V_0 = 1.02 \text{ V}$$

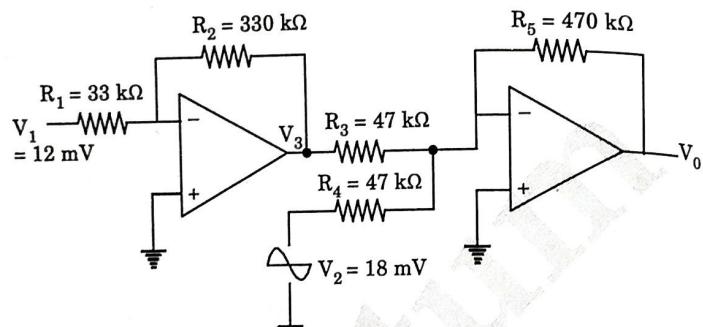


Fig. 3.15.2.

PART-3*Differential and Common-Mode Operation, Comparators.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

Que 3.16. Explain with the help of necessary diagram :

- a. Inverting amplifier
- b. Integrator
- c. Differential amplifier in two modes of operation.

AKTU 2015-16(Sem-I), Marks 10

OR

Analyse the differential amplifier with suitable circuit in two modes of operation.

Answer

- A. Inverting amplifier : Refer Q. 3.3, Page 3-4J, Unit-3.
- B. Integrator : Refer Q. 3.10, Page 3-11J, Unit-3.

Operational Amplifiers**3-18 J (Sem-1 & 2)**

- C. **Differential amplifier (in two modes of operation) :**
1. The differential amplifier circuit has two separate inputs and two separate outputs and that the emitters are connected together.
 2. It also consists of two separate voltage supplies.
 3. In differential amplifier circuit, the input signal operates both transistors in single-ended operation due to the common emitter connection, resulting in output from both collectors.
 4. In double-ended operation, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.
 5. In common-mode operation, the common input signal results in opposite signals at each collector; these signals cancel each other so that the resulting output signal is zero.
 6. The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs.
 7. Let's consider DC bias operation of the differential amplifier circuit. With each base voltage at 0 V, the common emitter DC bias voltage is

$$V_E = 0 \text{ V} - V_{BE} = -0.7 \text{ V}$$

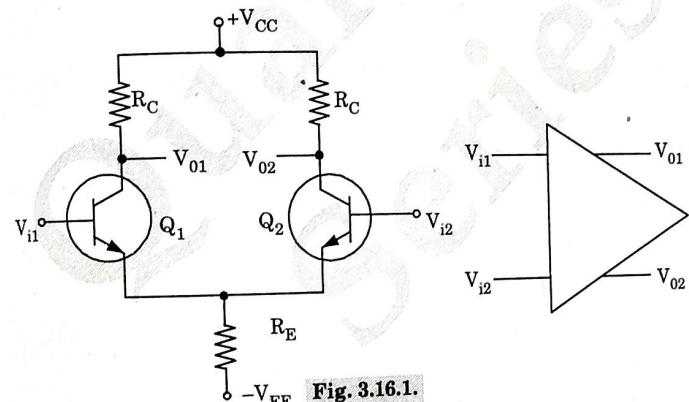


Fig. 3.16.1.

8. The emitter DC bias current is then,

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7 \text{ V}}{R_E}$$

9. Assuming the transistors are well matched, we get

$$I_{C1} = I_{C2} = \frac{I_E}{2}$$

∴ Collector voltage,

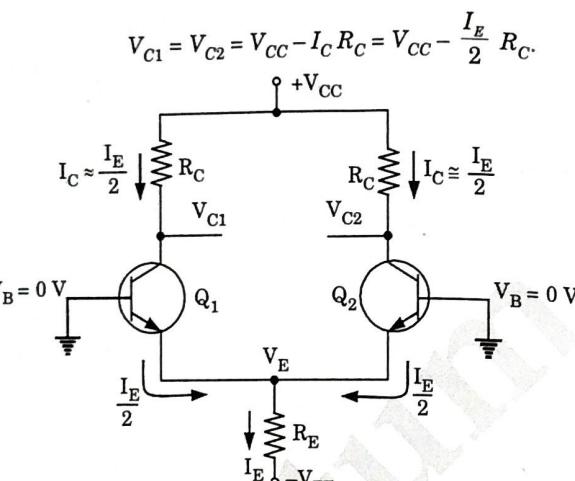


Fig. 3.16.2.

Que 3.17. Explain the basic parameters of Op-Amp.

OR

Explain the following characteristics of an Op-Amp :

i. CMRR

ii. Slew rate

AKTU 2017-18(Sem-I), Marks 3.5

OR

Draw and explain the differential amplifier. Define CMRR and slew rate in Op-Amp.

AKTU 2016-17(Sem-II), Marks 5.25

OR

Define the following terms :

1. CMRR

2. Peak Inverse Voltage

AKTU 2020-21(Sem-I), Marks 05

Answer

A. Differential amplifier : Refer Q. 3.16, Page 3-17J, Unit-3.

B. Basic parameters of Op-Amp :

1. Input bias current : The input bias currents I_{B1} and I_{B2} are the base bias currents of the two transistors in the input differential amplifier stage of the Op-Amp. An input bias current I_B is defined as the average of the two input bias currents I_{B1} and I_{B2} that is

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where, I_{B1} = DC bias current flowing into the inverting input,
 I_{B2} = DC bias current flowing into the non-inverting input.

2. Input offset current and voltage :

i. Input offset current : The input offset current, I_{io} is defined as the algebraic difference between two input bias currents I_{B1} and I_{B2} i.e., $I_{io} = |I_{B1} - I_{B2}|$

The value of I_{io} indicates the maximum amount by which the input bias current may differ.

ii. Input offset voltage : Input offset voltage, V_{io} is the differential input voltage that exists between two input terminals of an Op-Amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero.

3. Slew rate (SR) : It is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro-second.

$$\text{i.e., } SR = \left. \frac{dv_o}{dt} \right|_{\max} \text{ V/μsec}$$

Slew rate indicates how rapidly the output of Op-Amp can change in response to change in input frequency.

4. CMRR (common-mode rejection ratio) : It is an ability to reject the common mode noise which is present at both the inverting and non-inverting terminal.

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{CM}} \right|$$

C. Peak inverse voltage : Refer Q. 1.10, Page 1-14J, Unit-1.

Que 3.18. Determine the output voltage of an OP-AMP for the input voltage of $V_1 = 150 \mu\text{V}$ and $V_2 = 140 \mu\text{V}$. The amplifier has differential gain $A_d = 4000$ and CMRR is 100. **AKTU 2021-22(Sem-I), Marks 05**

Answer

Given : $V_1 = 150 \mu\text{V}$, $V_2 = 140 \mu\text{V}$, $A_d = 4000$, CMRR = 100

To Find : V_o .

$$\begin{aligned} V_o &= A_d V_d + A_{CM} V_{CM} \\ &= A_d (V_1 - V_2) + \frac{A_d}{CMRR} \left(\frac{V_1 + V_2}{2} \right) \\ &= 4000 (150 - 140) + \frac{4000}{100} \left(\frac{150 + 140}{2} \right) \\ &= 4000 \times 10 + 40 \times 145 \\ &= 40000 + 5800 \\ &= 45800 \end{aligned}$$

$$= 44800 \mu\text{V}$$

$$V_0 = 0.44 \text{ V}$$

Que 3.19. Determine the output voltage of an Op-Amp for input voltages of $V_{i1} = 200 \text{ V}$ and $V_{i2} = 140 \text{ V}$. The amplifier has a differential gain of $A_d = 6000$ and the value of CMRR is :

- i. 200
- ii. 10^5

AKTU 2015-16(Sem-I), Marks 05

Answer

Given : $V_{i1} = 200 \text{ V}$, $V_{i2} = 140 \text{ V}$, $A_d = 6000$

To Find : V_0 .

- i. For CMRR = 200 = A_d/A_{CM}

$$V_0 = A_d V_d + A_{CM} V_{CM} = A_d (V_{i1} - V_{i2}) + \frac{A_d}{CMRR} \left(\frac{V_{i1} + V_{i2}}{2} \right)$$

$$= 6000(200 - 140) + \frac{6000}{200} \left(\frac{200 + 140}{2} \right) = 365100 \text{ V}$$

$$= 36.51 \text{ kV}$$

- ii. For CMRR = $10^5 = A_d/A_{CM}$

$$V_0 = A_d V_d + A_{CM} V_{CM}$$

$$= 6000(200 - 140) + \frac{6000}{10^5} \left(\frac{200 + 140}{2} \right) = 360010.2 \text{ V}$$

$$= 360 \text{ kV}$$

Que 3.20. For an input of $V_I = 50 \text{ mV}$ in the circuit of Fig. 3.20.1, determine the maximum frequency that may be used. The Op-Amp slew rate $SR = 0.4 \text{ V/s}$.

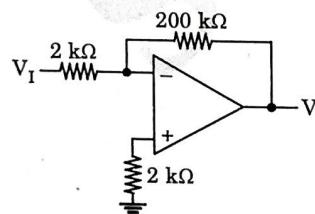


Fig. 3.20.1.

AKTU 2015-16(Sem-I), Marks 05

Answer

Given : $R_f = 200 \text{ k}\Omega$, $R_1 = 2 \text{ k}\Omega$, $V_I = 50 \text{ mV}$, $SR = 0.4 \text{ V/s}$

To Find : f_{max} .

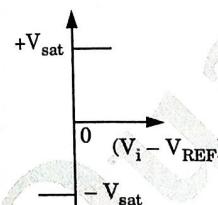
1. $A_{CL} = \left| \frac{R_f}{R_1} \right| = \frac{200 \text{ k}\Omega}{2 \text{ k}\Omega} = 100$
2. Output gain factor, $K = A_{CL} V_I = 100 \times 50 \times 10^{-3} = 5 \text{ V}$
3. Maximum signal frequency = $\frac{SR}{2\pi K} = \frac{0.4}{2\pi(5)} = 0.012 \text{ Hz}$

Que 3.21. Write a short note on comparator and enlist its applications.

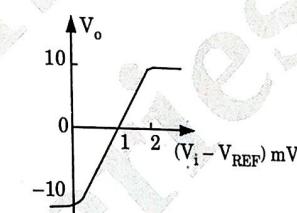
Answer

A. Comparator :

1. A comparator is a circuit that is used for comparing a signal voltage applied at one input of Op-Amp with a known reference voltage at other input.



(a) Ideal comparator.



(b) Practical comparator.

Fig. 3.21.1. The transfer characteristics.

2. It is basically an open-loop Op-Amp with output $\pm V_{sat}$ ($= V_{CC}$) as shown in ideal transfer characteristics of Fig. 3.21.1(a).
3. There are basically two types of comparator :
- i. **Non-inverting comparator :**
 1. The circuit of Fig. 3.21.2(a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (-ve) input and a time varying signal v_i is applied to (+ve) input.
 2. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$ And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$
 3. The output waveform for a sinusoidal input signal applied to the (+ve) input is shown in Fig. 3.21.2(b) and Fig. 3.21.2(c) for positive and negative V_{ref} respectively.

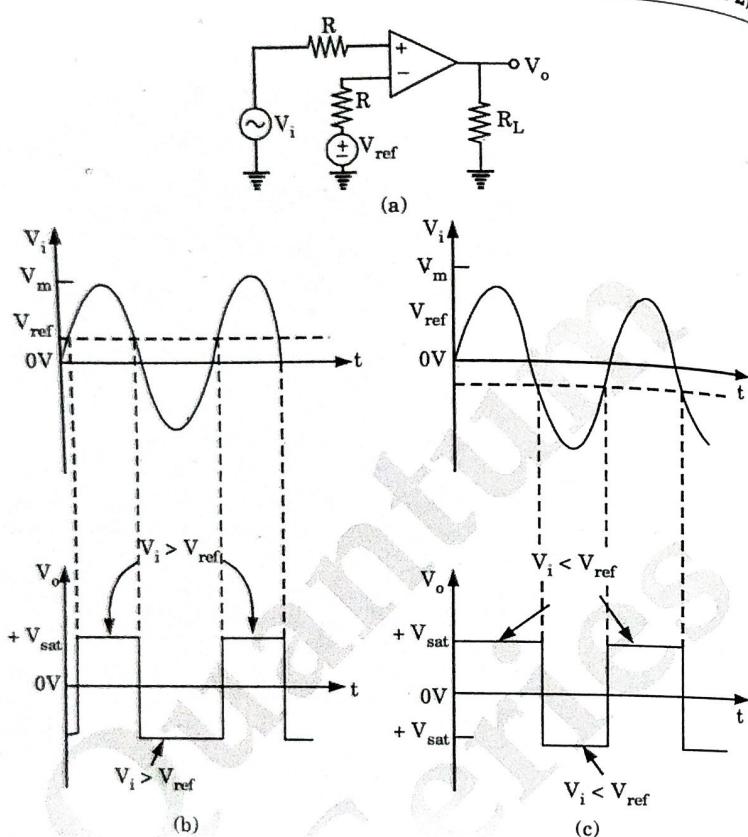


Fig. 3.21.2. (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative.

ii. Inverting comparator :

In inverting comparator, fixed reference voltage V_{ref} is applied to (+ve) input and a time varying signal v_i is applied to (-ve) input.

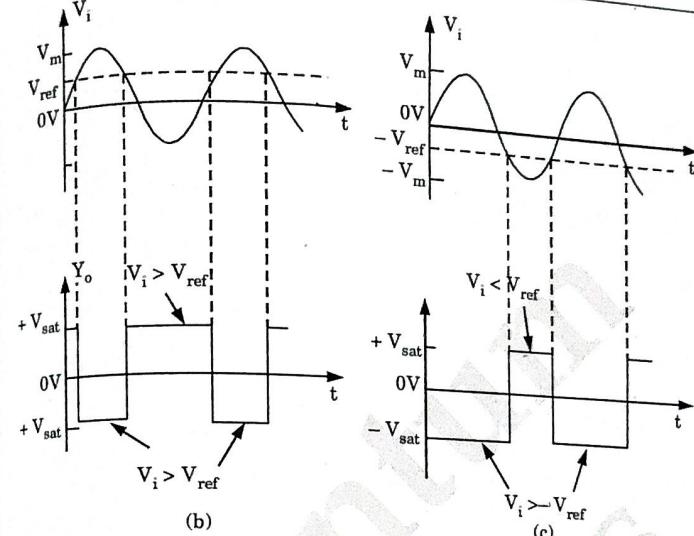
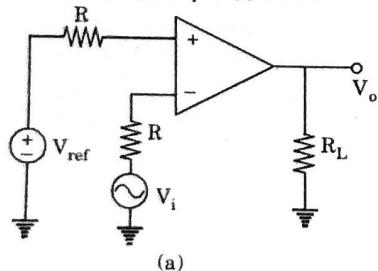


Fig. 3.21.3. (a) Inverting comparator. Input and output waveforms for (b) $V_{ref} > 0$ (c) $V_{ref} < 0$.

B. Applications of comparator :

- Zero crossing detector
- Window detector
- Phase meter.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Define Op-Amp with the help of block diagram. Also draw its equivalent circuit. List the ideal characteristics of Op-Amp.

Ans: Refer Q. 3.2.

Q. 2. Draw the circuit of an Op-Amp as voltage follower and find an expression for its voltage gain.

Ans: Refer Q. 3.3.

Q. 3. Explain integrator circuit using Op-Amp.

Ans. Refer Q. 3.10.

Q. 4. Design and draw an inverting amplifier using Op-Amp with a gain of -5 and $R_i = 10 \text{ k}\Omega$.

Ans. Refer Q. 3.13.

Q. 5. Calculate the output voltage V_0 of the circuit.

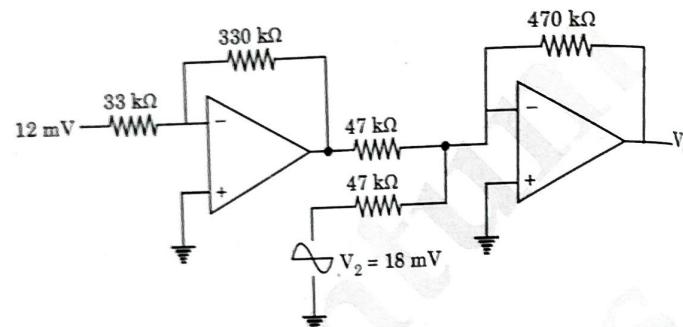


Fig. 1.

Ans. Refer Q. 3.15.

Q. 6. Draw and explain the differential amplifier. Define CMRR and slew rate in Op-Amp.

Ans. Refer Q. 3.17.

Q. 7. Determine the output voltage of an OP-AMP for the input voltage of $V_1 = 150 \mu\text{V}$ and $V_2 = 140 \mu\text{V}$. The amplifier has differential gain $A_d = 4000$ and CMRR is 100.

Ans. Refer Q. 3.18.



Digital Electronics

CONTENTS

Part-1 : Digital Electronics : 4-2J to 4-5J
Number System and Representation, Binary Arithmetic

Part-2 : Introduction of Basic and Universal Gates 4-6J to 4-10J

Part-3 : Using Boolean Algebra 4-10J to 4-19J
Simplification of Boolean Function, K-map Minimization upto 6 Variable

PART- 1

Digital Electronics : Number System and Representation, Binary Arithmetic.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 4.1. Define number system and also define signed and unsigned binary number ?

Answer

Number system : It is a language of digital systems consisting of a set of symbols called digits with rules defined for their addition, multiplication and other mathematical operations.

The classification of number system is as follows :

1. **Decimal number system :** It has 10 symbols, so the base or radix of this number system is 10. The 10 symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.
2. **Binary number system :** It is a base 2 number system. The two binary digits are 1 and 0.
3. **Octal number system :** It has a base of 8. It has eight possible digits 0, 1, 2, 3, 4, 5, 6 and 7.
4. **Hexadecimal number system :** It is a base 16 number system. It has digits from 0 to 9, A, B, C, D, E and F.
5. **Complements :** These are used in digital computers to simplify the subtraction operation and for logical manipulation.
6. **Signed binary number :** Binary number that carry identification as to their polarity is called signed binary number. Plus (+) and minus (-) signs for positive and negative numbers can be represented in a digital format. The three major signed binary notations are : Sign magnitude notation, 1's complement notation and 2's complement notation.
7. **Unsigned binary number :** In these type of numbers we do not consider the (+) or (-) sign and concentrate only on the magnitude (absolute value) of numbers.

Que 4.2. Convert the following :

- i. $(62.7)_8 = ()_{16} = ()_2$
- ii. $(BC6)_{16} = ()_{10} = ()_2$

Answer

i. $(62.7)_8 = ()_{16} = ()_2$
 $\begin{array}{r} 110 \\ 6 \end{array} \quad \begin{array}{r} 010 \\ 2 \end{array} \quad \begin{array}{r} .111 \\ 7 \end{array} \rightarrow \begin{array}{r} 0011 \\ 6 \end{array} \quad \begin{array}{r} 0010 \\ 2 \end{array} \quad \begin{array}{r} .1110 \\ 7 \end{array} \Rightarrow (32.E)_{16}$
 $(62.7)_8 = (32.E)_{16} = (00110010.1110)_2$

ii. $(BC6)_{16} = ()_{10} = ()_2$
 $(BC6)_{16} = 11 \times 16^2 + 12 \times 16^1 + 6 \times 16^0 = (3014)_{10}$
 $(3014)_{10} = (101111000110)_2$

Que 4.3. Explain binary arithmetic in detail.

Answer

Arithmetic operations in digital systems are usually done in binary because design of logic circuits to perform binary arithmetic is much easier than for decimal. The basic rules of binary arithmetic are given below :

i. **Binary addition rules :**

0	+	0	=	0
0	+	1	=	1
1	+	0	=	1
1	+	1	=	10

↓
Carry bit, carry it to the next higher order column

ii. **Binary subtraction rules :**

0	-	0	=	0
1	-	0	=	1
1	-	1	=	0
0	-	1	=	10

↓
Borrow bit, borrowed from to the next higher order column

iii. **Binary multiplication rules :**

0	×	0	=	0
0	×	1	=	0
1	×	0	=	0
0	×	1	=	1

iv. **Binary division :**

0	÷	1	=	0
1	÷	1	=	1

Que 4.4. Perform the addition for the given binary number.

- $(101101)_2 + (10110)_2$
- $(101.11)_2 + (111)_2$

Answer

$\begin{array}{r} 101101 \\ + 101101 \\ \hline 1000011 \end{array}$	$\begin{array}{r} 101.11 \\ + 111 \\ \hline 111.10 \end{array}$
---	---

Que 4.5. Perform following operation as indicated.

- Determine 2's complement of $(1010.110)_2$.
- Convert $(25.125)_{10}$ into Hexadecimal number.
- Add binary number $(1011)_2$ and $(1111)_2$.
- State De Morgan's Law.
- Define minterm and maxterm.

AKTU 2021-22 (Sem-II), Marks 10

Answer

i. 2's complement of $(1010.110)_2$:
 1's complement of $1010.110 = 0101.001$
 1's complement of $1010.110 = 0101.001$
 Now add number 1 to LSB = 0101.001

$$\begin{array}{r} & & + 1 \\ & 0101.001 \\ \hline 0101.010 \end{array}$$

- ii. Convert $(25.125)_{10}$ into Hexadecimal number:
 Convert integer part

$$\begin{array}{r} 16 \mid 25 \\ \quad \quad \quad | \\ \quad 16 \mid 1 \quad 9 \\ \quad \quad \quad | \\ \quad 0 \quad 1 \end{array}$$

Convert the fractional part into hex:

$$0.125 \times 16 = 2$$

∴ The result of conversion

$$(25.125)_{10} = (19.2)_{16}$$

- iii. Add binary number $(1011)_2$ and $(1111)_2$:

$$\begin{array}{r} 1011 \\ + 1111 \\ \hline 11010 \end{array} \quad \begin{array}{l} \text{As } 0+0=0 \\ 0+1=1 \\ 1+0=1 \\ 1+1=10 \end{array}$$

iv. De Morgan's Law :

First De Morgan theorem : It states, complement of two or more variables and then AND operation on these is equivalent to NOR operation on these variables. (NOR means complement of two or more variables OR).

$$\overline{A_1 + A_2} = \overline{A_1} \cdot \overline{A_2}$$

Second De Morgan theorem : It states that complement of two or more variables and then OR operation on these is equivalent to a NAND operation on these variables (NAND means complement of two or more variables AND).

$$\overline{A_1 A_2 A_3} = \overline{A_1} + \overline{A_2} + \overline{A_3} \dots$$

- v. **Define minterm and maxterm :** Minterm is a special product of literals in which each input variable appears exactly once.

For example $m_0 = \min(x, y, z) = x \cdot y \cdot z$

Maxterm is a sum of literals in which each input variable appears exactly once.

For example $M_0 = \max(x, y, z) = x + y + z$

Que 4.6.

- Subtract using 10's complement: $(9754)_{10} - (364)_{10}$
- Subtract using 1's complement: $(10111)_2 - (110011)_2$

AKTU 2021-22 (Sem-I), Marks 10

Answer

- i. $(9754)_{10} - (364)_{10}$
 1. 9's complement of (364) is

$$\begin{array}{r} 999 \\ 364 \\ \hline 635 \end{array}$$

2. 10's complement of (364) is

$$\begin{array}{r} 635 \\ + 1 \\ \hline 636 \end{array}$$

3.

$$\begin{array}{r} 636 \\ 636 \\ + 9754 \\ \hline 10390 \end{array}$$

- ii. $(10111)_2 - (110011)_2$
 1's complement of (110011) is 001100

$$\begin{array}{r} 010111 \\ + 001100 \\ \hline 010011 \end{array}$$

PART-2*Introduction of Basic and Universal Gates.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

Que 4.7. What are the logic gates? Explain each of them.

Answer

There are three logic gates:

i. AND gate :

- An AND gate will produce a HIGH output when all inputs are HIGH otherwise the output of AND gate is LOW. Fig. 4.7.1 shows the symbol of AND gate.

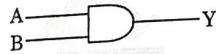


Fig. 4.7.1.

- Table 4.7.1 gives truth table for the two input AND gate. The inputs of AND gate is A and B, the output of gate is Y.

Table 4.7.1.

Input		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

ii. OR gate :

- An OR gate produces a HIGH output when any one of the inputs is HIGH. It produces a LOW output when all the inputs are LOW. Fig 4.7.2 shows the logic symbol of 2 input OR gate.

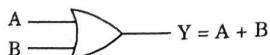


Fig. 4.7.2.

- Table 4.7.2 gives the truth table for the two input OR gate. The input and output variables are represented in the binary form.

Table 4.7.2.

Input		Output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

iii. NOT gate :

- The NOT gate is also called as an inverter. The output of NOT gate is also called as inverse input or complement of input.
- Fig. 4.7.3 shows the logic symbol of NOT gate and Table 4.7.3 shows the truth table of NOT gate.
- The NOT gate produces HIGH output when the input is LOW and the NOT gate output is LOW when the input is HIGH.



Fig. 4.7.3.

Table 4.7.3.

Input	Output
A	$Y = \bar{A}$
0	1
1	0

Que 4.8. Explain universal gates.

OR

What are universal gates? Why are they called so?

AKTU 2020-21 (Sem-I), Marks 05

Answer

NAND and NOR gates are universal gates because it is possible to implement any logic or expression using only NAND or only NOR gates.

i. NAND gate :

- NAND gate is a combination of AND gate followed by NOT gate. The output of NAND gate is inverse of AND gate output.
- Fig. 4.8.1 shows the logic symbol of a NAND gate. Table 4.8.1, shows the truth table of NAND gate. The NAND gate produce HIGH output when any one of the input is LOW.

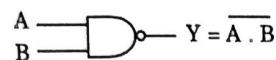


Fig. 4.8.1.

Table 4.8.1.

Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

ii. NOR gate :

1. NOR gate is combination of OR gate followed by NOT gate, so the output of NOR gate is inverse of OR gate output.
2. Fig. 4.8.2 shows the logic symbol of NOR gate and table 4.8.2, shows the truth table of NOR gate. The NOR gate gives a LOW output when any one of the input is HIGH otherwise the output is HIGH.

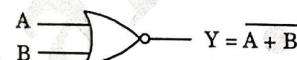


Fig. 4.8.2.

Table 4.8.2.

Input		Output
A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

Que 4.9. Define universal logic Gates. Realize basic logic gates using NAND and NOR gates. AKTU 2021-22 (Sem-II), Marks 10

OR
Implement XOR gate using NAND gate only.

AKTU 2020-21 (Sem-I), Marks 05

Answer

- A. Universal logic gates : Refer Q. 4.8, Page 4-7J, Unit-4.
 B. Realize basic logic gates using NAND and NOR gates :
 NAND as OR gate :

$$(A \cdot B)' = A' + B'$$

$$(A' \cdot B')' = A'' + B'' = A + B$$

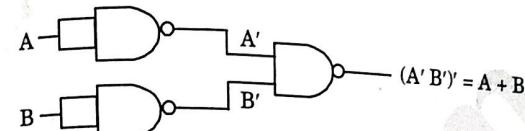


Fig. 4.9.1.

NAND as AND gate :

$$Y = [(A \cdot B)']' = (A \cdot B)$$

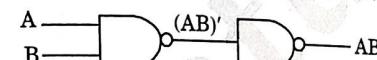


Fig. 4.9.2.

NAND as X-OR gate :

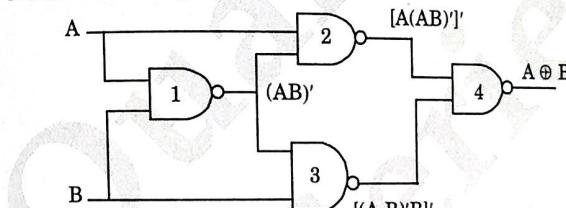


Fig. 4.9.3.

NAND as NOT gate :

$$Y = (A \cdot A)'$$

$$Y = (A)'$$



Fig. 4.9.4.

NOR gate as OR gate :

$$Y = [(A + B)']'$$

$$Y = A + B$$

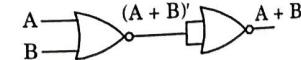


Fig. 4.9.5.

NOR gate as AND gate :

$$(A + B)' = A'B'$$

$$(A' + B')' = A'' \cdot B'' = AB$$

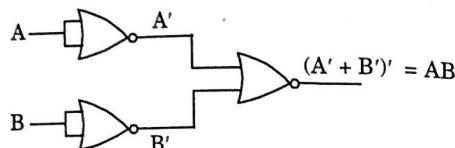


Fig. 4.9.6.

NOR gate as X-OR gate :

Ex-OR gate is actually Ex-NOR gate followed by NOT gate

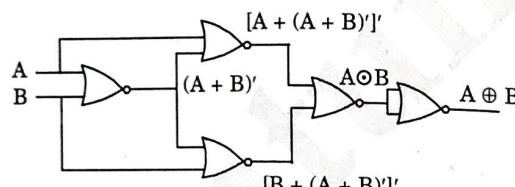


Fig. 4.9.7.

NOR gate as NOT gate :

$$Y = (A + A)'$$

$$Y = (A)'$$

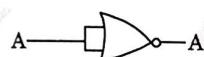


Fig. 4.9.8.

PART-3

*Using Boolean Algebra Simplification of Boolean Function,
K-Map Minimization Upto 6 Variable.*

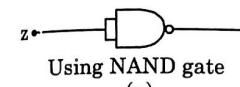
Questions-Answers**Long Answer Type and Medium Answer Type Questions****Que 4.10.** Simplify the following expression as much as possible:

$$F(w, x, y, z) = \bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}x\bar{y}\bar{z} + w\bar{y}\bar{z}$$

and implement your result using universal gates only.

Answer

$$\begin{aligned}
 F(w, x, y, z) &= \bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}x\bar{y}\bar{z} + w\bar{y}\bar{z} \\
 &= \bar{y}\bar{z} + w\bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}x\bar{y}\bar{z} \\
 &= \bar{z}(\bar{y} + w\bar{y}) + \bar{w}\bar{x}(\bar{x} + xy) \\
 &= \bar{z}(\bar{y} + w) + \bar{w}\bar{x}(\bar{x} + y) \quad [\because \bar{A} + AB = \bar{A} + \bar{B}] \\
 &= \bar{y}\bar{z} + w\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}y\bar{z} \\
 &= \bar{y}\bar{z} + \bar{w}y\bar{z} + w\bar{z} + \bar{w}\bar{x}\bar{z} \\
 &= \bar{z}(\bar{y} + \bar{w}y) + \bar{z}(w + \bar{w}\bar{x}) \\
 &= \bar{z}(\bar{y} + \bar{w}) + \bar{z}(w + \bar{x}) \\
 &= \bar{z}(\bar{y} + \bar{w} + w + \bar{x}) \\
 &= \bar{z}(\bar{y} + 1 + \bar{x}) \\
 &= \bar{z}(\bar{y} + 1) \quad [\because 1 + A = 1] \\
 &= \bar{z} \quad [\because 1 + \bar{A} = 1]
 \end{aligned}$$



Using NAND gate (a)



Using NOR gate (b)

Fig. 4.10.1.

Que 4.11. Simplify the following boolean expression to a minimum number of literals.

$$\text{i. } \bar{A}\bar{C} + ABC + A\bar{C} + A\bar{B}$$

$$\text{ii. } (\bar{x}\bar{y} + z) + z + xy + wz$$

Answer

$$\text{i. } \bar{A}\bar{C} + ABC + A\bar{C} + A\bar{B} :$$

$$\begin{aligned}
 \text{Let } Y &= \bar{A}\bar{C} + A\bar{C} + A\bar{B} + ABC \\
 &= \bar{C}(\bar{A} + A) + A(\bar{B} + BC) \\
 &= \bar{C} + A(\bar{B} + C) \quad [\because A + \bar{A} = 1] \\
 &= \bar{C} + AC + A\bar{B} \quad [\because \bar{C} + AC = (\bar{C} + A)(\bar{C} + C)] \\
 &= \bar{C} + A + A\bar{B} \\
 &= \bar{C} + A(1 + \bar{B}) \\
 &= A + \bar{C}
 \end{aligned}$$

$$\text{ii. } (\bar{x}\bar{y} + z) + z + xy + wz$$

$$\begin{aligned}
 \text{Let } Y &= (\bar{x}\bar{y} + z) + z + xy + wz \\
 &= \bar{x}\bar{y} + z + xy + wz
 \end{aligned}$$

$$\begin{aligned}
 &= \bar{x} \bar{y} + xy + z(1+w) \\
 &= \bar{x} \bar{y} + xy + z = x \odot y + z \quad [\because 1+w=1]
 \end{aligned}$$

Que 4.12. Convert the given expression into canonical SOP form

$$Y = A + AB + BC$$

Answer

$$\begin{aligned}
 Y &= A(B + \bar{B})(C + \bar{C}) + AB(C + \bar{C}) + BC(A + \bar{A}) \\
 Y &= (AB + A\bar{B})(C + \bar{C}) + ABC + A\bar{B}\bar{C} + ABC + \bar{A}BC \\
 &= ABC + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + ABC + A\bar{B}\bar{C} + ABC + \bar{A}BC \\
 &= ABC + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + \bar{A}B\bar{C}
 \end{aligned}$$

Que 4.13. By showing all the calculations, do as directed :

- For a boolean function of 4 variables, $\Sigma(3, 7, 11, 14, 15) = \pi(?)$
- $(110110.011)_2 = (?)_{16}$
- $(231.36)_{10} = (?)_2$
- $(11011.10)_2 = (?)_{10}$
- $(534)_8 = (?)_{10}$

AKTU 2020-21 (Sem-I), Marks 10

Answer

- Given, $Y(A, B, C, D) = \Sigma m(3, 7, 11, 14, 15)$
 $\Rightarrow Y(A, B, C, D) = \pi M(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13)$

- Given, 110110.011_2

$$= \overline{0011} \ 0110 \ . \overline{0110}$$

$$= (36.6)_{16}$$

- $(231.36)_{10}$

2	231	1
2	115	1
2	57	1
2	28	0
2	14	0
2	7	1
2	3	1
2	1	1
	0	

$$(231)_{10} = (1110111)_2$$

$$\begin{array}{l}
 0.36 \times 2 = 0.72 \quad 0 \\
 0.72 \times 2 = 1.44 \quad 1 \\
 0.44 \times 2 = 0.88 \quad 0 \\
 0.88 \times 2 = 1.76 \quad 1 \\
 (0.36)_{10} = (0101)_2
 \end{array}$$

So, $(231.36) = (1110111,0101)_2$

iv. $(11011.10)_2$
 $= 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2}$
 $= 16 + 8 + 0 + 2 + 1 + 0.5 + 0 = (27.5)_2$

v. $(534)_8$
 $= 5 \times 8^2 + 3 \times 8^1 + 4 \times 8^0$
 $= 320 + 24 + 4 = (348)_{10}$

$$\because A + A = A$$

Que 4.14. Convert the given expression into canonical POS form

$$Y = A(A + \bar{B})(A + B + \bar{C})$$

Answer

$$\begin{aligned}
 Y &= (A + B \bar{B} + C \bar{C})(A + \bar{B} + C \bar{C})(A + B + \bar{C}) \\
 &= (A + B \bar{B} + C)(A + B \bar{B} + \bar{C})(A + \bar{B} + C)(A + \bar{B} + \bar{C}) (A + B + \bar{C}) \\
 &= (A + B + C)(A + \bar{B} + C)(A + B + \bar{C})(A + \bar{B} + \bar{C}) \\
 &\quad (A + \bar{B} + C)(A + \bar{B} + \bar{C})(A + B + \bar{C})
 \end{aligned}$$

$$Y = (A + B + C)(A + \bar{B} + C)(A + B + \bar{C})(A + \bar{B} + \bar{C})$$

Que 4.15. Write a short note on Karnaugh map. Also show the reduction of boolean expression and how to mark pairs. How gate-level minimization is implemented ?

Answer

- Karnaugh map is another way of presenting the information given by a truth table. These maps are also known by the name *K-map*. Let us consider the map for two variables. There may be four possible combinations within four squares.
- Each square represents unique minterms as shown in Fig. 4.15.1 :

A	B	\bar{B}	B
\bar{A}	$\bar{A}\bar{B}$	$\bar{A}B$	AB
A	$A\bar{B}$	AB	$A\bar{B}$

A	B	0	1
0	0	0	1
1	0	1	1

Fig. 4.15.1.

For three variables :

- There are eight minterms for three binary variables. Hence the *K-map* consists of eight squares.

2. The K-map drawn in Fig. 4.15.2, for three variables is marked with numbers in each row and each column to show the relationship between the squares and the three variables.

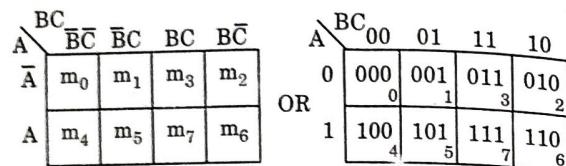


Fig. 4.15.2.

3. For example, the square assigned to m_5 , which corresponds to row 1 and column 01. When these two numbers reconsidered, they give the binary number 101, whose decimal equivalent is 5.

For four variables :

1. The map for boolean function of four binary variables require sixteen minterms, hence the map consists of sixteen squares.
2. The listed terms are from 0 to 15, i.e., 16 minterms. The map shows the relationship with the four variables.
3. In every square the numbers are written. The number denotes that this square corresponds to that number's minterm.

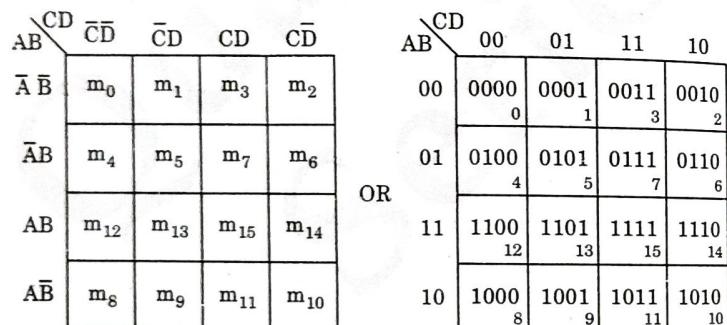


Fig. 4.15.3.

Que 4.16. Simplify the function $F(A, B, C, D) = \sum m(0, 2, 5, 6, 7, 13, 14, 15) + d(8, 10)$ using K-map and implement the simplified function using NAND gates only.

AKTU 2021-22 (Sem-II), Marks 10

Answer

$$F(A, B, C, D) = \sum m(0, 2, 5, 6, 7, 13, 14, 15) + d(8, 10)$$

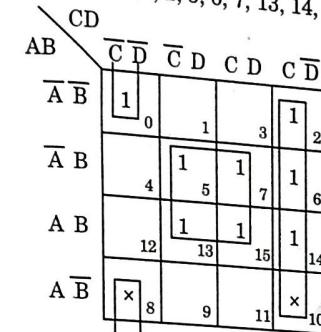


Fig. 4.16.1.

$$F(A, B, C, D) = \bar{B}\bar{C}\bar{D} + BD + C\bar{D}$$

Implementation using NAND gate
Taking double complement

$$F(A, B, C, D) = \overline{\overline{B}\bar{C}\bar{D}} + \overline{BD} + \overline{C\bar{D}}$$

Using De Morgan's theorem

$$F(A, B, C, D) = \overline{\overline{B}\bar{C}\bar{D}} \cdot \overline{BD} \cdot \overline{C\bar{D}}$$

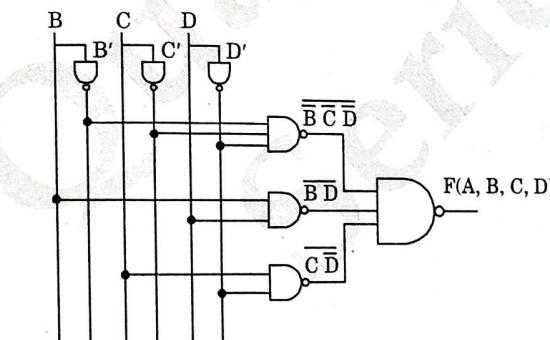


Fig. 4.16.2.

Que 4.17. Minimize using K-map and realize using NOR gates only.

$$F(A, B, C, D) = \prod M(3, 4, 5, 7, 9, 13, 14, 15) \cdot d(0, 2, 8)$$

AKTU 2021-22 (Sem-I), Marks 10

4-16 J (Sem-1 & 2)

Answer

Given, $F(A, B, C, D) = \prod M(3, 4, 5, 7, 9, 13, 14, 15)$ and $d(0, 2, 8)$

		CD	00	01	11	10	
AB		00	X	0	0	X	
		01	0	1	3	2	
AB		11	0	0	7	6	
		10	12	0	15	14	
		00	X	0	11	10	
		01	8	9			

$$F(A, B, C, D) = (A + \bar{B} + C) \cdot (\bar{B} + \bar{D}) \cdot (A + \bar{C} + \bar{D}) \\ (\bar{A} + \bar{C} + \bar{D}) \cdot (\bar{A} + C + \bar{D})$$

Implement using NOR gate taking double complement

$$F(A, B, C, D) = \overline{(A + \bar{B} + C) \cdot (\bar{B} + \bar{D}) \cdot (A + \bar{C} + \bar{D}) \cdot (\bar{A} + C + \bar{D})} \\ = \overline{(A + \bar{B} + C)} + \overline{(\bar{B} + \bar{D})} \cdot \overline{(A + \bar{C} + \bar{D})} + \overline{(\bar{A} + C + \bar{D})}$$

Realization :

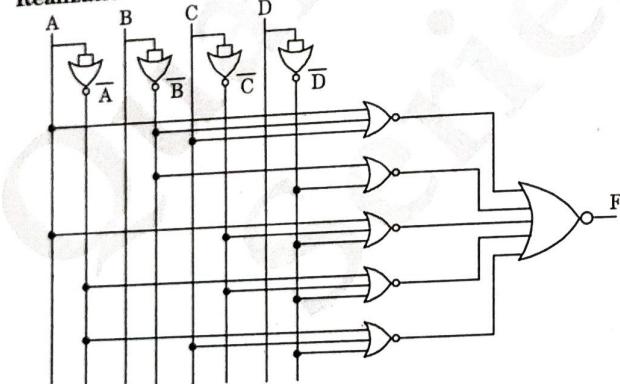


Fig. 4.17.1.

Que 4.18. Simplify the following function using K-map

$$F(A, B, C, D) = \Sigma(1, 3, 4, 5, 6, 7, 9, 11, 13, 15).$$

Also implement the simplified function using basic gates only.

AKTU 2020-21 (Sem-I), Marks 10

4-17 J (Sem-1 & 2)

Answer

Given, $F(A, B, C, D) = \Sigma(1, 3, 4, 5, 6, 7, 9, 11, 13, 15)$

		CD	00	01	11	10
AB		00	0	1	1	2
		01	1	5	7	6
AB		11	12	1	15	14
		10	8	9	11	10

$$F = \bar{A}B\bar{C} + D + BC$$

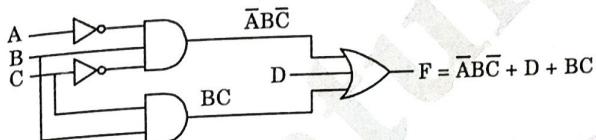


Fig. 4.18.1.

Que 4.19. Simplify the following Boolean function using K-map
 $Y = \Sigma m(0, 1, 3, 5, 6, 7, 9, 11, 16, 18, 19, 20, 21, 22, 24, 26)$

Answer

K-map :

		CDE	000	001	011	010	110	111	101	100
AB		00	1	0	4	12	8	24	28	16
		01	1	1	5	13	1	9	25	29
AB		11	1	1	7	15	11	27	31	23
		10	2	1	6	14	10	26	30	22

Fig. 4.19.1.

$$Y = \bar{D}\bar{E}\bar{A}\bar{B} + \bar{C}\bar{D}\bar{B} + \bar{A}\bar{C}\bar{D}\bar{E} + \bar{C}\bar{D}\bar{A}\bar{B} + \bar{C}\bar{D}\bar{E}\bar{B} + C\bar{D}\bar{E}\bar{B} + C\bar{D}\bar{E}\bar{A} + C\bar{D}\bar{E}\bar{A} \\ = \bar{D}\bar{B}(\bar{E}\bar{A} + CA) + \bar{C}B(\bar{D} + D\bar{E}) + \bar{D}E(A\bar{C} + \bar{A}C) + C\bar{E}(D\bar{B} + \bar{D}A) \\ = \bar{D}\bar{B}(\bar{E}\bar{A} + CA) + \bar{C}B(\bar{D} + \bar{E}) + \bar{D}E(A \oplus C) + C\bar{E}(D\bar{B} + \bar{D}A)$$

Que 4.20. $F(A, B, C, D, E) = \Sigma m(0, 1, 2, 4, 5, 6, 10, 13, 14, 18, 21, 22, 24, 26, 29, 30)$. Simplify the function with help of K-map and realize the simplified function using basic logic gates.

AKTU 2021-22 (Sem-I), Marks 10

Answer

K-map :

		CDE								
		AB	000	001	011	010	110	111	101	100
00			1 0	1 4	12	8	1 24	28	20	16
01			1 5	1 13	9	25	1 29	1 21	17	
11			3 0	0 7	0 15	0 11	27	0 31	0 23	0 19
10			1 2	1 6	1 14	1 10	1 26	0 26	1 22	1 18

$$F(A, B, C, D, E) = \bar{A}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + AB + \bar{B}C\bar{D}\bar{E}$$

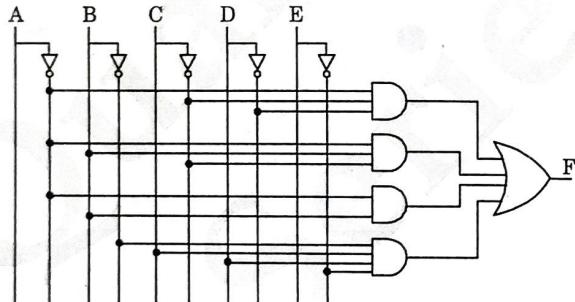


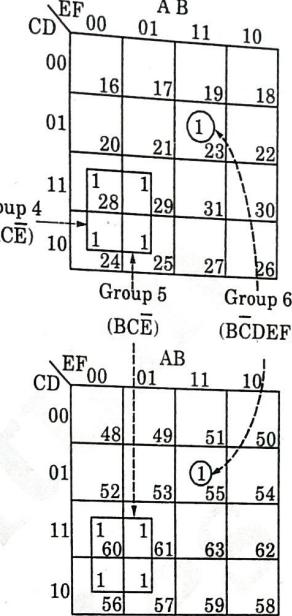
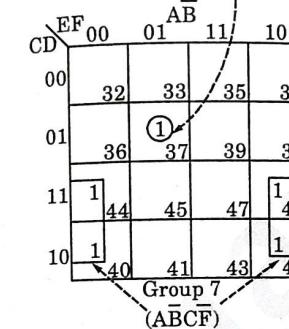
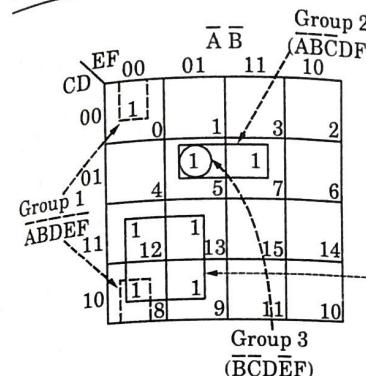
Fig. 4.20.1.

Que 4.21. Simplify the Boolean function

$$F(A, B, C, D, E, F) = \Sigma m(0, 5, 7, 8, 9, 12, 13, 23, 24, 25, 28, 29, 37, 40, 42, 44, 46, 55, 56, 57, 60, 61)$$

Answer

- Group 1 and group 2 are two pairs of 1's in the first 16-cell map.



- Group 3 is formed by two isolated 1's from first 16-cell map and third 16-cell map.
- Group 4 is a combination of two quads from first 16-cell and second 16-cell map.
- Similarly group 5 is a combination of two quads from second 16-cell map and fourth 16-cell map.
- Group 6 is again a combination of two quads from second 16-cell map and fourth 16-cell map.
- Finally group 7 is a quad within the third 16-cell map.

The expression is,

$$F = \overline{ABDEF} + \overline{ABCDF} + \overline{BCDEF} + \overline{ACE} + BCE + \overline{BCDEF} + A\bar{B}CF$$

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

Q. 1. Define number system and also define signed and unsigned binary number ?

Ans. Refer Q. 4.1.

Q. 2. i. Subtract using 10's complement : $(9754)_{10} - (364)_{10}$

ii. Subtract using 1's complement : $(10111)_2 - (110011)_2$

Ans. Refer Q. 4.6.

Q. 3. Define universal logic Gates. Realize basic logic gates using NAND and NOR gates.

Ans. Refer Q. 4.9.

Q. 4. Simplify the function $F(A, B, C, D) = \Sigma m(0, 2, 5, 6, 7, 13, 14, 15) + d(8, 10)$ using K-map and implement the simplified function using NAND gates only.

Ans. Refer Q. 4.16.

Q. 5. Minimize using K-map and realize using NOR gates only. $F(A, B, C, D) = \Pi M(3, 4, 5, 7, 9, 13, 14, 15). d(0, 2, 8)$.

Ans. Refer Q. 4.17.

Q. 6. $F(A, B, C, D, E) = \Sigma m(0, 1, 2, 4, 5, 6, 10, 13, 14, 18, 21, 22, 24, 26, 29, 30)$. Simplify the function with help of K-map and realize the simplified function using basic logic gates.

Ans. Refer Q. 4.20.



Fundamentals of Communication Engineering

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PART - 1

Fundamentals of Communication Engineering : Basics of Signal Representation and Analysis.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 5.1. What do you understand by signal? Define various types of signals with suitable examples.

Answer

A. Signal : A signal is defined as a physical quantity that varies with time, space or any other independent variable. The representation of a signal by mathematical expression is known as signal modeling.

B. Types of signals :

i. **Deterministic and Random Signals :**

1. Deterministic signals can be completely specified in time.
2. The pattern of this signal is regular and can be characterized mathematically. So, its future value at any instant can be determined easily. For example, $y(t) = b \sin(\pi t)$, $y(t) = ax(t)$.
3. Random signals take random values at any given time.
4. The pattern of this signal is irregular and it cannot be defined mathematically.
5. So, future value of the signals at any instant cannot be predicted. For example : Noise.

ii. **Even and Odd Signals :**

A signal $x(t)$ or $x[n]$ is referred to as symmetric or even signal if,

$$x(-t) = x(t) \text{ or } x[-n] = x[n]$$

and referred to as non-symmetric or odd signal if

$$x(-t) = -x(t) \text{ or } x[-n] = -x[n]$$

iii. **Energy and Power Signals :**

a. **Power signal :** A power signal is defined as a signal having finite average power and infinite energy i.e., $0 < P < \infty$ and $E = \infty$.

b. **Energy signal :** The energy signal is one that has a finite energy and zero average power i.e., $0 < E < \infty$ and $P = 0$.

Que 5.2. Sketch and explain the basic signals used as building blocks for the modeling of more complex signals.

Answer**Building blocks :****1. Unit Step Function :**

If a step function has unity magnitude then it is called unit step function

$$\begin{aligned} u(t) &= 1 \text{ for } t \geq 0 \\ &= 0 \text{ for } t < 0 \end{aligned}$$

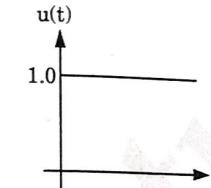


Fig. 5.2.1.

2. Unit Ramp Function :

It is defined as

$$\begin{aligned} r(t) &= t \text{ for } t \geq 0 \\ &= 0 \text{ for } t < 0 \end{aligned}$$

or

$$r(t) = t u(t)$$

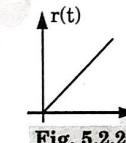


Fig. 5.2.2.

3. Unit Parabolic Function :

It is given by

$$\begin{aligned} p(t) &= \frac{t^2}{2} \text{ for } t \geq 0 \\ &= 0 \text{ for } t < 0 \end{aligned}$$

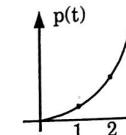


Fig. 5.2.3.

4. Impulse Function :

It is defined as

$$\int_{-\infty}^{\infty} \delta(t) dt = 1$$

and

$$\delta(t) = 0 \text{ for } t \neq 0$$

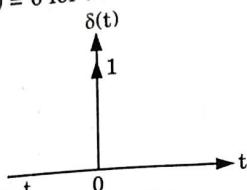


Fig. 5.2.4.

5. Rectangular Pulse Function :

It is defined as

$$\pi(t) = \begin{cases} 1 & \text{for } |t| < 1/2 \\ 0 & \text{otherwise} \end{cases}$$

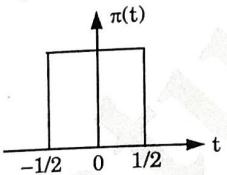


Fig. 5.2.5.

6. Triangular Pulse Function :

It is defined as

$$\Delta_a(t) = \begin{cases} 1 - \frac{|t|}{a}, & |t| \leq a \\ 0, & |t| > a \end{cases}$$

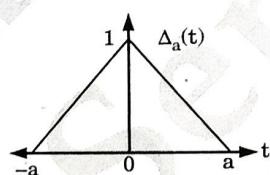


Fig. 5.2.6.

7. Signum Function :

It is defined as

$$\operatorname{sgn}(t) = \begin{cases} 1 & t > 0 \\ -1 & t < 0 \end{cases}$$

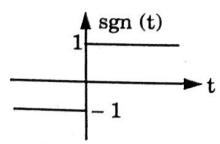


Fig. 5.2.7.

Que 5.3. How can we represent a signal with different ways ? Show at least four ways to represent a discrete time signal.

Answer

There are different types of representation for discrete time signals.

i. Graphical representation :

Let a signal $x[n]$ with values $x[-1] = 1, x[0] = 2, x[1] = 2, x[2] = 0$ and $x[3] = 1.5$, it can be shown as

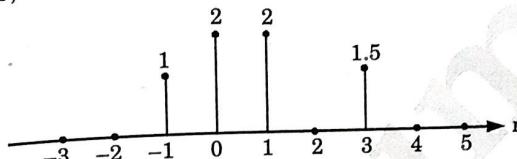


Fig. 5.3.1.

ii. Fundamental representation :

The discrete time signal shown in Fig. 5.3.1 can be represented using functional form as.

$$x[n] = \begin{cases} 1 & \text{for } n = -1 \\ 2 & \text{for } n = 0, 1 \\ 0 & \text{for } n = 2 \\ 1.5 & \text{for } n = 3 \\ 0 & \text{otherwise} \end{cases}$$

iii. Tabular representation :

In tabular term, it can be represented as

n	-1	0	1	2	3
x(n)	1	2	2	0	1.5

iv. Sequence representation :

1. A finite duration sequence with time origin ($n = 0$) indicated by the symbol ↑ is represented as,
 $x[n] = \{1, 2, 2, 0, 1.5\}$
2. A finite duration sequence can be represented as,
 $x[n] = \{\dots 0.2, 1, -1, 3, 2, \dots\}$
3. A finite duration sequence that satisfies the condition $x[n] = 0$, for $n < 0$ can be represented as,
 $x[n] = \{2, 4, 6, 8, -3\}$

PART-2

Electromagnetic Spectrum, Elements of a Communication System, Need of Modulation and Typical Applications.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 5.4. Explain the applications of electromagnetic spectrum. Also classify it further for Radio and Optical spectrum respectively.

Answer

Electromagnetic spectrum is the orderly distribution of electromagnetic radiations in accordance with their wavelength or frequency. It is classified as :

i. Radio waves :

1. These were discovered by Hertz in 1887.
2. The electromagnetic waves with the lowest frequencies and longest wavelengths are Radio waves.
3. Their frequencies may be as low as 10 Hz and their wavelengths can go upto millions of meters long.
4. Therefore, radio waves can be of extremely high frequency (EHF), super high frequency (SHF), ultra high frequency (UHF), very high frequency (VHF), high frequency (HF), medium frequency (MF), low frequency (LF), very low frequency (VLF), and extremely low frequency (ELF).
5. Surface wave EHF and SHF are used for radar and space communication.
6. UHF and VHF are used in TV transmission and line of sight communication.
7. Sky wave HF and ground wave MF have applications in radio communication.
8. Surface wave LF and VLF are also used in radio navigation and ELF has application in sub-surface communication.

ii. Microwaves :

1. Radio waves with wavelengths ranging from a few tenths to about one thousandth of a meter are known as Microwaves.
2. These are produced by specially designed oscillators.
3. This is also for radar and TV communications.

iii. Infrared (IR) :

1. Infrared frequencies are intermediate between those of microwaves and red visible light.
2. We sense infrared light as heat.

3. Infrared radiation can affect photographic plate coated with special chemicals.

iv. Visible light waves :

1. The next band of frequencies in the electromagnetic spectrum is visible light.
2. Visible light occupies only a small part of this spectrum and it produces the sensation of vision.
3. White light is composed of a mixture of many different wavelengths each of which can be seen on its own by the human eye as a colour.
4. It consists of different colours, they are violet, blue, green, yellow, orange, red.
5. When ordinary white light is passed through a prism, it is separated into the rainbow of colours known as visible spectrum.

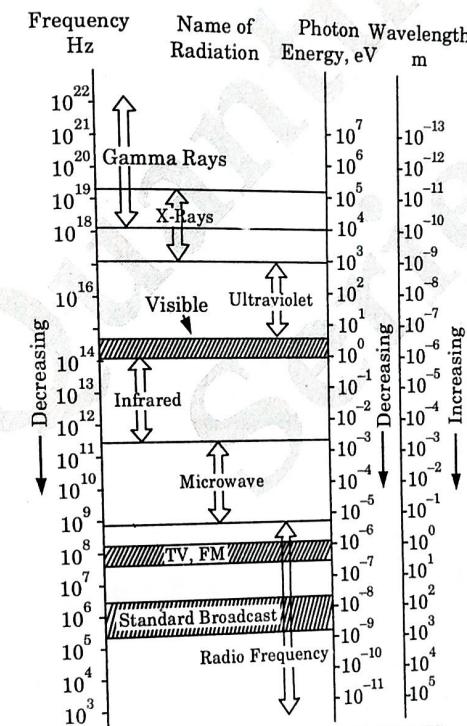
v. Ultraviolet light (UV) :

Fig. 5.4.1. Electromagnetic spectrum.

- Just above visible light in the electromagnetic spectrum is ultraviolet light (UV).
- This invisible light can be detected by photographic plate.
- Ultraviolet radiation is very useful in medical science as it is producing chemical effect on our body.

vii. X-rays :

- Frequencies higher than UV are X-ray.
- This radiation was discovered by Rontgen in 1895.
- These rays find several applications in medical science and industry.

viii. Gamma ray (γ) :

- Frequencies higher than X-rays are Gamma rays.
- These rays can affect photographic plates and cause ionization.
- The sources of gamma rays are nuclear transitions involving decays.
- X-rays are produced through electronic transitions deep in the electronic structure of the atom.
- Also ultraviolet (UV) waves, visible radiation and infrared (IR) radiation result from electronic transitions of different energy ranges.
- Microwaves and radio waves are produced by various types of electronic oscillations.

Que 5.5. Explain with the help of block diagram the elements of communication systems.

Answer

- A modern communication system is first concerned with the processing and storing of information before its transmission.
- The basic communication system consists of transmitter, channel and receiver. The input and output of communication system comes from information source and destination respectively.

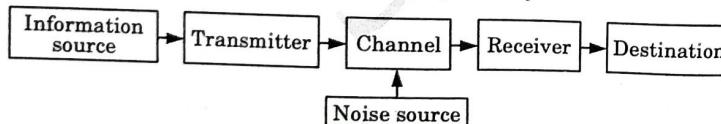


Fig. 5.5.1. Block diagram of basic communication system.

i. Information source :

- The communication system exists to convey a message. This message comes from the information source.
- Information may be words, groups of words, code symbols or any prearranged units.

- The amount of information contained in any given message can be measured in bits or dits.

$$\text{Information} = \log_2 \left(\frac{1}{P_i} \right) \text{ bits}$$

$$= \log_{10} \left(\frac{1}{P_i} \right) \text{ dits}$$

where P_i is the probability of occurrence. It must be realized that no real information is conveyed by a redundant message.

- Transmitter :** In transmitter the message from information source is superimposed on some high frequency wave with certain rule to have a coded form of the original message. This process is known as modulation.

iii. Channel :

- Channels are the medium to transmit information from source to destination.
- It should be noted that the term channel is often used to refer to the frequency range allocated to a particular service or transmission, such as a television channel.
- Noise may interfere with signal at any point in the communication system, but it will have its greatest effect when signal is weakest. It means the noise in the channel or at the input to the receiver is the most noticeable.

iv. Receiver :

- Receiver does the opposite process that of transmitter.
- Here demodulation of the wave coming from the receiver through channel is done to get original information.
- The output of receiver may be fed to a loudspeaker or video display.

Que 5.6. Discuss the need of modulation in the communication engineering. Which types of modulations are used in television ?

AKTU 2016-17(Sem-II), Marks 5.25

Answer**A. Need of modulation :**

Modulation is needed in communication system to achieve some basic needs :

i. Multiplexing :

- Simultaneous transmission of multiple messages over a channel is known as multiplexing.

2. If transmitted without modulation, the different message signals over a single channel will interfere with one another.
3. Different message signals can be transmitted over a single channel without interference using multiplexing technique.

ii. Practicability of Antennas :

1. The antenna radiates effectively when its height is of the order of the wavelength of the signal being transmitted.
2. In broadcast system the maximum audio frequency transmitted from a radio station is of the order of 5 kHz.
3. The height of antenna

$$= \frac{\lambda}{2} = \frac{c}{2f} = \frac{3 \times 10^8}{2 \times 5 \times 10^3} = 30,000 \text{ m} = 30 \text{ km}$$

Practically, such height of antenna is not possible.

4. Therefore, modulation is used by which frequency increases and thus, height of antenna decreases.
- B.** Television systems use vestigial sideband modulation, a form of amplitude modulation in which one sideband is partially removed. This reduces the bandwidth of the transmitted signal, enabling narrower channels to be used.

PART-3

Fundamental of Amplitude Modulation and Demodulation Techniques.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.7. Define the term modulation and demodulation. Also classify the modulation.

Answer

A. Modulation :

1. Modulation is defined as the process by which some characteristic of a signal called carrier is varied in accordance with the instantaneous value of baseband or modulating signal.
2. The signal resulting from the process of modulation is called modulated signal.

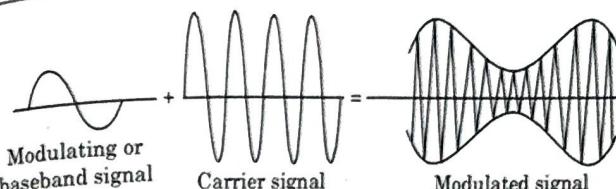
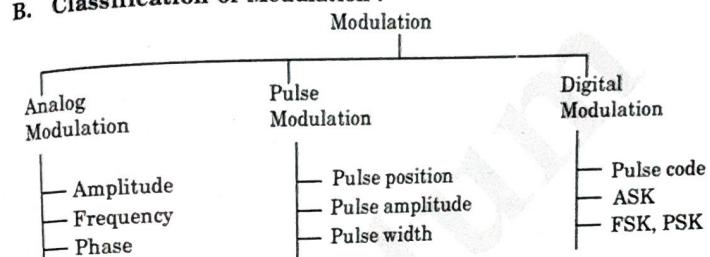


Fig. 5.7.1. Process of Modulation.

B. Classification of Modulation :



C. Demodulation :

1. The receiver recreates the original message signal from a degraded version of transmitted signal after propagation through the channel.
2. This recreation is accomplished by using a process called demodulation.

Que 5.8. Define Amplitude Modulation. Derive an expression for amplitude modulated wave.

AKTU 2017-18(Sem-II), Marks 3.5

OR

Define amplitude modulation. Derive the expression for AM modulated waveform. Define modulation index of AM.

AKTU 2016-17(Sem-I), Marks 10

AKTU 2017-18(Sem-I), Marks 07

OR

What do you mean by amplitude modulation ? Explain with help of proper waveforms.

AKTU 2020-21 (Sem-I), Marks 05

Answer

1. Amplitude Modulation (AM) is defined as a system of modulation in which the amplitude of the carrier is made proportional to the instantaneous amplitude of the modulating voltage keeping frequency of the carrier constant.
2. Baseband or modulating signal is generally low frequency audio signal and carrier is high frequency RF-signal.

3. Let the carrier voltage (v_c) and modulating voltage (v_m) respectively given as :

$$v_c = V_c \sin \omega_c t \quad \dots(5.8.1)$$

$$v_m = V_m \sin \omega_m t \quad \dots(5.8.2)$$

where V_c is the maximum amplitude of carrier wave and V_m is the maximum amplitude of modulating wave.

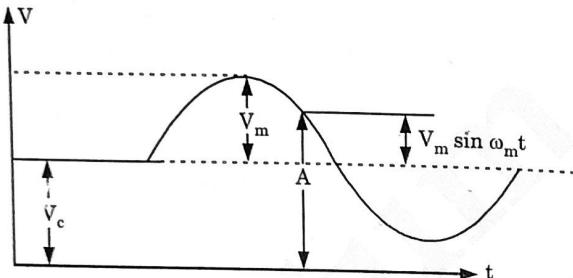


Fig. 5.8.1.

4. From the Fig. 5.8.1, it is clear that amplitude of AM wave A is given as :

$$A = V_c + v_m \quad \dots(5.8.3)$$

From eq. (5.8.2), we have

$$A = V_c + V_m \sin \omega_m t$$

$$A = V_c \left[1 + \frac{V_m}{V_c} \sin \omega_m t \right] \quad \dots(5.8.4)$$

5. The ratio V_m/V_c is known as modulation index (m_a).
6. The modulation index is a number lying between 0 and 1, and it is often expressed as a percentage and called the percentage modulation.
7. So, from eq. (5.8.4), we have amplitude of amplitude modulated wave

$$A = V_c (1 + m_a \sin \omega_m t) \quad \dots(5.8.5)$$

8. So the instantaneous voltage of amplitude modulated wave is given as :

$$V_{AM} = A \sin \omega_c t \quad (\text{since frequency is constant})$$

9. From eq. (5.8.5), we have

$$V_{AM} = V_c (1 + m_a \sin \omega_m t) \sin \omega_c t \quad \dots(5.8.6)$$

This is the complete equation of AM-wave.

10. Now expanding eq. (5.8.6) we have

$$V_{AM} = V_c \sin \omega_c t + \frac{m_a V_c}{2} (2 \sin \omega_m t \sin \omega_c t)$$

$$V_{AM} = \underbrace{V_c \sin \omega_c t}_{\text{Carrier}} + \underbrace{\frac{m_a V_c}{2} \cos(\omega_c - \omega_m)t}_{\text{LSB}} - \underbrace{\frac{m_a V_c}{2} \cos(\omega_c + \omega_m)t}_{\text{USB}}$$

11. Amplitude modulated wave consists of unmodulated carrier and two sidebands LSB and USB.

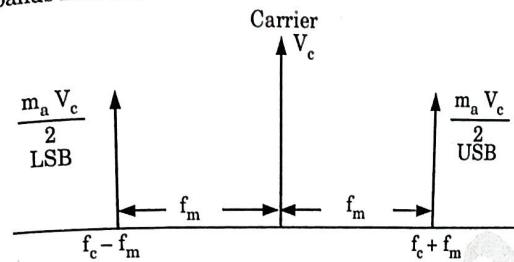


Fig. 5.8.2. Frequency spectrum of AM-wave.

- Que 5.9.** Describe AM modulation and demodulation technique with adequate diagram. AKTU 2021-22 (Sem-I), Marks 10

Answer

- A. **AM modulation :** Refer Q. 5.8, Page 5-11J, Unit-5.
B. **AM demodulation technique :**
- Demodulation is the process by which the original information bearing signal, i.e., the modulation is extracted from the incoming overall received signal.
 - In the demodulation process the audio or other signal carried by amplitude variations on the carrier is extracted from the overall signal to appear at the output.
 - As the most common use for amplitude modulation is for audio applications, the most common output is the audio.
 - There are a number of techniques that can be used to demodulate AM signals. Different types are used in different applications to suit their performance and cost.
- Diode rectifier envelope detector :**
- This form of detector is the simplest form, only requiring a single diode and a couple of other low cost components.

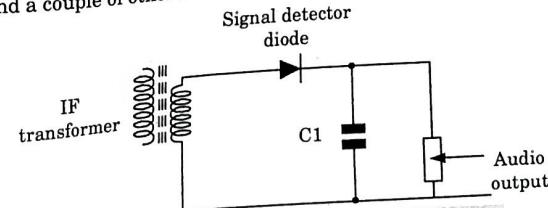


Fig. 5.9.1. Circuit of an envelope detector as used in an AM radio receiver.

2. The performance is adequate for low cost AM broadcast radios.
3. It has a high level of distortion, and performs badly under conditions of selective fading such as those experienced on the medium and short wave bands.

4. The signal diode detector consists of two main elements to the circuit :

A. Diode / rectifier :

- i. The diode in the detector serves to that enhances one half of the received signal over the other.
- ii. In many instances Schottky diodes are used for this form of detector, because signal levels may be low, and Schottky diodes have a much lower turn on voltage than standard silicon diodes.

B. Low pass filter :

- i. The low pass filter is required to remove the high frequency elements that remain within the signal after detection / demodulation.
- ii. The filter usually consists of a very simple RC network.
- iii. Since the capacitor in the circuit stores the voltage, the output voltage reflects the peak of the waveform. Sometimes these circuits are used as peak detectors.

Que 5.10. Define modulation. Derive the relation of total power of AM waves.

AKTU 2015-16 (Sem-I), Marks 05

Answer

- A. Modulation :** Refer Q. 5.7, Page 5-10J, Unit-5.
B. Power of AM waves :

1. We can write AM-wave equation as below :

$$v = \underbrace{V_c \sin \omega_c t}_{\text{Carrier}} + \underbrace{\frac{mV_c}{2} \cos(\omega_c - \omega_m)t}_{\text{LSB}} - \underbrace{\frac{mV_c}{2} \cos(\omega_c + \omega_m)t}_{\text{USB}} \quad \dots(5.10.1)$$

2. The total power in modulated wave,

$P_t = \text{Power in carrier} + \text{Power in two sidebands}$

3. The different power can be written as

$$P_c = \frac{\left(\frac{V_c}{\sqrt{2}}\right)^2}{R} = \frac{V_c^2}{2R} \quad \dots(5.10.3)$$

$$P_{\text{LSB}} = P_{\text{USB}} = \frac{V_{\text{SB}}^2}{R} = \frac{\left(\frac{mV_c}{2\sqrt{2}}\right)^2}{R} = \frac{m^2 V_c^2}{8R}$$

$$P_{\text{LSB}} = P_{\text{USB}} = \frac{m^2}{4} \left(\frac{V_c^2}{2R} \right) \quad \dots(5.10.4)$$

where R is resistance.

Now from eq. (5.10.2), (5.10.3) and (5.10.4),

$$P_t = \left(\frac{V_c^2}{2R} \right) + \frac{m^2}{4} \left(\frac{V_c^2}{2R} \right) + \frac{m^2}{4} \left(\frac{V_c^2}{2R} \right)$$

$$P_t = \frac{V_c^2}{2R} \left(1 + \frac{m^2}{4} + \frac{m^2}{4} \right) c$$

$$P_t = \frac{V_c^2}{2R} \left(1 + \frac{m^2}{2} \right)$$

We know that

$$P_c = \frac{V_c^2}{2R}$$

$$P_t = P_c \left(1 + \frac{m^2}{2} \right)$$

where P_c is unmodulated carrier power and m is modulation index in AM.

Que 5.11. Explain Amplitude modulation. Derive the expression for the total power radiated by the modulated signal. Also calculate modulation efficiency.

AKTU 2021-22 (Sem-II), Marks 10

Answer

- A. Amplitude modulation :** Refer Q. 5.8, Page 5-11J-Unit-5.
B. Expression : Refer Q. 5.10, Page 5-14J Unit-5.
1. Modulation efficiency or transmission efficiency of an Am wave is ratio of transmitted power which contains the information (i.e., the total sideband power) to the total transmitted power.

$$\eta = \frac{P_{\text{LSB}} + P_{\text{USB}}}{P_t} = \frac{\left[\frac{m^2}{4} P_c + \frac{m^2}{4} P_c \right]}{\left[1 + \frac{m^2}{2} \right] P_c}$$

$$\eta = \frac{\frac{m^2}{2}}{1 + \frac{m^2}{2}} = \frac{m^2}{2 + m^2}$$

$$\eta = \frac{m^2}{2 + m^2} \times 100 \%$$

Que 5.12. Explain DSB-SC modulation and demodulator.

OR

Explain Double Sideband Suppressed Carrier (DSB-SC) Techniques.

AKTU 2017-18(Sem-II), Marks 3.5

Answer

A. DSB-SC Modulator :

1. A DSB-SC modulator can be designed by using a mixer that generates the sidebands as well as carrier signal and the baseband message signal. For DSB-SC modulator only the base band message is to be filtered out.
2. Let us consider a simple switching modulator circuit with only one diode.

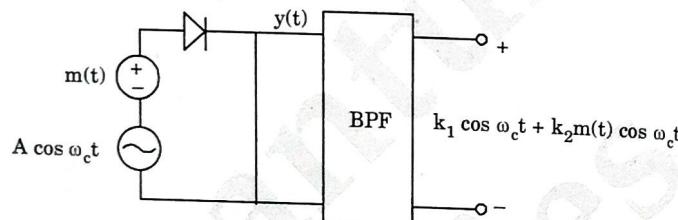


Fig. 5.12.1. An AM (DSB-SC) modulator.

3. The BPF passes frequency $\omega_c \pm \omega_m$ where ω_m is maximum frequency of message signal, carrier is represented by $A \cos \omega_c t$.
4. The switching action can be approximated by a pulse train as

$$s(t) = \frac{1}{2} + \frac{2}{\pi} \left[\cos \omega_c t - \frac{1}{3} \cos 3\omega_c t + \frac{1}{5} \cos 5\omega_c t - \frac{1}{7} \cos 7\omega_c t + \dots \right] \quad (5.12.1)$$

5. Now the combined signal message $m(t) + A \cos \omega_c t$ will appear at the output when the diode is switched ON and otherwise not.

$$\begin{aligned} y(t) &= [m(t) + A \cos \omega_c t] s(t) \\ &= [m(t) + A \cos \omega_c t] \\ &\quad \left[\frac{1}{2} + \frac{2}{\pi} \left(\cos \omega_c t - \frac{1}{3} \cos 3\omega_c t + \frac{1}{5} \cos 5\omega_c t - \frac{1}{7} \cos 7\omega_c t + \dots \right) \right] \end{aligned}$$

$$y(t) = \frac{m(t)}{2} + \frac{A}{2} \cos \omega_c t + \frac{2}{\pi} m(t) \cos \omega_c t + \frac{2A}{\pi} \cos^2 \omega_c t + \dots$$

6. The BPF passes $\omega_c \pm \omega_m$ and bring out $\frac{2}{\pi} m(t) \cos \omega_c t$ and the carrier component $\frac{A}{2} \cos \omega_c t$ which clearly is an AM or DSB-SC signal.

B. DSB-SC Demodulator :

1. Envelope detector can be used to detect the original message signal from the modulated signal.
2. This detector uses linear characteristics of diode.
3. In the circuit, C is a small capacitance and R is large resistance.
4. The parallel combination of R and C is the load resistance across which the rectified output voltage V_0 is developed.
5. At each positive peak of the RF cycle, C charges up to a potential almost equal to the peak signal voltage.

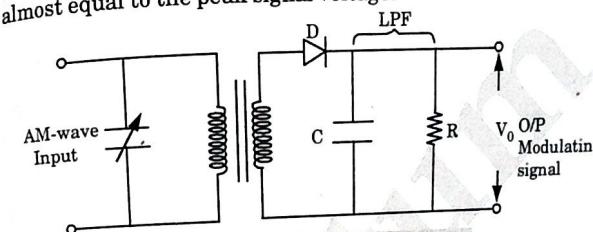


Fig. 5.12.2. Envelope detector.

6. The output voltage developed across R is replica of modulating signal with some ripples.

$$V_0 = A_c (1 + m_a \cos \omega_m t)$$

$$\frac{1}{RC} \geq m_a \omega_m$$

This is the condition for satisfactory detection of AM-wave.

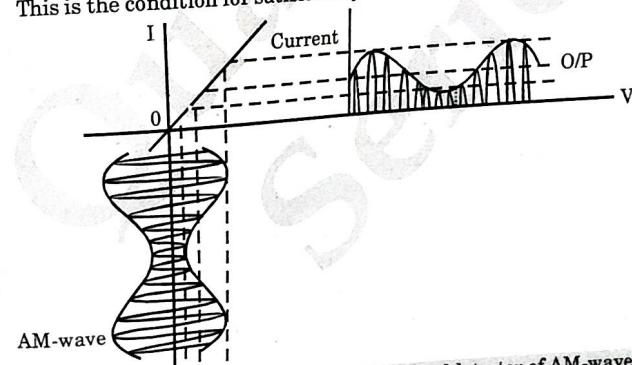


Fig. 5.12.3. Waveform representation of detector of AM-wave.

- Que 5.13.** A certain AM transmitter radiates 9 kW with the carrier unmodulated and 10.125 kW when the carrier is modulated. Calculate the modulation index. If another sine wave is simultaneously transmitted with the modulation index 0.4, determine the total radiated power.

AKTU 2017-18(Sem-I), Marks 07

Answer

Given : $P_C = 9 \text{ kW}$, $P_t = 10.125 \text{ kW}$, Modulation index, $m_2 = 0.4$
 To Find : Modulation index, total radiated power.

1. We know,

$$P_t = P_C \left[\frac{m^2}{2} + 1 \right]$$

$$\frac{m^2}{2} = \frac{P_t}{P_C} - 1 = \frac{10.125}{9} - 1 = 0.125$$

$$m^2 = 0.25$$

$$m = 0.5$$

2. Now, another sine wave is simultaneously transmitted with modulated index 0.4 with first sine wave of modulated index 0.5, therefore resultant modulated index,

$$m_t = \sqrt{m_1^2 + m_2^2}$$

$$\Rightarrow m_t = \sqrt{0.5^2 + 0.4^2} = 0.64$$

3. $\therefore P_t = P_C \left[1 + \frac{m_t^2}{2} \right] = 9 \left[1 + \frac{0.64^2}{2} \right] = 10.84 \text{ kW}$

Que 5.14. Draw the block diagram of communication system. Calculate the percentage power saving when one side band and carrier is suppressed in an AM signal with modulation index equal to 1.

AKTU 2017-18(Sem-I), Marks 07

Answer

A. Block diagram of communication system : Refer Q. 5.5, Page 5-8J, Unit-5.

B. Numerical :

Given : $m = 100\% = 1$
 To Find : Percentage power saving

1. We have,

$$P_T = P_C + \frac{m^2 P_C}{4} + \frac{m^2 P_C}{4} = P_C + \frac{P_C}{4} + \frac{P_C}{4}$$

$$= \frac{3}{2} P_C = 1.5 P_C$$

2. When carrier and one sideband are suppressed

$$P_T = P_{USB} = \frac{P_C}{4}$$

3. Power saved = $P_C + \frac{P_C}{4} = \frac{5}{4} P_C = 1.25 P_C$

4. % of power saved = $\frac{1.25 P_C}{1.5 P_C} \times 100 = 83.33\%$

Que 5.15. A sinusoidal carrier of 1 MHz and amplitude 100 V is amplitude modulated by a sinusoidal modulating signal of frequency 5 kHz providing 50 % modulation. Calculate the frequency and amplitude of USB and LSB. AKTU 2017-18(Sem-II), Marks 3.5

Answer

Given : $f_c = 1 \text{ MHz}$, $V_a = 100 \text{ V}$, $f_m = 5 \text{ kHz}$, $m = 0.5$
 To Find : Amplitude and frequency of USB and LSB.

1. We have modulation index,

$$m = \frac{V_a}{V_c}$$

$$0.5 = \frac{100}{V_c}$$

$$V_c = 200 \text{ V}$$

2. Amplitude of USB and LSB is,

$$\frac{mV_c}{2} = \frac{0.5 \times 200}{2} = 50 \text{ V}$$

3. Frequency of LSB = $f_c - f_m = 1000 \text{ kHz} - 5 \text{ kHz}$
 $= 995 \text{ kHz}$

4. Frequency of USB = $f_c + f_m = 1000 \text{ kHz} + 5 \text{ kHz}$
 $= 1005 \text{ kHz}$

Que 5.16. An audio frequency signal $5 \sin(2\pi \times 500t)$ is used to amplitude modulate a carrier of $25 \sin(2\pi \times 10^5 t)$. Calculate :

- Modulation index
- Amplitude of Each side band
- Total power
- Bandwidth
- Transmission efficiency

AKTU 2021-22 (Sem-I), Marks 10

Answer

Given : $v_m = 5 \sin(2\pi \times 500t)$, $v_c = \sin(2\pi \times 10^5 t)$
 To Find : Modulation index, Amplitude of each side band, Total power, Bandwidth, Transmission efficiency.

1. Given, amplitude signal $v_m = 5 \sin(2\pi \times 500t)$... (5.16.1)

- So, $V_m = 5 \text{ V}, f_m = 500 \text{ Hz}$
2. Given, carrier signal, $v_c = 25 \sin(2\pi \times 10^5 t)$
- $$V_C = 25 \text{ V}, f_c = 10^5 \text{ Hz} \quad \dots(5.16.2)$$
3. Modulation index, $m = \frac{v_m}{v_c} = \frac{5}{25} = 0.2$
4. Amplitude of each side band,

$$V_{LSB} = V_{USB} = \frac{m V_c}{2} = \frac{0.2 \times 25}{2} = 2.5 \text{ V}$$

5. Total power, $P_t = P_c \left(1 + \frac{m^2}{2}\right)$

And $P_c = \frac{V_c^2}{2R} = \frac{(25)^2}{2 \times 1} \quad [\because \text{Assume } R = 1]$

$$P_c = \frac{625}{2} = 312.5 \text{ W}$$

$$\begin{aligned} P_t &= 312.5 \left(\frac{1 + (0.2)^2}{2} \right) \\ &= 312.5 \left(\frac{1 + 0.4}{2} \right) = 312.5 \times 1.02 \\ &= 318.75 \text{ W} \end{aligned}$$

6. Bandwidth, BW $= 2f_m = 2 \times 500 = 1000 \text{ Hz}$
 7. Transmission efficiency,

$$h = \frac{m^2}{2 + m^2} = \frac{(0.2)^2}{2 + (0.2)^2} = \frac{0.04}{2.04} = 0.019 = 1.9\%$$

Que 5.17. Why do we need modulation? The antenna current of an AM transmitter is 8 A when only the carrier is sent, but it increases to 8.93 A, when the carrier is modulated by a single sine wave. Find percentage modulation. Determine the antenna current when the percent of modulation changes to 0.8.

AKTU 2021-22 (Sem-II), Marks 10

Answer

- A. Need of modulation : Refer Q. 5.6, Page 5-9J, Unit-5.
 B. Numerical :
 As we know

$$I_t = I_c \sqrt{1 + \frac{m^2}{2}}$$

$$\left(\frac{I_t}{I_c} \right)^2 = 1 + \frac{m^2}{2}$$

$$\left(\frac{8.93}{8} \right)^2 = 1 + \frac{m^2}{2}$$

$$m = 0.70$$

Determine antenna current when $m = 0.8$

$$I_c = 8 \text{ A}$$

$$\begin{aligned} I_t &= I_c \sqrt{1 + \frac{m^2}{2}} = 8 \sqrt{1 + \frac{(0.8)^2}{2}} \\ &= 8 \sqrt{1 + \frac{0.64}{2}} = 9.19 \text{ A} \end{aligned}$$

Que 5.18. AM radio transmitter radiates 6 kW power when modulation percentage is 70%. Determine the carrier power.

AKTU 2020-21 (Sem-I), Marks 05

Answer

Given : $P_t = 6 \text{ kW}, m = 70\% = 0.7$

To find : Carrier power

$$\begin{aligned} \text{We know, } P_t &= P_c \left[\frac{m^2}{2} + 1 \right] \\ 6 &= P_c \left[\frac{0.7^2}{2} + 1 \right] \\ P_c &= \frac{6}{1.245} = 4.82 \text{ kW} \end{aligned}$$

Que 5.19. An Audio frequency signal $10 \sin 6\pi \times 400t$ is used to amplitude modulate a carrier of $25 \sin 4\pi \times 10^5 t$. Calculate

- Modulation Index
- Amplitude of each side band
- Total power delivered to the load of 2 kΩ
- Bandwidth
- Transmission efficiency

AKTU 2021-22 (Sem-II), Marks 10

Answer

$$m(t) = A_m \sin \omega_m t = A_m \sin 2\pi f_m t$$

$$m(t) = 10 \sin 6\pi \times 400t$$

$$\text{Given } A_m = 10 \text{ and } f_m = \frac{400 \times 6\pi}{2\pi} = 1200 \text{ Hz} = 1.2 \text{ kHz}$$

$$c(t) = 25 \sin 4\pi \times 10^5 t$$

$$A_C = 25 \text{ and } f_C = \frac{4\pi \times 10^5}{2\pi} = 2 \times 10^5 \text{ Hz} \\ = 200 \text{ kHz}$$

i. Modulation index

$$m = \frac{A_m}{A_c} = \frac{10}{25} = 0.4$$

$$\% m = 40 \%$$

ii. Amplitude of each side band = $A_{LSB} = A_{USB}$

$$A_{LSB} = A_{USB} = \frac{m A_c}{2} = \frac{0.4 \times 25}{2} = 5 \text{ V}$$

iii. Total power delivered to the load of $2 \text{ k}\Omega$

$$P_t = P_c \left[1 + \frac{m^2}{2} \right]$$

As

$$P_c = \frac{A_c^2}{2R} = \frac{(25)^2}{2 \times 2 \times 10^3} = 156.25 \times 10^{-3} \text{ W}$$

$$P_t = 156.25 \times 10^{-3} \left[1 + \frac{(0.4)^2}{2} \right]$$

$$P_t = 168.48 \times 10^{-3} \text{ W}$$

iv. Bandwidth of AM = $F_{USB} - F_{LSB}$

$$= f_c + f_m - f_c + f_m = 2f_m = 2 \times 1.2 \text{ kHz} = 2.4 \text{ kHz}$$

v. Transmission efficiency

$$\eta = \frac{m^2}{2 + m^2} \times 100 \\ = \frac{(0.4)^2}{2 + (0.4)^2} \times 100 = \frac{0.16}{2.16} \times 100 = 7.4 \%$$

Que 5.20. Compare Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM).

AKTU 2017-18(Sem-II), Marks 3.5

Answer

S.No.	AM	FM	PM
1.	Amplitude of carrier is varied according to amplitude of modulating signal.	Frequency of carrier is varied according to amplitude of modulating signal.	Phase of carrier is varied according to amplitude of modulating signal.
2.	Modulation index does not greater than 1.	Modulation index may be greater than 1.	Modulation index may be greater than 1.
3.	AM is most commonly used for transmitting information via a radio carrier wave.	FM is commonly used at VHF radio frequencies for high-fidelity broadcasts of music and speech.	Phase modulation is widely used for transmitting radio waves.

Que 5.21. If a FM wave is represented by the equation :

$$V = 8 \sin (6 \times 10^8 t + 3 \sin 2000t)$$

Calculate :

- Carrier frequency
- Modulating frequency
- Modulation index.

AKTU 2016-17(Sem-I), Marks 05

Answer

$$V = 8 \sin (6 \times 10^8 t + 3 \sin 2000t) \quad \dots(5.21.1)$$

1. Given,

$$V = 8 \sin (6 \times 10^8 t + 3 \sin 2000t) \quad \dots(5.21.1)$$

2. The equation of FM wave is given by

$$V = A \sin \left(\omega_c t + \frac{\Delta\omega}{\omega_m} \sin \omega_m t \right) \quad \dots(5.21.2)$$

3. Compare eq. (5.21.1) with eq. (5.21.2)

$$i. \text{ Carrier frequency} = \omega_c = 6 \times 10^8 \text{ rad/sec.}$$

$$ii. \text{ Modulating frequency} = \omega_m = 2000 \text{ rad/sec.}$$

$$iii. \text{ Modulation index} = \frac{\Delta\omega}{\omega_m} = 3$$

PART-4

Introduction to Wireless Communication : Overview of Wireless Communication Cellular Communication.

Questions-Answers**Long Answer Type and Medium Answer Type Questions**

Que 5.22. Explain the term evolution of mobile radio communication fundamentals.

Answer

1. In the year 1887 Heinrich Hertz proves existence of EM waves.
2. Gugliemo Marconi developed the world's first commercial radio service in 1897.
3. The first use of mobile radio in an automobile was in 1921. Early radio telephone systems were too bulky.
4. The key technological breakthrough came in 1935, when Edwin Armstrong introduced frequency modulation (FM) to improve radio broadcasting.
5. This technology reduced the required bulk of radio equipment and improved transmission quality.
6. In 1946, Bell telephone labs inaugurated the first mobile system for public. The system was known as mobile telephone service (MTS).
7. In 1965, Bell system introduced improved version of MTS known as improved mobile telephone service (IMTS), which was the first automatic mobile system and full duplex in nature.
8. The ability to provide wireless communication to an entire population was made possible by Bell laboratories with the development of cellular concept in 1960s and 1970s.
9. With the development of highly reliable, miniature, solid state radio frequency hardware in the 1970s, the wireless communication era was born.

Que 5.23. Draw and explain the general model for wireless digital communication link.

Answer

1. Fig. 5.23.1 provides a block diagram of a digital communications link.

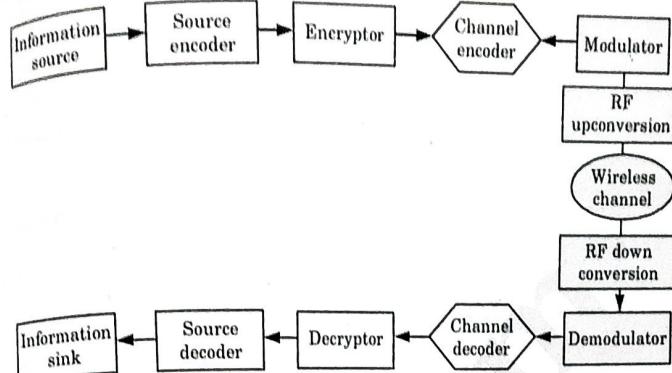


Fig. 5.23.1. Basic model of wireless digital communication link.

Source coding/decoding stage :

1. The first step is to convert a continuous analog signal into a discrete digital bit stream. This process is called digitization.
2. The next step is to add information coding for data compression.
3. The information to be transmitted from the source may be human-originated (speech) or machine-originated (data or image).
4. The source encoder with compression eliminates the inherent redundancy in the information (thus compressing) to maximize the transmission rate and the encrypter ensures secrecy of data.

Channel coding/decoding stage :

1. Data must be protected against perturbations introduced by the noisy channel, which could lead to misinterpretation of the transmitted message at the receiving end.
2. Line coding techniques are used for inserting systematic amplitude variations, power levels, and synchronization points, whereas channel coding techniques are used to insert structured sequences. Both techniques help in combating channel errors.

Modulator/demodulator stage :

1. The modulation method to be used should be selected based on the channel characteristics.
2. Corrections should take place before demodulation to reduce the probability of errors.
3. The modulator block generates a signal suitable for the transmission channel.
4. The block in the reverse path does the opposite of those in the forward path.

Intermediate frequency/radio frequency stage :

1. After the modulator, we have a typical RF or microwave transmitter.

2. The signal is converted up to an IF and then further upconverted to a higher RF. Any undesirable signal produced by the upconversion is filtered out.
3. Depending upon the requirements, the power amplifier is selected for amplifying the power to cover the required transmission distance.
4. The receiver RF section provides efficient coupling between the antenna and the rest of the hardware, which utilizes the energy abstracted from the radio wave.

PART-5

Cellular Communication, Different Generations and Standards in Cellular Communication Systems.

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.24. Explain cellular communication.

Answer

1. Cellular communication is a form of communication technology that enables the use of mobile phones.
2. A mobile phone is a bidirectional radio that enables simultaneous transmission and reception.
3. Cellular communication is based on the geographic division of the communication coverage area into cells, and within cells.
4. Each cell is allocated a given number of frequencies (or channels) that allow a large number of subscribers to conduct conversations simultaneously.
5. The common element of all generations of cellular communication technologies is the use of defined radiofrequencies (RF), as well as frequency reuse. This enables the provision of a service to a large number of subscribers while reducing the number of channels (band width).
6. It also enables the creation of wide communication networks by fully integrating the advanced capabilities of the mobile phone.

Que 5.25. What are the generations and standards in cellular communication system ? Explain each of them.

Answer

There are five generations and standards in cellular communication :

i. 1G-First Generation :

1. The very first generation of commercial cellular network was introduced in the late 70's with fully implemented standards being established throughout the 80's.
2. 1G is an analog technology and the phones generally had poor battery life and voice quality was large without much security, and would sometimes experience dropped calls.
3. These are the analog telecommunications standards that were introduced in the 1980s and continued until being replaced by 2G digital telecommunications. The maximum speed of 1G is 2.4 Kbps.

ii. 2G-Second Generation :

1. Cell phones received their first major upgrade when they went from 1G to 2G. The main difference between the two mobile telephone systems (1G and 2G), is that the radio signals used by 1G network are analog, while 2G networks are digital. This generation was to provide secure and reliable communication channel.
2. It implemented the concept of CDMA and GSM. Provided small data service like SMS and MMS.
3. Second generation 2G cellular telecom networks were commercially launched in 1991.
4. During 2G Cellular phones are used for data also along with voice. The advance in technology from 1G to 2G introduced many of the fundamental services are :
 - SMS
 - Internal roaming
 - Conference calls
 - Call hold
 - Billing based on services
5. The maximum speed of 2G with General Packet Radio Service (GPRS) is 50 Kbps or 1 Mbps with Enhanced Data Rates for GSM Evolution (EDGE).

iii. 3G-Third Generation :

1. This generation set the standards for most of the wireless technology such as, Web browsing, email, video downloading, picture sharing and other smartphone technology.
2. The goals for third generation mobile communication were to facilitate greater voice and data capacity, support a wider range of applications, and increase data transmission at a lower cost.

3. 3G has Multimedia services support along with streaming are more popular. In 3G, Universal access and portability across different device types are made possible (Telephones, PDA's, etc.).
4. 3G increased the efficiency of frequency spectrum by improving how audio is compressed during a call, so more simultaneous calls can happen in the same frequency range.
5. 3G technology is capable of allowing internet speeds that can reach 7 Mbps, but this speed is unrealistic and is often approximately 2 to 3 Mbps.

iv. 4G-Fourth Generation :

1. 4G is a very different technology as compared to 3G and was made possible practically only because of the advancements in the technology in the last 10 years.
2. Its purpose is to provide high speed, high quality and high capacity to users while improving security and lower the cost of voice and data services, multimedia and internet over IP.
3. Potential and current applications include :
 - Mobile web access
 - IP telephony
 - Gaming services
 - High-definition mobile TV
 - Video conferencing
 - 3D television.
 - Cloud computing
4. The development of 4G technology provided two main benefits, increased upload and download speeds and reduced latency.
5. 4G technology is approximately five times (and sometimes more) faster than 3G technology. This meant that the speed at which files could be downloaded was significantly increased. This significantly improved the experience of mobile devices and internet usage for the user.

v. 5G-Fifth Generation :

1. 5G is a generation currently under development, that's intended to improve on 4G. 5G promises significantly faster data rates, higher connection density, much lower latency, among other improvements.
2. Some of the plans for 5G include device-to-device communication, better battery consumption, and improved overall wireless coverage.
3. 5G technology is set to dramatically affect the use of mobile internet. In order to provide 5G access there is a major restructure occurring on parts of the radio network that is used to transmit data. This restructure is reported to allow data to be transmitted approximately 100 times faster.

4. The development from 3G to 4G technology and further developments into 5G technology will enable a number of advancements. These may include :
 - Greater speed in internet access
 - Faster loading speeds of applications, such as maps
 - The ability to have multiple people in video conferencing calls
 - More effective location services to allow for real-time updates, such as traffic and weather
 - The ability to stream high-definition (HD).

Que 5.26. | Compare 1G, 2G, 3G, 4G and 5G standards.

Answer

Features	1G	2G	3G	4G	5G
Technology	AMPS, NMT, TACS	GSM	WCDMA	LTE, WiMax	MIMO, MM waves
Frequency	30 KHz	1.8 GHz	1.6-2 GHz	2-8 GHz	3-30 GHz
Bandwidth	2 kbps	14.4-62 kbps	2 Mbps	2000 Mbps to 1 Gbps	1 Gbps and higher
Access System	FDMA	TDMA/CDMA	CDMA	CDMA	OFDM/BDMA
Core Network	PSTN	PSTN	Packet Network	Internet	Internet

PART-6

Questions-Answers

Long Answer Type and Medium Answer Type Questions

Que 5.27. | Describe briefly satellite communication.

AKTU 2021-22 (Sem-I), Marks 05

OR

Write a short note on satellite communication system.

AKTU 2020-21 (Sem-I), Marks 05

OR

Write short note on basic elements of communication system.

AKTU 2021-22 (Sem-I), Marks 05

Answer

1. The basic elements of satellite communication are users, earth station transmitter, satellite and earth station receivers.
2. Fig. 5.27.1 shows the basic block diagram of the satellite communication system. It consists of many earth stations on the ground and these stations are linked with a satellite in space.

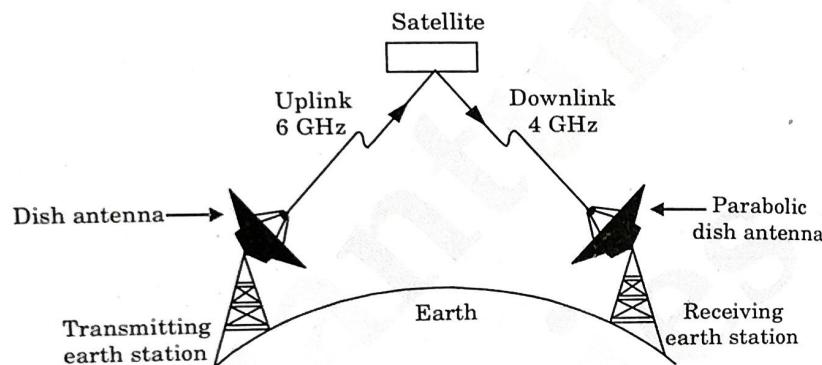


Fig. 5.27.1. Basic element of satellite communication system.

3. The user is connected to the earth station through a terrestrial network, and this network may be a telephone switch or dedicated link to an earth station.
4. The user generates a baseband signal that gets processed through the terrestrial network and transmitted to a satellite by the earth station.
5. The satellite consists of a large number of repeaters, that receives the modulated radio frequency carrier in its uplink frequency spectrum from all the earth stations in the network, amplifies these carriers, then retransmits them back to the earth station in the downlink frequency spectrum.
6. To avoid the interference, downlink and uplink frequency spectrum should have different frequencies.
7. The signal at the receiving earth station is processed to get back the base band signal; then it is sent to the user through a terrestrial network.

Que 5.28. Explain the block diagram of radar.

Answer

1. The block diagram of radar is shown in Fig. 5.28.1. In the block diagram the radar signal is produced at low power by a waveform generator, which is the input of power amplifier which acts as a transmitter.
2. When a power oscillator is used, it is also turned on and off by a pulse modulator to generate a pulse waveform.
3. The output of the transmitter is delivered to the antenna by a waveguide or transmission line.

i. Duplexer:

1. It allows a single antenna to be used for both transmitting and receiving.
2. It is generally a gaseous device that produces a short circuit at the input to the receiver when the transmitter is operating, so that high power flows to the antenna and not to the receiver.
3. On reception, the duplexer directs the echo signal to the receiver and not to the transmitter.

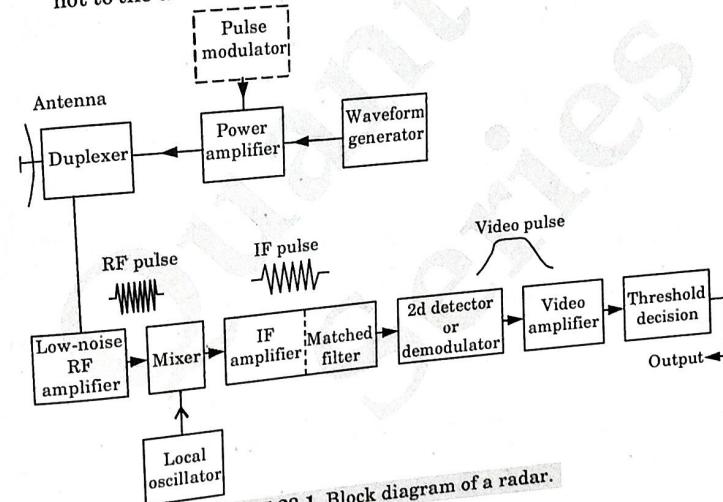


Fig. 5.28.1. Block diagram of a radar.

ii. Receiver:

1. It is always superheterodyne. The input or RF stage can be a low noise transistor amplifier.
2. The mixer or local oscillator (LO) convert the RF signal to an intermediate frequency (IF) where it is amplified by the IF amplifier.
3. The IF amplifier is designed as a matched filter, which maximizes the output peak-signal-to-mean-noise ratio.

4. Thus, the matched filter maximizes the detectability of weak echo signals and attenuated unwanted signals.

iii. 2d detector or demodulator :

1. Its purpose is to assist in extracting the signal modulation from the carrier.
2. The combination of IF amplifier, second detector and video amplifier acts as an envelope detector to pass the pulse modulation and reject the carrier frequency.
3. At the output of the receiver a decision is made whether a target is present or not.
4. The decision is based on the magnitude of the receiver output.
5. If the output is larger than the threshold level then target is present. If it does not cross the threshold, noise is present.

VERY IMPORTANT QUESTIONS

Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.

- Q. 1. What do you understand by signal ? Define various types of signals with suitable examples.**

Ans. Refer Q. 5.1.

- Q. 2. Discuss the need of modulation in the communication engineering. Which types of modulations are used in television ?**

Ans. Refer Q. 5.6.

- Q. 3. Define Amplitude Modulation. Derive an expression for amplitude modulated wave.**

Ans. Refer Q. 5.8.

- Q. 4. Explain Amplitude modulation. Derive the expression for the total power radiated by the modulated signal. Also calculate modulation efficiency.**

Ans. Refer Q. 5.11.

- Q. 5. A sinusoidal carrier of 1 MHz and amplitude 100 V is amplitude modulated by a sinusoidal modulating signal of frequency 5 kHz providing 50 % modulation. Calculate the frequency and amplitude of USB and LSB.**

Ans. Refer Q. 5.15.

- Q. 6. What are the generations and standards in cellular communication system ? Explain each of them.**

Ans. Refer Q. 5.25.

- Q. 7. Describe briefly satellite communication.**

Ans. Refer Q. 5.27.

