

LFSR (Linear Feedback Shift Register)

➤ Aim:

To design a circuit as well as Verilog code for a LFSR (linear feedback shift register) and observe the behavior of its output.

➤ Hardware and Software used:

1. Altera Quartus II
2. FPGA board (DE-1)

➤ Theory:

In computing, a linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value.

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits that appears random and has a very long cycle.

Applications of LFSRs include generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. Both hardware and software implementations of LFSRs are common.

The mathematics of a cyclic redundancy check, used to provide a quick check against transmission errors, are closely related to those of an LFSR.

➤ **Verilog Code:**

```
module lfsr (out, clk, rst);

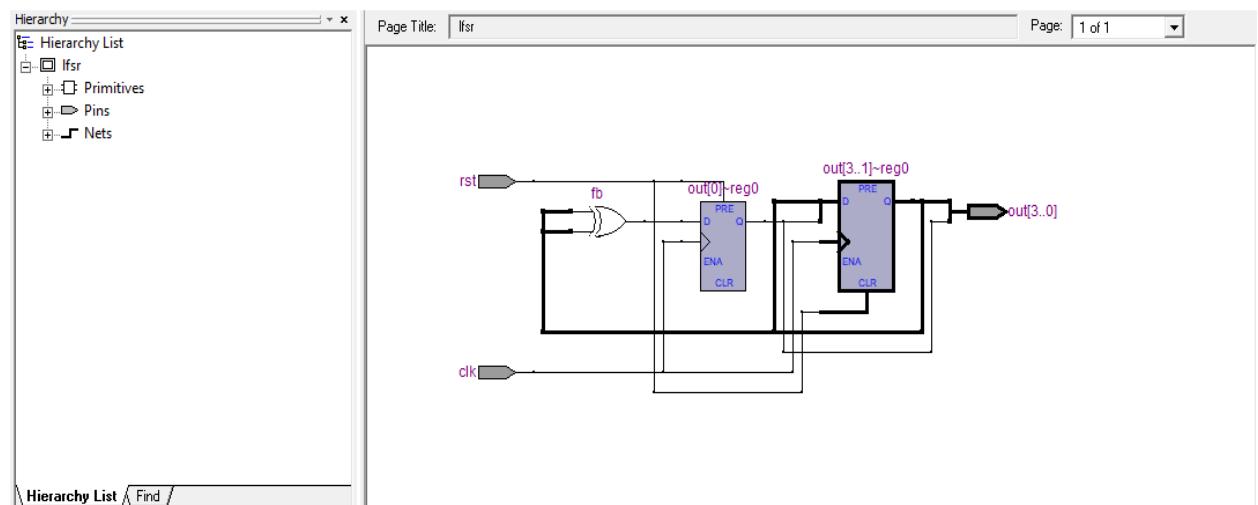
    output reg [3:0] out;
    input clk, rst;

    wire fb; //For feedback

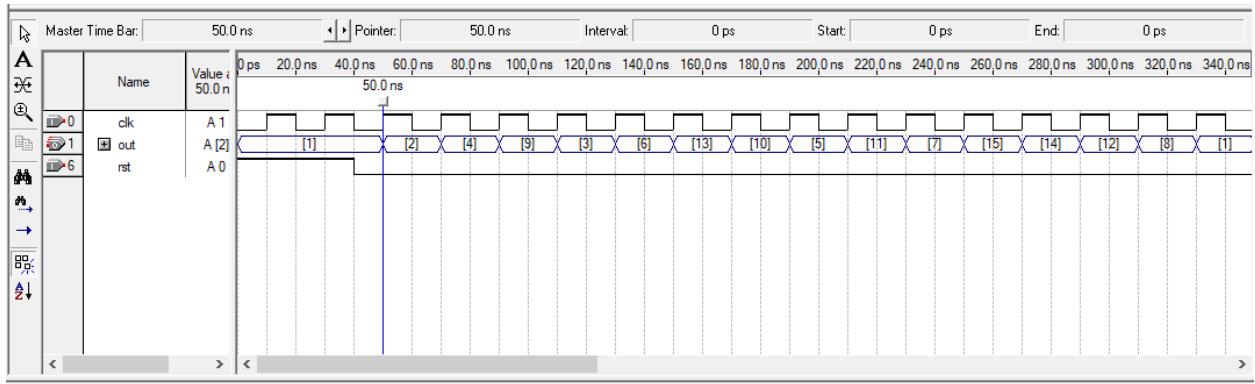
    assign fb = out[3]^out[2];

    always @(posedge clk, posedge rst)
    begin
        if (rst)
            out = 1'b1;
        else
            out = {out[2:0],fb};
    end
endmodule
```

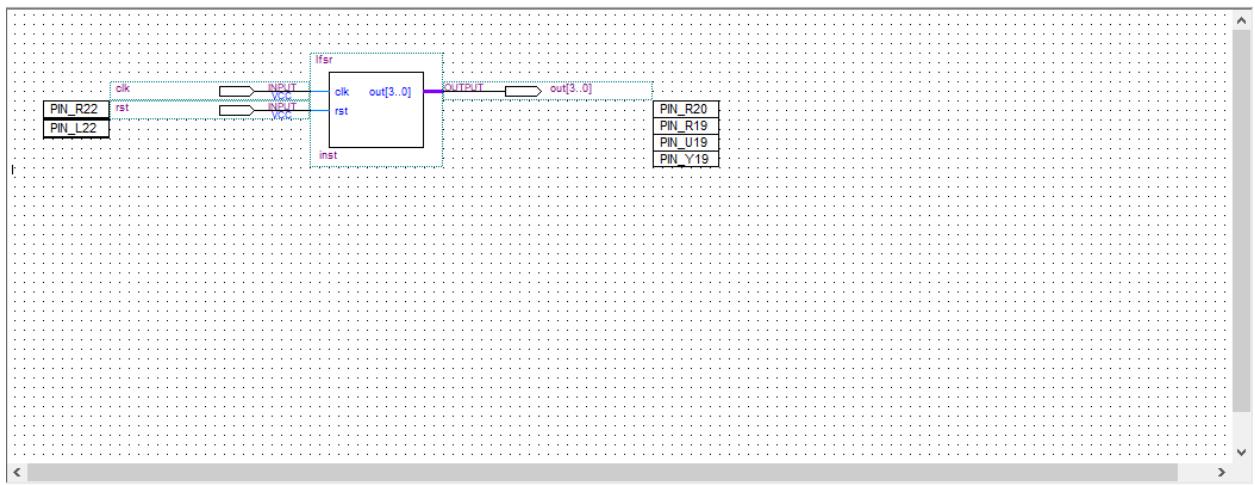
➤ **RTL View:**



➤ Test Waveform:



➤ Block Diagram File:



➤ Pin Assignment for FPGA:

Pin Assignment Table:

	To	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved	Enabled
1	clk	PIN_R22	6	3.3-V LVTTL	Row I/O	LVDS81p		Yes
2	out[0]	PIN_R20	6	3.3-V LVTTL	Row I/O	VREFB6N0		Yes
3	out[1]	PIN_R19	6	3.3-V LVTTL	Row I/O	LVDS84p		Yes
4	out[2]	PIN_U19	6	3.3-V LVTTL	Row I/O	LVDS89n		Yes
5	out[3]	PIN_Y19	6	3.3-V LVTTL	Row I/O	LVDS90n		Yes
6	rst	PIN_L22	5	3.3-V LVTTL	Dedicated Clock	CLK4, LVDSCLKp, In...		Yes
7	out							Yes

➤ **Conclusion:**

In this experiment, we implemented 4-bit LFSR design using x-or gate and D flip flops. It is basically a shift register which gives feedback in form of some function to the input. We implemented this design on the FPGA board and observed the output using LEDs. This circuit generates random sequences in a cyclic manner.